Video Electronics Standards Association

VESA DisplayPort (DP) Standard

Version 2.0

26 June, 2019

www.vesa.org

Purpose

The purpose of this document is to define a flexible system and apparatus capable of transporting video, audio and other data between a Source device and a Sink device over a digital communications interface.

Summary

The DisplayPort™ standard specifies an open digital communications interface for use in both internal connections, such as interfaces within a PC or monitor, and external display connections. Suitable external display connections include interfaces between a PC and monitor or projector, between a PC and TV, or between a device such as a DVD player and TV display.

DP v2.0 adds 128b/132b channel coding and new link rates up to 20Gbps/lane to boost the per-lane link data bandwidth by as much as three times that of HBR3, while maintaining full backward compatibility with *DP v1.4a*. *DP v2.0* also adds Panel Replay mode (based on the Panel Self Refresh 2 mode of *eDP v1.4b* and higher), both for system-level power reduction and for furthering of the Adaptive Sync solution. Furthermore, DSC support is mandated for *DP v2.0* devices that support 128b/132b channel coding for realizing the most deterministic and robust interoperability.

DP v1.4a was revised to correct errata items and add reference to *DSC v1.2a* for enabling YCbCr420 support.

DP v1.4 was revised to add VESA® Display Stream Compression (DSC) transport support for visually lossless 8Kp/10Kp60Hz video along with full extension of audio transport up to 32-channel L-PCM 3D Audio, at 192kHz and HBR 8-channel audio up to 1536kHz. For visual glitch-free DSC bitstream transport, Reed-Solomon (254, 250) Forward Error Correction (FEC) was added. In addition to the sheer video and audio transport bandwidth increase, *DP v1.4* incorporates metadata transport for both static and dynamic High Dynamic Range (HDR). Furthermore, *DP v1.4* enhances the Multi-Stream Transport (MST) feature to better enable multi-function dock supporting DP Alt Mode on USB Type-C.

DP v1.3 was revised to add 8.1Gbps/lane link rate and living-room friendliness improvement, both for direct connection to a living room display and through DP-to-HDMI protocol converter.

DP v1.2a was revised to correct errata items and add clarifications to *DP v1.2*.

DP v1.2 was revised to add enhancements including higher speed operation, more flexible topology management, multiple streams on a single connection, higher speed Auxiliary Channel communications, improved support for audio, and a new smaller connector. It also corrected errors and added clarifications to *DP v1.1a*. This version corrects errors and adds clarification to *DP v1.2*. Furthermore, this version adds DP_PWR voltage level options to a downstream DP device.

DP v1.1a was revised to correct errata items and add clarifications to *DP v1.1*.

Contents

Tables

Figures

Preface

Intellectual Property

While every precaution has been taken in the preparation of this Standard, the Video Electronics Standards Association and its contributors assume no responsibility for errors or omissions, and make no warranties, expressed or implied, of functionality or suitability for any purpose.

Trademarks

All trademarks used within this document are the property of their respective owners.

DisplayPort is a trademark and VESA is a registered trademark of the Video Electronics Standards Association.

CTA is a trademark of the Consumer Technology Association (formerly Consumer Electronics Association).

DVI is a trademark of the Digital Display Working Group.

HDCP is a trademark of Digital Content Protection, LLC.

HDMI and High-Definition Multimedia Interface are trademarks or registered trademarks of HDMI Licensing Administrator, Inc. in the United States and other countries.

I^2C is a trademark of NXP Semiconductors (formerly Philips Semiconductors).

Patents

VESA® draws attention to the fact that compliance with this Standard might involve the use of a patent or other intellectual property right (collectively, "IPR"). VESA takes no position concerning the evidence, validity, and scope of this IPR.

The following holders of this IPR have assured VESA that they are willing to license the IPR on Reasonable And Non-Discriminatory (RAND) terms. The statement of the holder of this IPR is registered with VESA.

Table 1: Patents

Holder Name	Contact Information	Claims Known
Advanced Micro Devices, Inc. 1 Commerce Valley Drive East Markham, ON L3T 7X6 Canada	Raymond Li (raymond.li@amd.com)	**US Patent Applications** 11/678,825 11/678,819 11/010,159
Apple, Inc. 1 Infinite Loop MS 169-3IPL Cupertino, CA 95014 408-996-1010	Jonathan Brown Senior Standards Counsel (jbrown1@apple.com)	**US Patents** US 20130050216 US 61/914,312 US 61/954,498 US 20130094557 US 61/914,322 **Foreign Counterparts Related to the Patents Identified Above** WO2013055510

Table 1: Patents (Continued)

Holder Name	Contact Information	Claims Known
Dell, Inc. One Dell Way Round Rock, TX 78682	Tom Lanzoni (tom_lanzoni@dell.com)	11/458130 11/678838 12/12334 11/458138 11/769803 12/148668 11/543574 12/029013
Genesis Microchip, Inc. 750 Canyon Drive, Suite 300 Coppell, TX 75019	Robert Krysiak (bob.krysiak@st.com)	**US Patents** 6,992,987 7,424,558 7,733,915 7,068,686 7,567,592 8,059,673 7,088,741 7,620,062 8,068,485 7,177,329 **US Patent Applications** 10/726,350 10/726,441 11/742,222 10/726,362 10/726,794 12/248,822 **China Patents** ZL200410038432.8 ZL200410071497.2 ZL200410047784.X ZL200410038545.8 ZL200410044503.5 ZL200810128376.5 **China Patent Applications** 20041038545 20041044503 20081095571 20041038546 20041045686 20081099136 20041043412 20041071497 20081128376 20041043419 20041071498 **EPO Patent Applications** 04251581.7 04252057.7 04252205.2 04251582.5 04252202.9 08153724.3 04252054.4 04252203.7 08153726.8 04252055.1 04252204.5 08155262.2 04252056.9 **Japan Patent Applications** 2004127749 2004130804 20040132494 2004127757 2004130812 20040135520 2004129464 2004133593 20040135542 2004129479 2008116510 20080125185 **Korea Patent Applications** 20040026008 20040026013 20040026486 20040026009 20040026483 20080039968 20040026010 20040026484 20080063251 20040026011 20040026485 20080043714 20040026012 **Singapore Patent Applications** 2008027534 20040001975 20040002060 20040001154 20040001979 20040002061 20040001166 20040002054 20080002448 20040001969 20040002057 20080002449 20040001973 **Taiwan Patent Applications** 93106707 93109757 93110863 93106751 93110851 97115572 93109369 93110857 97111673 93109370 93110861 97111674 93109747

Table 1: Patents (Continued)

Holder Name	Contact Information	Claims Known
Intel Corp. 2111 NE 25th Avenue Hillsboro, OR 97124	Srikanth Kambhatla (srikanth.kambhatla@intel.com)	11/648367 Sink device addressing mechanism 61/1298,936, Title: Audio/video streaming audio in a topology of devices. 12/774,023 (claims priority to P33959Z), Title: Audio/video streaming audio in a topology of devices. 12/782,040 (claims priority to P33959Z), Title: Binding for audio/video streaming in a topology of devices. 12/821,306 (claims priority to P33959Z), Title: Message passing framework for audio/video in a topology of devices. 12/789,893 (claims priority to P33959Z), Title: Identifying devices in a topology of devices for audio/video streaming.
INVECAS, Inc. 3385 Scott Boulevard Santa Clara, CA 95054	Madhu Reddy (madhu.reddy@invecas.com)	**US Patents** US 6151334 US 6914637 US 7599439 US 6857525 US 7088398
Molex, Inc. 2222 Wellington Court Lisle, IL 60532	Stephen L. Sheldon IP Counsel (slsheldon@molex.com)	**US Patents** US 6,457,983, claims 1 and 23 US 6,945,796, claims 5 and 13 US 6,280,209, claim 1 US 6,575,789, claim 1 US 7,165,981
Parade Technologies, Ltd. 2720 Orchard Parkway San Jose, CA 95134	Craig Wiley (craig.wiley@paradetech.com)	**US Patents** 7,397,383, Title: Digital AV Transmission PHY Signaling Format Conversion, Multiplexing & De-multiplexing. 8,094,684, Title: Link Training Scheme for DisplayPort Repeaters **US Patent Applications** 11/467,528 11/537,377 12/118,508
STMicroelectronics, Inc. 750 Canyon Drive, Suite 300 Coppell, TX 75019	Robert Krysiak (bob.krysiak@st.com)	**US Patent Applications** 12/365,678 12/423,724 12/484,796
Synaptics, Inc. 1251 McKay Drive San Jose, CA 95131	Wendy Cheng (wcheng@synaptics.com)	US 8,686,759, Title: Link-Train tunable PHY electrical repeater

Attention is drawn to the possibility that some of the elements of this VESA Standard might be the subject of IPR other than those identified above. VESA shall not be held responsible for identifying any or all such IPR, and has made no inquiry into the possible existence of any such IPR.

THIS STANDARD IS BEING OFFERED WITHOUT ANY WARRANTY WHATSOEVER, AND IN PARTICULAR, ANY WARRANTY OF NON-INFRINGEMENT IS EXPRESSLY DISCLAIMED. ANY IMPLEMENTATION OF THIS STANDARD SHALL BE MADE ENTIRELY AT THE IMPLEMENTER'S OWN RISK, AND NEITHER VESA, NOR ANY OF ITS MEMBERS OR SUBMITTERS, SHALL HAVE ANY LIABILITY WHATSOEVER TO ANY IMPLEMENTER OR THIRD PARTY FOR ANY DAMAGES OF ANY NATURE WHATSOEVER DIRECTLY OR INDIRECTLY ARISING FROM THE IMPLEMENTATION OF THIS STANDARD.

Support for this Standard

Clarifications and application notes to support this Standard might be written. To obtain the latest standard and any support documentation, contact VESA.

If you have a product that incorporates DisplayPort, ask the company that manufactured your product for assistance. If you are a manufacturer, VESA can assist you with any clarification you might require. Submit all comments to support@vesa.org.

Acknowledgments

This document would not have been possible without the efforts of VESA's DisplayPort Task Group. In particular, Table 2 lists the individuals and their companies that contributed significant time and knowledge to this version of the Standard.

Table 2: Main Contributors to *DP v2.0*

Company	Name	Contribution
Advanced Micro Devices, Inc.	Dennis Au	Technical Content
	Neela Baburamasamy	Technical Content
	Nick Chorney	Technical Content
	Wing-Chi Chow	Technical Content
	Mike Comai	Technical Content
	Vista Eydatoula	Technical Content
	Jim Foppiano	Technical Content
	James Hunkins	Technical Content
	Syed Athar Hussain	Technical Content
	Minghua Zhu	Technical Content
Analogix Semiconductor, Inc.	Greg Stewart	Technical Content
Apple, Inc.	Brian Baek	Technical Content
	Bill Cornelius	Technical Content
	Alan Kobayashi	Technical Content and Task Group Chair
	Christine Krause	Technical Content
	Inyeol Lee	Technical Content
	Alex Nadich	Technical Content
	Bob Ridenour	Technical Content
	Jennifer Tsai	Technical Content
Avatar Tech Pubs	Trish McDermott	Technical Writer
Bitec Spain SL	Marco Denicolai	Technical Content
Broadcom Corp.	Fred Walls	Technical Content
DisplayLink	Tony Lambord	Technical Content
EIZO Corp.	Yoshinobu Bamba	Technical Content
Foxconn Interconnect Technology, Ltd.	Glenn Moore	Technical Content

Table 2: Main Contributors to *DP v2.0* (Continued)

Company	Name	Contribution
Hardent, Inc.	Simon Bussières	Technical Content
	Alain Legault	Technical Content
	Avrum Warshawsky	Technical Content
Intel Corp.	Nausheen Ansari	Technical Content
	Michael Hamann	Technical Content
	Jamie Johnston	Technical Content
	Ziv Kabiry	Technical Content
	Ehud Shoor	Technical Content
	Alexander Vekker	Technical Content
INVECAS, Inc.	Guydong Kim	Technical Content
Keysight Technologies	Brian Fetz	Technical Content
	Francis Lin	Technical Content
LG Electronics, Inc.	Do Kyun Kim	Technical Content
	Seunghyun Yoo	Technical Content
MegaChips Corp.	Rahul Kuma Agarwal	Technical Content
	Yu Feng	Technical Content
Novatek Microelectronics Corp.	Andy Lin	Technical Content
NVIDIA Corp.	Raymond Barrios	Technical Content
	Spoorthi D'Silva	Technical Content
	Smore Hung	Technical Content
	Prathap Muthana	Technical Content
	Varun Sampath	Technical Content
	Bill Simms	Technical Content
	David Stears	Technical Content
	Fred Zhu	Technical Content
Parade Technologies, Ltd.	Craig Wiley	Technical Content and Vice Chair
Qualcomm, Inc.	James Goel	Technical Content
	Chris Wiesner	Technical Content
RealTek Semiconductor Corp.	Wesley Chuang	Technical Content
	Jay Lin	Technical Content
Samsung Electronics Co., Ltd.	Dale Stolitzka	Technical Content
Synaptics, Inc.	Zehra Allahbachayo	Technical Content
	Bruce Chin	Technical Content
	Brad Malemezian	Technical Content
	Prashant Shamarao	Technical Content
Synopsys	Bala Babu	Technical Content
	Morten Christiansen	Technical Content

Table 2: Main Contributors to *DP v2.0* (Continued)

Company	Name	Contribution
Teledyne LeCroy	Tim Falls	Technical Content
	Alok Soni	Technical Content
Texas Instruments, Inc.	Mike Campbell	Technical Content
Unigraf	Sergey Grushin	Technical Content
VESA	Bill Lempesis	Contributor
VESA Compliance Program Manager	Jim Choate	Technical Content
VESA Consultant	Kalev Sepp	Technical Content
VTM Group/VESA Consultant	Bob Crepps	Technical Content

Revision History

Table 3: Revision History

Date	Version	Description
June 26, 2019	2.0	• Added: • 128b/132b channel coding for Link Layer, PHY Logical Sub-layer, and PHY Electrical Sub-layer • Ultra-high Bit rates at 10, 13.5, and 20Gbps/lane link rates • Panel Replay • DSC support mandate and DSC bitstream pass-through across a DP Branch device • Appendices M, N, and O • Added changes made to *v1.4a* of this Standard through ratification of the following SCRs: • *Deprecate DockPort* • *DP1.4a Active Cable Sleep Power State* • *DSC Max Target BPP and Min Compression Clarification SCR* • *MST FEC Capability Clarification* • *Overall Peak DSC Throughput and Line Buffer Width* • *QSES Signature Removal* • *SCR to DP1.4a – Correction and Clarification to Link Training Sequence Flow Charts – Figures 3-12 and 3-13* • *SCR to DP1.4a – CRC Clarifications on YCbCr422 and YCbCr420 in Appendix J* • *SCR to DP1.4a – DP Source DPCD ESI Field read optionality* • *SCR to DP1.4a - DP Sink Fallback Video Formats Enumeration DPCD Register Addition* • *SCR to DP1.4a – GUID registers addition to virtual DPCD registers* • Added updates applied by the following SCRs: • *Changing SDP Splitting in SST to Nominal SCR*, rev 2 • *DP 2.0 DSC Policy SCR* • *DSC Color Conversion Bypass Mode* • *SCR to DP1.4a – Active Pixel Regeneration indication* • *SCR to DP1.4a – Correction and Clarification to Link Training Sequence Flow Charts – Figures 3-12 and 3-13*, rev 5 • *SCR to DP1.4a – FEC controls enhancements* • Applied minor grammatical edits, corrected typos, and continued applying VESA template style changes

Table 3: Revision History (Continued)

Date	Version	Description
April 19, 2018	1.4a	• *Adobe RGB* and *JEDEC* reference updates • Pixel data packing typo error correction (Section 2.2.1.3) • Inclusion of the following adopted SCR: • *4:2:2 and 4:2:0 Pixel Format Tables and Text editorial clarification* (v1, 06/29/17) • Horizontal blanking expansion clarification (Section 2.2.4.1.2) • Inclusion of the following adopted SCR: • *DP 1.4 Clarification for Horizontal Blanking Expansion* (v5, 09/13/17) • Detailed format definitions of VSC Extension SDPs (Section 2.2.5.9 and Section 2.2.5.10) • Inclusion of the following adopted SCR: • *Update to VSC_EXT Sections* (v4, 06/28/17) • Adaptive-Sync SDP definition (Section 2.2.5.11) • Top-to-bottom Stereo 3D value addition in Table 2-135 (Section 2.6.1) • ECF clarification for MST mode (Section 2.6.11) • Inclusion of the following adopted SCR: • *DP 1.4 ECF Order* (v1, 06/23/17 • DSC transport update (Section 2.8) • Permission of declaring 170MP/s maximum throughput for test/custom mode (at DPCD Address 0006Bh) • Definition of DSC bitstream transport of 3D stereo video (Section 2.8.6) • Inclusion of the following DSC-related SCRs: • *DP 1.4 Addition of DSC CRC For Verification* (v4, 07/28/16) • *DP1.4 DSC Decoder Color Format Capability Restriction* (v1, 03/31/17) • *Upcoming DP1.4a - Inclusion of DSC1.2a into DP1.4a Ver.5* (v5, 08/15/17) • *DSC Source Device Bandwidth Calculation Correction* (v1, 03/31/17) • DPCD register updates (Section 2.12.3) • Sideband MSG transaction error handling clarification (Section 2.14.8.2) • AUX_CH PHY specification change, errata correction, and clarification (Section 3.4.2) • Inclusion of the following AUX_CH PHY-related adopted SCRs: • *Source Detection by Sink* (v4, 7/16/16) • *AUX Channel PHY SCR Version 6* (v5, 10/13/17) • *Update Figure 3-17 to indicate differential AUX* (v2, 10/05/17)

Table 3: Revision History (Continued)

Date	Version	Description
April 19, 2018	1.4a	**Continued:** • Link Training errata correction and clarification (Section 3.5.1.2) • TPS4 support policy clarification • Link Training flow chart correction to cover infinite loop corner case • Inclusion of the following Link Training-related adopted SCRs: • *POST_LT_ADJ fallback* (v1, 08/05/16) • *Reduced Lane Fallback* (v2, 06/22/17) • FEC specification change, errata correction, and clarification (Section 3.5.1.5) • Inclusion of the following FEC-related adopted SCRs: • *Clarifications on FEC_DECODE_EN/_DIS sequence and the system behavior when FEC_READY bit is set* (v3, 01/13/17) • *FEC_ERROR_COUNT register clarification* (v5, 1/13/17) • *Clarification on Parity Splitting and 8b/10b encoding* (v2, 2/17/17) • *HDCP 1.1 Cipher Alignment with FEC Enabled* (v2, 02/17/17) • *Clarification on the Generation of the FEC CD_ADJ Symbol* (v2, 03/03/17) • *FEC_DECODE_EN/_DIS sequence symbol mapping change* (v1, 05/12/17) • *Making All FEC Error Counters Mandatory* (v5, 06/15/17) • *Error Counter Ambiguity in 1-Lane Configuration* (v1, 06/27/17) • *Clarification on FEC_PM Naming* (v1, 03/03/17) • *Deletion of a redundant sentence on link bandwidth management with DSC enabled* (v1, 10/07/16) • *Time slot count allocation to VC Payload clarification* (v1, 10/07/16) • *Clarification on FEC_PARITY_PH in the DPRX* (v1, 05/10/17) • *Further Cleanup of Figures 3-28 to 3-31* (v2, 10/05/17) • *FEC input bit order* (v2, 10/05/17) • *Clarification on Parity Codes* (v1, 07/27/17) • Main Link budget update (Section 3.5.4) • Addition of DPTX drive setting monotonicity specification for HBR3 and HBR2 • HBR3 jitter budget update at TP2_CTLE and TP3_CTLE; informative specification for TP1 and TP4 deleted for clarity • Reference DPRX CTLE update for HBR3

Table 3: Revision History (Continued)

Date	Version	Description
April 19, 2018	1.4a	**Continued:** • LTTPR specification change, errata correction and clarification (Section 3.6) • Section 2.11.3 also updated to cover AUX transaction timing change • Snooping requirement of AUX write to LINK_QUAL_LANE*x*_SET registers (DPCD Addresses 0010Bh through 0010Eh) • PHY_REPEATER_CNT register definition update (DPCD Address F0002h) • LTTPR support requirement clarification for boot software • Inclusion of the following LTTPR-related adopted SCRs: • *Training AUX Read Interval for PHY Repeater* (v2, 07/07/16) • *LTTPR_AUX_DEFER* (v3, 8/5/16) • *MAX_LANE_COUNT_PHY_REPEATER* (v3, 08/18/16) • *LTTPR AUX Timing* (v6, 08/18/16) • *LTTPR LINK TRAINING* (v3, 08/25/16) • *LTTPR_HPD* (v1, 09/01/16) • *FEC_CAPABILITY_PHY_REPEATER* (v2, 8/18/16) • *LTTPR POWER DOWN* (v1, 12/06/16) • *LTTPR Error Counters* (v3, 06/14/17) • *LTTPR LT Requirement Typo Fix* (v1, 09/07/17) • *DP1.4 LTTPR Mode Transitions and Reset* (v3, 09/21/17) • *Policies of DP Devices with an embedded PHY Repeater* (v2, 11/02/17) • Cable specification update (Section 4) • Addition of DP 8K HBR3 Cable specification (Section 4.1.7) • Inclusion of the following cable-related adopted SCR: • *Clarify HBR Cable Assembly Inter-pair Skew* (v1, 10/07/16) • Update to active cable specification (Section 5.13.3) • DP Tunneling (Section 5.14) • Inclusion of the following adopted SCR: • *Allocate DPCD Registers for Proprietary Tunneling Use* (v2, 4/16/16) • 3D Stereo Video Transport specification change, errata correction, and clarification (Appendix H) • *HDCP to DP r2.2* support addition to QSES (Appendix I) • Inclusion of the following adopted SCRs: • *QSES for HDCP 2.2* (v2, 03/3/17) • *DP1.4 QSES Link_S clarification for HDCP 2.2* (v2, 09/15/17) • Applied minor grammatical edits, corrected typos, and continued applying VESA template style changes

Table 3: Revision History (Continued)

Date	Version	Description
February 23, 2016	1.4	• Added DSC transport (Section 2.8) • Added FEC (forward error correction) mandated for, but not limited to, DSC transport (Section 3.5.1.5) • Extended supported audio formats (Section 2.2.5.1) • Added Audio_Stream SDP splitting in SST mode (Section 2.2.5.13) • Added chainable SDP types for, but not limited to, dynamic HDR metadata transport (Section 2.2.5.9 and Section 2.2.5.10) • Added CEA INFOFRAME SDP packing format Ver.1.3 (Section 2.2.5.12) • Added support for Horizontal Blanking Expansion (Section 2.2.4.1.2) • Added the enumeration of multi-function DP MST Branch device (Section 2.6.1.1) • Updated DP Link Training policy (Section 3.5.1.2) • Updated and added reference documents in Table 1-5 • Corrected Wireless DFP Byte 1 name at DPCD Address 000081h • Corrected SINK_COUNT field in DPCD Address 02002h references to include bit 7 • Corrected range RESERVED for Protocol Converter Extension to start at DPCD Address 03035h (instead of DPCD Address 03034h) • Incorporated the following SCRs: • *DP to VGA sink_source behavior* v3 • *DP1.3 Adaptive-Sync* v3 • *DP1.3 HBR EYE Mask Typo Errors* v1 • *DP1 3 TPS4 Symbol Sequence Info Correction SCR* v 1 • *DP1.3 BT2020 color gamut for RGB* • *DP1.3 HDMI Protocol Conv Source Control* v4 • *DP1.3 LT Tunable PHY Repeater Use Case* • *DP1.3 TRAINING LANEx Set* v2 • Applied editorial changes such as changing “must/is/will/is required to/is mandatory” to “shall”; “is optional” to “may”; “is recommended” to “should” • Applied minor grammatical edits, corrected typos, and continued applying VESA template style changes

Table 3: Revision History (Continued)

Date	Version	Description
September 2014	1.3	• Updated DPCD address mapping to include GTC-related registers that were added in *DP v1.2a* at DPCD Addresses 0005Ah and 0005Bh (Table 2-183), 00115h, 0015Ah, and 0015Bh (Table 2-184), and 02004h bit 1 (Table 2-192). • Added register at DPCD Address 0025Bh. • Added missing names for Byte 1 (bits 7:0), and Byte 2 (bits 7:2 RESERVED) of DPCD Addresses 00080h through 0008Fh, when DETAILED_CAP_INFO_AVAILABLE = 1. • 2.8.4.5.1 (was 2.9.3.6.1) – Corrected field reference from 00102h bits 3:2 to 0010Bh through 0010Eh bits 2:0. • 2.12.1.3.2.2 (previously not numbered), 2nd pg – Corrected bit reference from 00058h bit 0 to bit 1. • Corrected SINK_COUNT field in DPCD Address 00200h references to include bit 7. • Corrected DFP_COUNT field in DPCD Address 00007h references to include bit 3. • Appended "_ESI" to DPCD Address 0200Ch register name. • Standardized spelling of register names – DPCD Addresses 00005h, 0000Fh, and 001A0h. • Combined DPCD Addresses 00054h through 00058h into a single register with multiple bytes. • Deprecated FAUX, Post Cursor2, and Default Framing mode. • Applied global updates to bring standard parallel with DPCD-related content in VESA *eDP*, *DockPort*, and *MyDP Standards*. • Renamed terms: • downstream port → downstream-facing port (DFP) • upstream port → upstream-facing port (UFP) • M and N timestamps → Mvid and Nvid time stamps • AUX_CH → AUX_CH or AUX transactions, depending on use • uPacket receiver, DP receiver → DPRX • uPacket transmitter, DP transmitter → DPTX • Revised miscellaneous bit names to better identify their function. • Updated Acronym and Glossary lists to include new terms and expanded and/or corrected definitions. • Updated (preliminary updated) reference document table to include additional reference documents supported by this Standard. • Added "living-room friendliness" objective; both (1) DP directly to a living-room large screen display and (2) through active protocol conversion from DP to HDMI. • Global – Added 8.1Gbps/lane speed, and support for *MyDP Standard* 6.75Gbps/lane speed. • Global – Added support for YCbCr 4:2:0 and RAW. • 2.1 – Clarified terminology/device types (DP Source/Sink/Branch/PHY Repeater). • 2.1.4 – Updated SST Branch device EDID and DPCD access handling requirement.

Table 3: Revision History (Continued)

Date	Version	Description
September 2014	1.3	**Continued:** • 2.2.1 – Added Camera RAW mapping to Main-Link symbols. Incorporate "End of active line TU clarification" SCR. • 2.2.4 – Incorporated "Extend MS Timing Parameters Ignore Option" SCR (Active-Sync enabler); added MISC 1 bit 6 support (support added globally) • 2.2.5 – VSC SDP extension for Pixel Encoding/Colorimetry Format (globally added support). • 2.2.5 – Added Camera SDP. • 2.8 – Added comprehensive DPCD Address Mapping table covering all published DP-related standards: • New Extended Receiver Capability field for DPCD r1.4 (and higher) • *HDMI v2.0* Status and Control Data Channel (SCDC) abstraction • Metadata extension: *DVI/HDMI v1.4b/HDMI v2.0* mode selection; Pixel encoding conversion within Active protocol converter (e.g., YCbCr 4:4:4 to YCbCr 4:2:0); Colorimetry format • BT.2020 • Full-range $YCbCr_{601}/_{709}$: Content type • Game/video/still image: CEC-Tunneling-over-AUX; HDCP2.2-for-DP (DPCD 69xxxh) • Incorporated *eDP*, *DockPort*, and *MyDP Standard* DPCD register address mapping. • 2.11 – Added Intel SCR concerning ENUM_PATH_RESOURCES message transaction extension. • 3.4.2 – Added edge rate restriction of AUX_CH electrical sub-block for supporting HBR3. • 3.5.1 – Added HBR3, TPS4, Post LT ADJ REQ. • 3.5.2 – Added HBR3, updated jitter budget, Reference DFE, Enhanced HBR Reference CTLE. • 3.6 – Added new Link Training-tunable PHY Repeater section. • 5.3.2 – Added link rate/lane count configuration flexibility between UFP and DFP. • 5.3.3 – Expanded DP-to-HDMI protocol converter section to comprehend protocol conversion to *HDMI v2.0*. • 5.3.3 – Added CEC-Tunneling-over-AUX. • Figure G-3 – Replaced.

Table 3: Revision History (Continued)

Date	Version	Description
May 2013	1.2a	• Reformatted document to new style template. • Tabled or bulleted/numbered paragraphical data, as needed, and fixed typos. Other minor edits have also been applied as part of the changes listed below. • Corrected table or figure cross-references in 2.2.1.2, 2.2.1.3, 2.2.5.3.3, 2.6.5, 3.4.1.3.1, 3.4.2.7, and D.1.1.4. • Standardized mention of register-related information (bits, fields, registers, addresses, etc.) Hyperlinked register and state-related information, as well as some packet-related information. Edited text surrounding the newly hyperlinked text, as needed. • Corrected figure cross-references in 2.2.5.3.3 and 2.6.6 (was 2.6.5). • Organized registers into individual address mapping tables by DPCD field, with all master copies residing in Section 2. • Relabeled appendices alphabetically, with no numbers in their titles. • Corrected register name for DPCD Address 00114h.
May 2012	1.2a	• Patent information for Genesis Microchip, Intel, STMicrosystems, and Parade added. • FAUX bit rate changed from 720Mbps to 675Mbps throughout the document. • 2.3.1.1 Rules of DP_PWR State for a Source Device: Added text. • 2.2.5.6 VSC Packet: Added text regarding PSR function defined in *eDP v1.3*. • 2.2.5.6.1 VSC Packet Header, Table 2-55: Added text for VSC packets. • 2.2.5.6.2 VSC Packet Payload: Added text describing Table 2-56. • 2.3.3.2 Relative Address (RAD): Corrected port numbers. • 2.7.7.1.5.3 Upon I2C_DEFER|AUX Reply with MOT Bit in Request Transaction Set to 0 or 1: Added text. • 2.7.7.1.5.6 Upon Receiving AUX_DEFER Reply to Request Transaction with MOT Bit Set to 0 or 1: Added text, table, and sub-section. • 2.7.7.1.6.3 Upon I2C_DEFER|AUX_ACK Reply to a Request Transaction with MOT Bit Set to 0 or 1: Added text. • 2.7.7.1.6.6 Upon Receiving AUX_DEFER Reply to Request Transaction with MOT Bit Set to 0 or 1: Changed and added text, table, and sub-section. • 2.9.3 AUX Link Services: Added text regarding EDID Read requirements. • 2.9.3.1 Address Mapping for Link Configuration Management, Table 2-75: Added missing information to Read/Write over AUX column and requirement for Downstream device in area 0010Fh of table, changed rows. Also added new bit in DPCD and updated address entries for 00005h and 00080h-0008fh. Added entries from 00271h to 0027Ah. • 2.11 Messaging AUX Client: Replaced & renumbered sections 2.11.9.5.9 and 2.11.9.5.10. Corrected field names in Table 2-85. Resolved errors in Tables 2-81, 2-85. Corrected syntax in Tables 2-89, 2-90, 2-91, 2-94, 2-95, 2-96, 2-97, 2-98, 2-99, 2-100, 2-101, 2-103. Added new fields to Tables 2-81, 2-85. • 2.11.2.4 Handling of Multiple Message Transaction Requests: Removed Message Transaction requirement.

Table 3: Revision History (Continued)

Date	Version	Description
May 2012	1.2a	**Continued:** • 2.11.3.1.4 Sideband_MSG_Body_Length: Corrected field description text. • 2.11.3.1.5 Start_Of_Message Transaction: Changed text, clarified bit definition. • 2.11.3.2 Sideband_MSG_Body: Corrected table number referenced. • 2.11.4.1.1 MST_CAP Bit of MSTM_CAP DPCD Location: Removed device requirement. • 2.11.4.1.5 DOWN_REQ Sideband MSG Buffer: Corrected writing into message buffer, 2.11.4.1.6 UP_REP Sideband MSG Buffer: Corrected writing into message buffer, 2.11.4.1.7 DOWN_REP Sideband MSG Buffer: Corrected writing into message buffer. • 2.11.9.1.3 Payload_Bandwidth_Number: Removed last sentence. • 2.11.9.1.4 Allocated_Payload_Bandwidth_Number: Added this new section. • 2.11.9.4.1 This sub-section added covering Full Payload Bandwidth Number. • 2.11.9.4.2 This sub-section number changed from 2.11.9,4.1 to 2.11.9.4.1 due to the addition of new Section 2.11.9.4.1 and change the section title to “Available Payload Bandwidth Number.” • 2.11.9.4.3 Port Number: Section number has changed. • 2.11.9.10.7 Global_Unique_Identifier sub-section • 2.11.9.15 QUERY_STREAM_ENCRYPTION_STATUS: Updated text. • 2.13 Global Time Code and Audio Inter-channel Sync: Amended and added significant text. Added new table (Table 2-104). • 3.2 DP_PWR for Box-to-Box DisplayPort Connection: Added active cable assembly to list of device types, changed power pin voltage, removed some text in Table 3-3, column two. Text additions and footnote. • 3.1.3.1 DP_PWR/DP_PWR_RETURN: Added text and footnote. • 3.2 DP_PWR specification for a downstream device updated. • 3.2.1 DP_PWR User Detection Method: Added text regarding resistor requirements for CONFIG1 and 2. • 3.2.3 Inrush Energy: Changed peak current. • 3.4.2 AUX_CH Electrical Sub-block: Tables (3-6, 3-8, 3-9) and Figures (3-29, 3-30) were replaced to redefine eye vertices and bring Standard in line with CTS document(s). • 3.5.1 Transmitter and Receiver Electrical Parameters: Added to and amended Table 3-17, 3-20. • 3.5.1.2 Link Training: Added text defining transmitter response related to Post Cursor2 level. • 3.5.1.2.1 Clock Recovery Sequence: Added text regarding Downstream device. • 3.5.3.7.2 Differential Noise Budget: Added to and/or amended Tables 3-6, 3-7, and 3-23.

Table 3: Revision History (Continued)

Date	Version	Description
May 2012	1.2a	**Continued:** • 3.5.3.8 Differential Voltage/Timing EYE Diagram: Changed and added to CTLES, replaced Tables 3-40 and 3-41. • 4.1.1 Cable-Connector Assembly Definition: Added text to very end of section (before sub-section 4.1.1.1). • 4.1.3.1 Impedance Profile through DP Connector: Changed information in Tables 4-1, 4-2, replaced Fig 4-9. • 4.1.5.4.2 Inter-pair Skew: Amended text. • 4.4.6.4 Intra- and Inter-pair Skew: Restructured and added sub-section for Inter-pair Skew. • 5.1.2.1 Source Device Link Requirement when Other Interfaces are Supported: New sub-section. • 5.1.6 Transferred requirements for Source treatment of Branch devices from Interop Guide. • 5.2.2.1 Sink Device Link Requirement when Other Interfaces are Supported: New sub-section. • 5.3 Transferred requirements for protocol converting Branch devices and treatment by Sources from Interop Guide. • 5.3.2 Branch Device Link Configuration Requirements: Added info to address 0003h field. • 5.5.5 Sink Device uPacket RX Power-Save Mode, Figure 5-2: Added text to table and to STATE 1: ACTIVE section following figure. • 5.7.3 Active Cable Assembly, 5.7.3.1 Active Cable Assembly Electrical Parameters, 5.7.3.2 Active Cable Assembly DP_PWR Requirements: New sections added. • Appendix D: Amended Table 9-8. • Appendix H • 13.1.2.1 VSC Packet Header, Table 13-1: Added text to table. • 13.1.2.2 VSC Packet Payload: Added descriptive text. • 13.3 Added section/sub-sections and table related to 3D stereo. • Appendix I, 14.3 QUERY_STREAM_ENCRYPTION_STATUS Message Transaction Handling: Updated text, modified Tables 14-1, 14-2 and added text regarding L parameters in sub-sections. Removed path-message description. • Appendix J: Original was deleted and replaced with another appendix. • Other general edits and clarifications have also been made.

Table 3: Revision History (Continued)

Date	Version	Description
January 2010	1.2	While maintaining full backward-compatibility with *DP v1.1a*, *DP v1.2* added the following major features: • A new link rate, 5.4Gbps/lane, referred to as "HBR2" (or High Bit Rate 2). • Enhanced 3D stereo transport capability. • Color consistency/accuracy improvement support for wide color gamut contents and displays. • Multi-stream transport (MST) mode supporting the transmission of up to 63 independent AV streams from a single DP connector, taking full advantage of the micro-packet transport architecture. • Enhanced topology management using message transactions over Sideband CH (i.e., AUX_CH and Hot Plug Detect) so that a stream Source device has full knowledge of the devices and their capabilities in the topology. • High data rate audio, audio-to-video lip synchronization and audio inter-channel synchronization enablement. • Fast AUX transaction at the raw bit rate of 720Mbps, or application bit rate of 576Mbps, for enabling applications such as *USB2.0* transport over AUX_CH. • Incorporated Mini DisplayPort Connector Standard. • Highlighted the difference between DisplayPort Standard and Embedded DisplayPort (eDP) Standard. • Various clarifications and errata corrections to Version 1.1a were also made in this revision.
December 2007	1.1a	Revised to correct errata items and improve clarification.
March 2007	1.1	Revised to clarify details; introduce the class of "hybrid device"; extend support for content protection schemes to include HDCP; and change requirements for power at DisplayPort connectors.
May 2006	1.0	Initial release of the Standard.

1 Introduction

DisplayPort™ (DP) is an industry standard to accommodate the growing broad adoption of digital display technology within the PC and CE industries. It consolidates internal and external connection methods to reduce device complexity, supports necessary features for key cross industry applications, and provides performance scalability to enable the next generation of displays featuring higher color depths, refresh rates, and display resolutions.

1.1 Organization

This Standard is organized into the following sections that define the overall architecture and structure of the display interface:

- Section 1 – Introduction

  The introduction section defines the high-level industry needs for DisplayPort, and the resulting technical objectives that the protocol, electrical, and mechanical sections are intended to satisfy. This section also includes a glossary of terms for the overall Standard, references, and overview of DP architecture.

- Section 2 – Link Layer Specifications

  The Link Layer section describes the protocol for configuring and managing the topology and the flow of data over both the forward (host to display) transport channel and the auxiliary bidirectional channel. Both Single-Stream Transport (SST) and Multi-Stream Transport (MST) modes are covered.

- Section 3 – PHY Layer Specifications

  The Physical (PHY) Layer section describes the DPTX and DPRX electrical requirements. It also defines the circuitry and encoding methodology necessary for transmitting data to and from the DP Link Layer over a cable or circuit board traces.

- Section 4 – Mechanical Specifications

  The mechanical section defines the connector and cable requirements for both internal and external DisplayPort connectors used to convey the electrical signals defined by the DP PHY Layer.

- Section 5 – Source/Sink/Branch Device Policy Requirements for Interoperability

  The device and link media requirements section describes the policy requirements for Source, Sink, and Branch devices to support interoperability among devices that implement DisplayPort connections.

1.2 DisplayPort Objectives

This Standard defines a scalable digital display interface with optional audio and content protection capability for broad application within PC and consumer electronic (CE) devices. The interface is designed to support both internal chip-to-chip and external box-to-box digital display connections. Potential internal chip-to-chip applications include usage within a laptop for driving a panel from a graphics controller, and usage within a monitor or TV for driving the display component from a display controller. Examples of DP box-to-box applications include display connections between PCs and monitors, projectors, and TV displays. DisplayPort is also suitable for display connections between consumer electronics devices, such as high-definition optical disc players, set top boxes, and television displays.

DisplayPort is designed to meet several key needs within the PC and CE industries, as defined in Section 1.2.1. These industry needs are expanded into a set of technical objectives in Section 1.2.2 to ensure that the display interface can support current and future industry requirements.

Section 1.2.3 and Section 1.2.4 define specific external and internal display connection objectives. Section 1.2.5 defines additional CE device application objectives.

1.2.1 Key Industry Needs for DisplayPort

The following PC and CE industry needs were considered in the development of the DP architecture and resulting interface Standard:

- Drive maximum application and re-use of digital technology to enable reduced device costs associated with implementing a digital display connection.
- Enable a common signaling methodology for both internal and external display connections to reduce device complexity and promote commoditization.
- Enable an extensible architecture that supports an optional robust content protection capability that may be economically implemented.
- Enable high-quality optional digital audio transmission capability.
- Enable higher levels of silicon integration and innovation within rendering and display devices to reduce device complexity and enable digital interface commoditization.
  Examples of potential DisplayPort integration capability include transmitter integration within a graphics or display controller, and receiver integration within a timing controller on a module.
- Simplify cabling for internal and external digital display connections.
- Address performance concerns with existing technologies by providing higher bandwidth over fewer wires.
- Apply embedded clock architecture to reduce electromagnetic interference (EMI) susceptibility and physical wire count.
- Provide a small form factor connector that can be plugged in by feel, and a design that shall enable four connectors to be placed on a full height Peripheral Component Interconnect (PCI) card bracket.
- Enable broad PC and CE industry with an open and extensible industry standard.

DisplayPort addresses these industry needs by defining an electrical and protocol specification that may be readily implemented in module timing controllers, graphics processors, media processors, and display controllers.

A forward drive channel is defined that is scalable from one to four lanes, and implements a micro-packet architecture that supports variable color depths, refresh rates, and display pixel formats. A bidirectional auxiliary channel is defined that also implements micro-packet architecture for flexible delivery of control and status information.

DisplayPort includes a mechanical specification that defines a small, user-friendly external connector that is optimized for use on thin-profile laptops in addition to allowing up to four connectors on a graphics card. A standard module connector for internal applications is also defined in the mechanical section of this Standard.

1.2.2 Technical Objectives

The cross-industry needs defined above for DisplayPort may be translated into specific technical objectives. These technical objectives for DisplayPort are to:

- Provide a high bandwidth forward transmission link channel, with a bidirectional auxiliary channel capability.
- Provide application support for the 1-Mbps auxiliary channel (AUX_CH) throughput with a maximum latency of 500us (except for a topology with cascaded PHY Repeaters between DPTX and DPRX, as described in Section 3.6).
- Support variable color depth transmission of 6, 8, 10, 12, or 16bpc.
- Support EMI compliance to FCC/CISPR B standard with a margin of at least 6dB.
- Support existing VESA® and CTA™ standards where applicable.
- Architecture that does not preclude legacy transmission support (e.g., DVI™ and LVDS) to and from DisplayPort components.
- Support hot plug and unplug detection and link status failure detection.

1.2.3 External Connection Objectives

For external connections between a Source device and a Sink device, this Standard is designed to achieve the following technical objectives:

- Support reading of the display DisplayID or legacy EDID (Extended Display Identification Data) whenever the display is connected to power, even trickle AC power.
- Support DDC/CI (Display Data Channel/Command Interface) and MCCS (Monitor Control Command Set) command transmission.
- Support external display configurations that do not include scaling, a discrete display controller, or on-screen display (OSD) functions, enabling low-cost digital monitors.
- For external laptop applications, DisplayPort allows support for direct drive through a docking connector configuration. A repeater function should be used in the dock.
- External DP connector is identical for all display applications and provides support for four lanes. Captive cables may support one, two, or four lanes to reduce cost.
- External DP connector includes a multi-purpose power pin.
- External DP connector is symmetrical such that the same connector may be used on both Source and Sink devices.
- External DP connector supports connection without the need for visual alignment.
- External DP connector is sized to allow four connectors to fit on a standard full-height ATX/BTX bracket opening for PCI, Accelerated Graphics Port (AGP), and PCI Express add-in cards.

1.2.4 Internal Connection Objectives

For internal connections such as within a laptop or display, this Standard is designed to achieve the following technical objectives:

- DisplayPort defines a common module connector to simplify internal device connections.
- Number of lanes in the internal cable is implementation-specific, and may be one, two, or four.
- Internal DP connections may support both maximum and reduced link bandwidths.
- Internal DP connections support low link power states.
- Hot Plug support for internal DP connections is implementation-specific.

1.2.5 CE Connection Objectives

For application to CE devices, this Standard is designed to address the following technical objectives:

- DisplayPort may deliver digital audio data concurrently with display data.
- DisplayPort supports maintaining of synchronization for delivery of audio and video data to within ±1ms.
- DisplayPort architecture supports an optional robust content protection capability that may be economically implemented.
- DisplayPort supports equivalent functionality to the feature sets defined in *CTA-861-G* for transmission of high quality uncompressed audio-video content, and *CTA-931-C* for the transport of remote control commands between Sink and Source devices.
- DisplayPort supports variable audio formats, audio coding types, sample frequencies, sample sizes, and audio channel configurations. DisplayPort supports up to 32 channels of Linear Pulse Code Modulation audio (L-PCM 3D Audio) at 192kHz with a 24-bit sample size, High Bit Rate (HBR) audio from 256 to 1536kHz, and up to eight channels of One Bit audio and DST audio.
- DisplayPort supports variable video formats based on flexible aspect, pixel format, and refresh rate combinations based on *DMT Standard* and *CVT Standard* timing standards and those timing modes listed in *CTA-861-G*. DisplayPort also allows a Source device to indicate content types (i.e., games, video, and still image).
- DisplayPort supports industry-standard pixel encoding formats including RGB, YCbCr4:4:4, YCbCr4:2:2, and YCbCr4:2:0 with component bit depth up to 16bpc.
- DisplayPort supports colorimetry specifications such as *ITU-R BT.601*, *ITU-R BT.709*, *ITU-R BT.2020*, and *Adobe RGB*.
- DisplayPort supports protocol conversion, including *DVI r1.0*/*HDMI v1.4b*/*HDMI v2.0b*, as well as analog VGA. For conversion to HDMI®, DisplayPort also supports CEC message tunneling over the AUX_CH.
- DisplayPort supports VESA Display Stream Compression (DSC) transport for visually lossless 8Kp/10Kp60Hz video. For visual glitch-free DSC bitstream transport, DisplayPort also supports Reed-Solomon(254, 250) Forward Error Correction (FEC).
- DisplayPort supports multi-function Multi-Stream Transport (MST) dock with DP Alt Mode on USB Type-C capability, as defined in *DisplayPort Alt Mode Standard*.

1.2.6 Content Protection

For DP interface implementations in which content protection is needed, *HDCP for DP r1.3* and *HDCP to DP r2.2* should be used to minimize incompatibilities between DP devices in the market.

1.2.7 *DP v2.0* Objectives

New to *DP v2.0*.

DP v2.0 adds both a 128b/132b channel coding and new link rates up to 20Gbps/lane to boost the per-lane link data bandwidth by as much as three times that of HBR3.

The lowest link rate for 128b/132b channel coding of 10Gbps/lane (bit rate UHBR10) is supported over both DP8K cables (either a native DP cable with DP plug connectors on both ends, –or– a USB Type-C-to-DP adapter cable). Link rates that are higher than UHBR10 are limited to a tethered USB Type-C cable with a USB Type-C plug connector at the end, –or– a passive Thunderbolt™ 3 cable with USB Type-C plug connectors on both ends.

Multi-stream protocol, an **option** for up to HBR3 rates with 8b/10b channel coding, is an integral part of 128b/132b channel coding. The same pixel data-to-DP link symbols mapping is used, regardless of whether a DP link is carrying a single pixel data stream or multiple streams.

To maximize usefulness of the UHBR10 bit rate, DSC support along with DSC bitstream pass-through across a DP Branch device is mandated, as defined in Section 2.9 and Section 2.10.

DP v2.0 also adds Panel Replay mode, based on Panel Self Refresh 2 mode (*eDP v1.4b* and higher), both for its system level power reduction and for furthering the Adaptive Sync solution's flexibility.

1.3 Acronyms and Abbreviations

Table 1-1: Acronyms and Abbreviations

Term	Definition
AA	Audio-to-Audio.
ACM	Audio CopyManagement.
ACT	Allocation Change Trigger.
AEQ	Achieved EQualization.
AFREQ	Audio FREQuency (128b/132b channel coding only).
ANSI	American National Standards Institute.
API	Application Programming Interface.
AR/VR	Augmented Reality/Virtual Reality.
AV	Audio-to-Video (such as with AV lip synchronization).
	Audio/Video.
AVSDB	Audio-Video Sync Data Block.
AUX	Auxiliary transaction.
AUX_CH	Auxiliary CHannel.
BER	Bit Error Rate.
BF	Content Protection Scrambler Reset.
bpc	bits/(color) component.
bpp	bits/pixel.
BE	Blanking End.
BS	Blanking Start.
BU	Branching Unit.
CCS	Current Capabilities Structure.
CD_ADJ	Current Disparity ADJust.
CDF	Cumulative Distribution Function.
CDI	Control Data Indicator (128b/132b channel coding only).
CDR	Clock and Data Recovery.
CE	Consumer Electronics.
CEC	Consumer Electronics Channel.
CH	Channel.
CM	Common Mode.
CP	Content Protection.
CR	Clock Recovery.
CRC	Cyclic Redundancy Check.
CSN	Connection Status Notify.
CTA	Consumer Technology Association (formerly Consumer Electronics Association).

Table 1-1: Acronyms and Abbreviations (Continued)

Term	Definition
CTLE	Continuous Time Linear Equalizer.
CVT	Coordinated Video Timings (VESA).
DAC	Digital-to-Analog Converter.
DB	Data Byte.
DDC	Display Data Channel (VESA).
DDC/CI	Display Data Channel/Command Interface (VESA).
DDJ	Data-Dependent Jitter (also referred to as “Residual ISI”).
DE	Display Enable.
DEM	Downstream Event Monitor.
DFE	Decision Feedback Equalizer.
DFP	Downstream-Facing Port.
DisplayID	Display Identification Data (VESA).
DJ	Deterministic Jitter.
DLS	Data Link Symbol.
DMT	Discrete Monitor Timing (VESA).
DP	DisplayPort (VESA).
DPCD	DisplayPort Configuration Data.
DP_PWR	DP Power.
DPRX	DisplayPort Receiver.
DPRX_PHY	DPRX PHY Layer circuit.
DPTX	DisplayPort Transmitter.
DPTX_PHY	DPTX PHY Layer circuit.
DSC	Display Stream Compression.
DST	Direct Stream Transfer.
DTD	Detailed Timing Descriptor (legacy EDID).
DTS	Digital Theater Systems.
DVI	Digital Visual Interface.
EAN	European Article Number.
ECC	Error Correcting Code.
ECF	Encryption Control Field.
E-DDC	Enhanced Display Data Channel (VESA).
EDID	Extended Display Identification Data (legacy VESA structure, superseded by the DisplayID structure).
eDP	embedded DisplayPort (VESA).
E-EDID	Enhanced Extended Display Identification Data (legacy VESA structure, superseded by the DisplayID structure).

Table 1-1: Acronyms and Abbreviations (Continued)

Term	Definition
EMT	End_Of_Message_Transaction.
EOC	End Of Chunk.
EOM	End Of Message.
EOS	Electrical Over-Stress.
EQ	Equalization.
ESD	Electro Static Discharge.
ESI	Event Status Indicator.
FEC	Forward Error Correction.
FEN	Far-End Noise.
FFE	Feed Forward Equalization (128b/132b channel coding only).
FFT	Fast Fourier Transfer.
FT	Fall Time.
Fs	Pre-defined sample Frequency.
Gbps	Gigabits per second.
GF	Galois Fields.
GPU	Graphics Processor Unit.
GRB	Green Red Blue.
GTC	Global Time Code.
GUID	Globally Unique ID.
HA	Horizontal Active pixels (legacy EDID).
HB	Header Byte.
HBlank	Horizontal Blank.
HBR	High Bit Rate (2.7Gbps/lane).
HBR2	High Bit Rate 2 (5.4Gbps/lane).
HBR3	High Bit Rate 3 (8.1Gbps/lane).
HDCP™	High-bandwidth Digital Content Protection.
HDMI	High-Definition Multimedia Interface®.
HMD	Head-Mounted Display.
HPD	Hot Plug Detect.
HSP	HSync Polarity.
HSW	HSync Width.
IC	Integrated Circuit.
I^2C™	Inter-Integrated Circuit.
IEC	International Electrotechnical Commission.
IEEE	Institute of Electrical and Electronics Engineers.
IL	Insertion Loss.
ILFit	Insertion Loss Fit.

Table 1-1: Acronyms and Abbreviations (Continued)

Term	Definition
ILFitAtNq	Insertion Loss Fit At Nyquist frequency.
IMR	Integrated Multi-Reflection.
IRL	Integrated Return Loss.
IRQ	Interrupt Request.
ISI	Inter-Symbol Interference.
ISRC	International Standard Recording Code.
JTF	Jitter Tracking Function (HBR*x*/RBR).
JTOL	Jitter TOLerance.
LFSR	Linear Feedback Shift Register.
LL	Link Layer.
LLCP	Link Layer Control Packet (128b/132b channel coding only).
lsb	least significant bit.
LSB	Least Significant Byte.
L-PCM	Linear Pulse Code Modulation (*CTA-861-G*).
LT	Link Training.
LTTPR	Link Training-Tunable Phy Repeater.
LVP	Link Verification Pattern.
Maud	Maud value for audio (8b/10b channel coding only).
Mbps	Megabits per second.
MBps	Megabytes/second.
MCCS	Monitor Control Command Set (VESA).
Mcsc	Mega characters per second per channel (HDMI).
mDP	mini DisplayPort (VESA).
MEQ	Measured EQualization.
MOT	Middle Of Transaction (I^2C).
MP	MegaPixels.
MP/s	MegaPixels/second.
MSA	Main Stream Attribute.
msb	most significant bit.
MSB	Most Significant Byte.
MSG	Message.
MSN	Message Sequence Number.
MST	Multi-Stream Transport.
MTP	Multi-stream Transport Packet.
MTPH	Multi-stream Transport Packet Header (8b/10b channel coding only).
mUI	milliUnit Interval.
Mvid	Mvid value for video (8b/10b channel coding only).

Table 1-1: Acronyms and Abbreviations (Continued)

Term	Definition
Naud	Naud value for audio (8b/10b channel coding only).
nb	Nibble.
NEN	Near-End Noise.
NEXT	Near-End Crosstalk.
NPAR	Number of PARity.
Nvid	Nvid value for video (8b/10b channel coding only).
NORP	Number Of Receiver Ports.
OCP	Over Current Protection.
OJTF	Observed Jitter Transfer Function (UHBR*x*).
OSD	On-Screen Display.
OUI	Organizationally Unique ID (IEEE).
PB	Parity Byte.
PC	Parity Code.
PCB	Printed Circuit Board.
PE	Pre-Emphasis.
	Parity Even.
PFD	Phase Frequency Detector.
PH	Place Holder.
PHY	Physical (used with “PHY Layer”).
PJ	Periodic Jitter.
PLL	Phase-Locked Loop.
PLTPAT	Pre-emphasis Level Test PATtern. Consists of five consecutive 1s and five consecutive 0s.
PM	Parity Marker.
PnP	Plug-and-Play.
PO	Parity Odd.
PoS	Point of Sync.
ppm	parts per million.
ppr	peak pixel rate.
PPS	Picture Parameter Set.
PR	Preamble (Audio_Stream SDP field).
	Panel Replay (*DP v2.0* and higher).
PRBS	Pseudo Random Bit Sequence.
PSELFEN	Power Sum Equal Level Far-End Noise.
PSR	Panel Self Refresh (*eDP Standard*).
PSR2	Panel Self Refresh, Version 2 (*eDP v1.4b* and higher).

Table 1-1: Acronyms and Abbreviations (Continued)

Term	Definition
RAD	Relative Address.
RBR	Reduced Bit Rate (1.62Gbps/lane).
RC	Rate Control.
RCD	Room Configuration Descriptor (*CTA-861-G*).
RD	Read.
	Running Disparity.
RG	Rate Governing.
RGB	Red Green Blue.
RJ	Random Jitter.
RL	Return Loss.
ROO	Region Of Overlap.
RS	Reed-Solomon.
RSN	Resource Status Notify.
RT	Rise Time.
RTL	Register Transfer Level.
RX	Receiver.
RX EQ	Receiver EQualization.
S3D	Stereoscopic 3D.
SCMS	Serial Copy Management System (ANSI).
SDP	Secondary-Data Packet.
SE	SDP End.
SF	Stream Fill.
SMT	Start_Of_Message_Transaction.
SR	Scrambler Reset.
SS	SDP Start.
SSC	Spread-Spectrum Clock.
SPM	Speaker Presence Mask (*CTA-861-G*).
SST	Single-Stream Transport.
TBC	Time Base Converter.
TBR	Time Base Recovery unit.
TCON	Timing Controller.
TDR	Time Domain Reflectometry.
TG	Timing Generator.
TIA	Timing Interval Analyzer.
TIE	Timing Interval Error.
TJ	Total Jitter.
TMDS	Transition Minimized Differential Signaling.

Table 1-1: Acronyms and Abbreviations (Continued)

Term	Definition
TP	Test Point (see Table 3-1 for definitions).
TPS	link Training Pattern Sequence.
TTL	Transistor-Transistor Logic.
TU	Transfer Unit.
TX	Transmitter.
TX_EQL	Transmitter EQualization Level.
UDJ	Deterministic Jitter that is Uncorrelated to transmitted data (also referred to as “Non-ISI DJ”).
UFP	Upstream-Facing Port.
UHBR10	Ultra High Bit Rate 10 (10Gbps/lane) (*DP v2.0* and higher).
UHBR13.5	Ultra High Bit Rate 13.5 (13.5Gbps/lane) (*DP v2.0* and higher).
UHBR20	Ultra High Bit Rate 20 (20Gbps/lane) (*DP v2.0* and higher).
UI	Unit Interval.
UJ	Sum of UDJ and RJ components (all jitter components except for DDJ).
UPC	Universal Product Code.
VA	Vertical Active lines (legacy EDID).
VB-ID	Vertical Blanking ID.
VBlank	Vertical Blank.
VC	Virtual Channel.
VCO	Voltage Controlled Oscillator.
VCPF	Virtual Channel Payload Fill.
VESA	Video Electronics Standards Association.
VFREQ	Video FREQuency (128b/132b channel coding only).
VGA	Video Graphics Array.
VHDL	Very high-speed integrated circuit Hardware Description Language.
VS	Vertical Sync.
VSL	Voltage Swing Level.
VSP	VSync Polarity.
VSR	Vertical Space Region.
VSW	VSync Width.
WDE	WiGig Display Extension.
WR	WRite.

1.4 Glossary

Table 1-2: Glossary of Terms

Terminology	Definition
128b/132b	New channel coding added in *DP v2.0* for improving the channel-coding efficiency from 80% of 8b/10b channel coding to 97%. (See Section 3.5.2 for further details.)
8b/10b	Channel coding specification as specified in *ANSI INCITS 230*.
auxiliary channel	AUX_CH. Physical property (pins and signal traces) over which AUX transaction traffic is routed. Half-duplex, bidirectional channel between a DPTX and DPRX. Consists of one differential pair transporting data. An upstream DP device is the master (also referred to as "AUX requester") that initiates an AUX transaction. A downstream DP device is the slave (also referred to as "AUX replier") that replies to the AUX transaction initiated by the requester.
back channel	See the definition in directionality terminology.
Basic Audio	Two-channel *IEC 60958* L-PCM digital audio at sample rates of 32, 44.1, or 48kHz, and sample size of at least 16bps. Although not mandated, a Source device that supports only Basic Audio should send the Audio INFOFRAME SDP.
box-to-box connection	DisplayPort link between two boxes that is user-detachable. A DP cable-connector assembly for the box-to-box connection shall have four Main-Link lanes.
bits/component	bpc. Number of bits for each of R, G, B, –or– Y, Cb, and Cr.
bits/pixel	bpp. Number of bits for each pixel: • For RGB and YCbCr 4:4:4, the bpp value is 3x the bpc value • For YCbCr 4:2:2, the bpp value is 2x the bpc value • For YCbCr 4:2:0, the bpp value is 1.5x the bpc value • For Y-only, the bpp value is equal to the bpc value
Branch device	See DP Branch device.
captive cable	DP cable that is attached to Sink device and cannot be detached by a user. Captive DP cable may have one, two, or four Main-Link lanes, while a user-detachable cable shall have four Main-Link lanes.
chunk	Portion of the bitstream that comprises a set of data bytes. For each slice, there are the same number of chunks as lines within a slice. Every chunk is the same size because *DP v1.4* (and higher) assumes a constant bit rate bitstream. (See *DSC Standard* for further details.)

Table 1-2: Glossary of Terms (Continued)

Terminology	Definition
CTA range	Nominal zero luminance intensity level: • 16 for 24bpp • 64 for 30bpp • 256 for 36bpp • 1024 for 48bpp Maximum luminance intensity level at maximum code value allowed for bit depth: • 235 for 24bpp RGB • 940 for 30bpp RGB • 3760 for 36bpp RGB • 15040 for 48bpp RGB ***Note:*** *The RGB CTA range is defined for 24, 30, 36, and 48bpp RGB only.*
Current Disparity Adjust (CD_ADJ)	Single 10-bit code transmitted at the end of parity codes when FEC is enabled to carry the final four bits of the parity symbols and to ensure that the correct running disparity is maintained on the DP Main-Link lanes.
De-bouncing timer	Timer that counts the “de-bouncing period” to elapse after a mechanical contact (e.g., plugging in a cable-connector assembly to a receptacle connector) to give the signals on the connectors time to settle.
de-spreading	Sink device operation for removing the stream clock’s down spread when the clock is regenerated from the down spread link symbol clock.
directionality terminology (downstream-facing port, downstream link, downstream device, upstream-facing port, upstream link, upstream device, downward/upward message transactions, forward/back channel)	Link through which data is transmitted by a DPTX of a DP device (either DP Source or DP Branch device) is referred to as a “downstream link” of the DP device. The port through which the link is driven is referred to as a “downstream-facing port” (DFP). Link through which data is received by the DPRX of a DP device (either a DP Branch or Sink device) is referred to as an “upstream link” of the DP device. The port through which the link is receiving data is an “upstream-facing port” (UFP). From the point of view of the device that transmits Main-Link data, the device at the other end of the link that receives the data is its downstream device. From the point of view of the device that receives Main-Link data, the device at the other end of the link that transmits the data is its upstream device. For Sideband MSG and Message Transaction, a request Message Transaction (consisting of one or multiple request Sideband MSGs) originated by a DP device toward the downstream devices is referred to as a “downward-going request” or “DOWN_REQ_MSG.” A reply to the downward-going request is referred to as an “upward going reply” or UP_REP_MSG.” A request Message Transaction originated by a DP device toward upstream devices is referred to as an “upward-going request” or “UP_REQ_MSG.” A reply to the upward-going request is referred to as a “downward going reply” or “DOWN_REP_MSG.” For AUX transactions, the channel from an upstream device to a downstream device (used for request transactions) is the Forward channel and the channel from a downstream device to an upstream device (used for reply transactions) Back channel.
display line	Single row of active pixels across a display.

Table 1-2: Glossary of Terms (Continued)

Terminology	Definition
DisplayPort receiver	DPRX. Circuitry that receives the incoming DP Main-Link data. It also contains the transceiver circuit for the AUX_CH. Performs both PHY and Link Layer functions. Part of a DP downstream device (i.e., DP Sink device and DP Branch device).
DisplayPort transmitter	DPTX. Circuitry that transmits the DP Main-Link data. Also contains the transceiver circuit for the AUX_CH. Performs both PHY and Link Layer functions. Part of a DP upstream device (i.e., DP Sink device and DP Branch device).
DisplayPort Configuration Data (DPCD)	DPCD registers are mapped to the DPRX's 20-bit address space. Each register is 8 bits wide. The DPRX uses DPCD registers to declare DPRX capabilities and status. The DPTX uses DPCD registers to configure the DPRX, using AUX transactions.
down spread	Spreading a clock frequency downward from a peak frequency. As compared to "center spread," avoids exceeding the peak frequency specification.
downstream-facing port	See the definition in directionality terminology.
downstream link	
downstream device	
DP Branch device	Device containing DPRX and either DPTX or transmitter of another AV transport interface ("legacy interface"). A PHY Repeater, having only PHY Layer portions of a DPTX and DPRX, is **not** a DP Branch device. Also referred to as a "Branch device" within this Standard.
DP Sink device	Contains the DPRX and at least one stream sink. Leaf device of DP topology. Also referred to as a "Sink device" within this Standard.
DP Source device	Contains the DPTX and at least one stream source. Root device of DP topology. Also referred to as a "Source device" within this Standard.
DSC bitstream	Bitstream generated by compressing the pixel stream, using the DSC algorithm. The DSC bitstream is transported across a DP link to a downstream DSC decoder.
DSC decoding	DSC decompression (see *DSC Standard* for details).
DSC encoding	DSC compression (see *DSC Standard* for details).
DST audio	Direct Stream Transfer. Lossless compressed audio format based on 1-bit oversampling, outlined in *CSA ISO/IEC 14496-3[25], Subpart 10*.
DTS audio	Digital Theater Systems audio. Non-linear PCM audio format outlined in *IEC 61937-5*.
embedded DisplayPort	eDP. Embedded connection, as specified in *eDP Standard* (VESA).
embedded connection	DisplayPort link within a box that is not to be user-detachable. DisplayPort cable for the embedded connection may have one, two, or four Main-Link lanes.
forward channel	See the definition in directionality terminology.
gen-lock	Locking the output timing of a circuit to the input timing. For example, the DPRX may Gen-lock its Display Enable (DE) output timing to the timing of DE signal it receives from a transmitter on the other end of the link.
High-bandwidth Digital Content Protection	HDCP. One of the content protection system options for the DP link. ***Note:*** *HDCP is not part of the DP Standard.*

Table 1-2: Glossary of Terms (Continued)

Terminology	Definition
HPD pulse	There are two kinds of HPD (Hot Plug Detect) pulse, depending on the duration: • A Sink device, when issuing an IRQ (Interrupt ReQuest) to the Source device, shall generate a low-going 0.5 to 1ms HPD pulse. When the Source device detects this "IRQ_HPD pulse," the Source device shall read the DPCD Link/Sink Device Status registers and take corrective action. • When a Source device detects a low-going HPD pulse longer than 2ms, the pulse shall be regarded as a hot plug event HPD pulse. When the Source device detects this hot plug event HPD pulse, the Source device shall read the DPCD Receiver Capability and Link/Sink Device Status registers and take corrective action.
Hybrid device	Either a Branch device or PHY Repeater device responsible for transporting data between a Source device and Sink device by means other than that provided for by PHY Layer, as defined in Section 3, and mechanical, cable-connector assembly specifications, as defined in Section 4.1. A Hybrid device may use alternative wired or wire-free means, including optical or radio technology.
Idle Pattern	Main-Link symbol pattern transmitted over the link when the link is active with no stream data being transmitted.
IEEE OUI	For DP purposes, the assignment of an IEEE identifier for use in MAC addresses (MA-L, MA-M, MA-S) or an IEEE Company Identifier (CID) may be used wherever the Standard specifies use of an IEEE OUI.
leaf device	Sink device, located at a leaf in a DisplayPort tree topology.
link clock recovery	Operation of recovering the link clock from the link serial bitstream.
Link Layer	Layer that handles the mapping between upper layer data and link symbols for the Main-Link and AUX_CH.
Link Policy Maker	Manages the link and maintains link synchronization. All DP devices shall have a Link Policy Maker.
L-PCM 3D Audio	Linear Pulse Code Modulation 16-channel (1 to 16 channels) and 32-channel (17 to 32 channels) audio (*CTA-861-G*).
L-PCM Audio	Linear Pulse Code Modulation 2-channel (1 to 2 channels) and 8-channel (3 to 8 channels) audio (*CTA-861-G*).
Main-Link	Unidirectional channel for isochronous stream transport from DPTX to DPRX. Consists of one, two, or four lanes, or differential pairs. Supports the following bit rates: • **Ultra High Bit Rate 20 (UHBR20)** – 20Gbps/lane • **Ultra High Bit Rate 13.5 (UHBR13.5)** – 13.5Gbps/lane • **Ultra High Bit Rate 10 (UHBR10)** – 10Gbps/lane • **High Bit Rate 3 (HBR3)** – 8.1Gbps/lane • **High Bit Rate 2 (HBR2)** – 5.4Gbps/lane • **High Bit Rate (HBR)** – 2.7Gbps/lane • **Low or Reduced Bit Rate (RBR)** – 1.62Gbps/lane ***Note:*** *6.75Gbps/lane link rate is supported between a MyDP Standard DPTX and DPRX.*

Table 1-2: Glossary of Terms (Continued)

Terminology	Definition
Main-Link symbol	Symbol types can be data or control: **128b/132b channel coding** • Data link symbols and control link symbols are both 32 bits in size (for further details, see Section 3.5.2.4 and Section 3.5.2.5, respectively) **8b/10b channel coding** • Data symbols contain 8 bits of data and are encoded into 10-bit data characters by way of channel coding, as specified in *ANSI INCITS 230* (referred to as "8b/10b" within this Standard) before being transmitted over a link. • DisplayPort also defines control link symbols used to frame data symbols. Control link symbols are encoded into 10-bit special characters of 8b/10b (referred to as "K-codes").
Main-Link Symbol clock	Clock with which Main-Link symbols are transferred within PHY and Link Layer circuits of either a DPTX or DPRX for Main-Link transport. The clock frequency is as follows: **128b/132b channel coding** • See Section 3.5.2.8 for details **8b/10b channel coding** • **HBR3** – 810MHz for 8.1Gbps/lane • **HBR2** – 540MHz for 5.4Gbps/lane • **HBR** – 270MHz for 2.7Gbps/lane • **RBR** – 162MHz for 1.62Gbps/lane
Main Stream Attributes	MSA. Attributes that describe the main video stream format in terms of geometry and colorimetry format. Inserted once per video frame during the video blanking period. Used by the DPRX when reconstructing the stream.
Manchester transaction	AUX transaction using Manchester-II encoding used for transfers at 1Mbps on the AUX_CH.
micro-packet	Vessel used for transporting data over a DP link.
Multi-stream Transport	MST. Mode used for transporting multiple main video streams, each of which is enclosed in a VC Payload and may have a Secondary-data Packet (SDP) stream, such as an audio stream (or SDP stream only without main video stream). Uses MTP (Multi-stream Transport Packet) as the unit of micro-packet. See also Single-stream Transport.
One Bit audio	1-bit Sigma-Delta (Delta-Sigma) modulated signal stream.

Table 1-2: Glossary of Terms (Continued)

Terminology	Definition
parity codes	Five 10-bit (4- and 2-lane configurations) or eleven 10-bit (1-lane configuration) codes that are carried on the DP Main-Link lanes which, along with the CD_ADJ code, carry the parity symbols for the FEC block when FEC is enabled. The DPTX generates parity codes and CD_ADJ code from the parity symbols by performing parity splitting, 8b/10b encoding, and interleaving.
parity symbols	**128b/132b channel coding** • 32-bit parity symbol that consists of four parity bytes of RS(198,194) FEC. DP 128b/132b channel coding adopts 8-bit symbol RS. To avoid confusion between the 8-bit symbol size and 32-bit parity symbol, 8-bit parity is referred to as "parity bytes" instead of "8-bit parity symbol." **8b/10b channel coding** • Four 10-bit symbols per RS(254, 250) block generated by the RS(254, 250) encoder in the DPTX and used by the RS(254, 250) decoder in the DPRX.
peak pixel rate	ppr. Maximum data rate in megapixels per second (MP/s) that a display needs for a given video timing format mode (resolution and refresh).
PHY Repeater	Consists of the DPTX_PHY and DPRX_PHY.
Physical Layer	PHY Layer or PHY. Composed of the PHY Logical and Electrical Sub-layers, which are implemented by the PHY Logical and Electrical Sub-blocks, respectively. Handles channel encoding from/decoding to link symbols, serialization/de-serialization, and serial bitstream transmission/reception.
picture	Single frame of pixels.
Picture Parameter Set	PPS. Set of parameters that provide information necessary to decode the picture.
PRBS7	**UHBR*x* bit rates** See Appendix N for definition. **HBR*x* and RBR bit rates** 7-bit pseudo random bit sequence according to *ITU-T O.150*. $G(x) = x7 + x6 + 1$ (non-inverted signal) Length of sequence = 127 bits. The actual bit sequence shall be: `----- direction ---->` `00100000110000010100` `01111001000101100111010 1001` `11110100001110001001001 1011` `01011011110110001101001 0111` `01110011001010101111111 10000` ***Note:*** *Upper left transmitted first and lower right transmitted last.*
rendering function	Function of displaying/processing the stream data in devices such as video displays, speakers, and image format converters.
root device	DP Source device, located at a root in a DisplayPort tree topology.
Secondary-data	Data transported over the Main-Link which is not main video stream data, such as audio data and INFOFRAME SDPs.

Table 1-2: Glossary of Terms (Continued)

Terminology	Definition
Single-stream Transport	SST. Mode used for transporting a single main video stream which may have an SDP stream, such as an audio stream (or an SDP stream only without main video stream). Uses Transfer Unit (TU) as the unit of micro-packet. See also Multi-stream Transport.
Sink device	See DP Sink device.
slice	Independently decodable set of compressed bits that represent a specified set of samples. The set of samples forms a rectangle in the horizontal and vertical dimensions. Decoding of any one slice does not depend on the decoded result or availability of another slice.
Source device	See DP Source device.
stream clock	Used for transferring stream data into a DPTX within a DP Source device or from a DPRX within a DP Sink device. Video and audio (optional) are likely to have separate stream clocks.
stream clock regeneration	Operation of regenerating the stream clock from the Main-Link Symbol clock.
Stream Policy Maker	Manages transportation of an isochronous stream.
super symbol	Four sets of 32-bit link symbols, 128 bits total. Used for 128b/132b PHY Logical Sub-layer.
timing controller	TCON. Circuit that outputs control and data signals to driver electronics of a display device.
time stamp	Value used by a clock circuit to keep two systems synchronized.
transfer unit	TU. Used to carry main video stream data during its horizontal active period. TU has 32 to 64 symbols per lane (except at the end of the horizontal active period), each consisting of active data symbols and fill symbols.
trickle power	Power for a DP Sink device that is sufficient to let the DP Source device read DisplayID or legacy EDID by way of the AUX_CH, but insufficient to enable Main-Link and other DP Sink device functions. For a DP Sink device to drive the HPD signal high, at least trickle power shall be present. The amount of power needed for trickle power is DP Sink device implementation-specific.
TX emphasis	Transmitter Emphasis. **128b/132b channel coding** • TX Feed Forward Equalization (FFE), consisting of preshoot and de-emphasis. Used by UHBR*x*, as described in Section 3.5.5. **8b/10b channel coding** • Form of TX equalization, consisting of a combination of pre-emphasis and de-emphasis. Used by HBR3 and HBR2.
upstream-facing port	See the definition in directionality terminology.
upstream link	
upstream device	
Upstream Device Detection feature	Ability of a downstream DP device to detect an upstream DP device by sensing the DC levels on the AC-coupled AUX_CH lines. These DC levels are imposed by weak DC pull-up and pull-down components on the upstream AUX_CH connections, as described in this Standard.
Vertical Blanking ID	VB-ID. Data symbol transmitted immediately following a BS symbol sequence, indicating the AV stream transport status (e.g., vertical blanking interval or not, audio to be muted or not). Also used by the DPRX for content protection synchronization detection.

Table 1-2: Glossary of Terms (Continued)

Terminology	Definition
VESA range	Nominal zero luminance intensity level at code value 0. Maximum luminance intensity level is the maximum code value that is allowed for the bit depth: • 63 for 18bpp RGB • 255 for 24bpp RGB • 1023 for 30bpp RGB • 4095 for 36bpp RGB • 65535 for 48bpp RGB
video horizontal timing	Horizontal timing means video line timing. For example, horizontal period and horizontal synchronization pulse mean line period and line synchronization pulse, respectively. The term “horizontal” does not necessarily correspond to the physical orientation of the display device (e.g., a line may be oriented vertically on a “portrait” display).
video vertical timing	Vertical timing means video frame (or field) timing. For example, vertical period and vertical synchronization pulse mean a frame (or field) period and a frame synchronization pulse, respectively. The term “vertical” does not necessarily correspond to the physical orientation of the display device (e.g., a line may be oriented horizontally on a “portrait” display).

1.5 Conventions

1.5.1 Precedence

If there is a conflict between text, figures, and tables, the precedence shall be tables, figures, and then text.

1.5.2 Keywords

Table 1-3 lists keywords that differentiate between the levels of mandates and options within this Standard.

Table 1-3: Keywords

Keyword	Definition
Informative	Describes information that discusses and clarifies mandates and features as opposed to mandating them.
May	Indicates a choice with no implied preference.
N/A	Indicates that a field or value is **not** applicable and has no defined value, and shall **not** be checked or used by the recipient.
Normative	Describes features that are mandated by this Standard.
Optional	Describes features that are **not** mandated by this Standard. However, if an **optional** feature is implemented, the feature shall be implemented as defined by this Standard (optional normative).
RESERVED	Indicates RESERVED bits, bytes, words, fields, and code values that are set aside for future standardization. Their use and interpretation may be specified by future extensions to this Standard and, unless otherwise stated, shall **not** be used or adapted by vendor implementation. A RESERVED bit, byte, word, or field shall be cleared to 0 by the transmitter and ignored by the receiver. RESERVED field values shall **not** be transmitted by the transmitter and, if received, shall be ignored by the receiver.
Shall	Indicates a mandate. Designers are mandated to implement all such mandates to ensure interoperability with other compliant devices.
Should	Indicates flexibility of choice with a preferred alternative. Equivalent to the phrase “it is recommended that.”

1.5.3 Numbering

Table 1-4 lists the different types of numbering used within this Standard.

Table 1-4: Numbering

Number Type	Definition
Binary	Numbers that are immediately followed by a lowercase “b” (e.g., 01b). Also used for individual register bit values (i.e., 0, 1).
Decimal	Numbers that are not immediately followed by either a “b” or “h” (e.g., 5).
Hexadecimal	Numbers that are immediately followed by a lowercase “h” (e.g., 3Ah).
	Numbers that start with “0x” (e.g., 0x00).

1.5.4 Bit and Byte Ordering Nomenclature

This section describes the bit and byte ordering nomenclature that is used by the Main-Link and AUX_CH.

1.5.4.1 Bit Ordering

1.5.4.1.1 Parallel Bit Ordering – Main-Link

Within a byte, bit 0 is the least significant bit (lsb) and bit 7 is the most significant bit (msb).

msb							lsb
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

For 8 bits/component (bpc), **red** bit 7 (R7) is placed at bit 7 and **red** bit 0 (R0) is placed at bit 0.

msb							lsb
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R7	R6	R5	R4	R3	R2	R1	R0

For 6bpc, **red** bit 5 is placed at bit 7 (R5) and **green** bit 4 (G4) is placed at bit 0.

msb							lsb
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R5	R4	R3	R2	R1	R0	G5	G4

1.5.4.1.2 Parallel Bit Ordering – AUX_CH

Within a byte, bit 0 is the lsb and bit 7 is the msb.

1.5.4.1.3 Serial Bit Ordering after Channel Encoding – Main-Link

Within a byte, the lsb (bit 0) is transmitted first and the msb (bit 7) is transmitted last.

1.5.4.1.4 Serial Bit Ordering after Channel Encoding – AUX_CH (Manchester-II)

Within a byte, the msb (bit 7) is transmitted first and the lsb (bit 0) is transmitted last.

1.5.4.2 Byte Ordering

1.5.4.2.1 Byte Ordering – Main-Link, Main Stream

In an MSA packet, the MSB is transmitted first. For example, if an RGB pixel's color bit depth is 16bpc, R15:8 (**red** bits 15:8) is transmitted first, followed by R7:0 (**red** bits 7:0).

R15:8
R7:0

When certain parameters of the MSA packet have multiple bytes, the MSB is transmitted first. For example, Mvid23:16 is transmitted first, followed by Mvid15:8, and then by Mvid7:0.

Mvid23:16
Mvid15:8
Mvid7:0

1.5.4.2.2 Byte Ordering – Main-Link, SDP

In an SDP, the LSB is transmitted first, as indicated in the following audio sample data example.

Audio Sample 0 Channel 1 Byte 0
Audio Sample 0 Channel 1 Byte 1
Audio Sample 0 Channel 1 Byte 2
Audio Sample 0 Channel 1 Byte 3

1.5.4.2.3 Byte Ordering – AUX_CH

In burst write/read operations over the AUX_CH, the address is increased by one after each data byte. For DPCD registers that have multiple bytes, the LSB is stored at the lowest address, unless stated otherwise in the DPCD register tables (e.g., in DPCD Addresses 00222h through 00231h, the LSB is stored at the upper address). During the burst operation of an AUX transaction, therefore, the LSB is transported first, as indicated in the following IEEE OUI register example.

Source device IEEE OUI first two hex digits (DPCD Address 00300h)
Source device IEEE OUI second two hex digits (DPCD Address 00301h)
Source device IEEE OUI third two hex digits (DPCD Address 00302h)

Note: *As specified in Section 1.5.4.1, the msb is transported first and the lsb is transported last over the AUX_CH.*

1.6 Reference Documents

Table 1-5: Reference Documents

Document	Version/ Revision[a]	Date	Referenced As
Adobe® RGB (1998) Color Image Encoding	Version 2005-05	May 2005	*Adobe RGB*
ANSI INCITS 230, Information Technology – Fibre Channel – Physical and Signaling Interface (FC-PH)[b]	Edition 94	1999	*ANSI INCITS 230*
BT.601, Studio encoding parameters of digital television for standard 4:3 and wide screen 16:9 aspect ratios[c]	Version 7	March 2011	*ITU-R BT.601*
BT.709, Parameter values for the HDTV standards for production and international programme exchange[c]	Version 6	June 2015	*ITU-R BT.709*
BT.1359, Relative Timing of Sound and Vision for Broadcasting[c]	Version 1	November 30, 1998	*ITU-R BT.1359*
BT.2020, Parameter values for ultra-high definition television systems for production and international programme exchange[c]	Version 2	October 2015	*ITU-R BT.2020*
CSA ISO/IEC 14496-3, Information Technology – Coding of Audio-Visual Objects – Part 3: Audio[b]	2010	December 2010 Includes amendments and changes through October 2016	*CSA ISO/IEC 14496-3*
CTA-770.2, Standard Definition TV Analog Component Video Interface (formerly known as *CEA-770.2*)[b]	D	April 1, 2007	*CTA-770.2*
CTA-770.3, High Definition TV Analog Component Video Interface (formerly known as *CEA-770.3*)[b]	E	June 1, 2013	*CTA-770.3*
CTA-861, A DTV Profile for Uncompressed High Speed Digital Interfaces[b] (formerly known as *CEA-861*)	G	November 2, 2017	*CTA-861-G*
CTA-931, Remote Control Command Pass-through Standard for Home Networking[b] (formerly known as *ANSI/CEA-931-C*)	C	December 1, 2007	*CTA-931-C*
DICOM® PS3.14 – Grayscale Standard Display Function[d]	2018	2018	*DICOM PS3.14*
Digital Visual Interface (DVI)	1.0	April 2, 1999	*DVI r1.0*
EIA-364-09, TP-09C Durability Test Procedure for Electrical Connectors and Sockets[b]	C	June 1, 1999	*EIA-364-09*
EIA-364-13, TP-13E Mating and Unmating Force Test Procedure for Electrical Connectors and Sockets[b]	E	June 1, 2011	*EIA-364-13*

Table 1-5: Reference Documents (Continued)

Document	Version/ Revision[a]	Date	Referenced As
EIA-364-17, TP-17C Temperature Life with or without Electrical Load Test Procedure for Electrical Connectors and Sockets[b]	C	November 1, 2011	*EIA-364-17*
EIA-364-20, TP-20E Withstanding Voltage Test Procedure for Electrical Connectors, Sockets, and Coaxial Contacts[b]	E	February 1, 2015	*EIA-364-20*
EIA-364-21, TP-21E Insulation Resistance Test Procedure for Electrical Connectors, Sockets, and Coaxial Contacts[b]	E	May 1, 2014	*EIA-364-21*
EIA-364-23, TP-23C Low Level Contact Resistance Test Procedure for Electrical Connectors and Sockets[b]	C	June 1, 2006	*EIA-364-23*
EIA-364-27, TP-27C Mechanical Shock (Specified Pulse) Test Procedure for Electrical Connectors and Sockets[b]	C	June 1, 2011	*EIA-364-27*
EIA-364-28, TP-28F Vibration Test Procedure for Electrical Connectors and Sockets[b]	F	February 1, 2011	*EIA-364-28*
EIA-364-31, TP-31E Humidity Test Procedure for Electrical Connectors and Sockets[b]	E	April 1, 2017	*EIA-364-31*
EIA-364-32, TP-32G Thermal Shock (Temperature Cycling) Test Procedure for Electrical Connectors and Sockets[b]	G	August 1, 2014	*EIA-364-32*
EIA-364-41, TP-41E Cable Flexing Test Procedure for Electrical Connectors[b]	E	January 1, 2010	*EIA-364-41*
EIA-364-70, TP-70C Temperature Rise Versus Current Test Procedure for Electrical Connector and Sockets[b]	C	July 1, 2014	*EIA-364-70*
EIA-364-98, TP-98 Housing Locking Mechanism Strength Test Procedure for Electrical Connectors[b]	1997	June 1, 1997	*EIA-364-98*
EIA-364-1000, TS-1000A Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Controlled Environment Applications[b]	A	February 1, 2016	*EIA-364-1000*
ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Test – Human Body Model (HBM) – Component Level – see www.jedec.org/standards-documents	2017	May 2017	*ANSI/ESDA/ JEDEC JS-001*
High-Bandwidth Digital Content Protection System, Amendment for DisplayPort[e]	Version 1.3 Revision 1.1	January 15, 2010	*HDCP for DP r1.3*
High-Bandwidth Digital Content Protection System, Mapping HDCP to DisplayPort[e]	Revision 2.3	January 22, 2019	*HDCP to DP r2.3*

Table 1-5: Reference Documents (Continued)

Document	Version/ Revision[a]	Date	Referenced As
High-Definition Multimedia Interface Specification – see www.hdmi.org	Version 1.4b Version 2.0b	October 11, 2011 March 3, 2016	*HDMI v1.4b* *HDMI v2.0b* *HDMI Specification*
The I^2C-Bus Specification – see www.nxp.com	Version 2.1	January 2000	*I^2C Standard*
IEC 60958 SET, Digital Audio Interface – Complete Set[b]	Edition 1.0 en:2015	2015	*IEC 60958*
IEC 60958-1, Digital Audio Interface – Part 1, General[b]	Edition 3.1 b:2014	April 1, 2014	*IEC 60958-1*
IEC 60958-3, Digital Audio Interface – Part 3, Consumer Applications[b]	Edition 3.2 en:2015	June 1, 2015	*IEC 60958-3*
IEC 61000-4-2, Electromagnetic Compatibility (EMC) – Part 4-2: Testing and Measurement Techniques – Electrostatic Discharge Immunity Test[f]	2.0	December 9, 2008	*IEC 61000-4-2*
IEC 61937 SET, Digital Audio – Interface for Non-linear PCM Encoded Audio Bitstreams Applying IEC 60958 – Complete Set[b]	Edition 1.0 b:2017	2017	*IEC 61937*
IEC 61966-2-1:1999, Multimedia systems and equipment – Colour measurement and management – Part 2-1: Colour management – Default RGB colour space - sRGB[f]		October 18, 1999	*IEC 61966-2-1*
IEC 61966-2-2:2003, Multimedia systems and equipment – Colour measurement and management – Part 2-2: Colour management – Extended RGB colour space – scRGB[f]		January 23, 2003	*IEC 61966-2-2*
IETF RFC 4122, A Universally Unique IDentifier (UUID) URN Namespace – see www.ietf.org/rfc/rfc4122.txt		March 2, 2013	*RFC 4122*
Intel Converged IO Electrical Layer	Ver.0.95	May 6, 2019	*CIO Electrical Layer*
O.150 – Series O: Specifications of Measuring Equipment – Equipment for the Measurement of Digital and Analogue/Digital Parameters – General Requirements for Instrumentation for Performance Measurements on Digital Transmission Equipment[c]		May 1996	*ITU-T O.150*
SMPTE RP 431-2, D-Cinema Quality – Reference Projector and Environment[g]	2011	April 6, 2011	*SMPTE RP 431-2*
Stephens, Ransom. "What the Dual-Dirac Model is and What it is Not."[h]		October 2006	

Table 1-5: Reference Documents (Continued)

Document	Version/ Revision[a]	Date	Referenced As
Universal Serial Bus 3.2 Specification[i]	Release 3.2	September 22, 2017	*USB r3.2*
Universal Serial Bus Type-C Cable and Connector Specification[i]	Revision 1.3[j]	July 14, 2017	*USB Type-C Specification*
VESA Coordinated Video Timings (CVT) Standard[l]	Version 1.2	February 8, 2013	*CVT Standard*
VESA Display Data Channel Command Interface (DDC/CI) Standard[l]	Version 1.1	October 2004	*DDC/CI Standard*
VESA DisplayID Standard[l]	Version 2.0	September 11, 2017	*DisplayID Standard*
VESA Display Monitor Timing (DMT) Standard[l]	Version 1.13	March 2013	*DMT Standard*
VESA DisplayPort Alt Mode on USB Type-C Standard (DisplayPort Alt Mode)[l]	Version 1.0b	November 3, 2017	*DisplayPort Alt Mode Standard*
VESA DisplayPort Alt Mode on USB Type-C 1.0a Compliance Test Specification (DP Alt Mode on USB Type-C 1.0a CTS)	Revision 1.0	January 24, 2017	*DP Alt Mode on USB Type-C CTS*
VESA DisplayPort EDID Compliance Test Specification[l]	Version 1.2	March 2014	*DP EDID CTS*
VESA DisplayPort Interoperability Guideline[l]	Version 1.1a	February 2009	*DP Interoperability Guideline*
VESA DisplayPort Panel Connector Standard[l]	Version 1.1a	May 2009	*DP Panel Connector*
VESA DisplayPort 1.4a Link Layer Compliance Test Specification (Link CTS)[l]	DP 1.4a r1.0	June 12, 2019	*Link CTS*
VESA DisplayPort 1.4a PHY Layer Compliance Test Specification (PHY CTS)[l]	DP 1.4a r1.0	July 27, 2018	*PHY CTS*
VESA DisplayPort Dual-Mode (DP++) Standard[l]	Version 1.1	February 8, 2013	*Dual-Mode Standard*
VESA Display Stream Compression (DSC) Standard[l]	Version 1.2a	January 18, 2017	*DSC Standard*
VESA Embedded DisplayPort (eDP) Standard[l]	Version 1.4b	October 23, 2015	*eDP Standard*
VESA Enhanced Display Data Channel (E-DDC) Standard[l]	Version 1.3	September 11, 2017	*E-DDC Standard*
VESA Enhanced Extended Display Identification Data (E-EDID) Standard (which defines EDID r1.4)[l k]	Release A.2	September 25, 2006	*E-EDID Standard*
VESA Glossary of Terms[l]	Current	Current	
VESA Intellectual Property Rights (IPR) Policy[l]	200D	March 27, 2017	

Table 1-5: Reference Documents (Continued)

Document	Version/ Revision[a]	Date	Referenced As
VESA Mini DisplayPort Connector (mDP) Standard[l]	Version 1	October 2009	*mDP Standard*
VESA Monitor Control Command Set (MCCS) Standard[l]	Version 2.2a	January 2011	*MCCS Standard*
VESA MST Use Case Example[l]	Version 1	September 2011	
VESA Mobility DisplayPort (MyDP) Standard[l]	Version 1	May 2012	*MyDP Standard*
DVD FLLC, *DVD-Audio Book, Part 4: Audio Specifications*	Version 1.2_1, Part 4	April 2004	*DVD-Audio Book v1.2]p4*

a. All references include subsequently published errata, specification change notices or engineering change notices, etc.
b. Available for download from global.ihs.com.
c. Published by the International Telecommunication Union (ITU). See itu.int.
d. Published by Digital Imaging and Communications in Medicine (DICOM). Available for download from dicomstandard.org/current/.
e. Published by Digital Content Protection (DCP). See digital-cp.com.
f. Published by the International Electrotechnical Commission (IEC). See webstore.iec.ch.
g. Published by Society of Motion Picture and Television Engineers.
h. Available for download from ransomnotes.com.
i. Published by USB Implementers Forum, Inc. See www.usb.org/developers/docs.
j. This version of the referenced Standard/Specification is correct at the time of publication of this Standard. In the event that a later version of the referenced Standard/Specification is published, reference should be made to the latest published version.
k. Legacy VESA Standard, superseded by DisplayID Standard.
l. See vesa.org/vesa-member/downloads/.

1.7 Overview

A DP link is composed of the following:

- Main-Link

  The Main-Link is a unidirectional, high-bandwidth, low-latency channel that is used to transport isochronous data streams, such as uncompressed video and audio.

- AUX_CH

  The AUX_CH is a half-duplex, bidirectional channel that is used for link and device management.

- Hot Plug Detect (HPD) signal line

  The HPD signal also serves as an interrupt request by the DP Sink device.

In addition, the DP connector for a box-to-box connection has a power pin that is used for powering a local device.

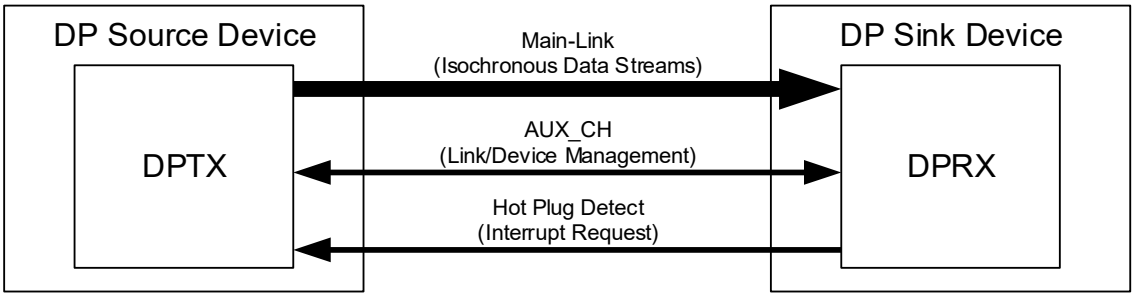


Figure 1-1: DP Data Transport Channels

1.7.1 Main-Link Composition

Updated in *DP v2.0*.

The Main-Link is composed of one, two, or four AC-coupled, doubly terminated differential pairs (referred to as “lanes”). AC-coupling facilitates the silicon process migration because the DPTX and DPRX may have different common mode voltages.

With 8b/10b channel coding, four link rates are supported – 8.1, 5.4, 2.7, and 1.62Gbps/lane (equivalent to the HBR3, HBR2, HBR, and RBR bit rates, respectively). With 128b/132b channel coding, new to *DP v2.0*, three link rates are supported – 20, 13.5, and 10Gbps/lane (equivalent to UHBR20, UHBR13.5, and UHBR10, respectively). All enabled lanes shall operate at the same link rate. The link rate is decoupled from the pixel rate. DPTX and DPRX capabilities, the channel (or a cable) quality, and application bandwidth need determine the link rate .

Note: *6.75Gbps/lane link rate is supported between a MyDP Standard DPTX and DPRX.*

For a DP device that supports 8b/10b channel-coded link rates, support for the maximum link rate and all the link rates below that is mandated. For example, a DP device that supports the 8.1Gbps/lane link rate shall support 5.4, 2.7, and 1.62Gbps/lane link rates.

For a DP device that supports 128b/132b channel-coded link rates, support for the 10Gbps/lane link rate is mandated; support for the 13.5 and 20Gbps/lane link rates is **optional**. Support for the 13.5Gbps/lane link rate is **optional** for a DP device that supports the 20Gbps/lane link rate.

The Main-Link has one, two, or four lanes. The number of lanes is decoupled from the pixel bit depth (bits/pixel, or bpp) and component bit depth (bits/component, or bpc). Component bit depths of 6, 8, 10, 12, and 16bpc are supported with the pixel encoding formats of RGB, YCbCr 4:4:4 / 4:2:2 / 4:2:0, and Y-only in DisplayPort, regardless of the number of Main-Link lanes. For RAW pixel encoding format, bit depths of 6, 7, 8, 10, 12, 14, and 16bpp are supported.

All lanes carry data. There is no dedicated clock channel. The clock is extracted from the data stream itself, which is encoded with either 8b/10b or 128b/132b channel coding.

Source and Sink devices are allowed to support the minimum number of lanes needed by the Main-Link’s application bandwidth. The devices that support two lanes shall support both one and two lanes, while those that support four lanes shall support one, two, and four lanes. An external user-detachable cable shall support four lanes to maximize interoperability between the Source and Sink devices.

The DP Main-Link provides for the application bandwidth listed in Table 1-6.

Table 1-6: DP Main-Link Application Bandwidth

Channel Coding	Bit Rate	Link Rate (Gbps/lane)	# of Main-Link Lanes	Application Bandwidth[a] (MBps)
128b/132b New to *DP v2.0*.	UHBR20	20	One	2418
			Two	4835
			Four	9670
	UHBR13.5	13.5	One	1631
			Two	3263
			Four	6525
	UHBR10	10	One	1209
			Two	2418
			Four	4836
8b/10b	HBR3	8.1	One	810
			Two	1620
			Four	3240
	–	6.75[b]	One	675
	HBR2	5.4	One	540
			Two	1080
			Four	2160
	HBR	2.7	One	270
			Two	540
			Four	1080
	RBR	1.62	One	162
			Two	324
			Four	648

a. Also referred to as "link symbol rate."
b. 6.75Gbps/lane link rate is supported between a MyDP Standard DPTX and DPRX.

DP devices may freely trade pixel bit depth with pixel format and the frame rate of a stream within the available bandwidth.

The data mapping of a stream to the Main-Link is devised to facilitate the support of various lane counts. For example, the pixel data is packed and mapped over a 4-lane Main-Link, as listed in Table 1-7, regardless of the pixel bit depth and colorimetry format.

Table 1-7: Pixel Data Mapping over 4-lane Main-Link

Pixel Numbers	Lane Numbers
0, 4	0
1, 5	1
2, 6	2
3, 7	3

The stream data is packed into “micro-packets” which are referred to as “transfer units” in SST (Single-Stream Transport) mode and MTP (Multi-stream Transport Packet) in MST (Multi-Stream Transport) mode. After the stream data is packed and mapped to the Main-Link, the packed stream data rate shall be less than or equal to the Main-Link’s link symbol rate. When the packed stream data rate is less than the Main-Link’s link symbol rate, stuffing symbols are inserted.

1.7.2 AUX_CH Composition

The AUX_CH is composed of an AC-coupled, doubly terminated differential pair. Manchester-II coding is used as the channel coding for an AUX transaction over the AUX_CH. As is the case with the Main-Link, the clock is extracted from the data stream.

The AUX_CH has a half-duplex, bidirectional PHY Layer. The Source device is the master and the Sink device is the slave. A Sink device may toggle the HPD signal to prompt the Source device to initiate an AUX request transaction to read DPCD Link/Sink status register bits, including the IRQ_HPD Vector register bits.

The AUX_CH provides a data rate of 1Mbps over the supported cable lengths of up to 15m and longer. Each transaction takes no more than 500us, with a maximum 16-byte burst data size. This avoids AUX_CH contention problems by one application starving other applications.

1.7.3 Link Configuration and Management

When an HPD event occurs, the Source device configures the link through link training. The correct number of lanes is enabled at the correct link rate with the correct drive current and equalization level through AUX transactions between a DPTX and DPRX over the AUX_CH.

During normal operation following link training, the Sink device may notify a link status change, for example, loss of synchronization, by toggling the HPD signal for interrupt request signaling. The Source device then checks the DPCD Link/Sink Device Status registers using AUX transactions and then takes corrective action. This closed-loop operation enhances the robustness and interoperability between the Source and Sink devices.

Because the link rate is decoupled from the stream rate, the DP link may stay active and stable, even when the timing of a transported AV stream changes.

1.7.4 Layered Modular Architecture

Figure 1-2 illustrates the layered architecture of DisplayPort.

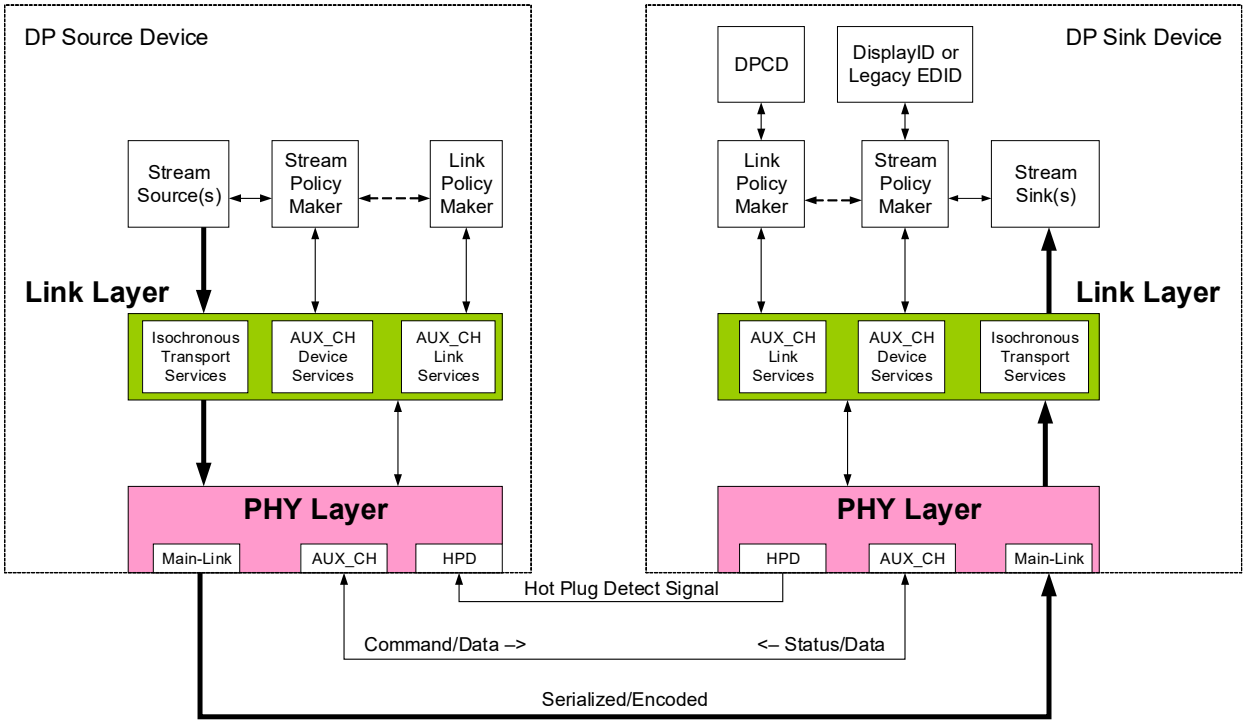


Figure 1-2: Layered DP Architecture

In Figure 1-2, DisplayPort Configuration Data (DPCD) in the Sink device describes the DPRX's capability, just as DisplayID or legacy EDID describes the stream sink's capability. Link and Stream Policy Makers manage the link and stream, respectively. Details (state machine, firmware, or system software) are implementation-specific.

Note: *At some future time, the PHY Layer may be replaced while the Link Layer remains unchanged. This allows this Standard to evolve along with the technology to maintain its cost and performance position.*

Also, the micro-packet-based data transport enables a seamless extension of this Standard toward supporting multiple audio-visual streams and other data types. Switches and hubs may be used to route streams among multiple Source and Sink devices.

HDCP for DP r1.3 and *HDCP to DP r2.2* should be used when content protection is needed.

2 Link Layer Specifications

2.1 SST Mode with 8b/10b Link Layer Introduction

This section describes the services provided by the DP Link Layer in Single-Stream Transport (SST) mode (sub-sections within this section that are applicable to both SST and MST modes are explicitly noted in the sub-section titles):

- Isochronous transport services over the Main-Link

  Isochronous transport services, based on a micro-packet architecture, map the video and audio streams onto the Main-Link symbols with a set of rules (explained in Section 2.2) so that the streams can be correctly reconstructed in the original format and time base within the Sink device.

- Link and device management services over the AUX_CH

  Link services are used for discovering, configuring, and maintaining the link. The AUX transaction to access the DisplayPort Configuration Data (DPCD) address is used for these purposes. Device services support device-level applications, such as DisplayID or legacy EDID read and MCCS control. In addition, AUX transactions may be used for optional content protection.

In conjunction with the description of these services, AUX states/arbitration and transaction syntax are also described in this section.

The Link Layer provides services as instructed or requested by the Stream/Link Policy Makers, as illustrated in Figure 2-1. The Stream Policy Maker manages the transport of the stream. The Link Policy Maker manages the link and maintains link synchronization.

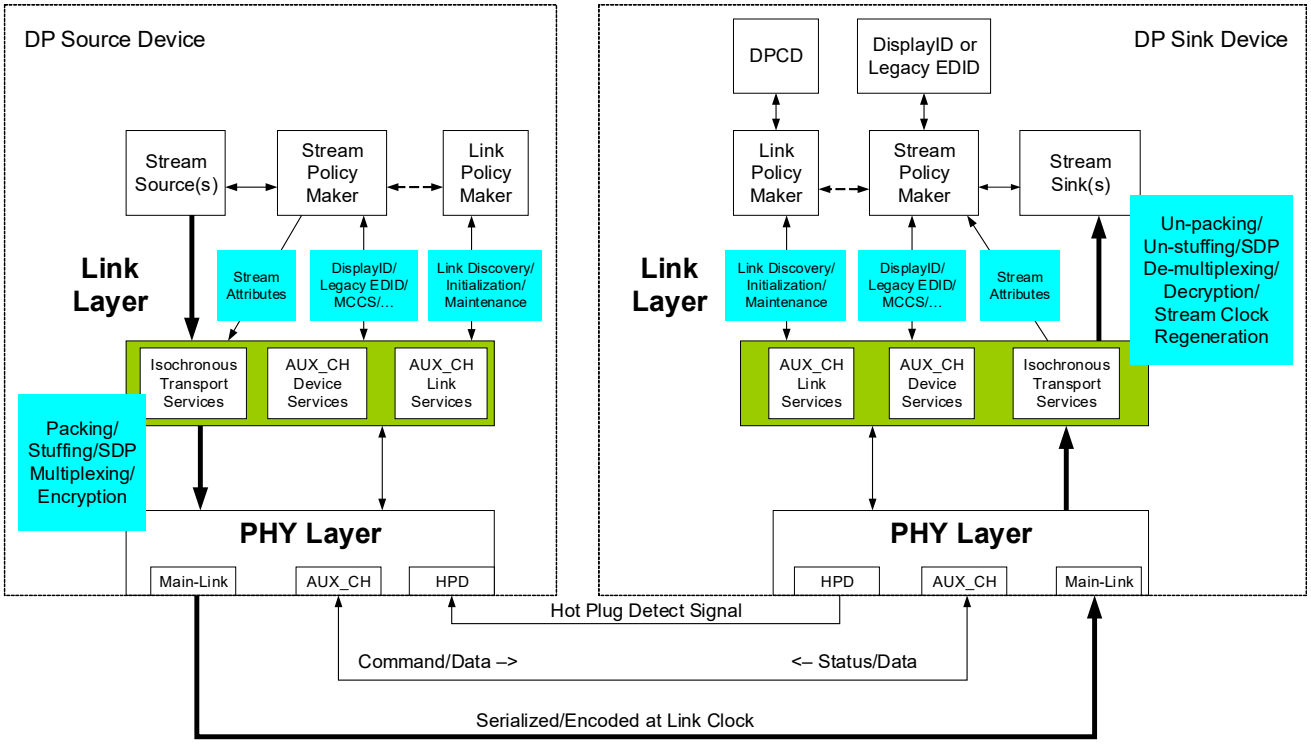


Figure 2-1: Link Layer Services Overview

In this section (and in the entire Standard), only the interactions between the policy makers and Link Layer are described. The syntax for these interactions (i.e., the API) is implementation-specific and beyond the scope of this Standard.

2.1.1 Number of Lanes and Per-lane Data Rate in SST and MST Modes

DisplayPort supports three options for the number of Main-Link lanes and four options for Main-Link data rate per lane, as follows:

- 4-, 2-, or 1-lane
- 8.1, 5.4, 2.7, or 1.62Gbps/lane

Note: *6.75Gbps/lane link rate is supported between a MyDP Standard DPTX and DPRX.*

The stream data to Main-Link symbols mapping is defined to facilitate the support of these lane count options.

The per-lane data rate is determined not only by the PHY Layer capabilities of DPTX and DPRX, but also by the quality of a channel consisting of PCB traces and/or a cable connector assembly.

A DP device with a DPRX shall indicate its receiver capability in the Receiver Capability registers (DPCD Addresses 00000h through 000FFh; see Table 2-183) and Extended Receiver Capability registers (DPCD Addresses 02200h through 022FFh; see Table 2-193), as described.

After reading the receiver capability, a DP device with a DPTX shall configure the link by writing to the Link Configuration field (DPCD Addresses 00100h through 001FFh; see Table 2-184) of the downstream device's DPRX, and then initiating link training.

Through this process of receiver capability discovery and link training, the upstream DP device and the downstream DP device are able to negotiate for the optimal lane count and per-lane data rate for a given connection.

2.1.2 Number of Main, Uncompressed Video Streams in SST Mode

The scope of this Standard is limited to the transport of a single, uncompressed video stream as the main video stream, with the optional insertion of SDPs such as an Audio_Stream SDP.

2.1.3 Basic Functions in SST and MST Modes

The basic functions of DP devices are as follows:

- **DPTX function** – Transmitter of Main-Link symbols
- **DPRX function** – Receiver of Main-Link symbols
- **Stream source function** – Sourcing of stream data
- **Stream sink function** – Sinking (i.e., consuming) of stream data

2.1.4 DP Device Types and Link Topology in SST Mode

A device contains at least one DP function, as well as other functions such as a stream source, display, speakers, recording device, or even an entire computer.

Table 2-1 lists the device types covered by this Standard.

Table 2-1: Device Types Covered by this Standard

Device Type		Description	Illustrated In
Source		Device that contains one or more stream source functions and DPTX functions and is a root in a DP tree topology.	
Sink		Device that contains one or more DPRX functions and one or more stream sink functions and is a leaf in a DP topology.	
Branch	DP Repeater (one input, one output)	Branch device that contains one DPRX and one DPTX.	Figure 2-3
	DP-to-Legacy Protocol Converter (one input, one output)	Branch device that contains one DPRX and one legacy TX.	Figure 2-4
	Legacy-to-DP Protocol Converter (one input, one output)	Branch device that contains one legacy RX and one DPTX. From the point of view of a DP topology, appears as a DP Source device.	Figure 2-5
	Input Switch (*k* DPRXs and one DPTX, where *k* is a positive integer >1)	Branch device that operates as a DP Repeater after a single DPRX is selected.	Figure 2-6
	Output Switch (one DPRX and *k* DPTXs/legacy TXs, where *k* is a positive integer > 1)	Branch device. Unlike a DP Replicator, only one DPTX (or legacy TX) is selected at a time. After one TX is selected, operates either as a DP Repeater or DP-to-Legacy Protocol Converter.	Figure 2-7
	DP Replicator (one DPRX and *k* DPTXs, where *k* is a positive integer > 1)	Branch device that may include one or more legacy protocol converter TXs.	
	DP Composite Sink	Branch device with a stream sink function. For example, a display that has one or more downstream-facing ports (DFPs). A stream format protocol converter that alters the stream format is regarded as a Composite Sink device.	

DP devices with a DPTX and/or DPRX shall have a Link Policy Maker. A DP Source device that originates or processes (e.g., stream format conversion) the stream data, and DP Sink devices, shall also have a Stream Policy Maker.

Note: *A device containing only the PHY Layer circuit of a DPRX and DPTX (i.e., DPRX_PHY and DPTX_PHY) is referred to as a "PHY Repeater" or "cable extender." Hybrid devices that perform the interface media protocol converter function (e.g., between electrical and optical) are typically built as cable extender devices.*

DP devices with a DPRX shall have DPCD registers. Sink devices and Composite Sink devices shall also have DisplayID or legacy EDID.

Using the device types listed in Table 2-1, DP networks consisting of a single link or multiple links (daisy chain or tree) may be configured.

From the perspective of the device location within a link, the devices are categorized as listed in Table 2-2.

Table 2-2: Topological Device Categories

Device Category	Device Type
Root	Source
Leaf	Sink
Intermediate	Branch devices listed in Table 2-1

The DP Source device needs to read the receiver capability (DPCD RX Capability registers), the stream sink capability (DisplayID or legacy EDID), and speaker presence (MCCS) from its downstream device to source a stream accordingly.

Figure 2-2 through Figure 2-7 illustrate DP link topology examples.

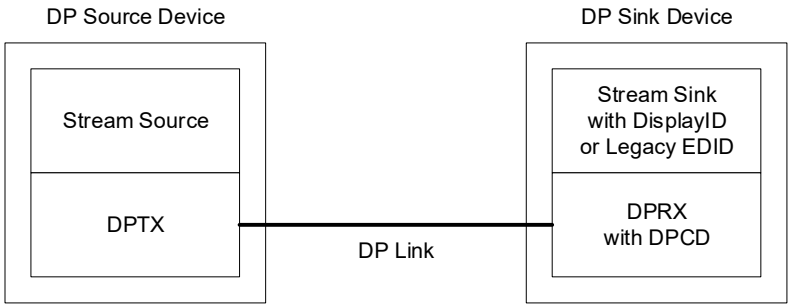


Figure 2-2: Single DP Link

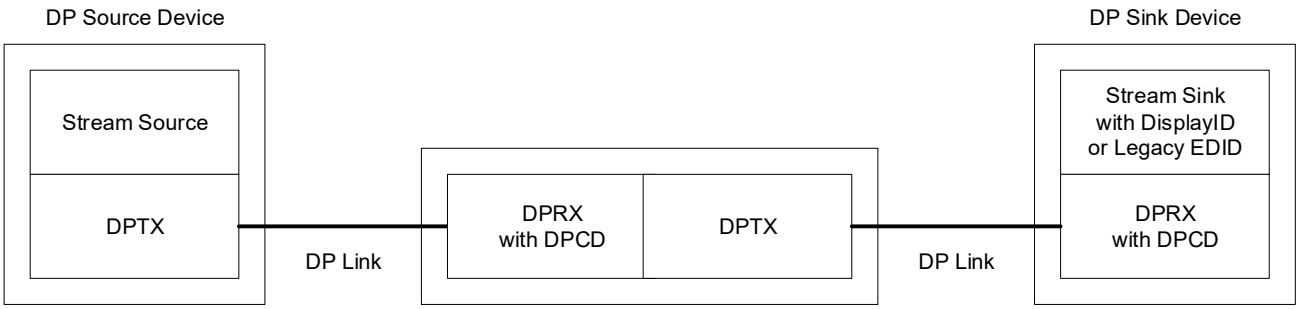


Figure 2-3: DP Source-to-Sink Device by way of a DP Repeater

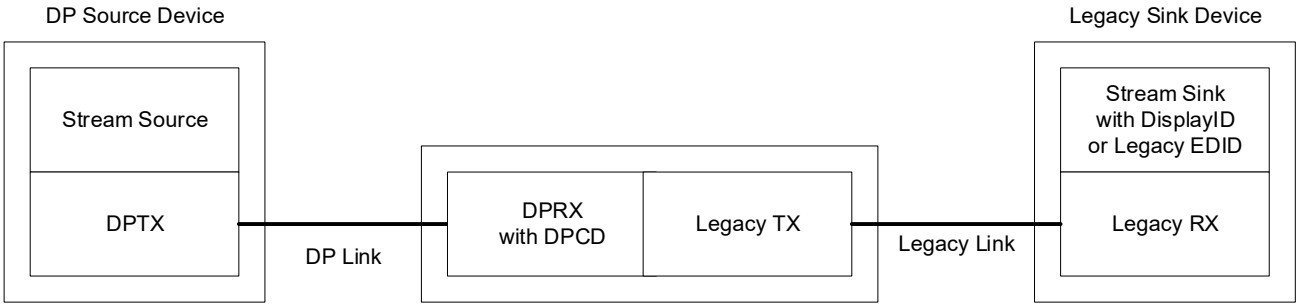


Figure 2-4: DP Source-to-Legacy Sink Device by way of a DP-to-Legacy Protocol Converter

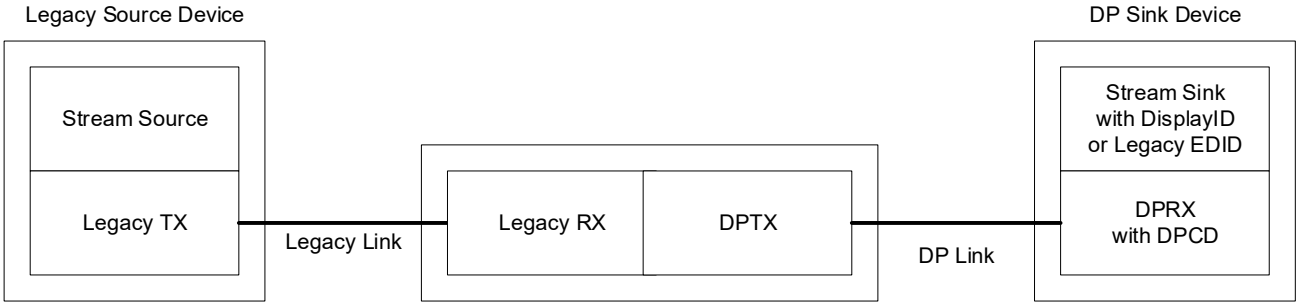


Figure 2-5: Legacy Source-to-DP Sink Device by way of a Legacy-to-DP Protocol Converter

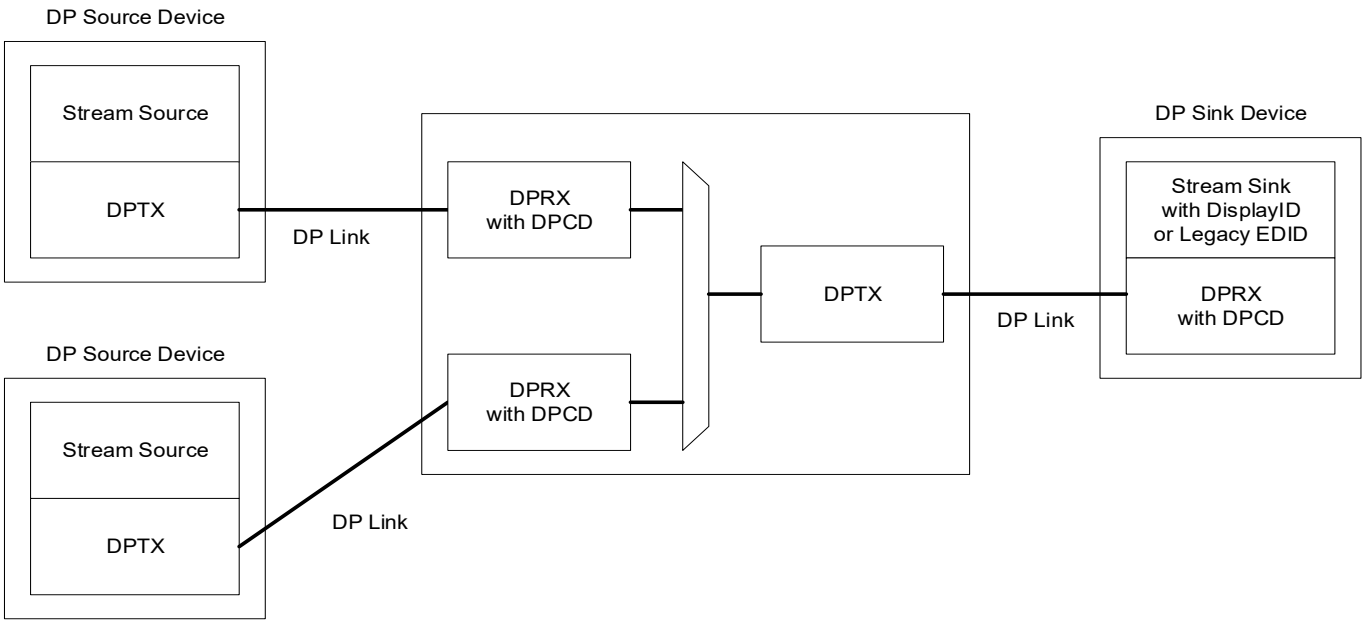


Figure 2-6: Multiple DP Source Devices to DP Sink Device by way of an Input Switch

When only one DPTX is selected at a given time, a Replicator device (as illustrated in Figure 2-7) becomes an Output Switch device.

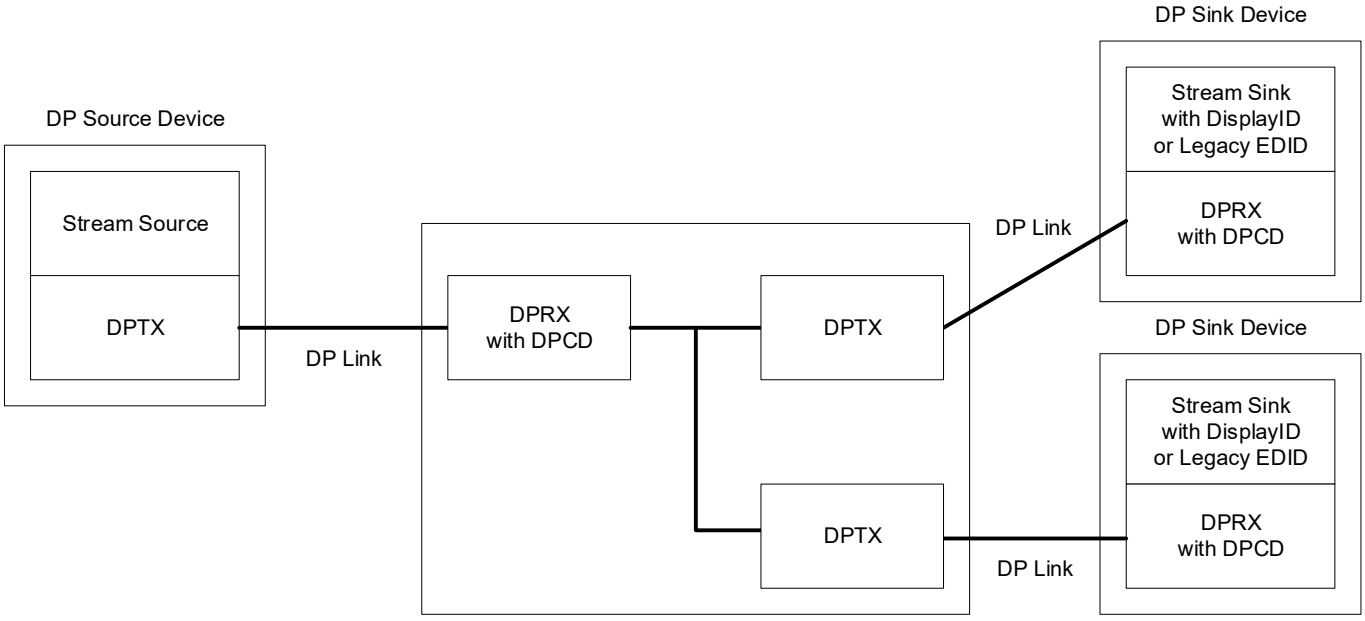


Figure 2-7: DP Source Device to Multiple DP Sink Devices by way of a DP Replicator/Output Switch

2.1.4.1 DisplayID or Legacy EDID and DPCD Access Handling by SST-only Mode Branch Devices

Upon a DisplayID or legacy EDID read by the DP Source device, a Branch device shall reply with the downstream DP Sink device's DisplayID or legacy EDID.

The DP Repeater shall update the 8b/10b_MAX_LINK_RATE and MAX_LANE_COUNT register (DPCD Addresses 00001h and 00002h, respectively) values to those of the downstream device's DPRX when both of the following conditions exist:

- DP Repeater is incapable of changing the link rate and lane count from the upstream link to the downstream link
- 8b/10b_MAX_LINK_RATE and MAX_LANE_COUNT register values of the downstream device's DPRX are smaller than those of the DP Repeater's DPRX

In case the DP Repeater is capable of programming the DFP's link rate and lane count independent of the upstream-facing port's (UFP's) link rate and lane count, and the downstream device is a DP Sink device, the DP Branch device does **not** need to update the Receiver Capability field registers (DPCD Addresses 00000h through 000FFh; see Table 2-183).

The description of the following two cases explains the rationale behind the above:

- **Case A – Maximum link bandwidth of the DP Branch device's DPRX is greater than or equal to the downstream DP Sink device's DPRX**

  The DP Sink device shall have the maximum link bandwidth that covers all the video timing formats that are declared in its DisplayID or legacy EDID. Because the DP Source device selects the video timing format from those listed in the DisplayID or legacy EDID, the maximum link bandwidth of the DP Sink device's DPRX does not gate the transmission of the video stream.

- **Case B – Maximum link bandwidth of the DP Branch device's DPRX is less than or equal to the downstream DP Sink device's DPRX**

  The DP Source device shall select the video timing format whose stream bandwidth fits within the maximum link bandwidth of the DP Branch device's DPRX

In case the DP Repeater is capable of programming the DFP's link rate and lane count independent of the UFP's link rate and lane count, and the downstream device is a DP-to-legacy downstream device, the DP Repeater shall update the following DFP Capability registers:

- DOWN_STREAM_PORT_PRESENT register(s) (DPCD Addresses 00005h and 02205h)
- Detailed Capabilities Info registers (DPCD Addresses 00080h through 0008Fh), including the maximum pixel clock rate and pixel bit depth of the downstream legacy transmitter

The reason is that when both of the following conditions exist, a DP Source device can choose to transmit a video stream whose stream bandwidth exceeds the DP-to-Legacy protocol converter DPRX's maximum link bandwidth:

- 8b/10b_MAX_LINK_RATE and MAX_LANE_COUNT register values of the DP Repeater's DPRX are larger than those of the DP-to-Legacy protocol converter's DPRX
- DisplayID or legacy EDID of a legacy Sink device plugged into the DP-to-Legacy protocol converter declaring support for video formats whose stream bandwidth mandates exceed the link bandwidth of the DP-to-legacy protocol converter's DPRX

A DP-to-Legacy protocol converter shall report the maximum pixel clock and pixel bit depth of the DFP legacy transmitter that fit within the link bandwidth of its DPRX. By the DP Repeater's copying the DP-to-Legacy protocol converter's DFP capability registers, the stream bandwidth transmitted by the DP Source device is kept within the DP-to-Legacy protocol converter's DPRX link bandwidth limit.

2.1.4.1.1 DisplayID or Legacy EDID and DPCD Access Handling by SST-only Replicator Device

A DP Replicator device shall use the DisplayID or legacy EDID and DPCD of the lowest DFP number that has the connected downstream device.

2.1.4.1.2 DisplayID or Legacy EDID and DPCD Access Handling by SST-only Composite Sink Device (Informative)

DisplayID or legacy EDID and DPCD access handling by a composite device is implementation-specific. For example, the composite device may reply with the DisplayID or legacy EDID of its own Sink device and may choose to not comprehend the DPCD of its downstream link.

Note: *In SST mode, this Standard does not currently define a mechanism through which the upstream device can read multiple DisplayID or legacy EDIDs of Sink devices connected to Branch device(s).*

2.1.4.2 Docking Station (Informative)

A docking station is either a Replicator device or a Composite Sink device (with format converting function) embedded in a Source device. Because it is embedded, the management policy is implementation-specific and beyond the scope of this Standard.

2.2 Isochronous Transport Services in SST Mode with 8b/10b Link Layer

The isochronous transport services of the Link Layer provide the following:

- Mapping of stream data to and from the Main-Link lanes
  - Packing and unpacking
  - Stuffing and unstuffing
  - Framing and unframing
  - Inter-lane skewing and de-skewing
- Stream clock regeneration
- Insertion of Main Stream Attribute (MSA) data
- **Optional** insertion Secondary-data Packet (SDP) with ECC
  - Audio_Stream SDP
  - *CTA-861-G* INFOFRAME SDP

2.2.1 Main Video Stream to Main-Link Lane Mapping in the Source Device

The Main-Link shall have one, two, or four lanes, with each lane capable of transporting eight bits of data per link symbol clock (LS_Clk). MSA data (the uncompressed video stream) shall be packed, stuffed, and framed. The data may also be multiplexed with SDPs and inter-lane skewed before the data is handed over to the PHY Layer after the Link Layer data mapping for transport over the Main-Link. The stream data shall enter the Link Layer at the original stream clock (Strm_Clk) rate and be delivered to the PHY Layer at the LS_Clk rate after this mapping.

Figure 2-8 and Figure 2-9 illustrate the data mapping in DP Source (DPTX) and Sink (DPRX) devices, respectively.

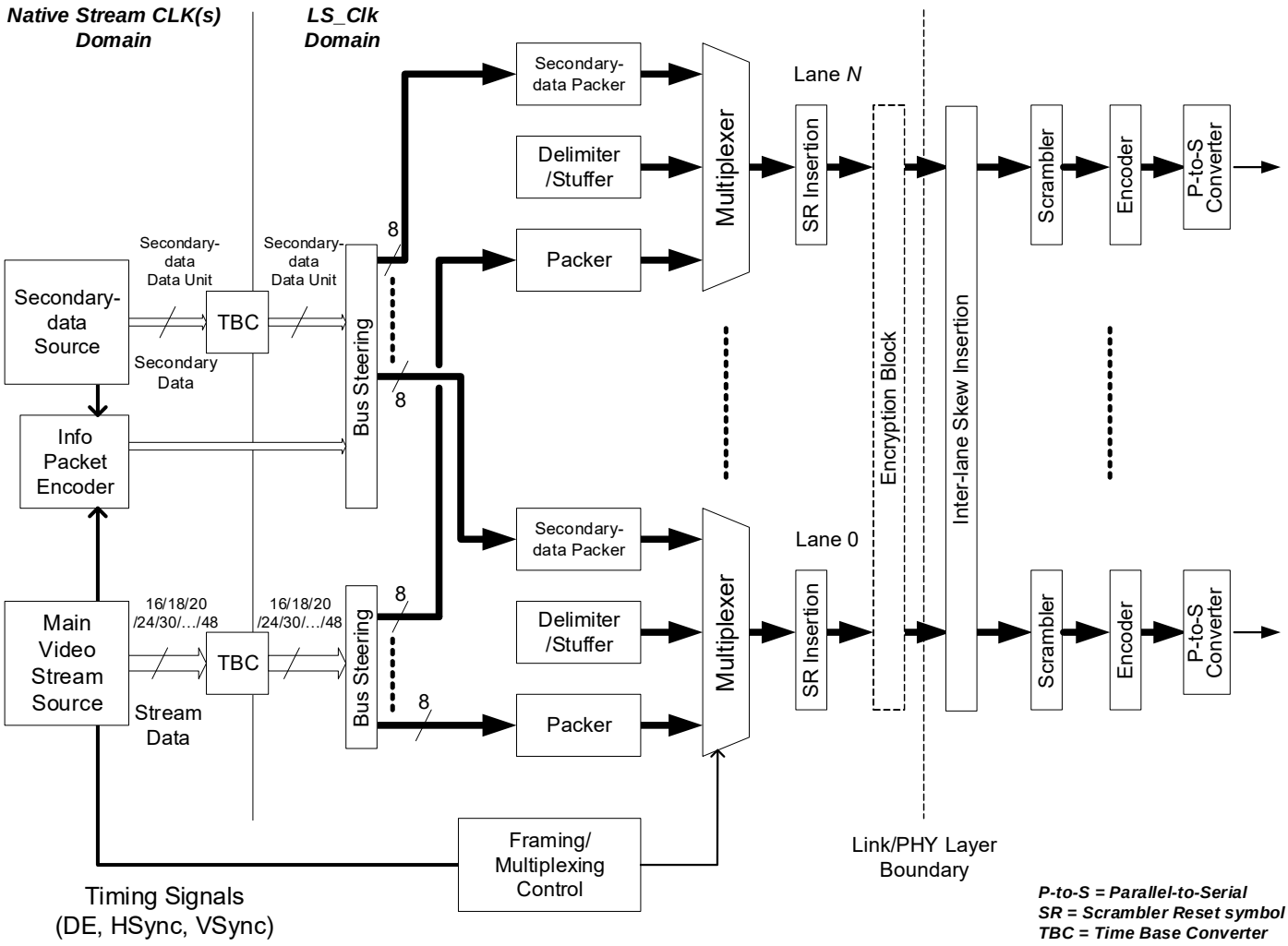


Figure 2-8: DPTX Main-Link Data Path High-Level Block Diagram

Notes: *Logic block diagram. Actual implementation may vary.*

ECC and CP encryption blocks are both ***optional****. To support SDPs, however, ECC shall be supported.*

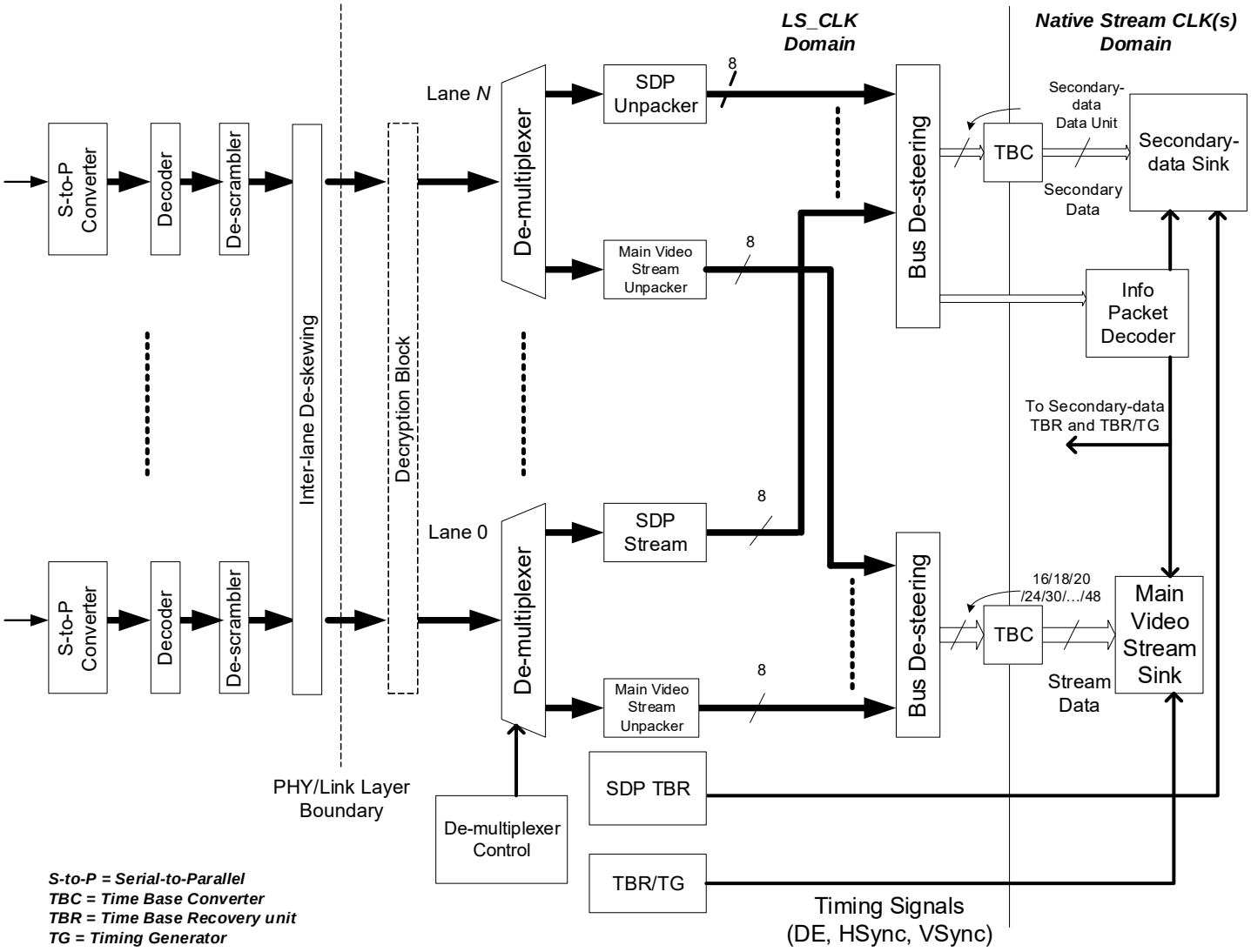


Figure 2-9: DPRX Main-Link Data Path High-Level Block Diagram

Notes: *Logic block diagram. Actual implementation may vary.*

ECC and CP decryption blocks are both ***optional****. To support SDPs, however, ECC shall be supported except for the Extension SDP (Section 2.2.5.4).*

Main-Link data mapping shall occur in the following order:

1 Main video stream data packing, stuffing, and framing.

2 Optional secondary-data framing and multiplexing.

2.2.1.1 Default Framing Mode Control Link Symbols

The use of Default Framing mode is deprecated. Table 2-3 lists the default framing mode symbols for the sake of completeness only.

Table 2-3: Default Framing Mode Control Link Symbols

Symbol	Name	Description
BS	Blanking Start	For a DPRX of DPCD r1.2 or higher, Enhanced Framing mode[a] shall be used when running in SST mode. An upstream device interoperating with a downstream device with DPCD r1.2 or higher shall enable Enhanced Framing mode. Blanking Start consists of a 4-symbol sequence on each lane: • Inserted after the last active pixel during the vertical display period. • Inserted at the same symbol time during vertical blanking period as during vertical display. • This framing symbol shall be periodically (every 2^{13} or 8192 symbols) inserted for active links with no main video stream data to transmit. In this condition, the BS symbol is immediately followed by the NoVideoStream_Flag bit in the VB-ID (bit 3) set to 1. (For more information on VB-ID, see Section 2.2.1.) This link symbol pattern is referred to as the "Idle Pattern."
BE	Blanking End	Inserted immediately before the first active pixel of a line only during the vertical display period.
FS	Fill Start	• Inserted at the beginning of stuffing symbols in the transfer unit. • Omitted when there is only one stuffing symbol. In this case, FE (Fill End) is inserted without FS. • FS and FE are inserted with no stuffing data symbols in between when there are only two stuffing symbols. ***Note:*** *Transfer unit is described in Section 2.2.1.4.1.*
FE	Fill End	Inserted at the end of stuffing symbols within transfer unit.
SS	Secondary-data Start	Inserted at the beginning of secondary-data.
SE	Secondary-data End	Inserted at the end of secondary-data.
SR	Scrambler Reset	For a DPRX of DPCD r1.2 or higher, Enhanced Framing mode[a] shall be used when running in SST mode. An upstream device interoperating with a downstream device of DPCD r1.2 or higher shall enable Enhanced Framing mode. In Enhanced Framing Mode, the Scrambler Reset consists of four symbol sequence on each lane. Every 512th BS symbol shall be replaced with an SR symbol by a DPTX to reset the LFSR of the scrambler.

Table 2-3: Default Framing Mode Control Link Symbols (Continued)

Symbol	Name	Description
CPBS	Content Protection BS	For a DPRX of DPCD r1.2 or higher, Enhanced Framing mode shall be used when running in SST mode. An upstream device interoperating with a downstream device of DPCD r1.2 or higher shall enable Enhanced Framing mode. In Enhanced Framing mode, the Content Protection BS consists of a 4-symbol sequence on each lane. Used by a CP system. Replaced by "CP" in Enhanced Framing mode.[a]
CPSR	Content Protection SR	For a DPRX of DPCD r1.2 or higher, Enhanced Framing mode shall be used when running in SST mode. An upstream device interoperating with a downstream device of DPCD r1.2 or higher shall enable Enhanced Framing mode. In Enhanced Framing mode, the Content Protection SR consists of a 4-symbol sequence on each lane. Used by a CP system. CPSR resets the LFSR of the scrambler just as SR does. Replaced by "BF" in Enhanced Framing mode.[a]

a. Enhanced Framing mode and its control link symbols are described in Section 2.2.1.2.

These control link symbols shall be inserted in all lanes within the same LS_Clk cycle (before they are inter-lane skewed by 2 LS_Clk cycles just before going to the PHY Layer). The Link Layer shall distinguish these control link symbols from data symbols so that the PHY Layer can properly encode these control link symbols using "special characters."

For example, the Link Layer may use the ninth bit to indicate whether the accompanying 8-bit data represents control link symbols or data symbols. There are many ways for the Link Layer to implement this distinction, the method used is implementation-specific and beyond the scope of this Standard.

2.2.1.2 Enhanced Framing Mode Control Link Symbols

Table 2-4 lists the control link symbols that are used for Enhanced Framing mode. (See Table 2-3 for framing symbol descriptions.) A DPRX shall support Enhanced Framing mode, and therefore set the ENHANCED_FRAME_CAP bit in the MAX_LANE_COUNT register (DPCD Address 00002h, bit 7). A DPTX shall always enable Enhanced Framing mode by writing 1 to the ENHANCED_FRAME_EN bit in the LANE_COUNT_SET register (DPCD Address 00101h, bit 7).

Table 2-4: Default Framing Mode (Deprecated) to Enhanced Framing Mode Control Link Symbol Mapping

Default Framing Mode Symbols (Deprecated)	Enhanced Framing Mode Symbols[a]
BS	BS + BF + BF + BS
SR	SR + BF + BF + SR
CPBS (CP in Enhanced Framing mode)	BS + CP + CP + BS
CPSR (BF in Enhanced Framing mode)	SR + CP + CP + SR
BE	BE (no change)
FS	FS (no change)
FE	FE (no change)
SS	SS (no change)
SE	SE (no change)

a. See Section 3.5.1.1 for control link symbol-to-8b/10b special character mapping.

These control link symbols shall be inserted in all lanes within the same LS_Clk cycle (before the symbols are inter-lane skewed by two LS_Clk cycles just before going to the PHY Layer). The Link Layer shall distinguish these control link symbols from data symbols so that the PHY Layer can use special characters to properly encode these control link symbols.

For example, the Link Layer can use the ninth bit to indicate whether the accompanying 8-bit data represents control link symbols or data symbols. There are many ways for the Link Layer to implement this distinction – the method used is implementation-specific and beyond the scope of this Standard.

When a DPTX is transmitting the Idle Pattern, the DPTX shall insert the 4-symbol sequence of BS (or SR) every 2^{13} or 8192 symbols. In other words, there shall be 8188 symbols between the last (fourth) symbol of the 4-symbol sequence for BS (or SR) and the first symbol of the next 4-symbol sequence.

Every 512th BS symbol sequence shall be replaced with an SR symbol sequence. The last symbol of the 4-symbol sequence for SR shall be used to reset the scrambler.

When switching between the Idle Pattern transmission and a stream transmission, the Source device shall avoid any overlap of the four symbols for BS and SR.

2.2.1.3 Main Video Stream Data Packing

The Link Layer shall first steer pixel data in a pixel-within-lane manner, as described in Table 2-5.

Table 2-5: Pixel Steering into Main-Link Lanes

# of Lanes	Pixel Steering[a]
Four	Pixel 4*N* to Lane 0 Pixel 4*N* + 1 to Lane 1 Pixel 4*N* + 2 to Lane 2 Pixel 4*N* + 3 to Lane 3
Two	Pixel 2*N* to Lane 0 Pixel 2*N* + 1 to Lane 1
One	All pixels to Lane 0

a. N is 0 or a positive integer.

These rules apply regardless of the color space/pixel bit depth of the video stream. As illustrated in Figure 2-10, the first set of active partial pixel data of a line shall follow the BE control link symbol.

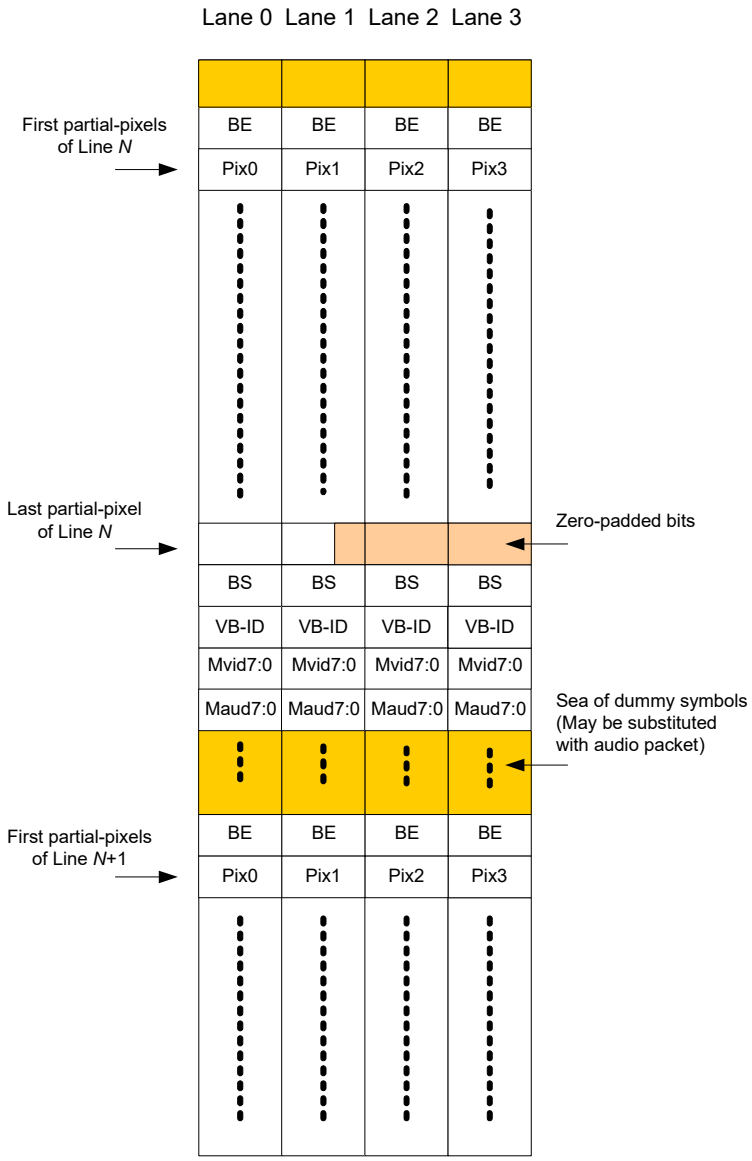


Figure 2-10: Main Video Stream Data Packing Example for a 4-Lane Main-Link

When there is no audio stream transported, Maud[7:0] shall be cleared to 00h. When there is no video stream transported, Mvid[7:0] shall be cleared to 00h.

During the last symbol time for a line of pixel data, there may be insufficient pixel data to provide data on all lanes of the link. The DPTX shall transmit 0s for those bits (zero-padded bits).

Immediately following the last symbol period of a line of data, the BS control link symbol sequence shall be inserted on all lanes of the link.

The Sink device, knowing the number of active pixels per horizontal line (from the MSA), shall discard zero-padded bits as "don't care." Figure 2-10 illustrates that a new line shall always start with Pixel 0 on Lane 0 following BE.

The BS shall be followed on all lanes by VB-ID, Mvid[7:0], and Maud[7:0], as follows:

- VB-ID shall carry the following information:
  - Whether the main video stream is in the vertical display period or the vertical blanking period.
  - Whether the main video stream is in the odd or even field for interlaced video.
  - Whether the main video stream is interlaced or non-interlaced (progressive).
  - Whether the BS is inserted while no video stream is being transported. The symbols transmitted over the Main-Link when no video stream is active are described in Table 2-6.
  - Whether to mute the audio.
  - Whether the ensuing video active frame is DSC-compressed.
- **Mvid[7:0]**

  The least significant eight bits of the time stamp value Mvid for the video stream. When there is no video stream transported, these bits shall be cleared to 00h. The DP Sink device shall use the time stamp as a hint for pixel clock recovery.
- **Maud[7:0]**

  The least significant eight bits of the time stamp value Maud for the audio stream. When there is no audio stream transported, these bits shall be cleared to 00h. The DP Sink device shall use the time stamp as a hint for audio clock recovery.

Table 2-6: VB-ID Bit Definition

VB-ID Bit #	Bit Definition
0	**VerticalBlanking_Flag** Shall be set to 1 at the end of the last active line of a video frame and remain set during the vertical blanking period. A Source device may clear this bit in the VB-ID either immediately prior to the first active line of a video frame (i.e., the first BE of a video frame) or immediately after the first active line (i.e., the first BS ending the first active line of a video frame). A Sink device shall be able to handle either case. Also set to 1 when there is no video stream (as indicated by bit 3 being set to 1).
1	**FieldID_Flag** This bit shall be cleared or set, as follows: • Cleared to 0 after the last active line in the top field • Set to 1 after the last active line of the bottom field See Section 2.2.4.2 for top and bottom field definitions. For progressive (non-interlaced) video, there is no bottom video and this bit remains cleared to 0.
2	**Interlace_Flag** Shall be set to 1 when the main video stream is an interlaced video. For non-interlaced video or no video, this bit shall remain cleared to 0.
3	**NoVideoStream_Flag** Shall be set to 1 when preceding BS is inserted while no video stream is transported. When set to 1, the Mvid[7:0] value shall be "don't care." ***Note:*** *An audio stream may be transported regardless of whether main video stream is also being transported.*
4	**AudioMute_Flag** Shall be set to 1 when the audio is to be muted.
5	**HDCP SYNC DETECT** Used by HDCP-capable DPRXs to detect CP lock status. See *HDCP for DP r1.3* and *HDCP to DP r2.2*.
6	**CompressedStream_Flag** New to *DP v1.4* to support Display Stream Compression (DSC). (See Section 2.8.3.3 and Section 2.8.3.4 for details.)
7	**RESERVED** Read 0.

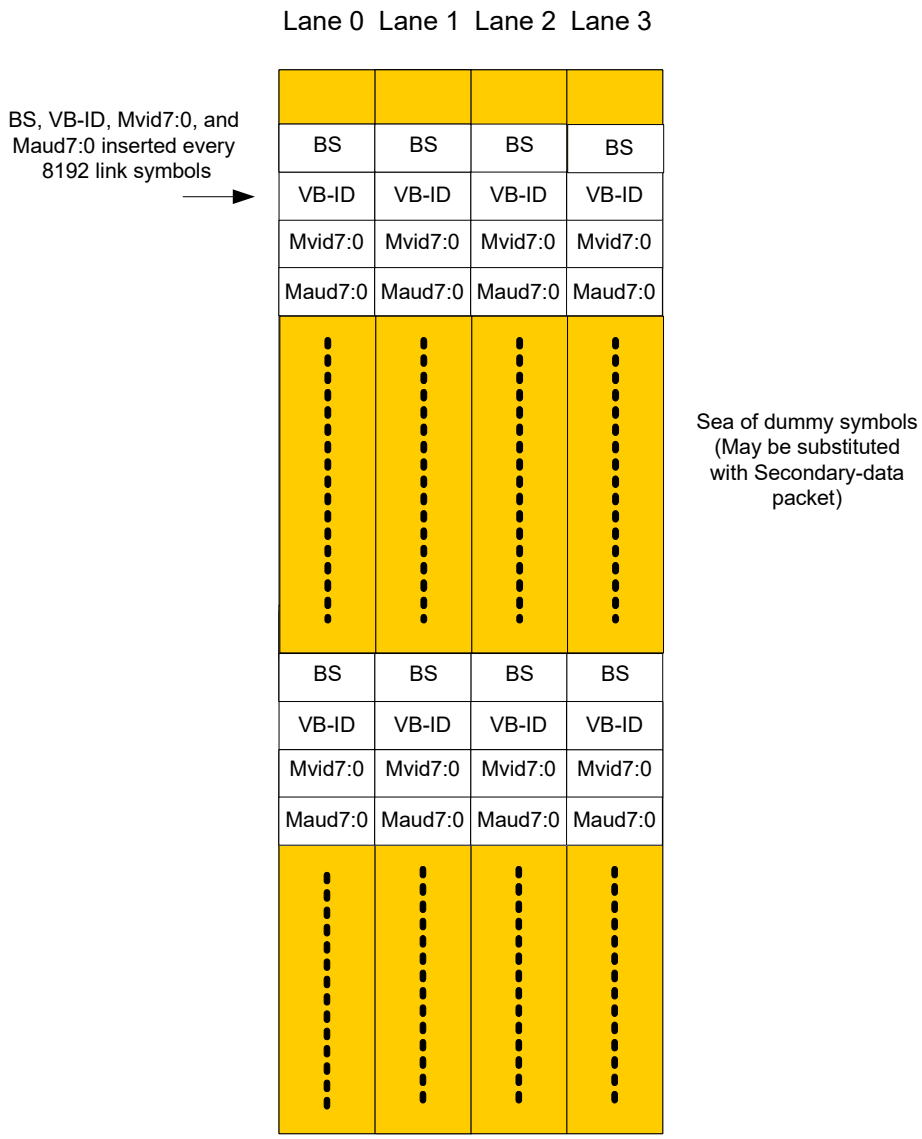


Figure 2-11: Link Symbols over the Main-Link without Main Video Stream

VB-ID, Mvid[7:0], and Maud[7:0] shall be transported four times, regardless of the number of lanes in the Main-Link, as illustrated in Figure 2-12.

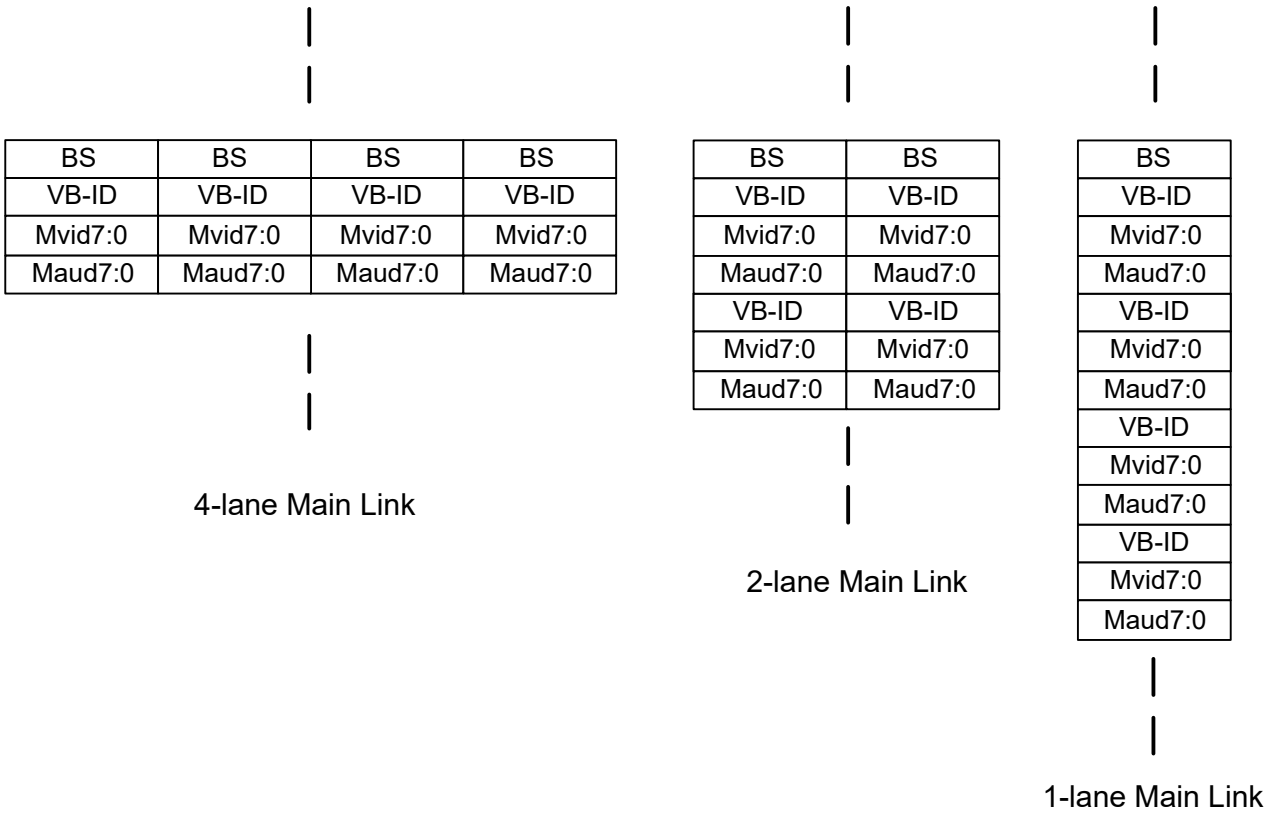


Figure 2-12: VB-ID, Mvid[7:0], and Maud[7:0] Packing over the Main-Link

If there is no audio stream, Maud[7:0] shall be cleared to 00h.

If there is no video stream, Mvid[7:0] shall be cleared to 00h.

Table 2-7 is an example of how a video stream with pixel format of 1366x768 and 10 bits/component (bpc) (= 30 bits/pixel (bpp)) RGB pixels are mapped to a 4-lane Main-Link.

Table 2-7: 10bpc RGB (30bpp) 1366x768 Packing to a 4-Lane Main-Link[a] [b]

Lane 0		Lane 1		Lane 2		Lane 3		
BE		BE		BE		BE		
R0-9:2		R1-9:2		R2-9:2		R3-9:2		<-- Start of Active Pixel
R0-1:0	G0-9:4	R1-1:0	G1-9:4	R2-1:0	G2-9:4	R3-1:0	G3-9:4	
G0-3:0	B0-9:6	G1-3:0	B1-9:6	G2-3:0	B2-9:6	G3-3:0	B3-9:6	
B0-5:0	R4-9:8	B1-5:0	R5-9:8	B2-5:0	R6-9:8	B3-5:0	R7-9:8	
R4-7:0		R5-7:0		R6-7:0		R7-7:0		
G4-9:2		G5-9:2		G6-9:2		G7-9:2		
G4-1:0	B4-9:4	G5-1:0	B5-9:4	G6-1:0	B6-9:4	G7-1:0	B7-9:4	
B4-3:0	R8-9:6	B5-3:0	R9-9:6	B6-3:0	R10-9:6	B7-3:0	R11-9:6	
R8-5:0	G8-9:8	R9-5:0	G9-9:8	R10-5:0	G10-9:8	R11-5:0	G11-9:8	
G8-7:0		G9-7:0		G10-7:0		G11-7:0		
B8-9:2		B9-9:2		B10-9:2		B11-9:2		
B8-1:0	R12-9:4	B9-1:0	R13-9:4	B10-1:0	R14-9:4	B11-1:0	R15-9:4	
R12-3:0	G12-9:6	R13-3:0	G13-9:6	R14-3:0	G14-9:6	R15-3:0	G15-9:6	
G12-5:0	B12-9:8	G13-5:0	B13-9:8	G14-5:0	B14-9:8	G15-5:0	B15-9:8	
B12-7:0		B13-7:0		B14-7:0		B15-7:0		

R1360-9:2		R1361-9:2		R1362-9:2		R1363-9:2		
R1360-1:0	G1360-9:4	R1361-1:0	G1361-9:4	R1362-1:0	G1362-9:4	R1363-1:0	G1363-9:4	
G1360-3:0	B1360-9:6	G1361-3:0	B1361-9:6	G1362-3:0	B1362-9:6	G1363-3:0	B1363-9:6	
B1360-5:0	R1364-9:8	B1361-5:0	R1365-9:8	B1362-5:0		B1363-5:0		
R1364-7:0		R1365-7:0						
G1364-9:2		G1365-9:2						
G1364-1:0	B1364-9:4	G1365-1:0	B1365-9:4					
B1364-3:0		B1365-3:0						<-- End of Active Pixel
BS		BS		BS		BS		
VB-ID		VB-ID		VB-ID		VB-ID		
Mvid[7:0]		Mvid[7:0]		Mvid[7:0]		Mvid[7:0]		
Maud[7:0]		Maud[7:0]		Maud[7:0]		Maud[7:0]		

a. R0-9:2 = red bits 9:2 of pixel, G = green, B = blue, BS = blanking start, BE = blanking end. VB-ID = video blanking ID. Mvid[7:0], and Maud[7:0] are portions of the time stamps for video and audio stream clocks.

b. Tan-shaded symbols and partial symbols indicate zero-padding.

The following sections describe how the data types listed below map into 4-, 2-, and 1-lane Main-Links:

- 6, 8, 10, 12, and 16bpc RGB pixels,
- 8, 10, 12, and 16bpc YCbCr4:4:4/4:2:2/4:2:0/Y-only, and
- 6, 7, 8, 10, 12, 14, and 16bpp RAW data

As defined in Table 2-8 through Table 2-34, when only one lane is enabled of either a 2- or 4-lane DP device, Lane 0 shall be enabled. When only two lanes are enabled, Lanes 0 and 1 shall be enabled.

2.2.1.3.1 6bpc RGB (18bpp)

Table 2-8 through Table 2-10 list 6bpc RGB stream mapping into 4-, 2-, and 1-lane Main-Links, respectively. Bit 5 of R0 is mapped to bit 7 of Lane 0 while bit 4 of G0 is mapped to bit 0 of Lane 0.

Table 2-8: 6bpc RGB Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
R0-5:0 | G0-5:4	R1-5:0 | G1-5:4	R2-5:0 | G2-5:4	R3-5:0 | G3-5:4
G0-3:0 | B0-5:2	G1-3:0 | B1-5:2	G2-3:0 | B2-5:2	G3-3:0 | B3-5:2
B0-1:0 | R4-5:0	B1-1:0 | R5-5:0	B2-1:0 | R6-5:0	B3-1:0 | R7-5:0
G4-5:0 | B4-5:4	G5-5:0 | B5-5:4	G6-5:0 | B6-5:4	G7-5:0 | B7-5:4
B4-3:0 | R8-5:2	B5-3:0 | R9-5:2	B6-3:0 | R10-5:2	B7-3:0 | R11-5:2
R8-1:0 | G8-5:0	R9-1:0 | G9-5:0	R10-1:0 | G10-5:0	R11-1:0 | G11-5:0
B8-5:0 | R12-5:4	B9-5:0 | R13-5:4	B10-5:0 | R14-5:4	B11-5:0 | R15-5:4
R12-3:0 | G12-5:2	R13-3:0 | G13-5:2	R14-3:0 | G14-5:2	R15-3:0 | G15-5:2
G12-1:0 | B12-5:0	G13-1:0 | B13-5:0	G14-1:0 | B14-5:0	G15-1:0 | B15-5:0

Table 2-9: 6bpc RGB Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
R0-5:0 | G0-5:4	R1-5:0 | G1-5:4
G0-3:0 | B0-5:2	G1-3:0 | B1-5:2
B0-1:0 | R2-5:0	B1-1:0 | R3-5:0
G2-5:0 | B2-5:4	G3-5:0 | B3-5:4
B2-3:0 | R4-5:2	B3-3:0 | R5-5:2
R4-1:0 | G4-5:0	R5-1:0 | G5-5:0
B4-5:0 | R6-5:4	B5-5:0 | R7-5:4
R6-3:0 | G6-5:2	R7-3:0 | G7-5:2
G6-1:0 | B6-5:0	G7-1:0 | B7-5:0

Table 2-10: 6bpc RGB Mapping to a 1-Lane Main-Link

Lane 0
R0-5:0 | G0-5:4
G0-3:0 | B0-5:2
B0-1:0 | R1-5:0
G1-5:0 | B1-5:4
B1-3:0 | R2-5:2

2.2.1.3.2 8bpc RGB/YCbCr 4:4:4 (24bpp)

Table 2-11 through Table 2-13 list 8bpc RGB/YCbCr 4:4:4 stream mapping into a 4-, 2-, or 1-lane Main-Link, respectively. Bit 7 of each color is mapped to bit 7 of each lane, while bit 0 of each color is mapped to bit 0 of each lane. For YCbCr 4:4:4, replace R with Cr, G with Y, and B with Cb.

Table 2-11: 8bpc RGB to a 4-Lane Main-Link Mapping

Lane 0	Lane 1	Lane 2	Lane 3
R0-7:0	R1-7:0	R2-7:0	R3-7:0
G0-7:0	G1-7:0	G2-7:0	G3-7:0
B0-7:0	B1-7:0	B2-7:0	B3-7:0
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-7:0	G5-7:0	G6-7:0	G7-7:0
B4-7:0	B5-7:0	B6-7:0	B7-7:0
R8-7:0	R9-7:0	R10-7:0	R11-7:0
G8-7:0	G9-7:0	G10-7:0	G11-7:0
B8-7:0	B9-7:0	B10-7:0	B11-7:0

Table 2-12: 8bpc RGB Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
R0-7:0	R1-7:0
G0-7:0	G1-7:0
B0-7:0	B1-7:0
R2-7:0	R3-7:0
G2-7:0	G3-7:0
B2-7:0	B3-7:0
R4-7:0	R5-7:0
G4-7:0	G5-7:0
B4-7:0	B5-7:0

Table 2-13: 8bpc RGB Mapping to a 1-Lane Main-Link

Lane 0
R0-7:0
G0-7:0
B0-7:0
R1-7:0
G1-7:0
B1-7:0

2.2.1.3.3 10bpc RGB/YCbCr 4:4:4 (30bpp)

Table 2-14 through Table 2-16 list 10bpc RGB/YCbCr 4:4:4 stream mapping into 4-, 2-, and 1-lane Main-Links, respectively. For YCbCr 4:4:4, replace R with Cr, G with Y, and B with Cb.

Table 2-14: 10bpc RGB Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
R0-9:2	R1-9:2	R2-9:2	R3-9:2
R0-1:0 | G0-9:4	R1-1:0 | G1-9:4	R2-1:0 | G2-9:4	R3-1:0 | G3-9:4
G0-3:0 | B0-9:6	G1-3:0 | B1-9:6	G2-3:0 | B2-9:6	G3-3:0 | B3-9:6
B0-5:0 | R4-9:8	B1-5:0 | R5-9:8	B2-5:0 | R6-9:8	B3-5:0 | R7-9:8
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-9:2	G5-9:2	G6-9:2	G7-9:2
G4-1:0 | B4-9:4	G5-1:0 | B5-9:4	G6-1:0 | B6-9:4	G7-1:0 | B7-9:4
B4-3:0 | R8-9:6	B5-3:0 | R9-9:6	B6-3:0 | R10-9:6	B7-3:0 | R11-9:6
R8-5:0 | G8-9:8	R9-5:0 | G9-9:8	R10-5:0 | G10-9:8	R11-5:0 | G11-9:8
G8-7:0	G9-7:0	G10-7:0	G11-7:0
B8-9:2	B9-9:2	B10-9:2	B11-9:2
B8-1:0 | R12-9:4	B9-1:0 | R13-9:4	B10-1:0 | R14-9:4	B11-1:0 | R15-9:4
R12-3:0 | G12-9:6	R13-3:0 | G13-9:6	R14-3:0 | G14-9:6	R15-3:0 | G15-9:6
G12-5:0 | B12-9:8	G13-5:0 | B13-9:8	G14-5:0 | B14-9:8	G15-5:0 | B15-9:8
B12-7:0	B13-7:0	B14-7:0	B15-7:0

Table 2-15: 10bpc RGB Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
R0-9:2	R1-9:2
R0-1:0 | G0-9:4	R1-1:0 | G1-9:4
G0-3:0 | B0-9:6	G1-3:0 | B1-9:6
B0-5:0 | R2-9:8	B1-5:0 | R3-9:8
R2-7:0	R3-7:0
G2-9:2	G3-9:2
G2-1:0 | B2-9:4	G3-1:0 | B3-9:4
B2-3:0 | R4-9:6	B3-3:0 | R5-9:6
R4-5:0 | G4-9:8	R5-5:0 | G5-9:8
G4-7:0	G5-7:0
B4-9:2	B5-9:2
B4-1:0 | R6-9:4	B5-1:0 | R7-9:4
R6-3:0 | G6-9:6	R7-3:0 | G7-9:6
G6-5:0 | B6-9:8	G7-5:0 | B7-9:8
B6-7:0	B7-7:0

Table 2-16: 10bpc RGB Mapping to a 1-Lane Main-Link

Lane 0
R0-9:2
R0-1:0 | G0-9:4
G0-3:0 | B0-9:6
B0-5:0 | R1-9:8
R1-7:0
G1-9:2
G1-1:0 | B1-9:4
B1-3:0 | R2-9:6

2.2.1.3.4 12bpc RGB/YCbCr 4:4:4 (36bpp)

Table 2-17 through Table 2-19 list 12bpc RGB/YCbCr 4:4:4 stream mapping into 4-, 2-, and 1-lane Main-Links, respectively. For YCbCr 4:4:4, replace R with Cr, G with Y, and B with Cb.

Table 2-17: 12bpc RGB Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
R0-11:4	R1-11:4	R2-11:4	R3-11:4
R0-3:0 | G0-11:8	R1-3:0 | G1-11:8	R2-3:0 | G2-11:8	R3-3:0 | G3-11:8
G0-7:0	G1-7:0	G2-7:0	G3-7:0
B0-11:4	B1-11:4	B2-11:4	B3-11:4
B0-3:0 | R4-11:8	B1-3:0 | R5-11:8	B2-3:0 | R6-11:8	B3-3:0 | R7-11:8
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-11:4	G5-11:4	G6-11:4	G7-11:4
G4-3:0 | B4-11:8	G5-3:0 | B5-11:8	G6-3:0 | B6-11:8	G7-3:0 | B7-11:8
B4-7:0	B5-7:0	B6-7:0	B7-7:0

Table 2-18: 12bpc RGB Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
R0-11:4	R1-11:4
R0-3:0 | G0-11:8	R1-3:0 | G1-11:8
G0-7:0	G1-7:0
B0-11:4	B1-11:4
B0-3:0 | R2-11:8	B1-3:0 | R3-11:8
R2-7:0	R3-7:0
G2-11:4	G3-11:4
G2-3:0 | B2-11:8	G3-3:0 | B3-11:8
B2-7:0	B3-7:0

Table 2-19: 12bpc RGB Mapping to a 1-Lane Main-Link

Lane 0
R0-11:4
R0-3:0 | G0-11:8
G0-7:0
B0-11:4
B0-3:0 | R1-11:8

2.2.1.3.5 16bpc RGB/YCbCr 4:4:4 (48bpp)

Table 2-20 through Table 2-22 list 16bpc RGB/YCbCr 4:4:4 stream mapping into 4-, 2-, and 1-lane Main-Links, respectively. For YCbCr 4:4:4, replace R with Cr, G with Y, and B with Cb.

Table 2-20: 16bpc RGB Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
R0-15:8	R1-15:8	R2-15:8	R3-15:8
R0-7:0	R1-7:0	R2-7:0	R3-7:0
G0-15:8	G1-15:8	G2-15:8	G3-15:8
G0-7:0	G1-7:0	G2-7:0	G3-7:0
B0-15:8	B1-15:8	B2-15:8	B3-15:8
B0-7:0	B1-7:0	B2-7:0	B3-7:0
R4-15:8	R5-15:8	R6-15:8	R7-15:8
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-15:8	G5-15:8	G6-15:8	G7-15:8
G4-7:0	G5-7:0	G6-7:0	G7-7:0
B4-15:8	B5-15:8	B6-15:8	B7-15:8
B4-7:0	B5-7:0	B6-7:0	B7-7:0

Table 2-21: 16bpc RGB Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
R0-15:8	R1-15:8
R0-7:0	R1-7:0
G0-15:8	G1-15:8
G0-7:0	G1-7:0
B0-15:8	B1-15:8
B0-7:0	B1-7:0
R2-15:8	R3-15:8
R2-7:0	R3-7:0
G2-15:8	G3-15:8
G2-7:0	G3-7:0
B2-15:8	B3-15:8
B2-7:0	B3-7:0

Table 2-22: 16bpc RGB Mapping to a 1-Lane Main-Link

Lane 0
R0-15:8
R0-7:0
G0-15:8
G0-7:0
B0-15:8
B0-7:0

2.2.1.3.6 8bpc YCbCr 4:2:2

Table 2-23 through Table 2-25 list 8bpc YCbCr 4:2:2 stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-23: 8bpc YCbCr 4:2:2 Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
Cb0-7:0	Cr0-7:0	Cb2-7:0	Cr2-7:0
Y0-7:0	Y1-7:0	Y2-7:0	Y3-7:0
Cb4-7:0	Cr4-7:0	Cb6-7:0	Cr6-7:0
Y4-7:0	Y5-7:0	Y6-7:0	Y7-7:0
Cb8-7:0	Cr8-7:0	Cb10-7:0	Cr10-7:0
Y8-7:0	Y9-7:0	Y10-7:0	Y11-7:0

Table 2-24: 8bpc YCbCr 4:2:2 Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
Cb0-7:0	Cr0-7:0
Y0-7:0	Y1-7:0
Cb2-7:0	Cr2-7:0
Y2-7:0	Y3-7:0
Cb4-7:0	Cr4-7:0
Y4-7:0	Y5-7:0
Cb6-7:0	Cr6-7:0
Y6-7:0	Y7-7:0
Cb8-7:0	Cr8-7:0
Y8-7:0	Y9-7:0
Cb10-7:0	Cr10-7:0
Y10-7:0	Y11-7:0

Table 2-25: 8bpc YCbCr 4:2:2 Mapping to a 1-Lane Main-Link

Lane 0
Cb0-7:0
Y0-7:0
Cr0-7:0
Y1-7:0
Cb2-7:0
Y2-7:0

2.2.1.3.7 10bpc YCbCr 4:2:2

Table 2-26 through Table 2-28 list 10bpc YCbCr 4:2:2 stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-26: 10bpc YCbCr 4:2:2 Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
Cb0-9:2	Cr0-9:2	Cb2-9:2	Cr2-9:2
Cb0-1:0 | Y0-9:4	Cr0-1:0 | Y1-9:4	Cb2-1:0 | Y2-9:4	Cr2-1:0 | Y3-9:4
Y0-3:0 | Cb4-9:6	Y1-3:0 | Cr4-9:6	Y2-3:0 | Cb6-9:6	Y3-3:0 | Cr6-9:6
Cb4-5:0 | Y4-9:8	Cr4-5:0 | Y5-9:8	Cb6-5:0 | Y6-9:8	Cr6-5:0 | Y7-9:8
Y4-7:0	Y5-7:0	Y6-7:0	Y7-7:0
Cb8-9:2	Cr8-9:2	Cb10-9:2	Cr10-9:2
Cb8-1:0 | Y8-9:4	Cr8-1:0 | Y9-9:4	Cb10-1:0 | Y10-9:4	Cr10-1:0 | Y11-9:4
Y8-3:0 | Cb12-9:6	Y9-3:0 | Cr12-9:6	Y10-3:0 | Cb14-9:6	Y11-3:0 | Cr14-9:6
Cb12-5:0 | Y12-9:8	Cr12-5:0 | Y13-9:8	Cb14-5:0 | Y14-9:8	Cr14-5:0 | Y15-9:8
Y12-7:0	Y13-7:0	Y14-7:0	Y15-7:0

Table 2-27: 10bpc YCbCr 4:2:2 Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
Cb0-9:2	Cr0-9:2
Cb0-1:0 | Y0-9:4	Cr0-1:0 | Y1-9:4
Y0-3:0 | Cb2-9:6	Y1-3:0 | Cr2-9:6
Cb2-5:0 | Y2-9:8	Cr2-5:0 | Y3-9:8
Y2-7:0	Y3-7:0
Cb4-9:2	Cr4-9:2
Cb4-1:0 | Y4-9:4	Cr4-1:0 | Y5-9:4
Y4-3:0 | Cb6-9:6	Y5-3:0 | Cr6-9:6
Cb4-5:0 | Y6-9:8	Cr6-5:0 | Y7-9:8
Y6-7:0	Y7-7:0

Table 2-28: 10bpc YCbCr 4:2:2 Mapping to a 1-Lane Main-Link

Lane 0
Cb0-9:2
Cb0-1:0 | Y0-9:4
Y0-3:0 | Cr0-9:6
Cr0-5:0 | Y1-9:8
Y1-7:0

2.2.1.3.8 12bpc YCbCr 4:2:2

Table 2-29 through Table 2-31 list 12bpc YCbCr 4:2:2 stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-29: 12bpc YCbCr 4:2:2 Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
Cb0-11:4	Cr0-11:4	Cb2-11:4	Cr2-11:4
Cb0-3:0 | Y0-11:8	Cr0-3:0 | Y1-11:8	Cb2-3:0 | Y2-11:8	Cr2-3:0 | Y3-11:8
Y0-7:0	Y1-7:0	Y2-7:0	Y3-7:0
Cb4-11:4	Cr4-11:4	Cb6-11:4	Cr6-11:4
Cb4-3:0 | Y4-11:8	Cr4-3:0 | Y5-11:8	Cb63:0 | Y6-11:8	Cr6-3:0 | Y7-11:8
Y4-7:0	Y5-7:0	Y6-7:0	Y7-7:0

Table 2-30: 12bpc YCbCr 4:2:2 Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
Cb0-11:4	Cr0-11:4
Cb0-3:0 | Y0-11:8	Cr0-3:0 | Y1-11:8
Y0-7:0	Y1-7:0
Cb2-11:4	Cr2-11:4
Cb2-3:0 | Y2-11:8	Cr2-3:0 | Y3-11:8
Y2-7:0	Y3-7:0

Table 2-31: 12bpc YCbCr 4:2:2 Mapping to a 1-Lane Main-Link

Lane 0
Cb0-11:4
Cb0-3:0 | Y0-11:8
Y0-7:0
Cr0-11:4
Cr0-3:0 | Y1-11:8
Y1-7:0

2.2.1.3.9 16bpc YCbCr 4:2:2

Table 2-32 through Table 2-34 list 16bpc YCbCr 4:2:2 stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-32: 16bpc YCbCr 4:2:2 Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
Cb0-15:8	Cr0-15:8	Cb2-15:8	Cr2-15:8
Cb0-7:0	Cr0-7:0	Cb2-7:0	Cr2-7:0
Y0-15:8	Y1-15:8	Y2-15:8	Y3-15:8
Y0-7:0	Y1-7:0	Y2-7:0	Y3-7:0
Cb4-15:8	Cr4-15:8	Cb6-15:8	Cr6-15:8
Cb4-7:0	Cr4-7:0	Cb6-7:0	Cr6-7:0
Y4-15:8	Y5-15:8	Y6-15:8	Y7-15:8
Y4-7:0	Y5-7:0	Y6-7:0	Y7-7:0

Table 2-33: 16bpc YCbCr 4:2:2 Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
Cb0-15:8	Cr0-15:8
Cb0-7:0	Cr0-7:0
Y0-15:8	Y1-15:8
Y0-7:0	Y1-7:0
Cb2-15:8	Cr2-15:8
Cb2-7:0	Cr2-7:0
Y2-15:8	Y3-15:8
Y2-7:0	Y3-7:0

Table 2-34: 16bpc YCbCr 4:2:2 Mapping to a 1-Lane Main-Link

Lane 0
Cb0-15:8
Cb0-7:0
Y0-15:8
Y0-7:0
Cr0-15:8
Cr0-7:0
Y1-15:8
Y1-7:0

2.2.1.3.10 8bpc YCbCr 4:2:0

Table 2-35 through Table 2-40 list 8bpc YCbCr 4:2:0 stream mapping into 4-, 2-, and 1-lane Main-Links, respectively (two tables per each lane count, one for even lines, and one for odd lines). Y0_1 means Luminance (Y) of Pixel 1 of Line 0.

Table 2-35: 8bpc YCbCr 4:2:0 Even Lines (Starting with Line 0) over Four Main-Link Lanes

Lane 0	Lane 1	Lane 2	Lane 3
Y0_1-7:0	Y0_3-7:0	Y0_5-7:0	Y0_7-7:0
Y0_0-7:0	Y0_2-7:0	Y0_4-7:0	Y0_6-7:0
Cb0_0-7:0	Cb0_2-7:0	Cb0_4-7:0	Cb0_6-7:0
Y0_9-7:0	Y0_11-7:0	Y0_13-7:0	Y0_15-7:0
Y0_8-7:0	Y0_10-7:0	Y0_12-7:0	Y0_14-7:0
Cb0_8-7:0	Cb0_10-7:0	Cb0_12-7:0	Cb0_14-7:0

Table 2-36: 8bpc YCbCr 4:2:0 Odd Lines (Starting with Line 0) over Four Main-Link Lanes

Lane 0	Lane 1	Lane 2	Lane 3
Y1_1-7:0	Y1_3-7:0	Y1_5-7:0	Y1_7-7:0
Y1_0-7:0	Y1_2-7:0	Y1_4-7:0	Y1_6-7:0
Cr0_0-7:0	Cr0_2-7:0	Cr0_4-7:0	Cr0_6-7:0
Y1_9-7:0	Y1_11-7:0	Y1_13-7:0	Y1_15-7:0
Y1_8-7:0	Y1_10-7:0	Y1_12-7:0	Y1_14-7:0
Cr0_8-7:0	Cr0_10-7:0	Cr0_12-7:0	Cr0_14-7:0

Table 2-37: 8bpc YCbCr 4:2:0 Even Lines (Starting with Line 0) over Two Main-Link Lanes

Lane 0	Lane 1
Y0_1-7:0	Y0_3-7:0
Y0_0-7:0	Y0_2-7:0
Cb0_0-7:0	Cb0_2-7:0
Y0_5-7:0	Y0_7-7:0
Y0_4-7:0	Y0_6-7:0
Cb0_4-7:0	Cb0_6-7:0

Table 2-38: 8bpc YCbCr 4:2:0 Odd Lines (Starting with Line 0) over Two Main-Link Lanes

Lane 0	Lane 1
Y1_1-7:0	Y1_3-7:0
Y1_0-7:0	Y1_2-7:0
Cr0_0-7:0	Cr0_2-7:0
Y1_5-7:0	Y1_7-7:0
Y1_4-7:0	Y1_6-7:0
Cr0_4-7:0	Cr0_6-7:0

Table 2-39: 8bpc YCbCr 4:2:0 Even Lines (Starting with Line 0) over One Main-Link Lane

Lane 0
Y0_1-7:0
Y0_0-7:0
Cb0_0-7:0
Y0_3-7:0
Y0_2-7:0
Cb0_2-7:0

Table 2-40: 8bpc YCbCr 4:2:0 Odd Lines (Starting with Line 0) over One Main-Link Lane

Lane 0
Y1_1-7:0
Y1_0-7:0
Cr0_0-7:0
Y1_3-7:0
Y1_2-7:0
Cr0_2-7:0

2.2.1.3.11 10bpc YCbCr 4:2:0

Table 2-41 through Table 2-46 list 10bpc YCbCr 4:2:0 stream mapping into 4-, 2-, and 1-lane Main-Links, respectively (two tables per each lane count, one for even lines, and one for odd lines). Y0_1 means Luminance (Y) of Pixel 1 of Line 0.

Table 2-41: 10bpc YCbCr 4:2:0 Even Lines (Starting with Line 0) over Four Main-Link Lanes

Lane 0	Lane 1	Lane 2	Lane 3
Y0_1-9:2	Y0_3-9:2	Y0_5-9:2	Y0_7-9:2
Y0_1-1:0 | Y0_0-9:4	Y0_3-1:0 | Y0_2-9:4	Y0_5-1:0 | Y0_4-9:4	Y0_7-1:0 | Y0_6-9:4
Y0_0-3:0 | Cb0_0-9:6	Y0_2-3:0 | Cb0_2-9:6	Y0_4-3:0 | Cb0_4-9:6	Y0_6-3:0 | Cb0_6-9:6
Cb0_0-5:0 | Y0_9-9:8	Cb0_2-5:0 | Y0_11-9:8	Cb0_4-5:0 | Y0_13-9:8	Cb0_6-5:0 | Y0_15-9:8
Y0_9-7:0	Y0_11-7:0	Y0_13-7:0	Y0_15-7:0
Y0_8-9:2	Y0_10-9:2	Y0_12-9:2	Y0_14-9:2
Y0_8-1:0 | Cb0_8-9:4	Y0_10-1:0 | Cb0_10-9:4	Y0_12-1:0 | Cb0_12-9:4	Y0_14-1:0 | Cb0_14-9:4
Cb0_8-3:0 | Y0_17-9:6	Cb0_10-3:0 | Y0_19-9:6	Cb0_12-3:0 | Y0_21-9:6	Cb0_14-3:0 | Y0_23-9:6
Y0_17-5:0 | Y0_16-9:8	Y0_19-5:0 | Y0_18-9:8	Y0_21-5:0 | Y0_20-9:8	Y0_23-5:0 | Y0_22-9:8
Y0_16-7:0	Y0_18-7:0	Y0_20-7:0	Y0_22-7:0

Table 2-42: 10bpc YCbCr 4:2:0 Odd Lines (Starting with Line 0) over Four Main-Link Lanes

Lane 0	Lane 1	Lane 2	Lane 3
Y1_1-9:2	Y1_3-9:2	Y1_5-9:2	Y1_7-9:2
Y1_1-1:0 | Y1_0-9:4	Y1_3-1:0 | Y1_2-9:4	Y1_5-1:0 | Y1_4-9:4	Y1_7-1:0 | Y1_6-9:4
Y1_0-3:0 | Cr0_0-9:6	Y1_2-3:0 | Cr0_2-9:6	Y1_4-3:0 | Cr0_4-9:6	Y1_6-3:0 | Cr0_6-9:6
Cr0_0-5:0 | Y1_9-9:8	Cr0_2-5:0 | Y1_11-9:8	Cr0_4-5:0 | Y1_13-9:8	Cr0_6-5:0 | Y1_15-9:8
Y1_9-7:0	Y1_11-7:0	Y1_13-7:0	Y1_15-7:0
Y1_8-9:2	Y1_10-9:2	Y1_12-9:2	Y1_14-9:2
Y1_8-1:0 | Cr0_8-9:4	Y1_10-1:0 | Cr0_10-9:4	Y1_12-1:0 | Cr0_12-9:4	Y1_14-1:0 | Cr0_14-9:4
Cr0_8-3:0 | Y1_17-9:6	Cr0_10-3:0 | Y1_19-9:6	Cr0_12-3:0 | Y1_21-9:6	Cr0_14-3:0 | Y1_23-9:6
Y1_17-5:0 | Y1_16-9:8	Y1_19-5:0 | Y1_18-9:8	Y1_21-5:0 | Y1_20-9:8	Y1_23-5:0 | Y1_22-9:8
Y1_16-7:0	Y1_18-7:0	Y1_20-7:0	Y1_22-7:0

Table 2-43: 10bpc YCbCr 4:2:0 Even Lines (Starting with Line 0) over Two Main-Link Lanes

Lane 0	Lane 1
Y0_1-9:2	Y0_3-9:2
Y0_1-1:0 | Y0_0-9:4	Y0_3-1:0 | Y0_2-9:4
Y0_0-3:0 | Cb0_0-9:6	Y0_2-3:0 | Cb0_2-9:6
Cb0_0-5:0 | Y0_5-9:8	Cb0_2-5:0 | Y0_7-9:8
Y0_5-7:0	Y0_7-7:0
Y0_4-9:2	Y0_6-9:2
Y0_4-1:0 | Cb0_4-9:4	Y0_6-1:0 | Cb0_6-9:4
Cb0_4-3:0 | Y0_9-9:6	Cb0_6-3:0 | Y0_11-9:6
Y0_9-5:0 | Y0_8-9:8	Y0_11-5:0 | Y0_10-9:8
Y0_8-7:0	Y0_10-7:0

Table 2-44: 10bpc YCbCr 4:2:0 Odd Lines (Starting with Line 0) over Two Main-Link Lanes

Lane 0	Lane 1
Y1_1-9:2	Y1_3-9:2
Y1_1-1:0 | Y1_0-9:4	Y1_3-1:0 | Y1_2-9:4
Y1_0-3:0 | Cr0_0-9:6	Y1_2-3:0 | Cr0_2-9:6
Cr0_0-5:0 | Y1_5-9:8	Cr0_2-5:0 | Y1_7-9:8
Y1_5-7:0	Y1_7-7:0
Y1_4-9:2	Y1_6-9:2
Y1_4-1:0 | Cr0_4-9:4	Y1_6-1:0 | Cr0_6-9:4
Cr0_4-3:0 | Y1_9-9:6	Cr0_6-3:0 | Y1_11-9:6
Y1_9-5:0 | Y1_8-9:8	Y1_11-5:0 | Y1_10-9:8
Y1_8-7:0	Y1_10-7:0

Table 2-45: 10bpc YCbCr 4:2:0 Even Lines (Starting with Line 0) over One Main-Link Lane

Lane 0
Y0_1-9:2
Y0_1-1:0 | Y0_0-9:4
Y0_0-3:0 | Cb0_0-9:6
Cb0_0-5:0 | Y0_3-9:8
Y0_3-7:0
Y0_2-9:2
Y0_2-1:0 | Cb0_2-9:4
Cb0_2-3:0 | Y0_5-9:6
Y0_5-5:0 | Y0_4-9:8
Y0_4-7:0

Table 2-46: 10bpc YCbCr 4:2:0 Odd Lines (Starting with Line 0) over One Main-Link Lane

Lane 0
Y1_1-9:2
Y1_1-1:0 | Y1_0-9:4
Y1_0-3:0 | Cr0_0-9:6
Cr0_0-5:0 | Y1_3-9:8
Y1_3-7:0
Y1_2-9:2
Y1_2-1:0 | Cr0_2-9:4
Cr0_2-3:0 | Y1_5-9:6
Y1_5-5:0 | Y1_4-9:8
Y1_4-7:0

2.2.1.3.12 12bpc YCbCr 4:2:0

Table 2-47 through Table 2-52 list 12bpc YCbCr 4:2:0 stream mapping into 4-, 2-, and 1-lane Main-Links, respectively (two tables per each lane count, one for even lines, and one for odd lines). Y0_1 means Luminance (Y) of Pixel 1 of Line 0.

Table 2-47: 12bpc YCbCr 4:2:0 Even Lines (Starting with Line 0) over Four Main-Link Lanes

Lane 0	Lane 1	Lane 2	Lane 3
Y0_1-11:4	Y0_3-11:4	Y0_5-11:4	Y0_7-11:4
Y0_1-3:0 | Y0_0-11:8	Y0_3-3:0 | Y0_2-11:8	Y0_5-3:0 | Y0_4-11:8	Y0_7-3:0 | Y0_6-11:8
Y0_0-7:0	Y0_2-7:0	Y0_4-7:0	Y0_6-7:0
Cb0_0-11:4	Cb0_2-11:4	Cb0_4-11:4	Cb0_6-11:4
Cb0_0-3:0 | Y0_9-11:8	Cb0_2-3:0 | Y0_11-11:8	Cb0_4-3:0 | Y0_13-11:8	Cb0_6-3:0 | Y0_15-11:8
Y0_9-7:0	Y0_11-7:0	Y0_13-7:0	Y0_15-7:0
Y0_8-11:4	Y0_10-11:4	Y0_12-11:4	Y0_14-11:4
Y0_8-3:0 | Cb0_8-11:8	Y0_10-3:0 | Cb0_10-11:8	Y0_12-3:0 | Cb0_12-11:8	Y0_14-3:0 | Cb0_14-11:8
Cb0_8-7:0	Cb0_10-7:0	Cb0_12-7:0	Cb0_14-7:0

Table 2-48: 12bpc YCbCr 4:2:0 Odd Lines (Starting with Line 0) over Four Main-Link Lanes

Lane 0	Lane 1	Lane 2	Lane 3
Y1_1-11:4	Y1_3-11:4	Y1_5-11:4	Y1_7-11:4
Y1_1-3:0 | Y1_0-11:8	Y1_3-3:0 | Y1_2-11:8	Y1_5-3:0 | Y1_4-11:8	Y1_7-3:0 | Y1_6-11:8
Y1_0-7:0	Y1_2-7:0	Y1_4-7:0	Y1_6-7:0
Cr0_0-11:4	Cr0_2-11:4	Cr0_4-11:4	Cr0_6-11:4
Cr0_0-3:0 | Y1_9-11:8	Cr0_2-3:0 | Y1_11-11:8	Cr0_4-3:0 | Y1_13-11:8	Cr0_6-3:0 | Y1_15-11:8
Y1_9-7:0	Y1_11-7:0	Y1_13-7:0	Y1_15-7:0
Y1_8-11:4	Y1_10-11:4	Y1_12-11:4	Y1_14-11:4
Y1_8-3:0 | Cr0_8-11:8	Y1_10-3:0 | Cr0_10-11:8	Y1_12-3:0 | Cr0_12-11:8	Y1_14-3:0 | Cr0_14-11:8
Cr0_8-7:0	Cr0_10-7:0	Cr0_12-7:0	Cr0_14-7:0

Table 2-49: 12bpc YCbCr 4:2:0 Even Lines (Starting with Line 0) over Two Main-Link Lanes

Lane 0	Lane 1
Y0_1-11:4	Y0_3-11:4
Y0_1-3:0 | Y0_0-11:8	Y0_3-3:0 | Y0_2-11:8
Y0_0-7:0	Y0_2-7:0
Cb0_0-11:4	Cb0_2-11:4
Cb0_0-3:0 | Y0_5-11:8	Cb0_2-3:0 | Y0_7-11:8
Y0_5-7:0	Y0_7-7:0
Y0_4-11:4	Y0_6-11:4
Y0_4-3:0 | Cb0_4-11:8	Y0_6-3:0 | Cb0_6-11:8
Cb0_4-7:0	Cb0_6-7:0

Table 2-50: 12bpc YCbCr 4:2:0 Odd Lines (Starting with Line 0) over Two Main-Link Lanes

Lane 0	Lane 1
Y1_1-11:4	Y1_3-11:4
Y1_1-3:0 | Y1_0-11:8	Y1_3-3:0 | Y1_2-11:8
Y1_0-7:0	Y1_2-7:0
Cr0_0-11:4	Cr0_2-11:4
Cr0_0-3:0 | Y1_5-11:8	Cr0_2-3:0 | Y1_7-11:8
Y1_5-7:0	Y1_7-7:0
Y1_4-11:4	Y1_6-11:4
Y1_4-3:0 | Cr0_4-11:8	Y1_6-3:0 | Cr0_6-11:8
Cr0_4-7:0	Cr0_6-7:0

Table 2-51: 12bpc YCbCr 4:2:0 Even Lines (Starting with Line 0) over One Main-Link Lane

Lane 0
Y0_1-11:4
Y0_1-3:0 | Y0_0-11:8
Y0_0-7:0
Cb0_0-11:4
Cb0_0-3:0 | Y0_3-11:8
Y0_3-7:0
Y0_2-11:4
Y0_2-3:0 | Cb0_2-11:8
Cb0_2-7:0

Table 2-52: 12bpc YCbCr 4:2:0 Odd Lines (Starting with Line 0) over One Main-Link Lane

Lane 0
Y1_1-11:4
Y1_1-3:0 | Y1_0-11:8
Y1_0-7:0
Cr0_0-11:4
Cr0_0-3:0 | Y1_3-11:8
Y1_3-7:0
Y1_2-11:4
Y1_2-3:0 | Cr0_2-11:8
Cr0_2-7:0

2.2.1.3.13 16bpc YCbCr 4:2:0

Table 2-53 through Table 2-58 list 16bpc YCbCr 4:2:0 stream mapping into 4-, 2-, and 1-lane Main-Links, respectively (two tables per each lane count, one for even lines, and one for odd lines). Y0_1 means Luminance (Y) of Pixel 1 of Line 0.

Table 2-53: 16bpc YCbCr 4:2:0 Even Lines (Starting with Line 0) over Four Main-Link Lanes

Lane 0	Lane 1	Lane 2	Lane 3
Y0_1-15:8	Y0_3-15:8	Y0_5-15:8	Y0_7-15:8
Y0_1-7:0	Y0_3-7:0	Y0_5-7:0	Y0_7-7:0
Y0_0-15:8	Y0_2-15:8	Y0_4-15:8	Y0_6-15:8
Y0_0-7:0	Y0_2-7:0	Y0_4-7:0	Y0_6-7:0
Cb0_0-15:8	Cb0_2-15:8	Cb0_4-15:8	Cb0_6-15:8
Cb0_0-7:0	Cb0_2-7:0	Cb0_4-7:0	Cb0_6-7:0
Y0_9-15:8	Y0_11-15:8	Y0_13-15:8	Y0_15-15:8
Y0_9-7:0	Y0_11-7:0	Y0_13-7:0	Y0_15-7:0
Y0_8-15:8	Y0_10-15:8	Y0_12-15:8	Y0_14-15:8
Y0_8-7:0	Y0_10-7:0	Y0_12-7:0	Y0_14-7:0
Cb0_8-15:8	Cb0_10-15:8	Cb0_12-15:8	Cb0_14-15:8
Cb0_8-7:0	Cb0_10-7:0	Cb0_12-7:0	Cb0_14-7:0

Table 2-54: 16bpc YCbCr 4:2:0 Odd Lines (Starting with Line 0) over Four Main-Link Lanes

Lane 0	Lane 1	Lane 2	Lane 3
Y1_1-15:8	Y1_3-15:8	Y1_5-15:8	Y1_7-15:8
Y1_1-7:0	Y1_3-7:0	Y1_5-7:0	Y1_7-7:0
Y1_0-15:8	Y1_2-15:8	Y1_4-15:8	Y1_6-15:8
Y1_0-7:0	Y1_2-7:0	Y1_4-7:0	Y1_6-7:0
Cr0_0-15:8	Cr0_2-15:8	Cr0_4-15:8	Cr0_6-15:8
Cr0_0-7:0	Cr0_2-7:0	Cr0_4-7:0	Cr0_6-7:0
Y1_9-15:8	Y1_11-15:8	Y1_13-15:8	Y1_15-15:8
Y1_9-7:0	Y1_11-7:0	Y1_13-7:0	Y1_15-7:0
Y1_8-15:8	Y1_10-15:8	Y1_12-15:8	Y1_14-15:8
Y1_8-7:0	Y1_10-7:0	Y1_12-7:0	Y1_14-7:0
Cr0_8-15:8	Cr0_10-15:8	Cr0_12-15:8	Cr0_14-15:8
Cr0_8-7:0	Cr0_10-7:0	Cr0_12-7:0	Cr0_14-7:0

Table 2-55: 16bpc YCbCr 4:2:0 Even Lines (Starting with Line 0) over Two Main-Link Lanes

Lane 0	Lane 1
Y0_1-15:8	Y0_3-15:8
Y0_1-7:0	Y0_3-7:0
Y0_0-15:8	Y0_2-15:8
Y0_0-7:0	Y0_2-7:0
Cb0_0-15:8	Cb0_2-15:8
Cb0_0-7:0	Cb0_2-7:0
Y0_5-15:8	Y0_7-15:8
Y0_5-7:0	Y0_7-7:0
Y0_4-15:8	Y0_6-15:8
Y0_4-7:0	Y0_6-7:0
Cb0_4-15:8	Cb0_6-15:8
Cb0_4-7:0	Cb0_6-7:0

Table 2-56: 16bpc YCbCr 4:2:0 Odd Lines (Starting with Line 0) over Two Main-Link Lanes

Lane 0	Lane 1
Y1_1-15:8	Y1_3-15:8
Y1_1-7:0	Y1_3-7:0
Y1_0-15:8	Y1_2-15:8
Y1_0-7:0	Y1_2-7:0
Cr0_0-15:8	Cr0_2-15:8
Cr0_0-7:0	Cr0_2-7:0
Y1_5-15:8	Y1_7-15:8
Y1_5-7:0	Y1_7-7:0
Y1_4-15:8	Y1_6-15:8
Y1_4-7:0	Y1_6-7:0
Cr0_4-15:8	Cr0_6-15:8
Cr0_4-7:0	Cr0_6-7:0

Table 2-57: 16bpc YCbCr 4:2:0 Even Lines (Starting with Line 0) over One Main-Link Lane

Lane 0
Y0_1-15:8
Y0_1-7:0
Y0_0-15:8
Y0_0-7:0
Cb0_0-15:8
Cb0_0-7:0
Y0_3-15:8
Y0_3-7:0
Y0_2-15:8
Y0_2-7:0
Cb0_2-15:8
Cb0_2-7:0

Table 2-58: 16bpc YCbCr 4:2:0 Odd Lines (Starting with Line 0) over One Main-Link Lane

Lane 0
Y1_1-15:8
Y1_1-7:0
Y1_0-15:8
Y1_0-7:0
Cr0_0-15:8
Cr0_0-7:0
Y1_3-15:8
Y1_3-7:0
Y1_2-15:8
Y1_2-7:0
Cr0_2-15:8
Cr0_2-7:0

2.2.1.3.14 8bpp Y-only

Table 2-59 through Table 2-61 list 8bpp Y-only stream mapping into 4-, 2-, and 1-lane Main-Links, respectively. Bit 7 of each color is mapped to bit 7 of each lane, while bit 0 of each color is mapped to bit 0 of each lane.

Table 2-59: 8bpp Y-only to a 4-Lane Main-Link Mapping

Lane 0	Lane 1	Lane 2	Lane 3
Y0-7:0	Y1-7:0	Y2-7:0	Y3-7:0
Y4-7:0	Y5-7:0	Y6-7:0	Y7-7:0

Table 2-60: 8bpp Y-only Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
Y0-7:0	Y1-7:0
Y2-7:0	Y3-7:0
Y4-7:0	Y5-7:0
Y6-7:0	Y7-7:0

Table 2-61: 8bpp Y-only Mapping to a 1-Lane Main-Link

Lane 0
Y0-7:0
Y1-7:0
Y2-7:0
Y3-7:0

2.2.1.3.15 10bpp Y-only

Table 2-62 through Table 2-64 list 10bpp Y-only stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-62: 10bpp Y-only Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
Y0-9:2	Y1-9:2	Y2-9:2	Y3-9:2
Y0-1:0 | Y4-9:4	Y1-1:0 | Y5-9:4	Y2-1:0 | Y6-9:4	Y3-1:0 | Y7-9:4
Y4-3:0 | Y8-9:6	Y5-3:0 | Y9-9:6	Y6-3:0 | Y10-9:6	Y7-3:0 | Y11-9:6
Y8-5:0 | Y12-9:8	Y9-5:0 | Y13-9:8	Y10-5:0 | Y14-9:8	Y11-5:0 | Y15-9:8
Y12-7:0	Y13-7:0	Y14-7:0	Y15-7:0

Table 2-63: 10bpp Y-only Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
Y0-9:2	Y1-9:2
Y0-1:0 | Y2-9:4	Y1-1:0 | Y3-9:4
Y2-3:0 | Y4-9:6	Y3-3:0 | Y5-9:6
Y4-5:0 | Y6-9:8	Y5-5:0 | Y7-9:8
Y6-7:0	Y7-7:0

Table 2-64: 10bpp Y-only Mapping to a 1-Lane Main-Link

Lane 0
Y0-9:2
Y0-1:0 | Y1-9:4
Y1-3:0 | Y2-9:6
Y2-5:0 | Y3-9:8
Y3-7:0

2.2.1.3.16 12bpp Y-only

Table 2-65 through Table 2-67 list 12bpp Y-only stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-65: 12bpp Y-only Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
Y0-11:4	Y1-11:4	Y2-11:4	Y3-11:4
Y0-3:0 | Y4-11:8	Y1-3:0 | Y5-11:8	Y2-3:0 | Y6-11:8	Y3-3:0 | Y7-11:8
Y4-7:0	Y5-7:0	Y6-7:0	Y7-7:0

Table 2-66: 12bpp Y-only Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
Y0-11:4	Y1-11:4
Y0-3:0 | Y2-11:8	Y1-3:0 | Y3-11:8
Y2-7:0	Y3-7:0

Table 2-67: 12bpp Y-only Mapping to a 1-Lane Main-Link

Lane 0
Y0-11:4
Y0-3:0 | Y1-11:8
Y1-7:0

2.2.1.3.17 16bpp Y-only

Table 2-68 through Table 2-70 list 16bpp Y-only stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-68: 16bpp Y-only Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
Y0-15:8	Y1-15:8	Y2-15:8	Y3-15:8
Y0-7:0	Y1-7:0	Y2-7:0	Y3-7:0
Y4-15:8	Y5-15:8	Y6-15:8	Y7-15:8
Y4-7:0	Y5-7:0	Y6-7:0	Y7-7:0

Table 2-69: 16bpp Y-only Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
Y0-15:8	Y1-15:8
Y0-7:0	Y1-7:0
Y2-15:8	Y3-15:8
Y2-7:0	Y3-7:0

Table 2-70: 16bpp Y-only Mapping to a 1-Lane Main-Link

Lane 0
Y0-15:8
Y0-7:0
Y1-15:8
Y1-7:0

2.2.1.3.18 6bpp RAW

Table 2-71 through Table 2-73 list 6bpp RAW stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-71: 6bpp RAW Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
RAW0-5:0 | RAW4-5:4	RAW1-5:0 | RAW5-5:4	RAW2-5:0 | RAW6-5:4	RAW3-5:0 | RAW7-5:4
RAW4-3:0 | RAW8-5:2	RAW5-3:0 | RAW9-5:2	RAW6-3:0 | RAW10-5:2	RAW7-3:0 | RAW11-5:2
RAW8-1:0 | RAW12-5:0	RAW9-1:0 | RAW13-5:0	RAW10-1:0 | RAW14-5:0	RAW11-1:0 | RAW15-5:0

Table 2-72: 6bpp RAW Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
RAW0-5:0 | RAW2-5:4	RAW1-5:0 | RAW3-5:4
RAW2-3:0 | RAW4-5:2	RAW3-3:0 | RAW5-5:2
RAW4-1:0 | RAW6-5:0	RAW5-1:0 | RAW7-5:0

Table 2-73: 6bpp RAW Mapping to a 1-Lane Main-Link

Lane 0
RAW0-5:0 | RAW1-5:4
RAW1-3:0 | RAW2-5:2
RAW2-1:0 | RAW3-5:0

2.2.1.3.19 7bpp RAW

Table 2-74 through Table 2-76 list 7bpp RAW stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-74: 7bpp RAW Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
RAW0-6:0 | RAW4-6	RAW1-6:0 | RAW5-6	RAW2-6:0 | RAW6-6	RAW3-6:0 | RAW7-6
RAW4-5:0 | RAW8-6:5	RAW5-5:0 | RAW9-6:5	RAW6-5:0 | RAW10-6:5	RAW7-5:0 | RAW11-6:5
RAW8-4:0 | RAW12-6:4	RAW9-4:0 | RAW13-6:4	RAW10-4:0 | RAW14-6:4	RAW11-4:0 | RAW15-6:4
RAW12-3:0 | RAW16-6:3	RAW13-3:0 | RAW17-6:3	RAW14-3:0 | RAW18-6:3	RAW15-3:0 | RAW19-6:3
RAW16-2:0 | RAW20-6:2	RAW17-2:0 | RAW21-6:2	RAW18-2:0 | RAW22-6:2	RAW19-2:0 | RAW23-6:2
RAW20-1:0 | RAW24-6:1	RAW21-1:0 | RAW25-6:1	RAW22-1:0 | RAW26-6:1	RAW23-1:0 | RAW27-6:1
RAW24-0 | RAW28-6:0	RAW25-0 | RAW29-6:0	RAW26-0 | RAW30-6:0	RAW27-0 | RAW31-6:0

Table 2-75: 7bpp RAW Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
RAW0-6:0 | RAW2-6	RAW1-6:0 | RAW3-6
RAW2-5:0 | RAW4-6:5	RAW3-5:0 | RAW5-6:5
RAW4-4:0 | RAW6-6:4	RAW5-4:0 | RAW7-6:4
RAW6-3:0 | RAW8-6:3	RAW7-3:0 | RAW9-6:3
RAW8-2:0 | RAW10-6:2	RAW9-2:0 | RAW11-6:2
RAW10-1:0 | RAW12-6:1	RAW11-1:0 | RAW13-6:1
RAW12-0 | RAW14-6:0	RAW13-0 | RAW15-6:0

Table 2-76: 7bpp RAW Mapping to a 1-Lane Main-Link

Lane 0
RAW0-6:0 | RAW1-6
RAW1-5:0 | RAW2-6:5
RAW2-4:0 | RAW3-6:4
RAW3-3:0 | RAW4-6:3
RAW4-2:0 | RAW5-6:2
RAW5-1:0 | RAW6-6:1
RAW6-0 | RAW7-6:0

2.2.1.3.20 8bpp RAW

Table 2-77 through Table 2-79 list 8bpp RAW stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-77: 8bpp RAW Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
RAW0-7:0	RAW1-7:0	RAW2-7:0	RAW3-7:0
RAW4-7:0	RAW5-7:0	RAW6-7:0	RAW7-7:0

Table 2-78: 8bpp RAW Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
RAW0-7:0	RAW1-7:0
RAW2-7:0	RAW3-7:0
RAW4-7:0	RAW5-7:0
RAW6-7:0	RAW7-7:0

Table 2-79: 8bpp RAW Mapping to a 1-Lane Main-Link

Lane 0
RAW0-7:0
RAW1-7:0
RAW2-7:0
RAW3-7:0

2.2.1.3.21 10bpp RAW

Table 2-80 through Table 2-82 list 10bpp RAW stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-80: 10bpp RAW Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
RAW0-9:2	RAW1-9:2	RAW2-9:2	RAW3-9:2
RAW0-1:0 | RAW4-9:4	RAW1-1:0 | RAW5-9:4	RAW2-1:0 | RAW6-9:4	RAW3-1:0 | RAW7-9:4
RAW4-3:0 | RAW8-9:6	RAW5-3:0 | RAW9-9:6	RAW6-3:0 | RAW10-9:6	RAW7-3:0 | RAW11-9:6
RAW8-5:0 | RAW12-9:8	RAW9-5:0 | RAW13-9:8	RAW10-5:0 | RAW14-9:8	RAW11-5:0 | RAW15-9:8
RAW12-7:0	RAW13-7:0	RAW14-7:0	RAW15-7:0

Table 2-81: 10bpp RAW Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
RAW0-9:2	RAW1-9:2
RAW0-1:0 | RAW2-9:4	RAW1-1:0 | RAW3-9:4
RAW2-3:0 | RAW4-9:6	RAW3-3:0 | RAW5-9:6
RAW4-5:0 | RAW6-9:8	RAW5-5:0 | RAW7-9:8
RAW6-7:0	RAW7-7:0

Table 2-82: 10bpp RAW Mapping to a 1-Lane Main-Link

Lane 0
RAW0-9:2
RAW0-1:0 | RAW1-9:4
RAW1-3:0 | RAW2-9:6
RAW2-5:0 | RAW3-9:8
RAW3-7:0

2.2.1.3.22 12bpp RAW

Table 2-83 through Table 2-85 list 12bpp RAW stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-83: 12bpp RAW Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
RAW0-11:4	RAW1-11:4	RAW2-11:4	RAW3-11:4
RAW0-3:0 | RAW4-11:8	RAW1-3:0 | RAW5-11:8	RAW2-3:0 | RAW6-11:8	RAW3-3:0 | RAW7-11:8
RAW4-7:0	RAW5-7:0	RAW6-7:0	RAW7-7:0

Table 2-84: 12bpp RAW Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
RAW0-11:4	RAW1-11:4
RAW0-3:0 | RAW2-11:8	RAW1-3:0 | RAW3-11:8
RAW2-7:0	RAW3-7:0

Table 2-85: 12bpp RAW Mapping to a 1-Lane Main-Link

Lane 0
RAW0-11:4
RAW0-3:0 | RAW1-11:8
RAW1-7:0

2.2.1.3.23 14bpp RAW

Table 2-86 through Table 2-88 list 14bpp RAW stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-86: 14bpp RAW Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
RAW0-13:6	RAW1-13:6	RAW2-13:6	RAW3-13:6
RAW0-5:0 | RAW4-13:12	RAW1-5:0 | RAW5-13:12	RAW2-5:0 | RAW6-13:12	RAW3-5:0 | RAW7-13:12
RAW4-11:4	RAW5-11:4	RAW6-11:4	RAW7-11:4
RAW4-3:0 | RAW8-13:10	RAW5-3:0 | RAW9-13:10	RAW6-3:0 | RAW10-13:10	RAW7-3:0 | RAW11-13:10
RAW8-9:2	RAW9-9:2	RAW10-9:2	RAW11-9:2
RAW8-1:0 | RAW12-13:8	RAW9-1:0 | RAW13-13:8	RAW10-1:0 | RAW14-13:8	RAW11-1:0 | RAW15-13:8
RAW12-7:0	RAW13-7:0	RAW14-7:0	RAW15-7:0

Table 2-87: 14bpp RAW Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
RAW0-13:6	RAW1-13:6
RAW0-5:0 | RAW2-13:12	RAW1-5:0 | RAW3-13:12
RAW2-11:4	RAW3-11:4
RAW2-3:0 | RAW4-13:10	RAW3-3:0 | RAW5-13:10
RAW4-9:2	RAW5-9:2
RAW4-1:0 | RAW6-13:8	RAW5-1:0 | RAW7-13:8
RAW6-7:0	RAW7-7:0

Table 2-88: 14bpp RAW Mapping to a 1-Lane Main-Link

Lane 0
RAW0-13:6
RAW0-5:0 | RAW1-13:12
RAW1-11:4
RAW1-3:0 | RAW2-13:10
RAW2-9:2
RAW2-1:0 | RAW3-13:8
RAW3-7:0

2.2.1.3.24 16bpp RAW

Table 2-89 through Table 2-91 list 16bpp RAW stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-89: 16bpp RAW Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
RAW0-15:8	RAW1-15:8	RAW2-15:8	RAW3-15:8
RAW0-7:0	RAW1-7:0	RAW2-7:0	RAW3-7:0
RAW4-15:8	RAW5-15:8	RAW6-15:8	RAW7-15:8
RAW4-7:0	RAW5-7:0	RAW6-7:0	RAW7-7:0

Table 2-90: 16bpp RAW Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
RAW0-15:8	RAW1-15:8
RAW0-7:0	RAW1-7:0
RAW2-15:8	RAW3-15:8
RAW2-7:0	RAW3-7:0

Table 2-91: 16bpp RAW Mapping to a 1-Lane Main-Link

Lane 0
RAW0-15:8
RAW0-7:0
RAW1-15:8
RAW1-7:0

2.2.1.4 Symbol Stuffing and Transfer Unit

To avoid the oversubscription of the link bandwidth, the packed data rate shall be less than or equal to the link symbol rate. When the packed data rate is lower than the link symbol rate, the Link Layer shall perform symbol stuffing. Stuffing symbols (both stuffing frame symbols and dummy data symbols) shall be inserted in all lanes within the same LS_Clk cycle before inter-lane skewing occurs. The dummy data symbols shall be all 0s before scrambling. The dummy data symbols are inserted between FS and FE, and between BS and BE.

The way in which symbols are stuffed shall be different between the active video period and blanking period, as follows:

- During the active video period:
  - Stuffing symbols shall be framed with FS and FE control link symbols within Transfer Unit (TU), as illustrated in Figure 2-13. (TU is described with an example in Section 2.2.1.4.1.) All symbols in the TU between FS and FE shall be stuffing dummy data symbols, while all symbols before FS shall be valid data symbols.
  - FS and FE shall be inserted in all lanes within the same LS_Clk cycle.
  - When there is only one symbol that needs to be stuffed, FE shall be used and FS is omitted.
  - TU size shall be 32 to 64 link symbols per lane, except for the last TU of the horizontal line which contains no stuffing symbols (FS/FE) and truncates with the last active pixel of the line.
  - The last TU of a horizontal video line shall end with a BS and shall not end with an FS/FE insertion.
- During the blanking period:
  - All non-control link symbols between the first BS of the blanking period and first BE of the active video period are dummy stuffing data symbols (except for VB-ID, Mvid[7:0], and Maud[7:0]). These dummy data symbols may be substituted with SDPs.

Note: *BS is inserted at the same symbol time during the vertical blanking period as during the active video period, as stated in Section 2.2.1.2.*

  - During the vertical blanking period, BS is transmitted on each lane and then followed by VB-ID, Mvid[7:0], and Maud[7:0]. All the other symbols that are between the BS at the beginning of vertical blanking interval and the BE at the end of the vertical blanking interval are dummy symbols that may be substituted with SDPs.

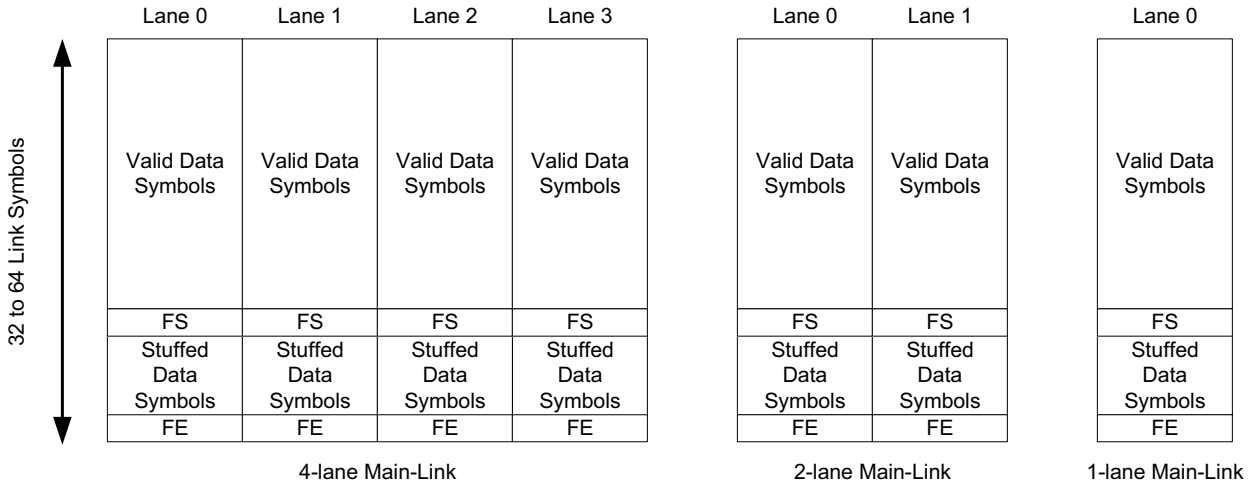


Figure 2-13: TU during Active Video Period

The first pixel data of the horizontal active display line, immediately after BE, shall be placed as the first valid data symbols of the first TU of a line. The partial pixel data of Pixel 0 shall always be placed on Lane 0.

TU may end at a partial pixel boundary. For example, a part of the blue data of a pixel may be transported in one TU while the remaining blue data for that pixel is transported in the next TU. The valid symbol to stuffing symbol ratio is determined by the ratio between the packed data stream and link symbol rates. Depending on the packed stream rate relative to the link symbol rate, a certain number of valid symbols shall accumulate every "TU-size" link symbol clock cycles. The DPTX within the Source device shall transmit those valid symbols over the Main-Link while the next accumulation starts. This process shall repeat until the end of a video line is reached, which is marked by the insertion of BS symbol on all lanes.

Using the above stuffing method, the number of valid data symbols per TU per lane (except for the last TU of a line, which may be cut because of the end of an active pixel) shall be approximated, using the following equation:

$$\#\ of\ valid\ data\ symbols\ per\ lane = packed\ data\ rate / link\ symbol\ rate \times TU\ size$$

The last TU at the end of the horizontal active display period may (or is likely to) have fewer valid data symbols than that obtained from the above equation. The DPRX shall discard all the data symbols after BS (except for VB-ID, Mvid[7:0], and Maud[7:0]), as well as those "zero-padded bits" at the end of the horizontal active display period.

2.2.1.4.1 TU Example (Informative)

Table 2-92 illustrates a TU example for a 1366x768, 30bpp RGB video stream (Strm_Clk = 80MHz) transported over a 4-lane Main-Link running at 2.7Gbps/lane (or 270Msymbols/sec/lane). The TU size is fixed to 64 link symbols/lane in this example.

The number of valid symbols within the TU is calculated as follows:

Stream: 30bpp, 80MHz → Packed data rate over four lanes = 75Msymbols/sec/lane

Average valid symbols per TU = 75M / 270M × 64 = 17.8

The number of valid data symbols per TU shall naturally alternate, and over time, the average number shall come to the appropriate non-integer value calculated from the above equation. As defined in Table 2-92, the valid data in a transfer unit may end at a non-pixel boundary.

Table 2-92: TU of 30bpp RGB Video over 2.7Gbps/lane Main-Link[a]

Lane 0	Lane 1	Lane 2	Lane 3
BE	BE	BE	BE
R0-9:2	R1-9:2	R2-9:2	R3-9:2
R0-1:0 | G0-9:4	R1-1:0 | G1-9:4	R2-1:0 | G2-9:4	R3-1:0 | G3-9:4
G0-3:0 | B0-9:6	G1-3:0 | B1-9:6	G2-3:0 | B2-9:6	G3-3:0 | B3-9:6
B0-5:0 | R4-9:8	B1-5:0 | R5-9:8	B2-5:0 | R6-9:8	B3-5:0 | R7-9:8
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-9:2	G5-9:2	G6-9:2	G7-9:2
G4-1:0 | B4-9:4	G5-1:0 | B5-9:4	G6-1:0 | B6-9:4	G7-1:0 | B7-9:4
B4-3:0 | R8-9:6	B5-3:0 | R9-9:6	B6-3:0 | R10-9:6	B7-3:0 | R11-9:6
R8-5:0 | G8-9:8	R9-5:0 | G9-9:8	R10-5:0 | G10-9:8	R11-5:0 | G11-9:8
G8-7:0	G9-7:0	G10-7:0	G11-7:0
B8-9:2	B9-9:2	B10-9:2	B11-9:2
B8-1:0 | R12-9:4	B9-1:0 | R13-9:4	B10-1:0 | R14-9:4	B11-1:0 | R15-9:4
R12-3:0 | G12-9:6	R13-3:0 | G13-9:6	R14-3:0 | G14-9:6	R15-3:0 | G15-9:6
G12-5:0 | B12-9:8	G13-5:0 | B13-9:8	G14-5:0 | B14-9:8	G15-5:0 | B15-9:8
B12-7:0	B13-7:0	B14-7:0	B15-7:0
R16-9:2	R17-9:2	R18-9:2	R19-9:2
R16-1:0 | G16-9:4	R17-1:0 | G17-9:4	R18-1:0 | G18-9:4	R19-1:0 | G19-9:4
G16-3:0 | B16-9:6	G17-3:0 | B17-9:6	G18-3:0 | B18-9:6	G19-3:0 | B19-9:6
FS	FS	FS	FS
Dummy Data Symbols (44 × 4)			
FE	FE	FE	FE
B16-5:0 | R20-9:8	B17-5:0 | R21-9:8	B18-5:0 | R22-9:8	B19-5:0 | R23-9:8
R20-7:0	R21-7:0	R22-7:0	R23-7:0
---			

a. The pixel rate in this example is 80MP/s. The Main-Link bit rate is 2.7Gbps/lane. The first TU of a line is marked by the blue arrow to the right of the table.

2.2.1.4.2 TU Generation with FEC Encoding/Decoding Enabled

New to *DP v1.4*. Updated in *DP v1.4a*.

When FEC encoding/decoding is enabled (see Section 3.5.1.5), a DPTX Link Layer shall insert FEC parity place holder and parity marker (FEC_PARITY_PH and FEC_PM, respectively) link symbols, as follows:

- **4- and 2-lane configurations**
  - Six FEC_PARITY_PH link symbols inserted after 250 Link Layer link symbols
  - Every 256th set of six FEC_PARITY_PH link symbols, followed by an FEC_PM link symbol
- **1-lane configuration**
  - 12 FEC_PARITY_PH link symbols inserted after 500 Link Layer link symbols
  - Every 128th set of 12 FEC_PARITY_PH link symbols, followed by an FEC_PM link symbol

The resulting FEC overhead is approximately 2.4%.

FEC_PARITY_PH and FEC_PM Link Layer symbol insertion is strictly periodic and is agnostic to other Link Layer link symbol transmission.

To avoid the 2.4% FEC overhead, a DP Source device may choose to not use FEC by clearing the FEC_READY bit in the FEC_CONFIGURATION register (DPCD Address 00120h, bit 0) to 0 prior to link training. If the DP Source device needs to use FEC at a later time, the device shall first set the FEC_READY bit, initiate link training, and then enable FEC encoding after link training completes.

To compensate for the bandwidth lost due to the FEC code transmission, a DP Source device may increase the amount of valid data packed in each TU relative to the non-FEC configuration. Alternatively, a DP Source device may transmit additional valid data in the TUs, immediately following the FEC codes, to account for the pixel data that accumulated while transmitting the FEC codes. The latter technique is possible only when the SST link bandwidth is not fully subscribed.

2.2.1.5 MSA Packet Insertion

Dummy stuffing data symbols within the HBlank and VBlank periods may be substituted with MSA data. MSA data shall be framed with SS and SE control link symbols, as illustrated in Figure 2-14.

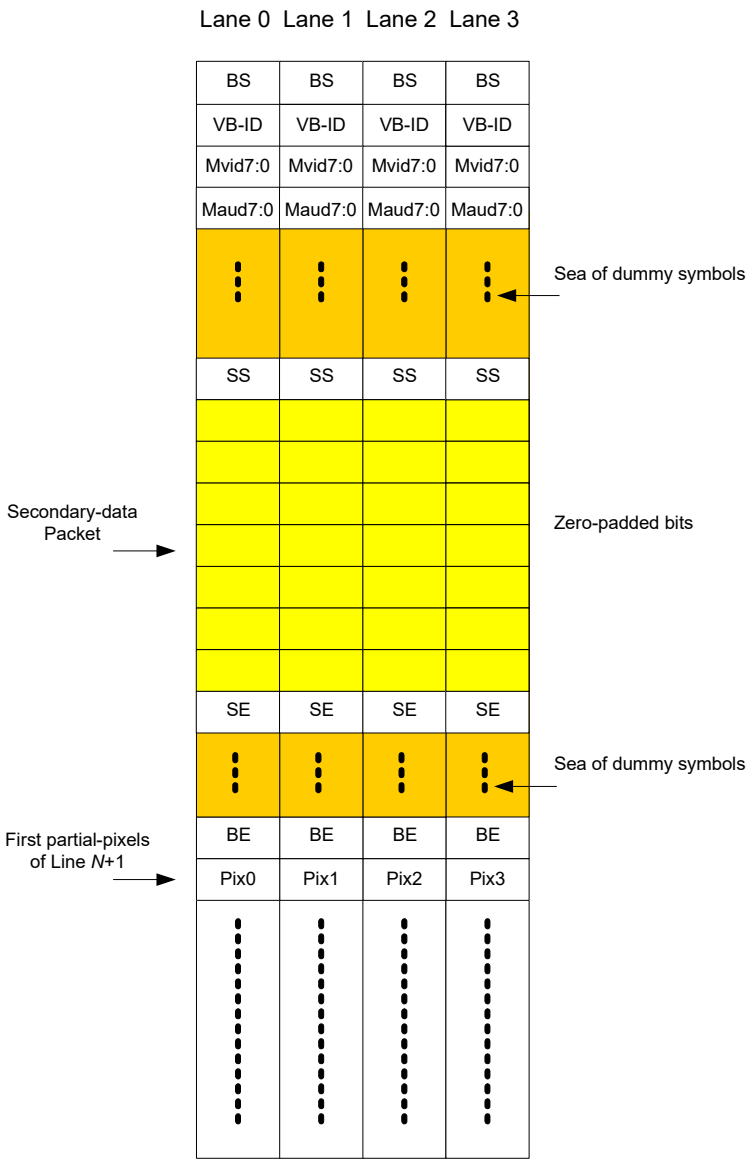


Figure 2-14: Secondary-data Insertion

SDPs are used, for example, for the following purposes:

- *CTA-861-G* INFOFRAME SDP
- Audio_Stream SDP
- Audio_TimeStamp SDP

MSA data shall be protected by way of redundancy. The redundancy shall be further enhanced by way of inter-lane skewing, as described in Section 2.2.1.6. SDPs shall be protected by error correcting code (ECC) based on Reed-Solomon code, as described in Section 2.2.6.

2.2.1.6 Inter-lane Skewing

After inserting the Main-Link attributes data (and optionally, SDP), the DPTX shall insert a skew of two LS_Clk cycles between adjacent lanes. Figure 2-15 illustrates how the symbols shall be transported after this inter-lane skewing. All symbols (i.e., those transmitted during the video display period and video blanking period) are skewed by two LS_Clk periods between adjacent lanes.

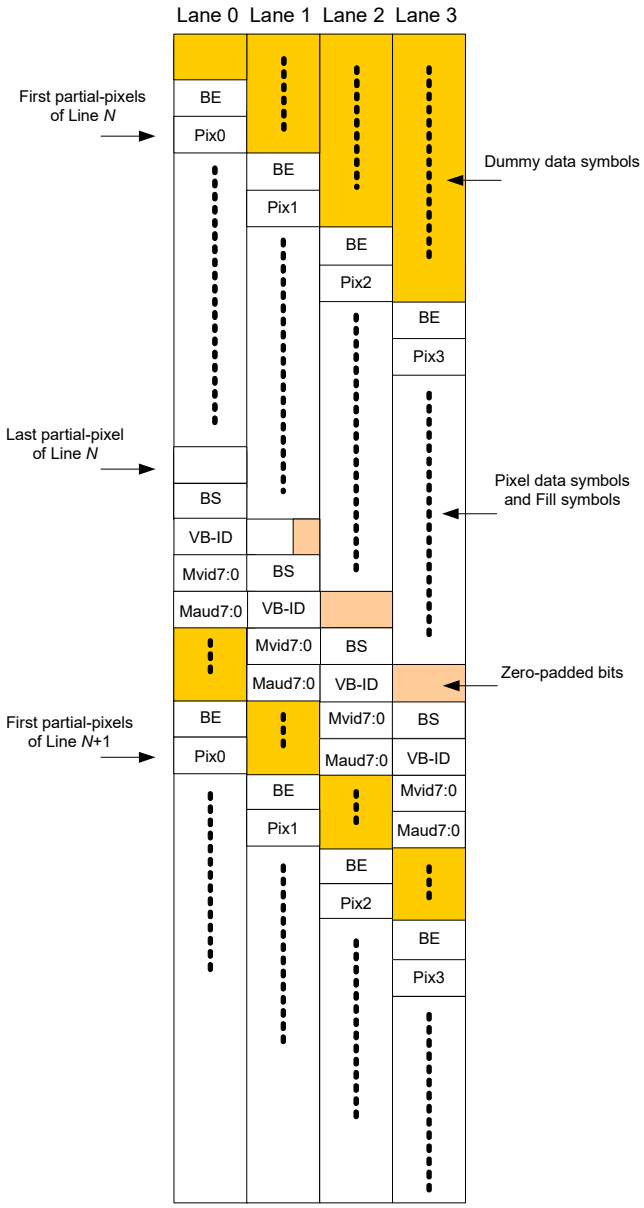


Figure 2-15: Inter-lane Skewing

The purpose of the inter-lane skewing is to increase the immunity of the link against external noise. Without inter-lane skewing an external impulse may, for example, corrupt the Mvid[7:0] symbols on all lanes. Inter-lane skewing reduces the possibility of such a corruption.

2.2.2 Stream Reconstruction in the Sink Device

The stream reconstruction by the Link Layer in the DPRX shall be a mirror image of what takes place within the DPTX. Table 2-93 lists the actions that shall be taken by the DPRX.

Table 2-93: DPRX Stream Reconstruction Actions within the Sink Device

Action[a]		Description
1	Inter-lane de-skewing	Shall remove the two LS_Clk skewing among adjacent lanes inserted by the DPTX.
2	Error correction	All DP MSA values, except for the time stamp value Mvid, shall remain constant. Therefore, the DPRX shall filter out any intermittent data corruption by comparing with the previous values. For time stamp values Mvid/Maud and VB-ID, majority voting shall be used to determine the value.
3	SDP de-multiplexing	Secondary data shall be de-multiplexed using SS and SE as the separator. The DPRX shall perform Reed-Solomon (15, 13) (RS(15, 13)) decoding after extracting the SDP.
4	Symbol un-stuffing	Remove stuffing symbols.
5	Data unpacking	Data unpacking shall reconstruct pixel data from data characters transported over the Main-Link. Unpacking is dependent on the pixel data color depth and format (as described in Section 2.2.1.3).
6	Stream clock regeneration	Stream clock regeneration is covered in Section 2.2.3.

a. Although the sequence listed is typical, some implementations may choose a different sequence.

2.2.3 Stream Clock Regeneration

This section describes the details of original stream clock regeneration from the stream transported over the Main-Link within the Sink device. The following equations conceptually explain how the stream clock (Strm_Clk) can be derived from the Main-Link Symbol clock (LS_Clk), using Time Stamps Mvid and Nvid:

$$f\_Strm\_Clk = Mvid / Nvid \times f\_LS\_Clk$$

where:

- f_Strm_Clk = Stream clock frequency
- Mvid = Feedback pulse period / t_Strm_Clk
- Nvid = Reference pulse period / t_LS_Clk
- f_LS_Clk = Main-Link symbol clock frequency

The t_Strm_Clk and t_LS_Clk are the stream clock and the Main-Link Symbol clock periods, respectively. Figure 2-16 illustrates the reference and feedback pulses.

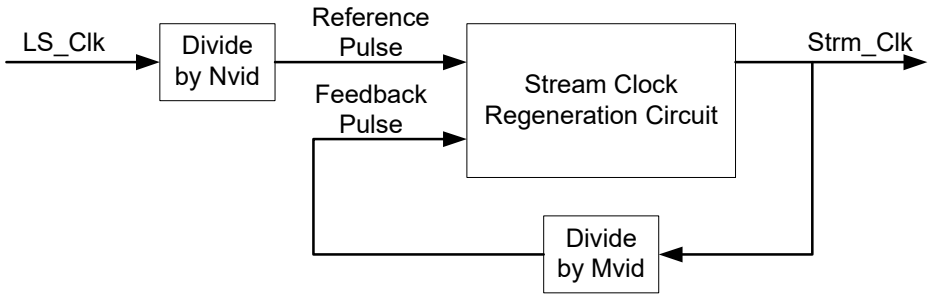


Figure 2-16: Reference Pulse and Feedback Pulse of Stream Clock Regeneration Circuit

The above equation can also be expressed as:

$$Mvid / Nvid = f\_Strm\_Clk / f\_LS\_Clk$$

Mvid/Nvid is a ratio determined by the pixel rate (typically expressed in MP/s) and Main-Link Symbol clock rate. Therefore, the Mvid and Nvid values are agnostic to either pixel encoding format or component bit depth.

The Mvid and Nvid time stamps shall both be 24-bit values.

When the DPTX and stream source share the same reference clock, the Mvid and Nvid time stamp values remain constant. This way of generating Main-Link Symbol clock and stream clock is referred to as "Synchronous Clock mode." A DP Source device may select a stream clock frequency that allows for static and relatively small (e.g., 64 or less) Mvid and Nvid values. These choices are implementation-specific.

If the stream clock and Main-Link Symbol clock are asynchronous with one another, the Mvid value changes over time. This way of generating Main-Link Symbol clock and stream clock is referred to as "Asynchronous Clock mode." The Mvid value is bound to change while the value Nvid remains constant. The Nvid value in this Asynchronous Clock mode shall be set to 2^{15} (= 32768) or higher. A value of power of two should be used.

When in Asynchronous Clock mode, the DPTX shall measure Mvid using a counter running at the LS_Clk frequency, as illustrated in Figure 2-17. The full counter value after every [Nvid × LS_Clk cycles] shall be transported in the DP MSA packet. Mvid's eight least significant bits (Mvid[7:0]) shall be transported once per main video stream horizontal period, following the BS symbol sequence and VB-ID.

When Mvid[7:0] crosses the 8-bit boundary, the entire Mvid23:0 changes. For example, when Mvid23:0 is 000FFFh at one point in time for a given main video stream, the value may change to 010000h at another point. The Sink device shall determine the entire Mvid23:0 value, based on the updated Mvid[7:0].

In Asynchronous Clock mode, the Sink device shall use the received Mvid and Nvid values as a hint for regenerating the pixel clock. The final stream clock regeneration shall be achieved so that the regenerated video active line and frame timings are in sync with BE framing control link symbol reception.

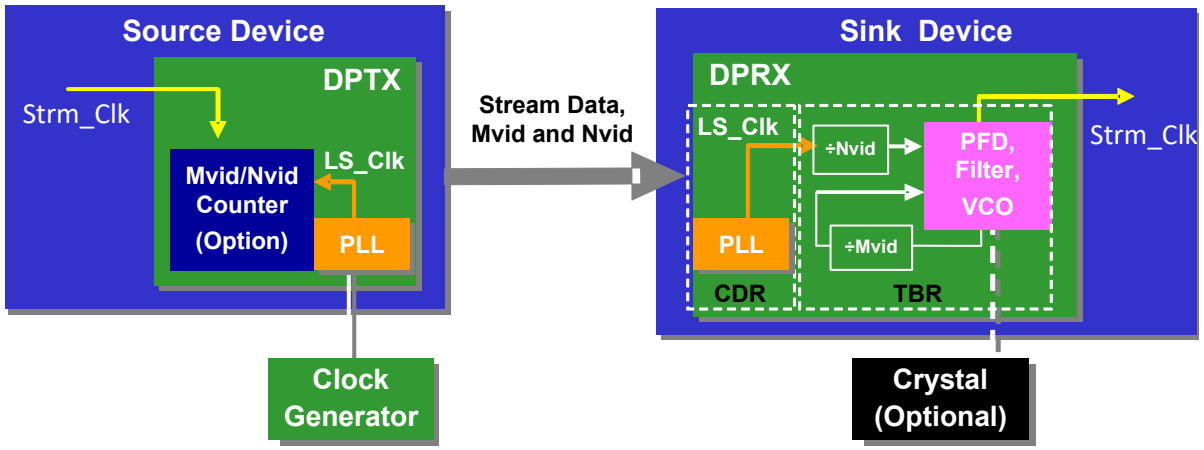


Figure 2-17: Mvid and Nvid Value Determination Example in Asynchronous Clock Mode in a Source Device

Note 1: *Use of a 32768 Nvid value does not dictate that the reference pulse period be 32768 × t_LS_Clk, which is approximately 121us for the Main-Link at HBR (2.7Gbps/lane). The values of Nvid (which is 32768 or 8000h) and Mvid (which is measured by the counter in the DPTX) may be divided by power of two (or right-shifted) to achieve the reference pulse period suited for each implementation.*

The method for right-shifting Mvid depends on the accuracy and jitter tolerance needed by each application. The simplest method of rounding up to the closest integer value (thus, resulting in approximated stream clock regeneration) may be used for certain applications where the regenerated stream timing is gen-locked to the incoming data. Other applications may use a more-elaborate fractional Mvid PLL based approach for increasing the accuracy while maintaining the low jitter.

In some implementations, the value of Mvid may be accumulated multiple times to use even larger Mvid and Nvid values for stream clock regeneration.

How a Sink device uses (or even does not use) Mvid and Nvid values for stream clock regeneration is implementation-specific.

Note 2: *This section covers the stream clock regeneration in SST mode and does not apply to MST mode, unless an MST Source device is directly driving an MST Sink device over a single link, because the Mvid and Nvid generated by a Source device describes the ratio between the Strm_Clk and the LS_Clk of the link that the Source device is driving. In case there are multiple links (using MST Branch devices) between a Source and Sink device, the Sink device shall ignore the Mvid and Nvid values. An MST Sink device shall be able to regenerate a stream clock without depending on Mvid and Nvid values because the MST Sink device might be plugged into an MST Branch device, not an MST Source device.*

2.2.3.1 De-spreading of the Regenerated Stream Clock

Down spreading of the link frequency (with modulation frequencies of 30 to 33kHz) to minimize EMI shall be supported for *DP v1.4a*-compliant Sink and Branch devices. Down spreading by a DPTX may be supported and is an implementation-specific decision. To facilitate testing, the MAX_DOWNSPREAD bit in the MAX_DOWNSPREAD register(s) (DPCD Address(es) 00003h and 02203h, bit 0) may be used by a Reference Sink device during compliance testing of devices that have chosen to implement enablement of spread-spectrum clocking (SSC) based on that bit.

Note: *SSC is supported when the MAX_DOWNSPREAD bit in the MAX_DOWNSPREAD register(s) (DPCD Address(es) 00003h and 02203h, bit 0) is set to 1. SSC is enabled or disabled when the SPREAD_AMP bit in the DOWNSPREAD_CTRL register (DPCD Address 00107h, bit 4) is set to 1 or cleared to 0, respectively.*

For a certain Sink device, such as an audio Sink device, the regenerated stream clock shall not have down spreading. Such Sink devices shall perform de-spreading when regenerating the stream clock. The de-spreading method used is implementation-specific.

2.2.3.2 DPRX Stream Clock Regeneration with FEC Encoding/Decoding Enabled

New to *DP v1.4*. Updated in *DP v1.4a*.

FEC_PARITY_PH and FEC_PM Link Layer symbol insertion is strictly periodic and is agnostic to other Link Layer link symbol transmission. With FEC_PARITY_PH and FEC_PM link symbol insertion, transmission of a BE and BS symbol sequence relative to the main video stream display enable (DE) rising edge and falling edge can be skewed, as follows:

- **4- and 2-lane configurations** – Up to seven link symbol clock cycles, time-to-time
- **1-lane configuration** – Up to 13 link symbol clock cycles, time-to-time

A DPRX shall be able to regenerate a stable main video, despite the skew of the BE and BS symbol sequence locations.

2.2.4 MSA Data Transport

Updated in *DP v1.4a*.

This section describes the MSA data that the DP Source device transports for reproducing the main video stream. Attribute data is transmitted once per frame during the main video stream's vertical blanking period. Table 2-94 describes the MSA attributes, as well as the DPCD registers associated with the attributes.

Table 2-94: MSA Data Fields

Symbol	# of Bits	Bit #	Description
Mvid	24	23:0	**Mvid** Video time stamp value used by a DP Sink device as a hint for regenerating pixel clock. Used for main video stream clock regeneration. Composed of three 8-bit bytes: • Mvid[23:16] • Mvid[15:8] • Mvid[7:0]
Nvid	24	23:0	**Nvid** Video time stamp value used by a DP Sink device as a hint for regenerating pixel clock. Used for main video stream clock regeneration. Composed of three 8-bit bytes: • Nvid[23:16] • Nvid[15:8] • Nvid[7:0]
HTotal	16	15:0	**Horizontal Total** Horizontal total of transmitted main video stream, measured in pixel count.
VTotal	16	15:0	**Vertical Total** Vertical total of transmitted main video stream, measured in line count.
HStart	16	15:0	**Horizontal Active Start** Horizontal active start from leading edge of HSync, measured in pixel count.
VStart	16	15:0	**Vertical Active Start** Vertical active start from leading edge of VSync, measured in line count.
HSyncPolarity (HSP)	1	0	**Horizontal Sync Polarity** HSync polarity, measured in pixel count. 0 = Active high pulse. Synchronization signal is high for the sync pulse width. 1 = Active low pulse. Synchronization signal is low for the sync pulse width.
HSyncWidth (HSW)	15	14:0	**Horizontal Sync Width** HSync width, measured in pixel count.

Table 2-94: MSA Data Fields (Continued)

Symbol	# of Bits	Bit #	Description
VSyncPolarity (VSP)	1	0	**Vertical Sync Polarity** VSync polarity, measured in line count. 0 = Active high pulse. Synchronization signal is high for the sync pulse width. 1 = Active low pulse. Synchronization signal is low for the sync pulse width.
VSyncWidth (VSW)	15	14:0	**Vertical Sync Width** VSync width, measured in line count.
HWidth	16	15:0	**Horizontal Active Video Width** Active video width, measured in pixel count.
VHeight	16	15:0	**Vertical Active Video Height** Active video height, measured in line count.
MISC0	8	7:0	**Miscellaneous0**
		0	**Synchronous Clock** Applies to the main video stream clock. Does **not** apply to the audio clock. (See Section 2.2.5.1.) Synchronousness/asynchronousness of the main video stream and of the audio stream clock may be independently set. 0 = Link clock and main video stream clock are asynchronous. 1 = Link clock and main video stream clock are synchronous. The value Mvid shall be constant, regardless of whether link clock down spread is enabled.
		7:1	**Colorimetry Indicator Field, Bits 7:1** Used with MISC1, bit 7:6, to comprise the Colorimetry Indicator field. (See Section 2.2.4.3.)

Table 2-94: MSA Data Fields (Continued)

Symbol	# of Bits	Bit #	Description
MISC1	8	7:0	**Miscellaneous1**
		0	**Interlaced Vertical Total Even** 0 = Number of lines per interlaced frame (consisting of two fields) is an odd number. 1 = Number of lines per interlaced frame (consisting of two fields) is an even number.
		2:1	**Stereo Video Attribute** 00b = No 3D stereo video in-band signaling was done using this field, indicating either no 3D stereo video transported or the in-band signaling done used a Video_Stream_Configuration (VSC) SDP. 01b = For progressive video, the next frame is right-eye view. 10b = RESERVED. 11b = For progressive video, the next frame is left-eye view. ***Note:*** *Frame/Field Sequential 3D stereo video transport in interlaced video timing format is* ***not*** *supported.*
		5:3	**RESERVED** Cleared to 0h.
		7:6	**Pixel Encoding/Colorimetry Format Indicator Field** Bit 6 is new to *DP v1.3*. Used with MISC0, bits 7:1, to comprise the Colorimetry Indicator field. (See Section 2.2.4.3.) When bit 6 is set to 1, a Source device uses a VSC SDP to indicate the Pixel Encoding/Colorimetry format and that a Sink device shall ignore bit 7, and MISC0, bits 7:1 (i.e., MISC1, bit 7, and MISC0, bits 7:1, become “don’t care”).

This MSA data shall be transported as illustrated in Figure 2-18 (after 2-LS_Clk-cycle inter-lane skewing). An MSA packet shall be distinguished from an SDP by the fact that the MSA packet starts with two consecutive “SS” symbols per lane.

4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 0
SS	SS	SS	SS	SS	SS	SS
SS	SS	SS	SS	SS	SS	SS
Mvid[23:16]	Mvid[23:16]	Mvid[23:16]	Mvid[23:16]	Mvid[23:16]	Mvid[23:16]	Mvid[23:16]
Mvid[15:8]	Mvid[15:8]	Mvid[15:8]	Mvid[15:8]	Mvid[15:8]	Mvid[15:8]	Mvid[15:8]
Mvid[7:0]	Mvid[7:0]	Mvid[7:0]	Mvid[7:0]	Mvid[7:0]	Mvid[7:0]	Mvid[7:0]
HTotal[15:8]	HStart[15:8]	HWidth[15:8]	Nvid[23:16]	HTotal[15:8]	HStart[15:8]	HTotal[15:8]
HTotal[7:0]	HStart[7:0]	HWidth[7:0]	Nvid[15:8]	HTotal[7:0]	HStart[7:0]	HTotal[7:0]
VTotal[15:8]	VStart[15:8]	VHeight[15:8]	Nvid[7:0]	VTotal[15:8]	VStart[15:8]	VTotal[15:8]
VTotal[7:0]	VStart[7:0]	VHeight[7:0]	MISC0[7:0]	VTotal[7:0]	VStart[7:0]	VTotal[7:0]
HSP|HSW[14:8]	VSP|VSW[14:8]	All 0s	MISC1[7:0]	HSP|HSW[14:8]	VSP|VSW[14:8]	HSP|HSW[14:8]
HSW[7:0]	VSW[7:0]	All 0s	All 0s	HSW[7:0]	VSW[7:0]	HSW[7:0]
SE	SE	SE	SE	Mvid[23:16]	Mvid[23:16]	Mvid[23:16]
				Mvid[15:8]	Mvid[15:8]	Mvid[15:8]
				Mvid[7:0]	Mvid[7:0]	Mvid[7:0]
				HWidth[15:8]	Nvid[23:16]	HStart[15:8]
				HWidth[7:0]	Nvid[15:8]	HStart[7:0]
				VHeight[15:8]	Nvid[7:0]	VStart[15:8]
				VHeight[7:0]	MISC0[7:0]	VStart[7:0]
				All 0s	MISC1[7:0]	VSP|VSW[14:8]
				All 0s	All 0s	VSW[7:0]
				SE	SE	Mvid[23:16]
						Mvid[15:8]
						Mvid[7:0]
						HWidth[15:8]
						HWidth[7:0]
						VHeight[15:8]
						VHeight[7:0]
						All 0s
						All 0s
						Mvid[23:16]
						Mvid[15:8]
						Mvid[7:0]
						Nvid[23:16]
						Nvid[15:8]
						Nvid[7:0]
						MISC0[7:0]
						MISC1[7:0]
						All 0s
						SE

Figure 2-18: DP MSA Packet Transport Mapping over Main-Link

2.2.4.1 MSA Packet Generation Options

Entire section rewritten for *DP v1.4*.

2.2.4.1.1 Ignore MSA Video Timing Parameters (Ignore MSA) Option

MSA packet video timing information is designed for video modes in which the parameters are static. For modes that dynamically change the video timing, the MSA fields **cannot** be used. Also, in some systems, HSync/VSync may **not** be used.

Therefore, a Source device that supports a special mode of operation in which one or more MSA parameters are non-static or unused may transmit invalid values for those MSA parameters, as long as the Source device is able to discover that the Sink device supports that special mode of operation.

A Source device shall query a Sink device's ability to ignore MSA video timing parameters (Ignore MSA option) by reading the MSA_TIMING_PAR_IGNORED bit in the DOWN_STREAM_PORT_COUNT register (DPCD Address 00007h, bit 6) and its ability to support seamless video timing change over a range of timing exposed by DisplayID and legacy EDID. The query shall occur before enabling a dynamic video timing change of the incoming video stream without valid MSA video timing parameters for the fields listed in Table 2-95.

Table 2-95: MSA Packet Timing Parameters that Can Be Ignored

HTotal[15:0]	HStart[15:0]	HSyncPolarity[0] (HSP)	HSyncWidth[14:0] (HSW)
VTotal[15:0]	VStart[15:0]	VSyncPolarity[0] (VSP)	VSyncWidth[14:0] (VSW)

2.2.4.1.2 Horizontal Blanking Expansion

New to *DP v1.4*. Updated in *DP v1.4a*.

Horizontal Blanking Expansion is an **optional** operation in which a DPRX regenerates a pixel clock cycle ($t_{\_Regen\_PixClk}$) that is shorter than the pixel clock of the DP video stream from the DP Source device ($t_{\_Src\_PixClk}$), while regenerating the same video horizontal period (in time units) and the same horizontal active pixel count (HWidth parameter in an MSA packet):

- Video horizontal period, HPeriod = HTotal × $t_{\_PixClk}$
- Alternately expressed, HTotal = HPeriod / $t_{\_PixClk}$

For DP Source video and DPRX-regenerated video:

- $HTotal_{\_Src}$ = HPeriod / $t_{\_Src\_PixClk}$
- $HTotal_{\_Regen}$ = HPeriod / $t_{\_Regen\_PixClk}$

Because HPeriod is the same and $t_{\_Regen\_PixClk} < t_{\_Src\_PixClk}$:

- $HTotal_{\_Regen} > HTotal_{\_Src}$

Horizontal blank pixel cycle count, HBlank = HTotal – HWidth.

Because HWidth is the same between the DP Source video and DPRX-regenerated video while $HTotal_{\_Src}$ is larger than $HTotal_{\_Regen}$:

- $HBlank_{\_Regen} > HBlank_{\_Src}$

Thus, Horizontal Blanking Expansion results from the reduction of $t_{\_Regen\_PixClk}$ relative to $t_{\_Src\_PixClk}$ (which means, in terms of pixel clock frequency, $f_{\_Regen\_PixClk} > f_{\_Src\_PixClk}$). Figure 2-19 illustrates Horizontal Blanking Expansion.

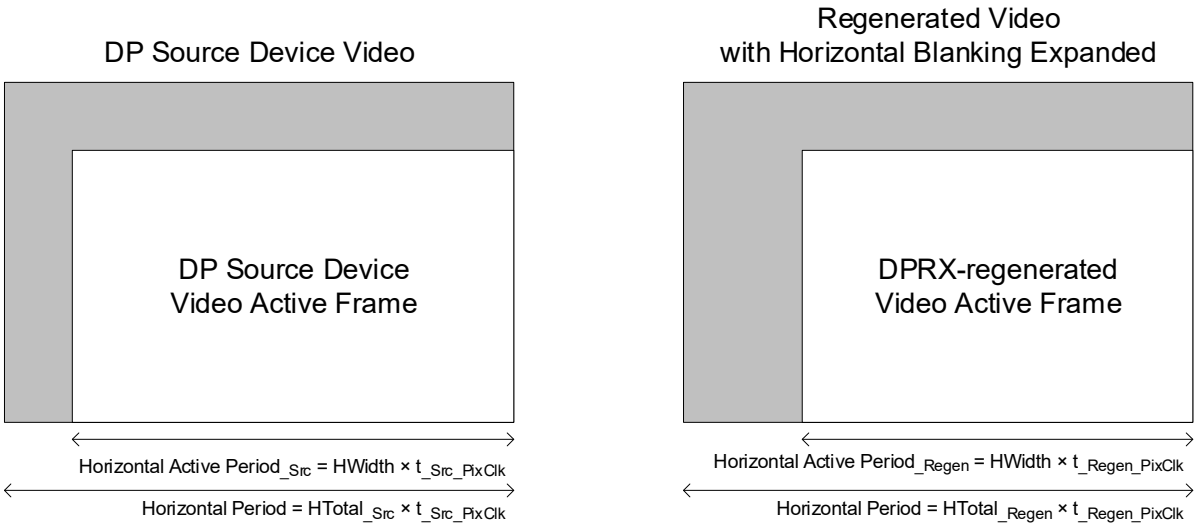


Figure 2-19: Horizontal Blanking Expansion

2.2.4.1.2.1 Enabling Horizontal Blanking Expansion

Updated in *DP v1.4a*.

When connected to a Horizontal Blanking Expansion-capable DPRX, a DP Source device may prompt the DPRX to enable Horizontal Blanking Expansion. To enable Horizontal Blanking Expansion, the DP Source device shall program the OUTPUT_HTOTAL, OUTPUT_HSTART, and OUTPUT_HSP_HSW registers (DPCD Addresses 03054h through 03059h, respectively) in a single AUX burst write transaction prior to transmitting the video stream to be expanded by a DPRX.

A Horizontal Blanking Expansion-capable DPRX shall initialize (power up) with the OUTPUT_HTOTAL, OUTPUT_HSTART, and OUTPUT_HSP_HSW registers cleared to all 0s. The DPRX shall also clear these registers to all 0s only in the event of a device reset –or– when a Powered-Source disconnect is detected by use of the Upstream Device Detection function. When these registers are all programmed to non-zero values by a DP Source device, such action enables Horizontal Blanking Expansion in the DPRX. To disable Horizontal Blanking Expansion, the DP Source device shall clear the OUTPUT_HTOTAL register to all 0s.

As with normal operation, when Horizontal Blanking Expansion is enabled, the DP Source device shall transmit MSA data field values that represent the DP data's format over the Main-Link. This rule may not apply, however, when the DP Source device is connected to a DPRX that has the MSA_TIMING_PAR_IGNORED bit in the DOWN_STREAM_PORT_COUNT register (DPCD Address 00007h, bit 6) set to 1.

2.2.4.1.2.2 DPRX Horizontal Blanking Expansion Capability Discovery

Updated in *DP v1.4a*.

A DPRX that supports Horizontal Blanking Expansion shall indicate the support by doing the following:

- Setting the HBLANK_EXPANSION_CAPABLE bit in the RECEIVE_PORT0_CAP_0 register (DPCD Address 00008h, bit 3) to 1
- Setting the remaining RECEIVE_PORT0_CAP_0 register bits appropriately
- Programming the RECEIVE_PORT0_CAP_1 register (DPCD Address 00009h) appropriately

A DP Source device discovers whether a connected DPRX operating in SST mode supports Horizontal Blanking Expansion by reading the RECEIVE_PORT0_CAP_0 and RECEIVE_PORT0_CAP_1 registers.

2.2.4.1.2.3 Horizontal Blanking Expansion Dependency on Buffer Size (Normative)

The maximum $HTotal_{\_Regen}$, $Max\_HTotal_{\_Regen}$ for a given $HTotal_{\_Src}$ is calculated as follows:

$$Max\_HTotal_{\_Regen} = HTotal_{\_Src} \times HWidth / (HWidth - [Buffer\ Size\ in\ Pixel\ Count])$$

The minimum $HTotal_{\_Src}$, $Min\_HTotal_{\_Src}$ for a given $HTotal_{\_Regen}$ is calculated as follows:

$$Min\_HTotal_{\_Src} = HTotal_{\_Regen} \times (HWidth - [Buffer\ Size\ in\ Pixel\ Count]) / HWidth$$

For $HTotal_{\_Regen}$ of 4400 pixel clock cycles and HWidth of 4096 pixels (i.e., a 4Kp60Hz timing as per *CTA-861-G*, with the pixel clock frequency of 594MHz), the buffer size of 200 pixels enables the $Min\_HTotal_{\_Src}$ of 4186 pixel clock cycles. The corresponding DP Source device pixel clock frequency, $f_{\_Src\_PixClk}$, is calculated as follows:

$$f_{\_Src\_PixClk} = 4186\ pixel\ clock\ cycles / 4400\ pixel\ clock\ cycles \times 594MHz = 566.11MHz$$

For pixel bit depth of 30bpp, the resulting DP Source video pixel bandwidth is:

$$Pixel\ bandwidth\ in\ MBps = 566.11MP/s \times 30bpp = 2119.16MBps$$

The above pixel bandwidth fits within the DP link bandwidth of 5.4Gbps/lane over four lanes which is 2160MBps (= 540MBps/lane × 4 lanes).

2.2.4.2 MSA for Interlaced Video Stream

An interlaced video streams frame consists of two fields:

- Top field, which contains the first active line of a frame
- Bottom field, which contains the second active line of a frame

Figure 2-20 illustrates the video format of an interlaced video stream that has an odd number of lines/frame. Figure 2-21 illustrates the video format of an interlaced video stream that has an even number of lines/frame.

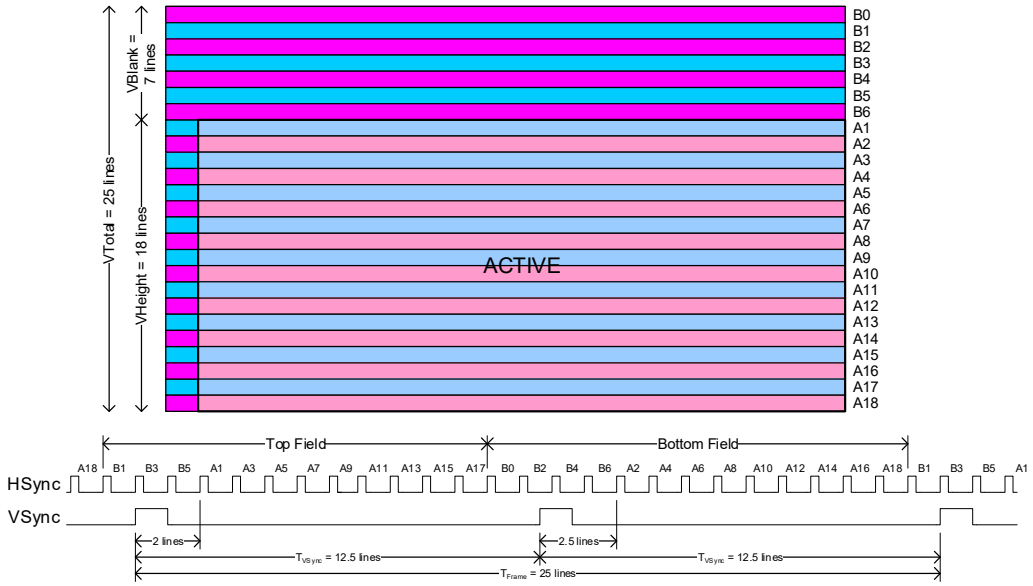


Figure 2-20: Interlaced Video Format/Timing for Odd Number of Lines/frame

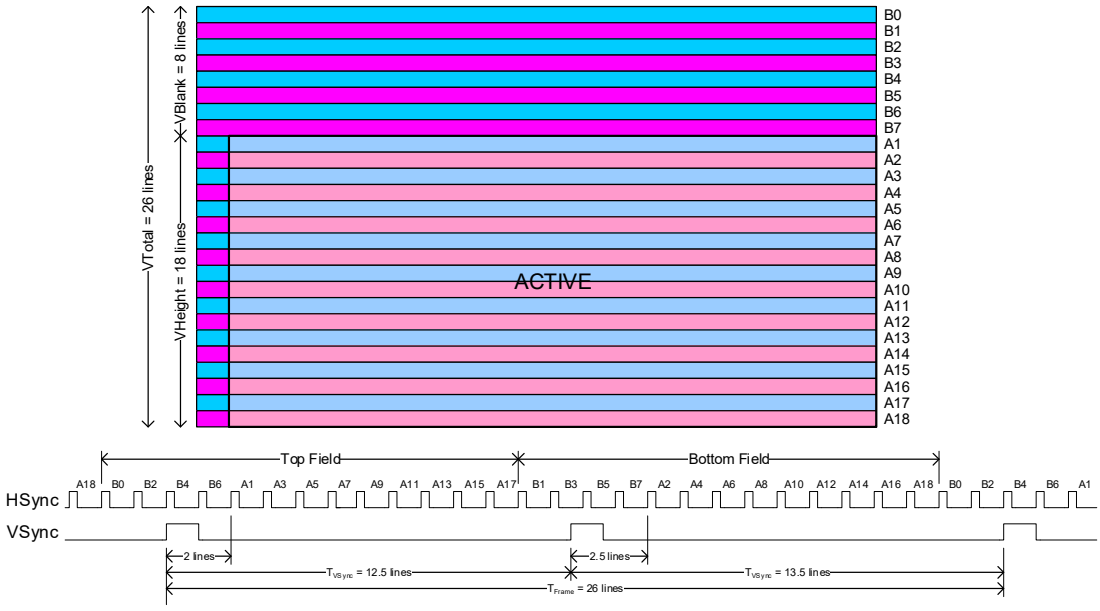


Figure 2-21: Interlaced Video Format/Timing for Even Number of Lines/frame

When transporting an interlaced video stream, the timing parameters of the top field shall always be conveyed in the MSA packet.

As defined in Table 2-6, the Interlace_Flag bit in the VB-ID (bit 2) shall be set to 1 when an interlaced video stream is transported. The FieldID_Flag bit in the VB-ID (bit 1) is cleared to 0 after the last active line of the top field and set to 1 after the last active line of the bottom field. For non-interlaced video, VB-ID bits 2:1 shall remain cleared to 00b.

In the example illustrated in Figure 2-20, the Vertical Active Start, Vertical Total, Vertical Sync Width, and Vertical Active Video Height of the MSA packet shall be programmed as follows:

- Vertical Active Start = 2 (decimal)
- Vertical Total = 12 (decimal)
- Vertical Sync Width = 1 (decimal)
- Vertical Active Video Height = 9 (decimal)

In the example illustrated in Figure 2-21 the Vertical Active Start, Vertical Total, Vertical Sync Width, and Vertical Active Video Height of the MSA packet shall be programmed as follows:

- Vertical Active Start = 2 (decimal)
- Vertical Total = 13 (decimal)
- Vertical Sync Width = 1 (decimal)
- Vertical Active Video Height = 9 (decimal)

In addition, MSA MISC1, bit 0, shall be set to 1 when the number of lines/frame of the interlaced video stream is an even number.

2.2.4.3 MSA Field for Indication of Color Encoding Format and Content Color Gamut

Table 2-96 describes how MSA MISC0 field, bits 7:1, and MISC1 field, bits 7:6, are used by a DP Source device to indicate the pixel encoding and colorimetry format of the transmitted video stream. A Source device can set the MISC1 field, bit 6, to instruct a Sink device to use a VSC (Video_Stream_Configuration) SDP, as described in Section 2.2.5.6 instead of the MISC1/MISC0 fields for pixel encoding/colorimetry format indication. For YCbCr 4:2:0 and *ITU-R BT.2020* colorimetry formats, VSC SDP shall be used. The Sink device declares that it can support VSC for colorimetry and pixel encoding formats in the Extended Receiver Capability field (DPCD Addresses 02200h through 022FFh; see Table 2-193).

Table 2-96: MSA MISC1 and MISC0 Fields for Pixel Encoding/Colorimetry Format Indication[a]

Pixel Encoding/ Colorimetry Format	MSA Bits					
	MISC1		MISC0			
	6	7	2:1	3	4	7:5[b]
RGB unspecified color space (Legacy RGB mode)	When MISC1, bit 6, is Set to 1, a Source device uses a VSC SDP to indicate the Pixel Encoding/Colorimetry Format and that a Sink device shall ignore MISC1, bit 7, and MISC0, bits 7:1 (MISC1, bit 7, and MISC0, bits 7:1, become "don't care").	0	00	0	0	000, 001, 010, 011, 100 (6, 8, 10, 12, 16bpc, respectively)
CTA RGB (sRGB (*IEC 61966-2-1*) primaries)		0	00	1	0	
RGB wide gamut fixed point (XR8, XR10, XR12)		0	11	0	0	001, 010, 011 (8, 10, 12bpc, respectively)
RGB wide gamut floating point (scRGB (*IEC 61966-2-2*))		0	11	0	1	100 (16bpc)
Y-only		1	00	0	0	001, 010, 011, 100 (8, 10, 12, 16 bits/luminance, respectively)
RAW		1	01	0	0	001, 010, 011, 100, 101, 110, 111 (6, 7, 8, 10, 12, 14, 16bpp, respectively) 000 = RESERVED
YCbCr (*ITU-R BT.601*, *ITU-R BT.709*)		0	01 = 4:2:2 10 = 4:4:4	1	0 = BT.601 1 = BT.709	001, 010, 011, 100 (8, 10, 12, 16bpc, respectively)
xvYCC ($xvYCC_{601}$/$xvYCC_{709}$)		0	01 = 4:2:2 10 = 4:4:4	0	0 = BT.601 1 = BT.709	
Adobe RGB		0	00	1	1	000, 001, 010, 011, 100 (6, 8, 10, 12, 16bpc RGB, respectively)
DCI-P3 (*SMPTE RP 431-2*)		0	11	1	0	011, 100 (12, 16bpc RGB, respectively)
Color Profile[c]		0	11	1	1	000, 001, 010, 011, 100 (6, 8, 10, 12, 16bpc RGB, respectively)

a. All other values are RESERVED.
b. bpc = bits/component.
c. The "Color Profile" to be transported from a DP Source device to DP Sink device as "Simplified Color Profile" VCP code in MCCS Standard.

2.2.5 SDP Formats

Table 2-97 lists how the SDP is constructed. Table 2-98 lists the DP SDP types.

Table 2-97: SDP Header Bytes

Byte #	Content
HB0	**Secondary-data Packet ID**
HB1	**Secondary-data Packet Type**
HB2	**Secondary-data-packet-specific Header, Byte 0**
HB3	**Secondary-data-packet-specific Header, Byte 1**

Table 2-98: SDP Types

Packet Type Value	Packet Type	Transmission Timing	See
00h	DisplayPort RESERVED		
01h	Audio_TimeStamp	At least once per video frame.	Section 2.2.5.1
02h	Audio_Stream	During Main Video stream HBlank/VBlank period.	Section 2.2.5.2
03h	DisplayPort RESERVED		
04h	Extension	During Main Video stream HBlank/VBlank period.	Section 2.2.5.3
05h	Audio_CopyManagement	During Main Video stream HBlank/VBlank period.	Section 2.2.5.4
06h	ISRC	During Main Video stream HBlank/VBlank period.	Section 2.2.5.5
07h	Video_Stream_Configuration (VSC)	During Main Video stream HBlank/VBlank period.	Section 2.2.5.6 (General) Section 2.17.5 (Panel Replay)
0Fh through 08h	Camera Generic 0 through 7	During Main Video stream HBlank/VBlank period.	Section 2.2.5.7
10h	Picture Parameter Set (PPS)	During Main Video stream HBlank/VBlank period.	Section 2.2.5.8
1Fh through 11h	DisplayPort RESERVED		
20h	Video_Stream_Configuration Extension for VESA (VSC_EXT_VESA)	During Main Video stream HBlank/VBlank period.	Section 2.2.5.9
21h	VSC_EXT_CTA for future CTA INFOFRAME with payload of more than 28 bytes		Section 2.2.5.10
22h	Adaptive-Sync SDP		Section 2.2.5.11

Table 2-98: SDP Types (Continued)

Packet Type Value	Packet Type	Transmission Timing	See
7Fh through 23h	DisplayPort RESERVED		
80h + Audio INFOFRAME Type (04h)	*CTA-861-G* Audio INFOFRAME	As per *CTA-861-G* for Audio INFOFRAME.	Section 2.2.5.12
80h + Non-audio INFOFRAME Type	*CTA-861-G* Non-audio INFOFRAME	As per *CTA-861-G* for INFOFRAME.	

If multiple audio streams are being transported simultaneously, the Secondary-data Packet ID in HB0 shall be used to associate the Audio_Stream SDP with its Audio_TimeStamp SDP and *CTA-861-G* Audio INFOFRAME SDP.

2.2.5.1 Audio_TimeStamp SDP

Figure 2-22 illustrates an Audio_TimeStamp SDP over the Main-Link.

For the transport of an Audio_TimeStamp SDP without the main video stream, see Section 2.2.5.2.7. For more information about audio transport over DisplayPort, see Appendix A.

4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 0
SS	SS	SS	SS	SS	SS	SS
HB0	HB1	HB2	HB3	HB0	HB1	HB0
PB0	PB1	PB2	PB3	PB0	PB1	PB0
Maud[23:16]	Maud[23:16]	Maud[23:16]	Maud[23:16]	HB2	HB3	HB1
Maud[15:8]	Maud[15:8]	Maud[15:8]	Maud[15:8]	PB2	PB3	PB1
Maud[7:0]	Maud[7:0]	Maud[7:0]	Maud[7:0]	Maud[23:16]	Maud[23:16]	HB2
All 0s	All 0s	All 0s	All 0s	Maud[15:8]	Maud[15:8]	PB2
PB4	PB5	PB6	PB7	Maud[7:0]	Maud[7:0]	HB3
Naud[23:16]	Naud[23:16]	Naud[23:16]	Naud[23:16]	All 0s	All 0s	PB3
Naud[15:8]	Naud[15:8]	Naud[15:8]	Naud[15:8]	PB4	PB5	Maud[23:16]
Naud[7:0]	Naud[7:0]	Naud[7:0]	Naud[7:0]	Maud[23:16]	Maud[23:16]	Maud[15:8]
All 0s	All 0s	All 0s	All 0s	Maud[15:8]	Maud[15:8]	Maud[7:0]
PB8	PB9	PB10	PB11	Maud[7:0]	Maud[7:0]	All 0s
SE	SE	SE	SE	All 0s	All 0s	PB4
				PB6	PB7	Maud[23:16]
				Naud[23:16]	Naud[23:16]	Maud[15:8]
				Naud[15:8]	Naud[15:8]	Maud[7:0]
				Naud[7:0]	Naud[7:0]	All 0s
				All 0s	All 0s	PB5
				PB8	PB9	…
				Naud[23:16]	Naud[23:16]	Naud[23:16]
				Naud[15:8]	Naud[15:8]	Naud[15:8]
				Naud[7:0]	Naud[7:0]	Naud[7:0]
				All 0s	All 0s	All 0s
				PB10	PB11	PB10
				SE	SE	Naud[23:16]
						Naud[15:8]
						Naud[7:0]
						All 0s
						PB11
						SE

Figure 2-22: Audio_TimeStamp SDP Mapping over Main-Link

The Audio_TimeStamp SDP consists of Maud23:0 and Naud23:0. The relationship of Maud and Naud is expressed in the following equation:

$$Maud / Naud = 512 \times Fs / f\_LS\_Clk$$

where:

- *Fs* is the sampling frequency of the audio stream being transported

The Naud value is set to 2^{15} (=32768) when the audio clock is asynchronous to the LS_Clk.

In addition to the Audio_TimeStamp SDP, Maud[7:0] are transported once per main video stream horizontal line period, immediately following Mvid[7:0].

A Sink device shall avoid audio glitch as long as the Audio_TimeStamp SDP value's accuracy is within ±0.5%.

Note: *In MST mode, the Sink device shall ignore the Maud and Mvid values that are transmitted by an MST Source device unless the MST Sink device is directly connected to the MST Source device by way of a single link because the Source device generates those values based on the LS_Clk of the link that it is driving. An MST Sink device shall be able to regenerate a stream clock without depending on Mvid and Mvid time stamp values because the MST Sink device might be plugged into an MST Branch device, not an MST Source device.*

2.2.5.1.1 Audio_TimeStamp SDP Header

Table 2-99 describes the Audio_TimeStamp SDP header bytes.

Table 2-99: Audio_TimeStamp SDP Header Bytes

Byte #	Bit #	Content
HB0	7:0	**Secondary-data Packet ID** INFOFRAME SDP, Audio_TimeStamp SDP, Audio_Stream SDP, and Audio_CopyManagement SDP, and ISRC SDP shall have the same Packet ID when they are associated with the same audio stream.
HB1	7:0	**Secondary-data Packet Type** 01h.
HB2	7:0	**Least Significant Eight Bits of (Data Byte Count – 1)** 17h (i.e., Data Byte Count = 24 bytes). Unused bytes shall be zero-padded.
HB3	1:0	**Most Significant Two Bits of (Data Byte Count – 1)**
	7:2	**Audio_TimeStamp Version Number** 12h.

2.2.5.1.2 Audio_TimeStamp SDP Values (Informative)

Table 2-100 illustrates some examples of the Audio_TimeStamp SDP values for various audio sampling frequencies when the audio clock and Main-Link Symbol clock are synchronous.

Table 2-100: Audio_TimeStamp SDP Maud and Naud Value Examples (Informative)[a]

Coding Type	Audio Sample Frequency (kHz)	LS_Clk Frequency							
		162MHz		270MHz		540MHz		810MHz	
		Maud	Naud	Maud	Naud	Maud	Naud	Maud	Naud
L-PCM Audio and Compressed Audio with $Fs \leq$ 6.144Mbps	32	1024	10125	1024	16875	1024	33750	1024	50625
	44.1	784	5625	784	9375	784	18750	784	28125
	48	512	3375	512	5625	512	11250	512	16875
	64	2048	10125	2048	16875	2048	33750	2048	50625
	88.2	1568	5625	1568	9375	1568	18750	1568	28125
	96	1024	3375	1024	5625	1024	11250	1024	16875
	128	4096	10125	4096	16875	4096	33750	4096	50625
	176.4	3136	5625	3136	9375	3136	18750	3136	28125
	192	2048	3375	2048	5625	2048	11250	2048	16875
HBR	256	8192	10125	8192	16875	8192	33750	8192	50625
	352.8	6272	5625	6272	9375	6272	18750	6272	28125
	384	4096	3375	4096	5625	4096	11250	4096	16875
	512	16384	10125	16384	16875	16384	33750	16384	50625
	705.6	12544	5625	12544	9375	12544	18750	12544	28125
	768	8192	3375	8192	5625	8192	11250	8192	16875
	1024	32768	10125	32768	16875	32768	33750	32768	50625
	1411.2	25088	5625	25088	9375	25088	18750	25088	28125
	1536	16384	3375	16384	5625	16384	11250	16384	16875

Table 2-100: Audio_TimeStamp SDP Maud and Naud Value Examples (Informative)[a] (Continued)

Coding Type	Audio Sample Frequency (kHz)	LS_Clk Frequency							
		162MHz		270MHz		540MHz		810MHz	
		Maud	Naud	Maud	Naud	Maud	Naud	Maud	Naud
One Bit and DST audio at normal or double rate	2048 (64 × 32)	65536	10125	65536	16875	65536	33750	65536	50625
	2822.4 (64 × 44.1)	50176	5625	50176	9375	50176	18750	50176	28125
	3072 (64 × 48)	32768	3375	32768	5625	32768	11250	32768	16875
	4096 (128 × 32)	131072	10125	131072	16875	131072	33750	131072	50625
	5644.8 (128 × 44.1 and 64 × 88.2)	100352	5625	100352	9375	100352	18750	100352	28125
	6144 (128 × 48 and 64 × 96)	65536	3375	65536	5625	65536	11250	65536	16875
	11289.6 (128 × 88.2 and 64 × 176.4)	200704	5625	200704	9375	200704	18750	200704	28125
	12288 (128 × 96 and 64 × 192)	131072	3375	131072	5625	131072	11250	131072	16875
	22579.2 (128 × 176.4)	401408	5625	401408	9375	401408	18750	401408	28125
	24576 (128 × 192)	262144	3375	262144	5625	262144	11250	262144	16875

a. No down spreading, with synchronous clock, is assumed.

2.2.5.2 Audio_Stream SDP

Audio streams may be transported. When an audio stream is transported, the Audio INFOFRAME (non-Basic Audio) SDP that describes the attribute of the audio stream and Audio_TimeStamp SDP shall also be transported, once per frame during the main video stream's vertical blanking period.

Audio_Stream SDPs shall be transmitted during both horizontal and vertical blanking periods of the main video stream. During the horizontal and vertical blanking periods, a DP Source device shall transmit an Audio_Stream SDP whenever it has sufficient data to form a packet and access to the Main-Link to transmit the packet(s). For further details regarding audio transport over DisplayPort, see Section 2.2.5.2 and Appendix A.

Audio_Stream SDPs with compressed audio that uses the *IEC 61937* Transport standard shall program the HB3.Coding Type, as follows:

- 0000b = Encoded content ≤ 6.144Mbps is transmitted
- 0001b = Encoded content exceeding 6.144Mbps is transmitted over the link

IEC 61937-encoded bit rates that exceed 6.144Mbps shall be known as Audio High Bit Rate. DisplayPort allows nine different types of high bit rate transports, as listed in Table 2-101. Dolby TrueHD and DTS-HD Master Audio formats require higher bit rates for transport. A DP Source device shall use one of these nine high bit rates to transmit such encoded content.

Table 2-101: Audio High Bit Rate Mode (Informative)

DP 8-channel Layout Rate (kHz)	*IEC 61937* Payload Bit Rate 2 × 16 Bits/frame, 4 Frames/layout (Mbps)	*IEC 60958* Transport Bit Rate 2 × 32 Bits/frame (Mbps)	*IEC 60958* Frame Rate (kHz)	Audio_TimeStamp SDP *Fs* Indication (kHz)
64	8.192	16.384	256[a]	256
88.2	11.2896	22.5792	352.8[a]	352.8
96	12.288	24.576	384[a]	384
128	16.384	32.768	512[a]	512
176.4	22.5792	45.1584	705.6[a]	705.6
192	24.576	49.152	768	768
256[b]	32.768	65.536	1024[a]	1024
352.8[b]	45.1584	90.3168	1411.2[a]	1411.2
384[b]	49.152	98.304	1536[a]	1536

a. Audio High Bit Rate is ***not*** *supported in DP v1.3 (and lower).*
b. DP 8-channel layout rate exceeds DP v1.3 (and lower) maximum 8-channel layout rate.

HBR audio delivery shall use the 8-channel layout configuration. This results in four *IEC 60958* transport frames/layout. Audio_Stream SDP Header configuration should be as follows:

- *HB2.3DChannelCount* = 0 through 31 (N/A)
- *HB2.OneBit_DST_Double_Rate* = 0 through 1 (N/A)
- *HB3.ChannelCount* = 7 (8-channel mode)
- *HB3.CodingType* = 001b (*IEC 61937*-encoded audio High Bit Rate)

IEC 61937-encoded audio streams with bit rates less than or equal to 6.144Mbps shall be known as "Non-HBR *IEC 61937*-encoded audio." Non-HBR *IEC 61937*-encoded audio shall use the 2-channel layout configuration. DisplayPort allows nine different Non-HBR *IEC 61937* transports that use the 2-channel layout configuration (see Table 2-102). This configuration uses one *IEC 60958* transport frame/layout. The Audio_Stream SDP header configuration for this method should be as follows:

- *HB2.3DChannelCount* = 0 through 31 (N/A)
- *HB2.OneBit_DST_Double_Rate* = 0 through 1 (N/A)
- *HB3.ChannelCount* = 1 (2-channel mode)
- *HB3.CodingType* = 000b (Non-HBR *IEC 61937*-encoded audio)

Table 2-102: Non-HBR-encoded Audio 2-channel Layout (Informative)

DP 2-channel Layout Rate (kHz)	*IEC 61937* Payload Bit Rate 2 × 16 Bits/frame, 1 Frame/layout (Mbps)	*IEC 60958* Transport Bit Rate 2 × 32 Bits/frame (Mbps)	*IEC 60958* Frame Rate (kHz)	Audio_TimeStamp SDP *Fs* Indication (kHz)
32	1.024	2.048	32	32
44.1	1.4112	2.8224	44.1	44.1
48	1.536	3.072	48	48
64	2.048	4.096	64[a]	64
88.2	2.8224	5.6448	88.2	88.2
96	3.072	6.144	96	96
128	4.096	8.192	128[a]	128
176.4	5.6448	11.2896	176.4	176.4
192	6.144	12.288	192	192

*a. Audio Bit Rate is **not** supported in DP v1.3 (and lower).*

While it is theoretically possible to use the 8-channel layout configuration (see Table 2-103) to transport Non-HBR *IEC 61937*-encoded audio at 32, 44.1, and 48kHz sampling rates, the 8-channel layout shall **not** be used to convey Non-HBR *IEC 61937*-encoded audio.

Table 2-103: Non-HBR-encoded Audio 8-channel Layout (Informative)

DP 8-channel Layout Rate (kHz)	*IEC 61937* Payload Bit Rate 2 × 16 Bits/frame, 4 Frames/layout (Mbps)	*IEC 60958* Transport Bit Rate 2 × 32 Bits/frame (Mbps)	*IEC 60958* Frame Rate (kHz)	Audio_TimeStamp SDP *Fs* Indication (kHz)
32	4.096	8.192	128[a]	128
44.1	5.6448	11.2896	176.4	176.4
48	6.144	12.288	192	192

*a. Audio Bit Rate is **not** supported in DP v1.3 (and lower).*

Audio_Stream SDPs with no compression, L-PCM Audio and L-PCM 3D Audio can have four layouts (two each), as listed in Table 2-104. The Audio_Stream SDP header configuration for L-PCM Audio and L-PCM 3D Audio is as follows:

- 2-channel L-PCM Audio
  - *HB2.3DChannelCount* = 0 through 31 (N/A)
  - *HB2.OneBit_DST_Double_Rate* = 0 through 1 (N/A)
  - *HB3.ChannelCount* = 0 or 1 (2-channel mode)
  - *HB3.CodingType* = 000b (L-PCM Audio, coding type indicated in *IEC 60958* header)
- 8-channel L-PCM Audio
  - *HB2.3DChannelCount* = 0 through 31 (N/A)
  - *HB2.OneBit_DST_Double_Rate* = 0 through 1 (N/A)
  - *HB3.ChannelCount* = 2 through 7 (8-channel mode)
  - *HB3.CodingType* = 000b (L-PCM Audio, coding type indicated in *IEC 60958* header)
- 16-channel L-PCM 3D Audio
  - *HB2.3DChannelCount* = 0 through 15 (16-channel mode)
  - *HB2.OneBit_DST_Double_Rate* = 0 through 1 (N/A)
  - *HB3.ChannelCount* = 0 through 7 (N/A)
  - *HB3.CodingType* = 010b (L-PCM 3D Audio)
- 32-channel L-PCM 3D Audio
  - *HB2.3DChannelCount* = 16 through 31 (32-channel mode)
  - *HB2.OneBit_DST_Double_Rate* = 0 through 1 (N/A)
  - *HB3.ChannelCount* = 0 through 7 (N/A)
  - *HB3.CodingType* = 010b (L-PCM 3D Audio)

Table 2-104: L-PCM Audio and L-PCM 3D Audio Modes (Informative)

DP Layout Rate (kHz)	*IEC 60958* Data Transport Rate 2 × 32 Bits/frame				Audio_TimeStamp SDP *Fs* Indication (kHz)
	2-channel L-PCM Audio 1 Frame/layout (Mbps)	8-channel L-PCM Audio 4 Frames/layout (Mbps)	16-channel L-PCM 3D Audio 8 Frames/layout (Mbps)	32-channel L-PCM 3D Audio 16 Frames/layout (Mbps)	
32	2.048	8.192	16.384	32.768	32
44.1	2.8224	11.2896	22.5792	45.1584	44.1
48	3.072	12.288	24.576	49.152	48
64[a]	4.096	16.384	N/A	N/A	64
88.2	5.6448	22.5792	45.1584	90.3168	88.2
96	6.144	24.576	49.152	98.304	96
128[a]	8.192	32.768	N/A	N/A	128
176.4	11.2896	45.1584	90.3168	180.6336	176.4
192	12.288	49.152	98.304	196.608	192

*a. Audio Bit Rate is **not** supported in DP v1.3 (and lower).*

Audio_Stream SDPs with One Bit or DST audio can have three layouts, as listed in Table 2-105. The Audio_Stream SDP header configuration for One Bit and DST audio is as follows:

- 2-channel One Bit audio
  - *HB2.3DChannelCount* = 0 through 31 (N/A)
  - *HB2.OneBit_DST_Double_Rate* = 0 or 1 (64x or 128x)
  - *HB3.ChannelCount* = 0 or 1 (2-channel mode)
  - *HB3.CodingType* = 011b (One Bit audio coding type)
- 8-channel One Bit audio
  - *HB2.3DChannelCount* = 0 through 31 (N/A)
  - *HB2.OneBit_DST_Double_Rate* = 0 or 1 (64x or 128x)
  - *HB3.ChannelCount* = 2 through 7 (8-channel mode)
  - *HB3.CodingType* = 011b (One Bit audio coding type)
- DST audio
  - *HB2.3DChannelCount* = 0 through 31 (N/A)
  - *HB2.OneBit_DST_Double_Rate* = 0 or 1 (64x or 128x)
  - *HB3.ChannelCount* = 0 through 7 (N/A)
  - *HB3.CodingType* = 100b (DST audio coding type)

Table 2-105: One Bit and DST Audio Modes (Informative)

Sample Frequency, as Indicated in Audio INFOFRAME (kHz)	HB2.OneBit_DST_Double_Rate	# of Bytes/frame at 75 fps	One Bit Layouts/frame at 75fps[a]	One Bit Layout Rate (kHz)	2-channel One Bit Transport Rate at 64 Bits/layout (Mbps)	8-channel One Bit Transport Rate at 256 Bits/layout (Mbps)	DST Layouts/frame at 75fps[b]	DST Layout Rate (kHz)	DST Transport Rate at 256 Bits/layout (Mbps)	Audio_TimeStamp SDP *Fs* Indication (kHz)
32	0	3413.333	975.238	73.143	4.681	18.725	–	–	–	2048
	1	6826.667	1950.476	146.286	9.362	37.449	–	–	–	4096
44.1	0	4704	1344	100.8	6.451	25.805	168	12.6	3.226	2822.4
	1	9408	2688	201.6	12.902	51.610	336	25.2	6.451	5644.8
48	0	5120	1462.857	109.714	7.022	28.087	–	–	–	3072
	1	10240	2925.714	219.429	14.043	56.174	–	–	–	6144
88.2	0	9408	2688	201.6	12.902	51.610	336	25.2	6.451	5644.8
	1	18816	5376	403.2	25.805	103.219	672	50.4	12.902	11289.6
96	0	10240	2925.714	219.429	14.043	56.174	–	–	–	6144
	1	20480	5851.429	438.857	28.087	112.347	–	–	–	12288
176.4	0	18816	5376	403.2	25.805	103.219	672	50.4	12.902	11289.6
	1	37632	10752	806.4	51.610	206.438	1344	100.8	25.805	22579.2
192	0	20480	5851.429	438.857	28.087	112.347	–	–	–	12288
	1	40960	11702.857	877.714	56.174	224.695	–	–	–	24576

a. One Bit audio format follows CSA ISO/IEC 14496-3, Subpart 10, and the 44.1kHz group of sampling frequencies listed in that standard. Although One Bit audio operation at 32, 48, 96, and 192kHz is possible, it is beyond the scope of the CSA ISO/IEC 14496-3-specified 44.1kHz group of sample frequencies. Transport at these non-standard sample frequencies shall yield 1/75-second data frame boundaries that reside within the layout and **not** *on the layout boundary, as is the case for the standard 44.1kHz group. Introduction of the frame flag to the One Bit audio stream allows for optional insertion of the GTC presentation time at a fixed 1/75-second interval, as outlined in Section 2.16.2. Operation of One Bit audio at non-standard sample frequencies, however, does* **not** *allow for use of GTC because the fixed 1/75-second interval cannot be achieved after the frame flag is moved to the closest layout boundary.*

b. DST audio format follows the CSA ISO/IEC 14496-3, Subpart 10, and the 44.1kHz group of sampling frequencies listed in that standard. DST Audio operation at 32, 48, 96, and 192kHz sample frequency is **not** *supported because it is not specified in the CSA ISO/IEC 14496-3, Subpart 10 coding technique.*

2.2.5.2.1 Audio Playback Latency Mandate

A DP Sink device audio recovery time from idle to playback (i.e., audio being presented to the user) shall not exceed 50ms from the time the first Audio Sample, Audio INFOFRAME, or audio clock regeneration packet is received. The Sink device shall mute playback during recovery of the local audio clock to avoid audible noise. A DP Source device may transmit Audio_TimeStamp and/or INFOFRAME SDPs prior to transmitting the Audio_Stream SDP to ensure that any recovery necessary at the DP Sink device has completed.

2.2.5.2.2 Audio_Stream SDP Header

Table 2-106 describes the Audio_Stream SDP header bytes.

Table 2-106: Audio_Stream SDP Header Bytes

Byte #	Bit #	Content
HB0	7:0	**Secondary-data Packet ID** INFOFRAME SDP, Audio_TimeStamp SDP, Audio_Stream SDP, Audio_CopyManagement SDP, and ISRC SDP shall have the same Packet ID when they are associated with the same audio stream.
HB1	7:0	**Secondary-data Packet Type** 02h.
HB2	4:0	**3DChannelCount** New to *DP v1.4*. Applicable only for L-PCM 3D Audio coding types. Indicates *Number of Channels – 1*. Available in 16- and 32-channel layouts: • 16-channel layout is identified exclusively as using this field, and is greater than or equal to 0, but less than 16. Includes the possibility of Mono or Stereo Audio carried in this L-PCM 3D Audio Coding Type layout. Values range from 0000b to 1111b. • 32-channel layout is identified exclusively as using this field, and is greater than or equal to 16, but less than 32. Values range from 10000b to 11111b. For all 3D-channel layouts, there is no mandate on a DP Source device to match this value to the actual channel count. A DP Sink device shall use this field to determine whether the incoming Audio_Stream SDP has a 16- or 32-channel layout. Actual channel count and the channel-to-speaker mapping shall be obtained from the Audio INFOFRAME SDP Channel Allocation field, as well as DB6 through DB9.
	5	**OneBit_DST_Double_Rate** New to *DP v1.4*. Applicable only for One Bit audio or DST audio coding types. 0 = One Bit audio or underlying uncompressed DST bitstream sample rate = 64x sample frequency, as indicated in DB2 of the Audio INFOFRAME SDP. 1 = One Bit audio or underlying uncompressed DST bitstream sample rate = 128x sample frequency, as indicated in DB2 of Audio INFOFRAME SDP.
	7:6	**RESERVED** Read all 0s.

Table 2-106: Audio_Stream SDP Header Bytes (Continued)

Byte #	Bit #	Content
HB3	2:0	**ChannelCount** 2-channel layout and mono vs. stereo are identified exclusively using this field: 000b = Mono. 001b = Stereo. 8-channel layout is identified exclusively as using this field, and is greater than or equal to 010b. For 8-channel layout, there is no mandate on a Source device to match this value to the actual channel count, and a Sink device shall use this field to determine whether the incoming Audio_Stream SDP has an 8-channel layout. Actual channel count and the channel-to-speaker mapping shall be obtained from the Audio INFOFRAME SDP Channel Allocation field. 010b = Three channels. 011b = Four channels. 100b = Five channels. 101b = Six channels. 110b = Seven channels. 111b = Eight channels.
	3	**RESERVED** Read 0.
	7:4	**Coding Type** Support for values 2h through 4h added in *DP v1.4*. 0h = 2- to 8-channel L-PCM Audio 192kHz content/*IEC 61937*-encoded content with bit rates less than or equal to 6.144Mbps (*IEC 60958*-like encoding). 1h = *IEC 61937*-encoded content for bit rates exceeding 6.144Mbps (*IEC 60958*-like encoding). 2h = 1- to 32-channel L-PCM 3D Audio, up to 192kHz content; used in conjunction with the HB2 3DChannelCount field (bits 4:0), which renders the ChannelCount field inapplicable. 3h = One Bit audio; used in conjunction with the ChannelCount field, which renders the HB2 3DChannelCount field (bits 4:0) inapplicable. 4h = DST audio; both ChannelCount and 3DChannelCount are inapplicable. The number of DST Audio channels is carried in the audio payload stream itself. All other values are RESERVED for DisplayPort.

2.2.5.2.3 Audio_Stream Data Mapping over the Main-Link

The HB3 ChannelCount field (bits 2:0) of an Audio_Stream SDP is the count of non-L-PCM 3D Audio or One Bit audio channels transmitted through a DP Main-Link. The DPRX shall use this 3-bit value to decide how to interpret the payload of an Audio_Stream SDP. One to eight channels are supported in non-L-PCM 3D Audio, *IEC 61937*-encoded, or One Bit DP audio transport.

The HB2 3DChannelCount field (bits 4:0) of an Audio_Stream SDP is the count of L-PCM 3D Audio channels transmitted through a DP Main-Link. The DPRX shall use this 5-bit value to determine how to interpret the Audio_Stream SDP payload. DP L-PCM 3D Audio transport shall support 1 to 32 channels.

Figure 2-23 illustrates the Audio_Stream SDP mapping over the Main-Link for 1- to 2-channel L-PCM Audio, *IEC 61937*-encoded Non-HBR audio, or One Bit audio. Figure 2-24 illustrates the Audio_Stream SDP mapping over the Main-Link for 3- to 8-channel L-PCM Audio, *IEC 61937*-encoded HBR audio, or One Bit audio. Figure 2-32 illustrates the mapping within each 4-byte payload of the L-PCM Audio or *IEC 61937*-encoded Audio_Stream SDP. Figure 2-33 illustrates the mapping within each 4-byte payload of the One Bit Audio_Stream SDP.

4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 0
SS	SS	SS	SS	SS	SS	SS
HB0	HB1	HB2	HB3	HB0	HB1	HB0
PB0	PB1	PB2	PB3	PB0	PB1	PB0
S0_Ch1_B0	S0_Ch2_B0	S1_Ch1_B0	S1_Ch2_B0	HB2	HB3	HB1
S0_Ch1_B1	S0_Ch2_B1	S1_Ch1_B1	S1_Ch2_B1	PB2	PB3	PB1
S0_Ch1_B2	S0_Ch2_B2	S1_Ch1_B2	S1_Ch2_B2	S0_Ch1_B0	S0_Ch2_B0	HB2
S0_Ch1_B3	S0_Ch2_B3	S1_Ch1_B3	S1_Ch2_B3	S0_Ch1_B1	S0_Ch2_B1	PB2
PB4	PB5	PB6	PB7	S0_Ch1_B2	S0_Ch2_B2	HB3
S2_Ch1_B0	S2_Ch2_B0	S3_Ch1_B0	S3_Ch2_B0	S0_Ch1_B3	S0_Ch2_B3	PB3
S2_Ch1_B1	S2_Ch2_B1	S3_Ch1_B1	S3_Ch2_B1	PB4	PB5	S0_Ch1_B0
S2_Ch1_B2	S2_Ch2_B2	S3_Ch1_B2	S3_Ch2_B2	S1_Ch1_B0	S1_Ch2_B0	S0_Ch1_B1
S2_Ch1_B3	S2_Ch2_B3	S3_Ch1_B3	S3_Ch2_B3	S1_Ch1_B1	S1_Ch2_B1	S0_Ch1_B2
PB8	PB9	PB10	PB11	S1_Ch1_B2	S1_Ch2_B2	S0_Ch1_B3
SE	SE	SE	SE	S1_Ch1_B3	S1_Ch2_B3	PB4
				PB6	PB7	S0_Ch2_B0
				S2_Ch1_B0	S2_Ch2_B0	S0_Ch2_B1
				S2_Ch1_B1	S2_Ch2_B1	S0_Ch2_B2
				S2_Ch1_B2	S2_Ch2_B2	S0_Ch2_B3
				S2_Ch1_B3	S2_Ch2_B3	PB5
				PB8	PB9	S1_Ch1_B0
				S3_Ch1_B0	S3_Ch2_B0	S1_Ch1_B1
				S3_Ch1_B1	S3_Ch2_B1	S1_Ch1_B2
				S3_Ch1_B2	S3_Ch2_B2	S1_Ch1_B3
				S3_Ch1_B3	S3_Ch2_B3	PB6
				PB10	PB11	S1_Ch2_B0
				SE	SE	S1_Ch2_B1
						S1_Ch2_B2
						S1_Ch2_B3
						PB7
						…
						S3_Ch1_B0
						S3_Ch1_B1
						S3_Ch1_B2
						S3_Ch1_B3
						PB10
						S3_Ch2_B0
						S3_Ch2_B1
						S3_Ch2_B2
						S3_Ch2_B3
						PB11
						SE

where:

- S = Sample
- B = Byte
- Ch = Channel

For example, “S0_Ch1_B0” refers to Byte 0 of Channel 1 of Sample 0.

Figure 2-23: Audio_Stream SDP over Main-Link for 2-Channel Layout Audio

4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 0
SS	SS	SS	SS	SS	SS	SS
HB0	HB1	HB2	HB3	HB0	HB1	HB0
PB0	PB1	PB2	PB3	PB0	PB1	PB0
S0_Ch1_B0	S0_Ch2_B0	S0_Ch3_B0	S0_Ch4_B0	HB2	HB3	HB1
S0_Ch1_B1	S0_Ch2_B1	S0_Ch3_B1	S0_Ch4_B1	PB2	PB3	PB1
S0_Ch1_B2	S0_Ch2_B2	S0_Ch3_B2	S0_Ch4_B2	S0_Ch1_B0	S0_Ch2_B0	HB2
S0_Ch1_B3	S0_Ch2_B3	S0_Ch3_B3	S0_Ch4_B3	S0_Ch1_B1	S0_Ch2_B1	PB2
PB4	PB5	PB6	PB7	S0_Ch1_B2	S0_Ch2_B2	HB3
S0_Ch5_B0	S0_Ch6_B0	S0_Ch7_B0	S0_Ch8_B0	S0_Ch1_B3	S0_Ch2_B3	PB3
S0_Ch5_B1	S0_Ch6_B1	S0_Ch7_B1	S0_Ch8_B1	PB4	PB5	S0_Ch1_B0
S0_Ch5_B2	S0_Ch6_B2	S0_Ch7_B2	S0_Ch8_B2	S0_Ch3_B0	S0_Ch4_B0	S0_Ch1_B1
S0_Ch5_B3	S0_Ch6_B3	S0_Ch7_B3	S0_Ch8_B3	S0_Ch3_B1	S0_Ch4_B1	S0_Ch1_B2
PB8	PB9	PB10	PB11	S0_Ch3_B2	S0_Ch4_B2	S0_Ch1_B3
SE	SE	SE	SE	S0_Ch3_B3	S0_Ch4_B3	PB4
				PB6	PB7	S0_Ch2_B0
				S0_Ch5_B0	S0_Ch6_B0	S0_Ch2_B1
				S0_Ch5_B1	S0_Ch6_B1	S0_Ch2_B2
				S0_Ch5_B2	S0_Ch6_B2	S0_Ch2_B3
				S0_Ch5_B3	S0_Ch6_B3	PB5
				PB8	PB9	S0_Ch3_B0
				S0_Ch7_B0	S0_Ch8_B0	S0_Ch3_B1
				S0_Ch7_B1	S0_Ch8_B1	S0_Ch3_B2
				S0_Ch7_B2	S0_Ch8_B2	S0_Ch3_B3
				S0_Ch7_B3	S0_Ch8_B3	PB6
				PB10	PB11	S0_Ch4_B0
				SE	SE	S0_Ch4_B1
						S0_Ch4_B2
						S0_Ch4_B3
						PB7
						S0_Ch5_B0
						S0_Ch5_B1
						S0_Ch5_B2
						S0_Ch5_B3
						PB8
						…
						S0_Ch8_B0
						S0_Ch8_B1
						S0_Ch8_B2
						S0_Ch8_B3
						PB11
						SE

where:

- S = Sample
- B = Byte
- Ch = Channel

For example, “S0_Ch1_B0” refers to Byte 0 of Channel 1 of Sample 0.

Figure 2-24: Audio_Stream SDP over Main-Link for 8-Channel Layout Audio

Figure 2-25 illustrates the Audio_Stream SDP mapping over the Main-Link for 1- to 16-channel L-PCM 3D Audio. Figure 2-26 illustrates the mapping for 17- to 32-channel L-PCM 3D Audio. Figure 2-32 illustrates the mapping within each 4-byte payload of the L-PCM 3D Audio Audio_Stream SDP. Table 2-107 lists the number of audio samples carried by each L-PCM 3D Audio Audio_Stream SDP.

Table 2-107: Audio Samples Carried By Each L-PCM 3D Audio Audio_Stream SDP

Audio # of Channels	# of Sets of 32-bit Audio Packet Payload	# of Audio Samples Carried
1 to 2	2	1
3 to 8	8	1
1 to 16	16	1
17 to 32	32	1

4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 0
SS	SS	SS	SS	SS	SS	SS
HB0	HB1	HB2	HB3	HB0	HB1	HB0
PB0	PB1	PB2	PB3	PB0	PB1	PB0
S0_Ch1_B0	S0_Ch2_B0	S0_Ch3_B0	S0_Ch4_B0	HB2	HB3	HB1
S0_Ch1_B1	S0_Ch2_B1	S0_Ch3_B1	S0_Ch4_B1	PB2	PB3	PB1
S0_Ch1_B2	S0_Ch2_B2	S0_Ch3_B2	S0_Ch4_B2	S0_Ch1_B0	S0_Ch2_B0	HB2
S0_Ch1_B3	S0_Ch2_B3	S0_Ch3_B3	S0_Ch4_B3	S0_Ch1_B1	S0_Ch2_B1	PB2
PB4	PB5	PB6	PB7	S0_Ch1_B2	S0_Ch2_B2	HB3
S0_Ch5_B0	S0_Ch6_B0	S0_Ch7_B0	S0_Ch8_B0	S0_Ch1_B3	S0_Ch2_B3	PB3
S0_Ch5_B1	S0_Ch6_B1	S0_Ch7_B1	S0_Ch8_B1	PB4	PB5	S0_Ch1_B0
S0_Ch5_B2	S0_Ch6_B2	S0_Ch7_B2	S0_Ch8_B2	S0_Ch3_B0	S0_Ch4_B0	S0_Ch1_B1
S0_Ch5_B3	S0_Ch6_B3	S0_Ch7_B3	S0_Ch8_B3	S0_Ch3_B1	S0_Ch4_B1	S0_Ch1_B2
PB8	PB9	PB10	PB11	S0_Ch3_B2	S0_Ch4_B2	S0_Ch1_B3
S0_Ch9_B0	S0_Ch10_B0	S0_Ch11_B0	S0_Ch12_B0	S0_Ch3_B3	S0_Ch4_B3	PB4
S0_Ch9_B1	S0_Ch10_B1	S0_Ch11_B1	S0_Ch12_B1	PB6	PB7	S0_Ch2_B0
S0_Ch9_B2	S0_Ch10_B2	S0_Ch11_B2	S0_Ch12_B2	S0_Ch5_B0	S0_Ch6_B0	S0_Ch2_B1
S0_Ch9_B3	S0_Ch10_B3	S0_Ch11_B3	S0_Ch12_B3	S0_Ch5_B1	S0_Ch6_B1	S0_Ch2_B2
PB12	PB13	PB14	PB15	S0_Ch5_B2	S0_Ch6_B2	S0_Ch2_B3
S0_Ch13_B0	S0_Ch14_B0	S0_Ch15_B0	S0_Ch16_B0	S0_Ch5_B3	S0_Ch6_B3	PB5
S0_Ch13_B1	S0_Ch14_B1	S0_Ch15_B1	S0_Ch16_B1	PB8	PB9	S0_Ch3_B0
S0_Ch13_B2	S0_Ch14_B2	S0_Ch15_B2	S0_Ch16_B2	S0_Ch7_B0	S0_Ch8_B0	S0_Ch3_B1
S0_Ch13_B3	S0_Ch14_B3	S0_Ch15_B3	S0_Ch16_B3	S0_Ch7_B1	S0_Ch8_B1	S0_Ch3_B2
PB16	PB17	PB18	PB19	S0_Ch7_B2	S0_Ch8_B2	S0_Ch3_B3
SE	SE	SE	SE	S0_Ch7_B3	S0_Ch8_B3	PB6
				PB10	PB11	S0_Ch4_B0
				S0_Ch9_B0	S0_Ch10_B0	S0_Ch4_B1
				S0_Ch9_B1	S0_Ch10_B1	S0_Ch4_B2
				S0_Ch9_B2	S0_Ch10_B2	S0_Ch4_B3
				S0_Ch9_B3	S0_Ch10_B3	PB7
				PB12	PB13	S0_Ch5_B0
				S0_Ch11_B0	S0_Ch12_B0	S0_Ch5_B1
				S0_Ch11_B1	S0_Ch12_B1	S0_Ch5_B2
				S0_Ch11_B2	S0_Ch12_B2	S0_Ch5_B3
				S0_Ch11_B3	S0_Ch12_B3	PB8
				PB14	PB15	…
				S0_Ch13_B0	S0_Ch14_B0	S0_Ch15_B0
				S0_Ch13_B1	S0_Ch14_B1	S0_Ch15_B1
				S0_Ch13_B2	S0_Ch14_B2	S0_Ch15_B2
				S0_Ch13_B3	S0_Ch14_B3	S0_Ch15_B3
				PB16	PB17	PB18
				S0_Ch15_B0	S0_Ch16_B0	S0_Ch16_B0
				S0_Ch15_B1	S0_Ch16_B1	S0_Ch16_B1
				S0_Ch15_B2	S0_Ch16_B2	S0_Ch16_B2
				S0_Ch15_B3	S0_Ch16_B3	S0_Ch16_B3
				PB18	PB19	PB19
				SE	SE	SE

where:

- S = Sample
- B = Byte
- Ch = Channel

For example, “S0_Ch1_B0” refers to Byte 0 of Channel 1 of Sample 0.

Figure 2-25: Audio_Stream SDP over Main-Link for 16-Channel Layout Audio (L-PCM 3D Audio Extension Type Code 13)

4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 0
SS	SS	SS	SS	SS	SS	SS
HB0	HB1	HB2	HB3	HB0	HB1	HB0
PB0	PB1	PB2	PB3	PB0	PB1	PB0
S0_Ch1_B0	S0_Ch2_B0	S0_Ch3_B0	S0_Ch4_B0	HB2	HB3	HB1
S0_Ch1_B1	S0_Ch2_B1	S0_Ch3_B1	S0_Ch4_B1	PB2	PB3	PB1
S0_Ch1_B2	S0_Ch2_B2	S0_Ch3_B2	S0_Ch4_B2	S0_Ch1_B0	S0_Ch2_B0	HB2
S0_Ch1_B3	S0_Ch2_B3	S0_Ch3_B3	S0_Ch4_B3	S0_Ch1_B1	S0_Ch2_B1	PB2
PB4	PB5	PB6	PB7	S0_Ch1_B2	S0_Ch2_B2	HB3
S0_Ch5_B0	S0_Ch6_B0	S0_Ch7_B0	S0_Ch8_B0	S0_Ch1_B3	S0_Ch2_B3	PB3
S0_Ch5_B1	S0_Ch6_B1	S0_Ch7_B1	S0_Ch8_B1	PB4	PB5	S0_Ch1_B0
S0_Ch5_B2	S0_Ch6_B2	S0_Ch7_B2	S0_Ch8_B2	S0_Ch3_B0	S0_Ch4_B0	S0_Ch1_B1
S0_Ch5_B3	S0_Ch6_B3	S0_Ch7_B3	S0_Ch8_B3	S0_Ch3_B1	S0_Ch4_B1	S0_Ch1_B2
PB8	PB9	PB10	PB11	S0_Ch3_B2	S0_Ch4_B2	S0_Ch1_B3
S0_Ch9_B0	S0_Ch10_B0	S0_Ch11_B0	S0_Ch12_B0	S0_Ch3_B3	S0_Ch4_B3	PB4
S0_Ch9_B1	S0_Ch10_B1	S0_Ch11_B1	S0_Ch12_B1	PB6	PB7	S0_Ch2_B0
S0_Ch9_B2	S0_Ch10_B2	S0_Ch11_B2	S0_Ch12_B2	S0_Ch5_B0	S0_Ch6_B0	S0_Ch2_B1
S0_Ch9_B3	S0_Ch10_B3	S0_Ch11_B3	S0_Ch12_B3	S0_Ch5_B1	S0_Ch6_B1	S0_Ch2_B2
PB12	PB13	PB14	PB15	S0_Ch5_B2	S0_Ch6_B2	S0_Ch2_B3
S0_Ch13_B0	S0_Ch14_B0	S0_Ch15_B0	S0_Ch16_B0	S0_Ch5_B3	S0_Ch6_B3	PB5
S0_Ch13_B1	S0_Ch14_B1	S0_Ch15_B1	S0_Ch16_B1	PB8	PB9	S0_Ch3_B0
S0_Ch13_B2	S0_Ch14_B2	S0_Ch15_B2	S0_Ch16_B2	S0_Ch7_B0	S0_Ch8_B0	S0_Ch3_B1
S0_Ch13_B3	S0_Ch14_B3	S0_Ch15_B3	S0_Ch16_B3	S0_Ch7_B1	S0_Ch8_B1	S0_Ch3_B2
PB16	PB17	PB18	PB19	S0_Ch7_B2	S0_Ch8_B2	S0_Ch3_B3
S0_Ch17_B0	S0_Ch18_B0	S0_Ch19_B0	S0_Ch20_B0	S0_Ch7_B3	S0_Ch8_B3	PB6
S0_Ch17_B1	S0_Ch18_B1	S0_Ch19_B1	S0_Ch20_B1	PB10	PB11	S0_Ch4_B0
S0_Ch17_B2	S0_Ch18_B2	S0_Ch19_B2	S0_Ch20_B2	S0_Ch9_B0	S0_Ch10_B0	S0_Ch4_B1
S0_Ch17_B3	S0_Ch18_B3	S0_Ch19_B3	S0_Ch20_B3	S0_Ch9_B1	S0_Ch10_B1	S0_Ch4_B2
PB20	PB21	PB22	PB23	S0_Ch9_B2	S0_Ch10_B2	S0_Ch4_B3
S0_Ch21_B0	S0_Ch22_B0	S0_Ch23_B0	S0_Ch24_B0	S0_Ch9_B3	S0_Ch10_B3	PB7
S0_Ch21_B1	S0_Ch22_B1	S0_Ch23_B1	S0_Ch24_B1	PB12	PB13	S0_Ch5_B0
S0_Ch21_B2	S0_Ch22_B2	S0_Ch23_B2	S0_Ch24_B2	S0_Ch11_B0	S0_Ch12_B0	S0_Ch5_B1
S0_Ch21_B3	S0_Ch22_B3	S0_Ch23_B3	S0_Ch24_B3	S0_Ch11_B1	S0_Ch12_B1	S0_Ch5_B2
PB24	PB25	PB26	PB27	S0_Ch11_B2	S0_Ch12_B2	S0_Ch5_B3
S0_Ch25_B0	S0_Ch26_B0	S0_Ch27_B0	S0_Ch28_B0	S0_Ch11_B3	S0_Ch12_B3	PB8
S0_Ch25_B1	S0_Ch26_B1	S0_Ch27_B1	S0_Ch28_B1	PB14	PB15	S0_Ch6_B0
S0_Ch25_B2	S0_Ch26_B2	S0_Ch27_B2	S0_Ch28_B2	S0_Ch13_B0	S0_Ch14_B0	S0_Ch6_B1
S0_Ch25_B3	S0_Ch26_B3	S0_Ch27_B3	S0_Ch28_B3	S0_Ch13_B1	S0_Ch14_B1	S0_Ch6_B2
PB28	PB29	PB30	PB31	S0_Ch13_B2	S0_Ch14_B2	S0_Ch6_B3
S0_Ch29_B0	S0_Ch30_B0	S0_Ch31_B0	S0_Ch32_B0	S0_Ch13_B3	S0_Ch14_B3	PB9
S0_Ch29_B1	S0_Ch30_B1	S0_Ch31_B1	S0_Ch32_B1	PB16	PB17	S0_Ch7_B0
S0_Ch29_B2	S0_Ch30_B2	S0_Ch31_B2	S0_Ch32_B2	S0_Ch15_B0	S0_Ch16_B0	S0_Ch7_B1
S0_Ch29_B3	S0_Ch30_B3	S0_Ch31_B3	S0_Ch32_B3	S0_Ch15_B1	S0_Ch16_B1	S0_Ch7_B2
PB32	PB33	PB34	PB35	S0_Ch15_B2	S0_Ch16_B2	S0_Ch7_B3
SE	SE	SE	SE	S0_Ch15_B3	S0_Ch16_B3	PB10

Figure 2-26: Audio_Stream SDP over Main-Link for 32-Channel Layout Audio (L-PCM 3D Audio Extension Type Code 13)

4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 0
where: • S = Sample • B = Byte • Ch = Channel For example, “S0_Ch1_B0” refers to Byte 0 of Channel 1 of Sample 0.				PB18	PB19	S0_Ch8_B0
				S0_Ch17_B0	S0_Ch18_B0	S0_Ch8_B1
				S0_Ch17_B1	S0_Ch18_B1	S0_Ch8_B2
				S0_Ch17_B2	S0_Ch18_B2	S0_Ch8_B3
				S0_Ch17_B3	S0_Ch18_B3	PB11
				PB20	PB21	S0_Ch9_B0
				S0_Ch19_B0	S0_Ch20_B0	S0_Ch9_B1
				S0_Ch19_B1	S0_Ch20_B1	S0_Ch9_B2
				S0_Ch19_B2	S0_Ch20_B2	S0_Ch9_B3
				S0_Ch19_B3	S0_Ch20_B3	PB12
				PB22	PB23	S0_Ch10_B0
				S0_Ch21_B0	S0_Ch22_B0	S0_Ch10_B1
				S0_Ch21_B1	S0_Ch22_B1	S0_Ch10_B2
				S0_Ch21_B2	S0_Ch22_B2	S0_Ch10_B3
				S0_Ch21_B3	S0_Ch22_B3	PB13
				PB24	PB25	S0_Ch11_B0
				S0_Ch23_B0	S0_Ch24_B0	S0_Ch11_B1
				S0_Ch23_B1	S0_Ch24_B1	S0_Ch11_B2
				S0_Ch23_B2	S0_Ch24_B2	S0_Ch11_B3
				S0_Ch23_B3	S0_Ch24_B3	PB14
				PB26	PB27	S0_Ch12_B0
				S0_Ch25_B0	S0_Ch26_B0	S0_Ch12_B1
				S0_Ch25_B1	S0_Ch26_B1	S0_Ch12_B2
				S0_Ch25_B2	S0_Ch26_B2	S0_Ch12_B3
				S0_Ch25_B3	S0_Ch26_B3	PB15
				PB28	PB29	S0_Ch13_B0
				S0_Ch27_B0	S0_Ch28_B0	S0_Ch13_B1
				S0_Ch27_B1	S0_Ch28_B1	S0_Ch13_B2
				S0_Ch27_B2	S0_Ch28_B2	S0_Ch13_B3
				S0_Ch27_B3	S0_Ch28_B3	PB16
				PB30	PB31	…
				S0_Ch29_B0	S0_Ch30_B0	S0_Ch31_B0
				S0_Ch29_B1	S0_Ch30_B1	S0_Ch31_B1
				S0_Ch29_B2	S0_Ch30_B2	S0_Ch31_B2
				S0_Ch29_B3	S0_Ch30_B3	S0_Ch31_B3
				PB32	PB33	PB34
				S0_Ch31_B0	S0_Ch32_B0	S0_Ch32_B0
				S0_Ch31_B1	S0_Ch32_B1	S0_Ch32_B1
				S0_Ch31_B2	S0_Ch32_B2	S0_Ch32_B2
				S0_Ch31_B3	S0_Ch32_B3	S0_Ch32_B3
				PB34	PB35	PB35
				SE	SE	SE

Figure 2-26: Audio_Stream SDP over Main-Link for 32-Channel Layout Audio (L-PCM 3D Audio Extension Type Code 13) (Continued)

Figure 2-27 illustrates the Audio_Stream SDP mapping over the Main-Link for DST audio. Figure 2-34 illustrates the mapping within each of the eight sub-layouts of the DST Audio_Stream SDP.

Those sets of 32-bit audio packet payloads that carry the same audio sample shall have the same value in the SP (Sample Present) bit. If the sample is present, SP shall be set to 1. If the sample is absent, SP shall be cleared to 0.

An Audio_Stream SDP transfer shall not stop in the middle of an audio sample, and shall be zero-padded, if necessary, so that it meets the minimum 16-byte payload size. For designs that support Split SDP transactions, an Audio_Stream SDP may be temporarily interrupted, if needed, at the end of a horizontal blanking period and resume at the start of the next horizontal blanking period. (See Section 2.2.5.13 for details.)

For example, when 2-channel audio is transmitted over a 1-lane Main-Link, the packet may be ended after PB7 in Figure 2-23 because the transmission of Sample 0 is complete at that point. However, the packet shall **not** end after PB6. Furthermore, the packet shall **not** end after PB5 because the packet would not meet the minimum 16-byte payload size. If only S0 is available for transmission, 0s shall be transmitted in the S1 location.

Audio high bit rate transmission shall always use the 8-channel layout to transmit the content. Pa/Pb sync words shall be located only on the Channel 1 and Channel 2 locations in the 8-channel layout, this Pa/Pb sync word location restriction applies to only Dolby TrueHD and DTS-HD Master Audio transmission. The Pa/Pb sync word is a specific embedded code that is required by the *IEC 61937* bitstream.

The mapping of audio data to channels depends on the audio-data-to-speaker mapping.

4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 0
SS	SS	SS	SS	SS	SS	SS
HB0	HB1	HB2	HB3	HB0	HB1	HB0
PB0	PB1	PB2	PB3	PB0	PB1	PB0
S0_SL1_B0	S0_SL2_B0	S0_SL3_B0	S0_SL4_B0	HB2	HB3	HB1
S0_SL1_B1	S0_SL2_B1	S0_SL3_B1	S0_SL4_B1	PB2	PB3	PB1
S0_SL1_B2	S0_SL2_B2	S0_SL3_B2	S0_SL4_B2	S0_SL1_B0	S0_SL2_B0	HB2
S0_SL1_B3	S0_SL2_B3	S0_SL3_B3	S0_SL4_B3	S0_SL1_B1	S0_SL2_B1	PB2
PB4	PB5	PB6	PB7	S0_SL1_B2	S0_SL2_B2	HB3
S0_SL5_B0	S0_SL6_B0	S0_SL7_B0	S0_SL8_B0	S0_SL1_B3	S0_SL2_B3	PB3
S0_SL5_B1	S0_SL6_B1	S0_SL7_B1	S0_SL8_B1	PB4	PB5	S0_SL1_B0
S0_SL5_B2	S0_SL6_B2	S0_SL7_B2	S0_SL8_B2	S0_SL3_B0	S0_SL4_B0	S0_SL1_B1
S0_SL5_B3	S0_SL6_B3	S0_SL7_B3	S0_SL8_B3	S0_SL3_B1	S0_SL4_B1	S0_SL1_B2
PB8	PB9	PB10	PB11	S0_SL3_B2	S0_SL4_B2	S0_SL1_B3
SE	SE	SE	SE	S0_SL3_B3	S0_SL4_B3	PB4
				PB6	PB7	S0_SL2_B0
				S0_SL5_B0	S0_SL6_B0	S0_SL2_B1
				S0_SL5_B1	S0_SL6_B1	S0_SL2_B2
				S0_SL5_B2	S0_SL6_B2	S0_SL2_B3
				S0_SL5_B3	S0_SL6_B3	PB5
				PB8	PB9	S0_SL3_B0
				S0_SL7_B0	S0_SL8_B0	S0_SL3_B1
				S0_SL7_B1	S0_SL8_B1	S0_SL3_B2
				S0_SL7_B2	S0_SL8_B2	S0_SL3_B3
				S0_SL7_B3	S0_SL8_B3	PB6
				PB10	PB11	S0_SL4_B0
				SE	SE	S0_SL4_B1
						S0_SL4_B2
						S0_SL4_B3
						PB7
						S0_SL5_B0
						S0_SL5_B1
						S0_SL5_B2
						S0_SL5_B3
						PB8
						…
						S0_SL8_B0
						S0_SL8_B1
						S0_SL8_B2
						S0_SL8_B3
						PB11
						SE

where:

- S = Sample
- B = Byte
- SL = Sub-layout

For example, “S0_SL1_B0” refers to Byte 0 of Sub-layout 1 of Sample 0.

Figure 2-27: Audio_Stream SDP over Main-Link for DST Audio Layout

2.2.5.2.4 Speaker Mapping

Entire section rewritten for *DP v1.4*.

Audio INFOFRAME Byte 4, as defined in *CTA-861-G*, *Section 6.6.2*, contains information that describes the mapping of speaker locations into the audio transport channels. This 8-bit Channel Allocation field, CA 7:0, applies to 3- to 8-channel uncompressed audio. The speaker location mapping of the 3- to 8-channel L-PCM Audio or 3- to 8-channel One Bit audio data transported shall match the 8-bit data (CA7:0) that is transported within the Audio INFOFRAME.

A Sink device can indicate the active speaker configuration through the use of the Speaker Allocation Data Block as described in *CTA-861-G*, *Section 7.5.3*. Sink devices that support 3- to 8-channel L-PCM Audio or 3- to 8-channel One Bit audio shall include this data block.

A Sink device that supports Object-Based Audio or High Channel-Count Audio shall use the Room Configuration Descriptor Data Block as described in *CTA-861-G*, *Table 94*, instead of the Speaker Allocation information. In addition, the Sink device may choose to provide additional information and include Speaker Location Descriptors, as described in *CTA-861-G*, *Table 93*.

A Source device that needs to transport L-PCM 3D Audio shall use either the *Delivery According to the Speaker Mask* or *Delivery by Channel Index* method, as described in *CTA-861-G*, *Section6.6.3* and *Section 6.6.4*, respectively. Similar to the 2- or 8-channel layout, all SP bits of the 16- or 32-channel L-PCM 3D Audio layout shall carry the same value:

- All asserted if the sample is present, –or–
- All de-asserted if the sample is ***not*** present

Active L-PCM 3D Audio channel ordering within the 32-channel layout shall follow the rules as described in *CTA-861-G*, *Section 6.6.3*, when the Source device uses the *Delivery According to the Speaker Mask* method, –or– the rules as described in *CTA-861-G*, *Section 6.6.4*, when the Source device uses the *Delivery by Channel Index* method. The 16-channel layout may be used when 16 or fewer active channels are needed.

Figure 2-28 through Figure 2-31 describe the channel ordering within the L-PCM 3D Audio 16- or 32-channel layout for examples of fully or partially populated L-PCM 3D Audio systems.

Note: *See CTA-861-G for definitions of RCD and SPM.*

Channel Number															
16	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
–	–	–	–	–	–	FRC	FLC	–	BC	BR	BL	FC	LFE1	FR	FL

Figure 2-28: L-PCM 3D Audio Data Allocation with Audio INFOFRAME Byte 4 = FEh, 8.1 SPM Asserted (Informative)

Channel Number															
16	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
–	–	–	–	–	–	–	FRC	FLC	BC	BR	BL	FC	LFE1	FR	FL

Figure 2-29: L-PCM 3D Audio Data Allocation with Audio INFOFRAME Byte 4 = FFh, 8.1 SPM Asserted, RCD Order Used (Informative)

Channel Number															
16	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
LFE2	TpFC	TpFR	TpFL	FRW	FLW	FRC	FLC	TpC	BC	BR	BL	FC	LFE1	FR	FL
Channel Number															
32	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**
–	–	TpRS	TpLS	BtFR	BtFL	TpBR	TpBL	TpSiR	TpSiL	SiR	SiL	BtFC	TpBC	RS	LS

Figure 2-30: L-PCM 3D Audio Data Allocation with Audio INFOFRAME Byte 4 = FEh, All SPM Asserted (Informative)

Channel Number															
16	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
LS	TpFC	TpC	TpFR	TpFL	FRW	FLW	FRC	FLC	BC	BR	BL	FC	LFE1	FR	FL
Channel Number															
32	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**
–	–	TpRS	TpLS	BtFR	BtFL	BtFC	TpBR	TpBL	TpSiR	TpSiL	SiR	SiL	TpBC	LFE2	RS

Figure 2-31: L-PCM 3D Audio Data Allocation with Audio INFOFRAME Byte 4 = FFh, All SPM Asserted, RCD Order Used (Informative)

2.2.5.2.5 Data Mapping within Audio_Stream SDP Payload

Entire section rewritten for *DP v1.4*.

An Audio_Stream SDP payload consists of four bytes of data per lane, with each set of four bytes protected by a parity byte.

Figure 2-32 illustrates the data mapping within the 4-byte payload of an Audio_Stream SDP that contains data with *IEC 60958*-encoding or *IEC 61937* transport. In these cases, the audio payload would use the 2- or 8-channel layout with L-PCM Audio or *IEC 61937*-compressed audio, as well as the 16- or 32-channel layout with L-PCM 3D Audio. In Figure 2-23 and Figure 2-24, these four bytes correspond to, for example, S0_Ch1_B0, S0_Ch1_B1, S0_Ch1_B2, and S0_Ch1_B3. (See Figure 2-23 through Figure 2-26 for the 4-byte payload mapping of the L-PCM Audio, *IEC 61937*-encoded audio, or L-PCM 3D Audio within the Audio_Stream SDP over the Main-Link.)

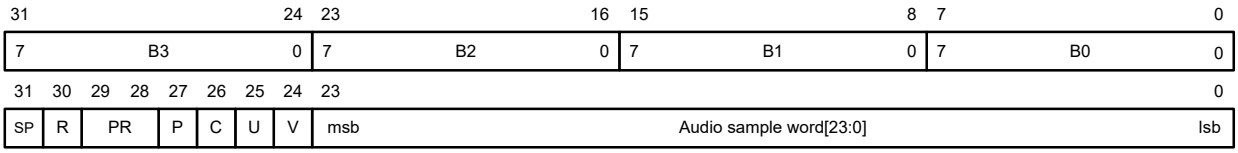


Figure 2-32: Data Mapping within the 4-byte Payload of an Audio_Stream SDP with *IEC 60958*-like Coding

Figure 2-33 illustrates the data mapping within the 4-byte payload of a One Bit Audio_Stream SDP. Pack the 28-bit payload layout from MSB to LSB order, as follows:

- Pack the first sampled or oldest One Bit audio sample in the MSB position, Byte 3 (bit 3) or bit 27 position of the 32-bit layout
- Pack the latest sampled or newest One Bit audio sample in the LSB position, Byte 0 (bit 0) or bit 0 position of the 32-bit layout

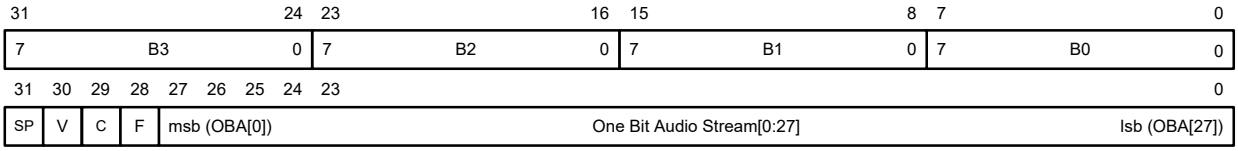


Figure 2-33: Data Mapping within the 4-byte Payload of an Audio_Stream SDP with One Bit Audio Coding

Figure 2-34 illustrates the data mapping within each of the eight 4-byte sub-layout payloads of a DST Audio_Stream SDP. Pack the 224-bit payload layout from LSB to MSB, in each of eight 28-bit sub-layout sections, as follows:

- Pack the first bit of the DST stream in Sub-layout 1, bit 0
- Pack the 224th bit of the DST stream in Sub-layout 8, bit 27; continue this packing order for all subsequent DST layouts

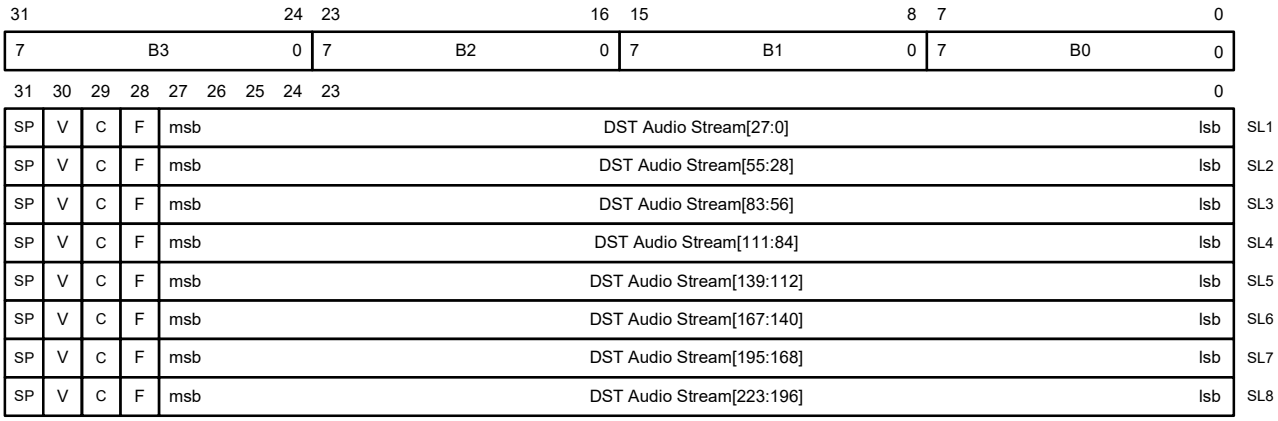


Figure 2-34: Data Mapping within the 4-Byte Payload Sub-layout of a DST Audio_Stream SDP with DST Audio Coding

Table 2-108 describes the bit definition of the 4-byte Audio_Stream SDP payload illustrated in Figure 2-32. Table 2-109 describes the bit definitions of an Audio_Stream SDP Payload with One Bit Audio Coding. Table 2-110 describes the bit definitions of an Audio_Stream SDP Payload with DST Audio Coding.

Table 2-108: Audio_Stream SDP Payload with *IEC 60958*-like Coding Bit Definitions

Bit Name	Byte #	Bit #	Description
Audio sample word	0	7:0	**Audio Data** Content of this data depends on the audio coding type. For L-PCM Audio, the most significant bit of the audio is placed in Byte 2, bit 7. If the audio data size is less than 24 bits, unused least significant bits shall be zero-padded.
	1	7:0	
	2	7:0	
V	3	0	**Validity Flag**
U		1	**User Bit**
C		2	**Channel Status**
P		3	**Parity Bit**
PR		5:4	**Preamble Code and its Correspondence with *IEC 60958* Preamble** 00b = Sub-frame 1 and start of the audio block (11101000b preamble). 01b = Sub-frame 1 (1110010b preamble). 10b = Sub-frame 2 (1110100b preamble). 11b = RESERVED.
R		6	**RESERVED** Shall be 0.
SP		7	**Sample Present Bit** 0 = Sample information is not present. 1 = Sample information is present and can be processed. All channels of one audio sample, whether used or unused, shall have the same state for this flag. Useful when 2-channel audio is transported over a 4-lane Main-Link. In this operation, Main-Link Lanes 2 and 3 may or may not have the audio sample data. Indicates whether the audio sample is present.

Table 2-109: Audio_Stream SDP Payload with One Bit Audio Coding Bit Definitions

Bit Name	Byte #	Bit #	Description
Audio sample bitstream	0	7:0	**Audio Data Stream** One Bit audio data consists of a single bit per sample. Each SDP payload layout consists of a 28-bit portion of a continuous stream of 1-bit consecutive samples belonging to the given audio channel. The first sampled bit of the 28-bit portion is placed in Byte 0, bit 0. The last sampled bit of the 28-bit portion is placed in Byte 3, bit 3.
	1	7:0	
	2	7:0	
	3	3:0	
F	3	4	**Frame Start Flag** Valid only when the matching Sample Present Bit is set to 1. All channels layouts of the One Bit audio sample shall have the same state for this flag. 0 = Setting for all but the first One Bit SDP payload layout in a series of layouts comprising the One Bit audio frame. 1 = Indicates the first One Bit SDP payload layout in a series of layouts comprising the One Bit audio frame.
C		5	**Channel Status** Valid only when the matching Sample Present Bit is set to 1. All channel layouts of the One Bit audio sample shall have the same state for this flag. C(0:NLPF – 33) = 0 as RESERVED. C(NLPF – 32:NLPF – 2) = GTC(31:1). C(NLPF – 1) = GTC Field Validity. If GTC Field Validity is 0, the Sink device should ignore the GTC. These bits carry channel status, assembled from One Bit Layout Sample 0 to One Bit Layout Sample NLPF – 1, one bit/layout. One Bit Layout Sample 0 is marked with the Frame Start Flag bit set to 1. ***Note:*** • *NLPF = Number of One Bit audio layouts/frame* • *GTC = Global Time Code presentation time*
V		6	**Valid Flag** Valid only when the matching Sample Present Bit is set to 1. 0 = Sample information is not valid. 1 = Sample information is valid and can be processed.
SP		7	**Sample Present Bit** 0 = Sample information is not present. 1 = Sample information is present and can be processed. All channels of one audio sample, whether used or unused, shall have the same state for this flag. Useful when 2-channel audio is transported over a 4-lane Main-Link. In this operation, Main-Link Lanes 2 and 3 may or may not have the audio sample data. Indicates whether the audio sample is present.

Table 2-110: Audio_Stream SDP Payload with DST Audio Coding Bit Definitions

Bit Name	Byte #	Bit #	Description
Audio sample bitstream	0	7:0	**Audio Data Stream** DST audio data consists of a stream of compressed One Bit audio data. Each of the eight 4-byte sub-layouts of the DST SDP payload layout consists of a 28-bit portion of a continuous stream of the compressed audio data. The first sampled bit of the 28-bit portion is placed in Byte 0, bit 0. The last sampled bit of the 28-bit portion is placed in Byte 3, bit 3. The DST data bitstream is loaded into the eight payload sub-layouts in ascending payload layout order, Sub-layouts 1 to 8.
	1	7:0	
	2	7:0	
	3	3:0	
F	3	4	**Frame Start Flag** Valid only when the matching Sample Present Bit is set to 1. All eight 4-byte sub-layouts of the DST layout shall have the same state for this flag. 0 = Setting for all but the first DST SDP payload layout in a series of layouts comprising the DST audio frame. 1 = Indicates the first DST SDP payload layout in a series of layouts comprising the DST audio frame.
C		5	**Channel Status** Valid only when the matching Sample Present Bit is set to 1. All eight sub-layouts of the DST layout shall have the same state for this flag. C(0:NLPF – 33) = 0 as RESERVED. C(NLPF – 32:NLPF – 2) = GTC(31:1). C(NLPF – 1) = GTC Field Validity. If GTC Field Validity is 0, the Sink device should ignore the GTC. These bits carry channel status, assembled from DST Layout Sample 0 to DST Layout Sample NLPF – 1, one bit/DST layout. DST Layout Sample 0 is marked with the Frame Start Flag bit set to 1. ***Note:*** • *NLPF = Number of DST layouts/frame* • *GTC = Global Time Code presentation time*
V		6	**Valid Flag** Valid only when the matching Sample Present Bit is set to 1. All eight sub-layouts of the DST layout shall have the same state for this flag. 0 = Sample information is not valid. 1 = Sample information is valid and can be processed.
SP		7	**Sample Present Bit** 0 = Sample information is not present. 1 = Sample information is present and can be processed. All eight sub-layouts of the DST layout shall have the same state for this flag. Can be used to mark non-active DST layouts in long packet sequences.

2.2.5.2.6 Audio_Stream SDP Transport Capacity and Video Dependency

New to *DP v1.4*. Updated in *DP v2.0*.

DP v1.4 (and higher) supports concurrent audio stream and video stream transport over a link.

Audio_Stream SDPs shall be transmitted during the main video stream's HBlank and VBlank periods. Audio bandwidth needs can be expressed in terms of the audio sample rate and main video line rate that shall be supported, as follows:

$$AudioSamplesReqPerLine = AudioFs / VideoHFreq$$

where:

- *AudioFs* = Audio sample frequency needed, as listed in Table 2-100
- *VideoHFreq* = Main video stream's horizontal line frequency

During the VBlank period, Audio_Stream SDPs can appear at any time during the entire line period. The bandwidth consumed by the other SDPs that could occupy the VBlank period does **not** practically constrain the audio samples/line mandate within that period.

However, the HBlank period's available capacity shall determine whether the audio bandwidth needs can be met. Besides the Audio_Stream SDP, the VSC_EXT SDP may occupy the HBlank region of the video vertical active period. It is the responsibility of a DP Source device that sources both SDPs and the main video stream to determine whether a particular audio mode can be supported.

The number of symbols available for the Audio_Stream SDP during the HBlank period depends on the main video stream timing and Main-Link configuration, specifically the Link Symbol Clock Frequency and Lane Count. The number of Audio_Stream SDP symbols needed per line and HBlank is determined by the Audio Coding Type and related layouts/sample and symbols/layout.

2.2.5.2.6.1 Audio Stream SDP Concatenation and Splitting Requirements (Normative)

Concatenating the audio layouts within a single SDP increases efficiency by reducing the overhead for SDP header and SE footer symbols. Therefore, a DPTX may concatenate multiple sets of minimum SDP payloads to form a long packet.

Support for concatenated audio streams is mandatory for a DPRX, for all audio formats.

Splitting the SDP across more than one line and HBlank period increases efficiency by avoiding the mandate of rounding up to the next integer number of layouts/line. Therefore, a DPTX may split an SDP across more than one line and HBlank period.

Support of SDP splitting is mandatory for a DPRX, both in a single-stream transport and in a multi-stream transport. A DPRX shall set the SST_SPLIT_SDP_CAP bit in the DPRX_FEATURE_ENUMERATION_LIST register (DPCD Address 02210h, bit 1) to 1.

2.2.5.2.6.2 Audio Stream SDP Transport Feasibility for a Given Video Stream (Informative)

However, even with these efficiency measures, there may be some main video stream mode and audio mode combinations that shall have a restricted maximum audio sample rate. This maximum audio sample rate may be determined by comparing the available HBlank period symbol capacity against the audio SDP symbol count that is needed for each sample frequency. Video modes that reduce link rates that use options such as reduced blanking timing and/or HBlank Expansion should be analyzed for any audio mode restrictions.

The number of symbols available for an Audio_Stream SDP during the HBlank period shall be as follows:

$$StrmSymbolCntAvailPerHBlank = FLOOR(t\_HBlank \times LSClkFreq \times LaneCnt - MainLinkOverhead)$$

where:

- *t_HBlank* = Main video stream HBlank period
- *LSClkFreq* = Link Symbol Clock frequency
- *LaneCnt* = Main-Link's lane count
- *MainLinkOverhead* = Symbol count needed on the Main-Link at the beginning and end of the HBlank period, and is defined as follows:

  $$MainLinkOverhead = BSSymbolCnt + VBIDSymbolCnt + MvidSymbolCnt + MaudSymbolCnt + BESymbolCnt$$

  where:

  - *BSSymbolCnt* = *LaneCnt* × 4, the number of Blanking Start (BS) symbols; Enhanced Framing mode provides the worst case number
  - *VBIDSymbolCnt* = 4, the number of VB-ID symbols
  - *MvidSymbolCnt* = 4, the number of Mvid symbols
  - *MaudSymbolCnt* = 4, the number of Maud symbols
  - *BESymbolCnt* = *LaneCnt*, the number of Blanking End (BE) symbols

  Using the above definitions, the Main-Link overhead can be simplified as follows:

  $$MainLinkOverhead = LaneCnt \times 5 + 12$$

The number of symbols needed for an Audio_Stream SDP during the HBlank period shall be as follows:

$$AudioSymbolCntReqPerHBlank = \texttt{CEIL((AudioSamplesReqPerLine} \times \texttt{AudioLayoutsPerSample} \times \texttt{AudioSymbolsPerLayout +} \texttt{CEIL(AudioSamplesReqPerLine} \times \texttt{AudioLayoutsPerSample /} \texttt{MaxLayoutsPerAudioSDP)} \times \texttt{AudioSDPOverhead)} \times \texttt{AudioSDPMargin)}$$

where:

- *AudioSamplesReqPerLine* = Number of audio samples that shall be transmitted over DP per a main video stream line period is roughly constant for the given video format
- *AudioLayoutsPerSample* = Number of audio layouts needed per audio sample for the given audio mode (see Table 2-111)
- *AudioSymbolsPerLayout* = Number of symbols needed per audio layout for the given audio mode (see Table 2-111)
- *MaxLayoutsPerAudioSDP* = Maximum number of audio layouts that can be assembled into a single Audio_Stream SDP (see Table 2-111)

- *AudioSDPMargin* is an implementation-specific safety margin that is used to prevent possible audio sample under-run; values of 1.05 to 1.1 should be used
- *AudioSDPOverhead* is the symbol count needed at the beginning and end of the Audio_Stream SDP, and is defined as follows:

  AudioSDPOverhead = SSSymbolCnt + HeaderSymbolCnt + HeaderParitySymbolCnt + SESymbolCnt

where:

- *SSSymbolCnt* = *LaneCnt*, the number of Audio_Stream SDP Start symbols
- *HeaderSymbolCnt* = 4, the number of Audio_Stream SDP Header symbols
- *HeaderParitySymbolCnt* = 4, the number of Audio_Stream SDP Header Parity symbols
- *SESymbolCnt* = *LaneCnt*, the number of Audio_Stream SDP End symbols

Using the above definitions, the Audio_Stream SDP overhead can be simplified as follows:

AudioSDPOverhead = LaneCnt × 2 + 8

Table 2-111 summarizes the supported audio mode conversion details:

- Samples to layouts
- Layouts to symbols
- Maximum layouts allowed within a single Audio_Stream SDP

Table 2-111: Audio_Stream SDP Coding Type Payload Capacity Summary (Informative)

Audio Coding Type	AudioLayoutsPerSample	AudioSymbolsPerLayout	MaxLayoutsPerAudioSDP
2-channel L-PCM Audio	1/2	20	16
8-channel L-PCM Audio	1	40	32
16-channel L-PCM 3D Audio	1	80	32
32-channel L-PCM 3D Audio	1	160	32
2-channel One Bit	1/56	20	16
8-channel One Bit	1/28	40	32
DST	1/224	40	32
HBR	1/4	40	32

Main video mode and audio combinations that meet the following mandates can be supported as follows:

$$AudioSymbolCntReqPerHBlank < StrmSymbolCntAvailPerHBlank$$

Consider the limitations of 32-channel L-PCM 3D Audio audio support on the 4096x2160p60 video mode with *CVT Standard* Reduced Blanking Timing v2, DMT ID = 57h. The relevant details of this video mode with two Main-Link configurations are as follows:

- Horizontal Line Frequency = *VideoHFreq* = 133.32kHz
- Horizontal Blanking Period = *t_HBlank* = 0.1436925us
- Details for 4-lane at 540MHz Link Symbol clock frequency, 24bpp RGB:

$$StrmSymbolCntAvailPerHBlank = FLOOR(t\_HBlank \times LSClkFreq \times LaneCnt - MainLinkOverhead) = FLOOR(0.1436925us \times 540MHz \times 4 - (4 \times 5 + 12)) = 278\ symbols$$

- Details for 4-lane at 270MHz Link Symbol clock frequency, 12bpp 4:2:0 YCbCr:

$$StrmSymbolCntAvailPerHBlank = FLOOR(t\_HBlank \times LSClkFreq \times LaneCnt - MainLinkOverhead) = FLOOR(0.1436925us \times 270MHz \times 4 - (4 \times 5 + 12)) = 123\ symbols$$

Table 2-112 lists relevant details for the 32-channel L-PCM 3D Audio audio support needed for the seven available sample frequencies. A 110% margin was used for *AudioSDPMargin*.

Table 2-112: 32-channel L-PCM 3D Audio Mandates on DMT ID = 57h Mode (Informative)

AudioFs	**Audio Sample Frequencies**						
	32kHz	**44.1kHz**	**48kHz**	**88.2kHz**	**96kHz**	**176.4kHz**	**192kHz**
AudioSamplesReqPerLine	0.24	0.33	0.36	0.66	0.72	1.32	1.44
AudioSymbolCntReqPerHBlank	60	76	81	135	145	251	272

Considering that 278 symbols should be available during the horizontal blanking period that uses the 4-Lane 540MHz configuration, all Audio sample frequencies up to 192kHz should be supported. However, with only 123 symbols available in the 4-Lane 270MHz configuration, only 32, 44.1, and 48kHz 32-channel audio sample rates can be supported because there is insufficient HBlank capacity to support 88.2, 96, 176.4, and 192kHz audio sample frequencies in this configuration.

2.2.5.2.7 Transport of Audio Packets without Main Video Stream

This Standard supports the transport of audio stream while no video stream is being transported over the link.

When the link is active without a main video stream, a Source device shall insert a BS symbol followed by VB-ID, Mvid[7:0], and Maud[7:0], referred to as "BS symbol set," every 2^{13}, or 8192 link symbols.

Both the NoVideoStream_Flag and VerticalBlanking_Flag bits in the VB-ID (bits 3 and 0, respectively) shall be set to 1 in this condition and Mvid[7:0] is cleared to 00h.

A Source device shall transmit an Audio_Stream SDP after each BS symbol set. In addition, a Source device shall insert an Audio INFOFRAME (non-Basic Audio) SDP and Audio_TimeStamp SDP once after every 512th BS symbol set.

2.2.5.3 Extension SDP

Extension SDP transport is an application- or vendor-specific option. A DP Source device shall write its 24-bit IEEE_OUI registers (DPCD Addresses 00300h through 00302h) and additional data, as needed, by way of AUX transactions. Then, it shall read the Sink device's 24-bit IEEE_OUI registers (DPCD Addresses 00400h through 00402h) and additional data, as needed, by way of the AUX_CH. The 24-bit ID shall be supported. If the downstream device is a Branch device, the IEEE_OUI registers are located at DPCD Addresses 00500h through 00502h.

Extension SDP shall be used only after a DP Source and Sink device have both confirmed that they support the vendor-specific Extension SDP usage.

A Branch device shall forward the AUX_CH write or read request transactions for the 24-bit IEEE OUI to its downstream device.

Figure 2-35 illustrates the minimum size of an Extension SDP mapped onto the Main-Link. The DP Source device shall generate parity bytes for both the header and data. The DP Sink device's use of parity for error checking and correction is an implementation-specific option.

4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 0
SS	SS	SS	SS	SS	SS	SS
HB0	HB1	HB2	HB3	HB0	HB1	HB0
PB0	PB1	PB2	PB3	PB0	PB1	PB0
DB0	DB4	DB8	DB12	HB2	HB3	HB1
DB1	DB5	DB9	DB13	PB2	PB3	PB1
DB2	DB6	DB10	DB14	DB0	DB4	HB2
DB3	DB7	DB11	DB15	DB1	DB5	PB2
PB4	PB5	PB6	PB7	DB2	DB6	HB3
SE	SE	SE	SE	DB3	DB7	PB3
				PB4	PB5	DB0
				DB8	DB12	DB1
				DB9	DB13	DB2
				DB10	DB14	DB3
				DB11	DB15	PB4
				PB6	PB7	DB4
				SE	SE	DB5
						DB6
						DB7
						PB5
						…
						DB12
						DB13
						DB14
						DB15
						PB7
						SE

Figure 2-35: Extension SDP Mapping over Main-Link

2.2.5.3.1 Extension SDP Header

Table 2-113 summarizes the Extension SDP header bytes.

Table 2-113: Extension SDP Header Bytes

Byte#	Content
HB0	Use of this byte is vendor-specific.
HB1	**Secondary-data Packet Type** 04h.
HB2	Use of this byte is vendor-specific.
HB3	Use of this byte is vendor-specific.

2.2.5.4 Audio_CopyManagement SDP

Transport of an Audio_CopyManagement SDP is an application-specific option. When an audio stream is transported and has a specific copy management mandate from the higher level application, the Audio_CopyManagement SDP describing the copy management attribute of the audio stream shall also be transported. For general audio streams that do not have a copy management mandate, Audio_CopyManagement SDP transmission is **optional** (with HB3 Copy Management Type field (bits 7:2) cleared to 00h if transmitted).

A DP Sink device may indicate that it does **not** support ACM or ISRC by clearing the ACM_ISRC_sup bit in its capability declaration. In this case, the DP Source device shall not transmit any Audio_CopyManagement SDPs to the DP Sink device (on top of not transmitting any audio stream with copy management mandate to the Sink device). If the DP Sink device supports ACM, and does not see the Audio_CopyManagement SDP within two video frames after an audio stream is transported, the device shall treat the transported audio stream as if the stream does not have a copy management mandate.

A DP Source device shall support Audio_CopyManagement SDP transmission if enabled by a higher-level application (unless the Sink device does not support ACM/ISRC).

When a new audio stream with a copy management mandate is transported, –or– there is a change in the audio stream copy management mandates, an Audio_CopyManagement SDP with up-to-date information shall be transmitted within one frame of the affected audio stream's start of transmission. The packet shall continue to be transmitted once per frame, for as long as the copy management mandate persists.

2.2.5.4.1 Audio_CopyManagement SDP Header

Table 2-114 describes the Audio_CopyManagement SDP header bytes.

Table 2-114: Audio_CopyManagement SDP Header Bytes

Byte #	Bit #	Content
HB0	7:0	**Secondary-data Packet ID** INFOFRAME SDP, Audio_TimeStamp SDP, Audio_Stream SDP, Audio_CopyManagement SDP, and ISRC SDP shall have the same Packet ID when they are associated with the same audio stream.
HB1	7:0	**Secondary-data Packet Type** 05h.
HB2	7:0	**Least Significant Eight Bits of (Data Byte Count – 1)** 0Fh (i.e., Data Byte Count = 16 bytes). Unused bytes shall be zero-padded.
HB3	1:0	**Most Significant Two Bits of (Data Byte Count – 1)**
	7:2	**Copy Management Type** Indicates the type of copy management associated with the audio stream. 00h = No Copy Management mandate is indicated by the higher-level application, Equivalent to no transmission of the Audio_CopyManagement SDP. 01h = *IEC 60958* Audio. Copy management is needed through *IEC 60958* Serial Copy Management System (SCMS) control bits, which are embedded in the audio stream channel status. 02h = DVD Audio. DVD audio copy management is needed. See *DVD-Audio Book v1.2*$_1$*p4* for details regarding the data payload's copy control attributes. All other values are RESERVED.

2.2.5.4.2 Audio_CopyManagement SDP Data

The Audio_CopyManagement SDP's data payload depends on the HB3 Copy Management Type field (bits 7:2) value:

- Copy Management Type = No Copy Management – No valid data. All 16 bytes are 0s.
- Copy Management Type = *IEC 60958* Audio – No valid data. All 16 bytes are 0s.
- Copy Management Type = DVD Audio – One byte of data content exists, with the remaining 15 bytes padded with 0s. See *DVD-Audio Book v1.2*$_1$*p4* for details regarding the data payload's copy control attributes.
    - Bit 1:0 – Audio quality
    - Bit 3:2 – Audio copy permission
    - Bit 6:4 – Audio copy number
    - Bit 7 – Audio transaction

Figure 2-36 illustrates the payload size equal to 16 bytes. It is allowed to have the payload size equal to 32 bytes, with unused bytes zero-padded.

4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 0
SS	SS	SS	SS	SS	SS	SS
HB0	HB1	HB2	HB3	HB0	HB1	HB0
PB0	PB1	PB2	PB3	PB0	PB1	PB0
DB0	DB4	DB8	DB12	HB2	HB3	HB1
DB1	DB5	DB9	DB13	PB2	PB3	PB1
DB2	DB6	DB10	DB14	DB0	DB4	HB2
DB3	DB7	DB11	DB15	DB1	DB5	PB2
PB4	PB5	PB6	PB7	DB2	DB6	HB3
SE	SE	SE	SE	DB3	DB7	PB3
				PB4	PB5	DB0
				DB8	DB12	DB1
				DB9	DB13	DB2
				DB10	DB14	DB3
				DB11	DB15	PB4
				PB6	PB7	DB4
				SE	SE	DB5
						DB6
						DB7
						PB5
						DB8
						DB9
						DB10
						DB11
						PB6
						DB12
						DB13
						DB14
						DB15
						PB7
						SE

Figure 2-36: Audio_CopyManagement SDP Mapping over Main-Link

2.2.5.5 ISRC SDP

Transport of an International Standard Recording Code (ISRC) SDP is an application-specific option. When an audio stream is transported and the stream has a specific ISRC and/or UPC/EAN mandate from the higher level application, the ISRC SDP describing the audio stream's UPC_EAN_ISRC information shall also be transported. For a general audio stream that does not have an ISRC or UPC/EAN mandate, an ISRC SDP shall **not** be transmitted.

A DP Sink device may indicate it does not support ACM or ISRC by clearing the ACM_ISRC_sup bit in its capability declaration. In this case, the DP Source device shall not transmit an ISRC SDP to the Sink device (in addition to not transmitting an audio stream with an ISRC mandate to the Sink device). If the DP Sink device supports ISRC, and does not see the ISRC SDP within two frames after an audio stream is transported, the device shall treat the transported audio stream as if the stream does not have an ISRC mandate.

A DP Source device shall support ISRC SDP transmission if enabled by a higher-level application (unless the Sink device does not support ACM/ISRC). When an audio track with ISRC information is transported, the ISRC SDP shall be transmitted multiple times (see the HB3 ISRC Status field (bits 7:5) description for further details) following the transmission of the affected audio track. If transported, ISRC SDPs shall be transmitted during the main video stream's horizontal and vertical blanking periods.

See *DVD-Audio Book v1.2*$_1$*p4* for details regarding the UPC_EAN_ISRC fields.

2.2.5.5.1 ISRC SDP Header

Table 2-115 describes the ISRC SDP header bytes.

Table 2-115: ISRC SDP Header Bytes

Byte #	Bit #	Content
HB0	7:0	**Secondary-data Packet ID** INFOFRAME SDP, Audio_TimeStamp SDP, Audio_Stream SDP, Audio_CopyManagement SDP, and ISRC SDP shall have the same Packet ID when they are associated with the same audio stream.
HB1	7:0	**Secondary-data Packet Type** 06h.
HB2	7:0	**Least Significant Eight bits of (Data Byte Count – 1)** 0Fh (i.e., Data Byte Count = 16 bytes).

Table 2-115: ISRC SDP Header Bytes (Continued)

Byte #	Bit #	Content
HB3	1:0	**Most Significant Two Bits of (Data Byte Count – 1)**
	2	**ISRC Type** Indicates whether the ISRC information is delivered in a single ISRC SDP or two ISRC SDPs. A complete set of UPC_EAN_ISRC information can be transmitted in one or two ISRC SDPs. 0 = UPC_EAN_ISRC information has only 16 bytes; therefore, only a single SDP is transmitted. 1 = UPC_EAN_ISRC information has the full 32 bytes; therefore, two ISRC SDPs shall be transmitted. ***Note:*** *SDP size limitation was kept mainly to ease DP-to-HDMI protocol converter device implementation.*
	3	**ISRC SDP #** Indicates the packet number if the ISRC information is to be transmitted in two ISRC SDPs (i.e., bit 2 (ISRC Type bit) is set to 1). Always cleared to 0 if the ISRC Type bit is cleared to 0. 0 = ISRC SDP contains the first 16 bytes (Bytes 15:0) of UPC_EAN_ISRC information. 1 = ISRC SDP contains the second 16 bytes (Bytes 31:16) of UPC_EAN_ISRC information.
	4	**ISRC Valid** Indicates the UPC_EAN_ISRC information contained within the ISRC SDP is valid. 0 = Source device cannot obtain the complete UPC_EAN_ISRC information. 1 = ISRC information is complete and valid.
	7:5	**ISRC Status** Indicates ISRC information status in reference to an audio track position. Each audio track may have the specific ISRC and/or UPC/EAN information. Per *DVD-Audio Book v1.2*$_{1}$*p4*, if UPC_EAN_ISRC information exists, the DP Source device shall transmit the set of ISRC SDPs multiple times per audio track: • At least two complete sets of ISRC SDPs with the ISRC Status of 000b at the beginning of the audio track • Multiple complete set of ISRC SDPs with the ISRC Status of 010b in the middle of the audio track • At least two complete sets of ISRC SDPs with the ISRC Status of 100b before the end of the audio track

2.2.5.5.2 ISRC SDP Data

The ISRC SDP data payload depends on the HB3 ISRC Type bit (bit 2):

- If the HB3 ISRC SDP # bit (bit 3) of an ISRC SDP is cleared to 0, the data payload contains bytes 15:0 of the UPC_EAN_ISRC information.
- If the HB3 ISRC SDP # bit of an ISRC SDP is set to 1, the data payload contains bytes 31:0 of the UPC_EAN_ISRC information.

Figure 2-37 illustrates the payload size equal to 16 bytes. It is allowed to have the payload size equal to 32 bytes, with unused bytes zero-padded.

4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 0
SS	SS	SS	SS	SS	SS	SS
HB0	HB1	HB2	HB3	HB0	HB1	HB0
PB0	PB1	PB2	PB3	PB0	PB1	PB0
DB0	DB4	DB8	DB12	HB2	HB3	HB1
DB1	DB5	DB9	DB13	PB2	PB3	PB1
DB2	DB6	DB10	DB14	DB0	DB4	HB2
DB3	DB7	DB11	DB15	DB1	DB5	PB2
PB4	PB5	PB6	PB7	DB2	DB6	HB3
SE	SE	SE	SE	DB3	DB7	PB3
				PB4	PB5	DB0
				DB8	DB12	DB1
				DB9	DB13	DB2
				DB10	DB14	DB3
				DB11	DB15	PB4
				PB6	PB7	DB4
				SE	SE	DB5
						DB6
						DB7
						PB5
						…
						DB12
						DB13
						DB14
						DB15
						PB7
						SE

Figure 2-37: ISRC SDP Mapping over the Main-Link

2.2.5.6 Video_Stream_Configuration SDP

Note: *For VSC SDP use specific to Panel Replay, see Section 2.17.5.*

When a DP Sink device has a DPCD r1.2 or higher and 3D stereo rendering capability (as expressed in DisplayID or legacy EDID), a DP Source device may transmit 3D stereo in-band signaling using a VSC SDP by clearing the MSA MISC1 field, bits 2:1, to 00b. When a DP Sink device has its VSC_SDP_EXTENSION_FOR_COLORIMETRY_SUPPORTED bit in the DPRX_FEATURE_ENUMERATION_LIST register (DPCD Address 02210h, bit 3) set to 1, a DP Source device may transmit Pixel Encoding/Colorimetry Format indication using a VSC by setting the MISC1 field, bit 6, to 1. Besides checking the VSC_SDP_EXTENSION_FOR_COLORIMETRY_SUPPORTED bit, the DP Source device shall also read the DP Sink device's supported pixel encoding and colorimetry formats by reading DisplayID or legacy EDID, and shall select the format supported by the DP Sink device.

For an eDP interface, a VSC SDP may also be used to communicate Panel Self Refresh (PSR) control. Both a VSC rev 1 SDP and a VSC rev 2 SDP, as identified by HB2 in Table 2-116, carry the 3D Stereo in-band signaling within Byte 0 (DB0) of the SDP payload. A VSC rev 2 SDP has seven additional payload bytes to carry the PSR control information. Details of these additional VSC rev 2 SDPs are described in *eDP Standard*. When non-stereo video is being transmitted by the Source device, this can be indicated by clearing DB0 to 00h. (See Table H-3 in Section H.1.2.2.)

2.2.5.6.1 VSC SDP Header

Table 2-116 describes the VSC SDP header bytes.

Table 2-116: VSC SDP Header Bytes

Byte #	Bit #	Content
HB0	7:0	**Secondary-data Packet ID** 00h.
HB1	7:0	**Secondary-data Packet Type** 07h.
HB2	4:0	**Revision Number** 01h = VSC SDP supporting 3D stereo only. 02h = VSC SDP supporting 3D stereo + PSR (applies to *eDP v1.3* or higher). 03h = VSC SDP supporting 3D stereo + PSR2 (applies to *eDP v1.4* or higher). 04h = RESERVED for PSR2 use extension (applies to *eDP v1.4* or higher). 05h = VSC SDP supporting 3D stereo + PSR2 + Pixel Encoding/Colorimetry Format indication. A DP Source device is allowed to indicate the pixel encoding/colorimetry format to the DP Sink device with VSC SDP only when the DP Sink device supports it (i.e., VSC_SDP_EXTENSION_FOR_COLORIMETRY_SUPPORTED bit in the DPRX_FEATURE_ENUMERATION_LIST register (DPCD Address 02210h, bit 3) is set to 1). 06h = VSC SDP supporting 3D stereo + PR. 07h = VSC SDP supporting 3D stereo + PR + Pixel Encoding/Colorimetry Format indication. All other values are RESERVED.
	7:5	**RESERVED** Read all 0s.
HB3	4:0	**Number of Valid Data Bytes** 01h = VSC SDP supporting 3D stereo only (HB2 = 01h). 08h = VSC SDP supporting 3D stereo + PSR (HB2 = 02h). 0Ch = VSC SDP supporting 3D stereo + PSR2 (HB2 = 03h). 0Eh = VSC SDP supporting 3D stereo + PSR2 with Y-coordinate of first scan line of the SU region (applies to *eDP v1.4b* and higher). 10h = VSC SDP supporting 3D stereo + PR (HB2 = 06h). 13h = VSC SDP supporting 3D stereo + PSR2 + Pixel Encoding/Colorimetry Format indication (HB2 = 05h). 13h = VSC SDP supporting 3D stereo + PR + Pixel Encoding/Colorimetry Format indication (HB2 = 07h).
	7:5	**RESERVED** Read all 0s.

2.2.5.6.2 VSC SDP Payload Mapping

Figure 2-38 illustrates the VSC SDP mapping over Main-Link with the payload size equal to 16 bytes. It is allowed to have the payload size equal to 32 bytes, with unused bytes zero-padded.

4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 0
SS	SS	SS	SS	SS	SS	SS
HB0	HB1	HB2	HB3	HB0	HB1	HB0
PB0	PB1	PB2	PB3	PB0	PB1	PB0
DB0	DB4	DB8	DB12	HB2	HB3	HB1
DB1	DB5	DB9	DB13	PB2	PB3	PB1
DB2	DB6	DB10	DB14	DB0	DB4	HB2
DB3	DB7	DB11	DB15	DB1	DB5	PB2
PB4	PB5	PB6	PB7	DB2	DB6	HB3
SE	SE	SE	SE	DB3	DB7	PB3
				PB4	PB5	DB0
				DB8	DB12	DB1
				DB9	DB13	DB2
				DB10	DB14	DB3
				DB11	DB15	PB4
				PB6	PB7	DB4
				SE	SE	DB5
						DB6
						DB7
						PB5
						…
						DB12
						DB13
						DB14
						DB15
						PB7
						SE

Figure 2-38: VSC SDP Mapping over the Main-Link

2.2.5.6.3 VSC SDP Payload for 3D Stereo Video

See Appendix H.

2.2.5.6.4 VSC SDP Payload for PSR2

See *eDP Standard*.

2.2.5.6.5 VSC SDP Payload for Pixel Encoding/Colorimetry Format

Table 2-117 describes the VSC SDP DB16 through DB18 bit definitions for Pixel Encoding and Colorimetry Format indication.

Table 2-117: VSC SDP Payload for DB16 through DB18

VSC Byte Offset	Value, by Bit Number								Description/Format
	7	6	5	4	3	2	1	0	
10h = DB16	**Pixel Encoding and Colorimetry Formats**								
	RGB = 0h				RGB				
					0h				sRGB (*IEC 61966-2-1*).
					1h				RGB wide gamut fixed point.
					2h				RGB wide gamut floating point (scRGB (*IEC 61966-2-2*)).
					3h				*Adobe RGB*.
					4h				DCI-P3 (*SMPTE RP 431-2*).
					5h				Custom Color Profile.
					6h				*ITU-R BT.2020* R'G'B'.
					7h – Fh				RESERVED.
	YCbCr 4:4:4 = 1h				YCbCr 4:4:4				
					0h				*ITU-R BT.601*.
					1h				*ITU-R BT.709*.
					2h				$xvYCC_{601}$.
					3h				$xvYCC_{709}$.
					4h				$sYCC_{601}$.
					5h				$opYCC_{601}$.
					6h				*ITU-R BT.2020* $Y'_{C}C'_{BC}C'_{RC}$.
					7h				*ITU-R BT.2020* $Y'C'_{B}C'_{R}$.
					8h – Fh				RESERVED.

Table 2-117: VSC SDP Payload for DB16 through DB18 (Continued)

VSC Byte Offset	Value, by Bit Number								Description/Format
	7	6	5	4	3	2	1	0	
10h = DB16	**Pixel Encoding and Colorimetry Formats (Continued)**								
	YCbCr 4:2:2 = 2h				YCbCr 4:2:2				
					0h				*ITU-R BT.601*.
					1h				*ITU-R BT.709*.
					2h				$xvYCC_{601}$.
					3h				$xvYCC_{709}$.
					4h				$sYCC_{601}$.
					5h				$opYCC_{601}$.
					6h				*ITU-R BT.2020* $Y'_CC'_{BC}C'_{RC}$.
					7h				*ITU-R BT.2020* $Y'C'_BC'_R$.
					8h – Fh				RESERVED.
	YCbCr 4:2:0 = 3h				YCbCr 4:2:0				
					0h				*ITU-R BT.601*.
					1h				*ITU-R BT.709*.
					2h				$xvYCC_{601}$.
					3h				$xvYCC_{709}$.
					4h				$sYCC_{601}$.
					5h				$opYCC_{601}$.
					6h				*ITU-R BT.2020* $Y'_CC'_{BC}C'_{RC}$.
					7h				*ITU-R BT.2020* $Y'C'_BC'_R$.
					8h – Fh				RESERVED.
	Y Only = 4h				Y Only				
					0h				*DICOM PS3.14*.
					1h – Fh				RESERVED.
	RAW = 5h				RAW				
					0h				Custom Color Profile.
					1h – Fh				RESERVED.
	RESERVED = 6h – Fh				–				RESERVED.

Table 2-117: VSC SDP Payload for DB16 through DB18 (Continued)

VSC Byte Offset	Value, by Bit Number								Description/Format
	7	6	5	4	3	2	1	0	
11h = DB17	**Dynamic Range and Component Bit Depth**								
	0, 1	–							**Dynamic Range** 0 = VESA range. 1 = CTA range.
	–	0h				–			**RESERVED**
						0h – 7h			**Component Bit Depth Type** Possible Component Bit Depth values are dependent on the encoding format and colorimetry.
	–					0h – 4h			For pixel encoding format RGB, the following Component Bit Depth values are defined: 000b = 6bpc. 011b = 12bpc. 001b = 8bpc. 100b = 16bpc. 010b = 10bpc. All other values are RESERVED.
	–					1h – 4h			For pixel encoding formats YCbCr 4:4:4, YCbCr 4:2:2, YCbCr 4:2:0, and Y Only, the following Component Bit Depth values are defined: 001b = 8bpc. 011b = 12bpc. 010b = 10bpc. 100b = 16bpc. All other values are RESERVED.
	–					0h – 4h			For pixel encoding format RAW, the following Component Bit Depth values are defined: 000b = RESERVED. 100b = 10bpc. 001b = 6bpc. 101b = 12bpc. 010b = 7bpc. 110b = 14bpc. 011b = 8bpc. 111b = 16bpc.
12h = DB18	**Content Type**								
	0h				0	–			**RESERVED**
	–					0h – 7h			**Content Type** 000b = Not defined. 011b = Video. 001b = Graphics. 100b = Game. 010b = Photo. All other values are RESERVED. ***Note:*** *See CTA-861-G for the definition and expected processing by a stream sink for the above content types.*

2.2.5.7 Camera SDP

SDP type values 08h through 0Fh shall be reserved for vendor-specific camera application use.

2.2.5.7.1 Camera SDP Header

Table 2-118 describes the Camera SDP header bytes.

Table 2-118: Camera SDP Header Bytes

Byte	Content
HB0	**Secondary-data Packet ID**
HB1	**Secondary-data Packet Type** Valid values are 08h through 0Fh, which shall be RESERVED for vendor-specific camera application use.
HB2	Use of this byte is vendor-specific.
HB3	Use of this byte is vendor-specific.

The Camera SDP payload contains the vendor-specific auxiliary data of the frame's main video stream. Figure 2-39 lists the Main-Link mappings of the header and data payloads.

4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	**Lane 1**	**Lane 2**	**Lane 3**	**Lane 0**	**Lane 1**	**Lane 0**
SS	SS	SS	SS	SS	SS	SS
HB0	HB1	HB2	HB3	HB0	HB1	HB0
PB0	PB1	PB2	PB3	PB0	PB1	PB0
DB0	DB4	DB8	DB12	HB2	HB3	HB1
DB1	DB5	DB9	DB13	PB2	PB3	PB1
DB2	DB6	DB10	DB14	DB0	DB4	HB2
DB3	DB7	DB11	DB15	DB1	DB5	PB2
PB4	PB5	PB6	PB7	DB2	DB6	HB3
…	…	…	…	DB3	DB7	PB3
DB(N – 16)	DB(N – 12)	DB(N – 8)	DB(N – 4)	PB4	PB5	DB0
DB(N – 15)	DB(N – 11)	DB(N – 7)	DB(N – 3)	…	…	DB1
DB(N – 14)	DB(N – 10)	DB(N – 6)	DB(N – 2)	DB(N – 8)	DB(N – 4)	DB2
DB(N – 13)	DB(N – 9)	DB(N – 5)	DB(N – 1)	DB(N – 7)	DB(N – 3)	DB3
PB(N / 4)	PB(N / 4 + 1)	PB(N / 4 + 2)	PB(N / 4 + 3)	DB(N – 6)	DB(N – 2)	PB4
SE	SE	SE	SE	DB(N – 5)	DB(N – 1)	…
				PB(N / 4 + 2)	PB(N / 4 + 3)	DB(N – 4)
				SE	SE	DB(N – 3)
						DB(N – 2)
						DB(N – 1)
						PB(N / 4 + 3)
						SE

Figure 2-39: Camera SDP Mapping over Main-Link

2.2.5.7.2 Camera SDP Transport (Informative)

A video stream comprising RAW data is framed identically to any other rasterized video, using vertical blanking periods, horizontal blanking periods, and active video periods, and transported using Single-Stream Transport (SST) mode, –or– as a stream within Multi-Stream Transport (MST) mode. MSA and related SDPs (if needed) shall be transported during the blanking period(s).

Camera SDPs can be transmitted with or without the presence of a main video stream. Figure 2-40 illustrates the transport timing of Camera RAW active pixels (main video stream) and Camera SDPs.

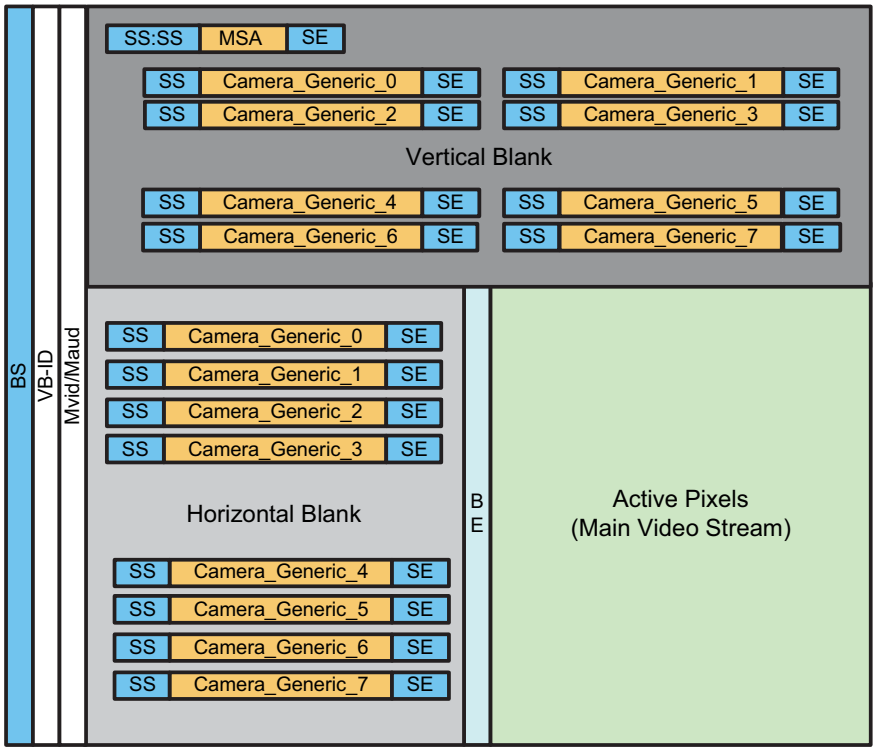


Figure 2-40: Camera RAW Active Pixels (Main Video Stream) and Camera SDP Transport

2.2.5.8 PPS SDP

Note: *See DSC Standard and relevant supporting documents for guidance on PPS values.*

Picture Parameter Set secondary-data packet (PPS SDP) support is new to *DP v1.4*.

The PPS is defined within the PPS syntax definition in *DSC Standard*, *Section 4.1.1*. The PPS is transmitted using the SDP format over the Main-Link during the vertical blanking interval. The Sink device uses the last PPS transmitted before the BS symbol sequence of the scan line prior to the active region, as illustrated in Figure 2-41. The compression parameters may be changed in between compressed frames by transmitting a new PPS. The PPS applies to all subsequent pictures until another PPS is transmitted. The Sink device shall retain the most-recent PPS until the DSC Enable bit in the DSC ENABLE register (DPCD Address 00160h, bit 0) is cleared to 0.

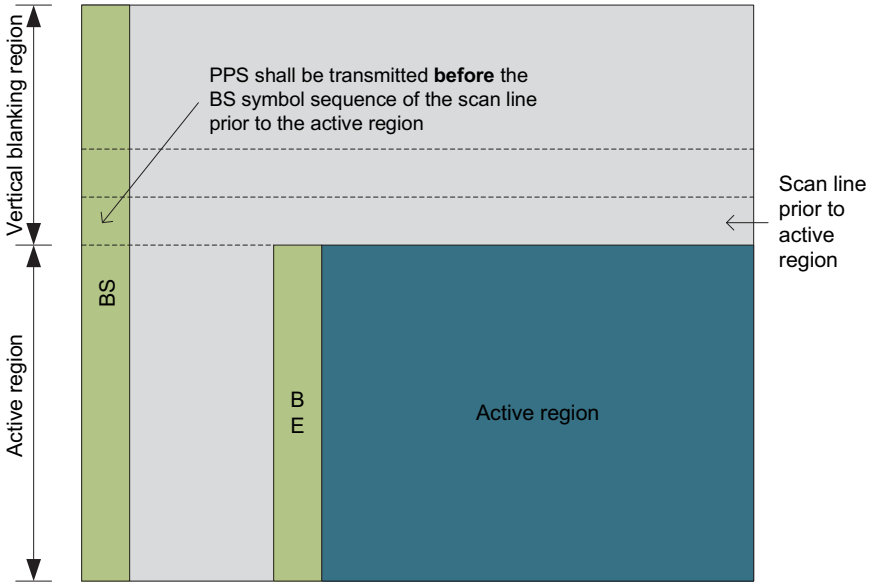


Figure 2-41: PPS Timing – No Change from Prior PPS

Starting with *DP v2.0*, a DP Source device shall transmit the PPS once per frame, regardless of whether PPS changes. The DP Source device shall ensure that the PPS has been transmitted before the BS symbol sequence of the scan line prior to the active region. If a PPS has changed from the prior-transmitted PPS, the PPS transmission shall be completed 150us before the active region if a DP Sink device is capable of a seamless target bit per pixel change, as indicated by the following Dynamic PPS Update Support-related bits in the DSC SUPPORT and DSC SUPPORT AND DSC DECODER COUNT register(s) (DPCD Address(es) 00060h and DPCD Address 02260h, respectively):

- Dynamic PPS Update Support – Compressed-to-Compressed bit (bit 2)
- Dynamic PPS Update Support – Uncompressed-to/from-Compressed bit (bit 3)

2.2.5.8.1 PPS SDP Header and Payload Bytes

Table 2-119 defines the PPS SDP header bytes. Figure 2-42 illustrates the PPS SDP over the Main-Link in 4-, 2-, and 1-lane configuration payload bytes.

Table 2-119: PPS SDP Header Bytes

Byte #	Bit #	Content
HB0	7:0	**Secondary-data Packet ID** 00h.
HB1	7:0	**Secondary-data Packet Type** 10h.
HB2	7:0	**Number of Payload Data Bytes – 1** 7Fh.
HB3	7:0	**RESERVED** Read all 0s.

4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 0
SS	SS	SS	SS	SS	SS	SS
HB0	HB1	HB2	HB3	HB0	HB1	HB0
PB0	PB1	PB2	PB3	PB0	PB1	PB0
PPS0[7:0]	PPS4[7:0]	PPS8[7:0]	PPS12[7:0]	HB2	HB3	HB1
PPS1[7:0]	PPS5[7:0]	PPS9[7:0]	PPS13[7:0]	PB2	PB3	PB1
PPS2[7:0]	PPS6[7:0]	PPS10[7:0]	PPS14[7:0]	PPS0[7:0]	PPS4[7:0]	HB2
PPS3[7:0]	PPS7[7:0]	PPS11[7:0]	PPS15[7:0]	PPS1[7:0]	PPS5[7:0]	PB2
PB4	PB5	PB6	PB7	PPS2[7:0]	PPS6[7:0]	HB3
…	…	…	…	PPS3[7:0]	PPS7[7:0]	PB3
PPS112[7:0]	PPS116[7:0]	PPS120[7:0]	PPS124[7:0]	PB4	PB5	PPS0[7:0]
PPS113[7:0]	PPS117[7:0]	PPS121[7:0]	PPS125[7:0]	…	…	PPS1[7:0]
PPS114[7:0]	PPS118[7:0]	PPS122[7:0]	PPS126[7:0]	PPS120[7:0]	PPS124[7:0]	PPS2[7:0]
PPS115[7:0]	PPS119[7:0]	PPS123[7:0]	PPS127[7:0]	PPS121[7:0]	PPS125[7:0]	PPS3[7:0]
PB32	PB33	PB34	PB35	PPS122[7:0]	PPS126[7:0]	PB4
SE	SE	SE	SE	PPS123[7:0]	PPS127[7:0]	…
				PB34	PB35	PPS124[7:0]
				SE	SE	PPS125[7:0]
						PPS126[7:0]
						PPS127[7:0]
						PB35
						SE

Figure 2-42: PPS SDP Payload Mapping over Main-Link

2.2.5.9 Video_Stream_Configuration Extension VESA SDP

Updated in *DP v1.4a*.

Support for Video_Stream_Configuration Extension VESA (VSC_EXT_VESA) is new to *DP v1.4*.

The VSC_EXT_VESA SDP allows a DP Source device to transmit video stream-related metadata aligned with the stream. The VSC_EXT_VESA SDP chaining framework enables a flexible metadata transportation framework that can handle transport of a few bytes of payload, using a single VSC_EXT_VESA SDP, by chaining multiple VSC_EXT_VESA SDPs per video frame.

Note: *A single VSC_EXT_VESA SDP is typically less than or equal to 2KB, but can be larger.*

A single VSC_EXT_VESA SDP is composed of four header bytes and 32 payload bytes. *DP v1.4* (and higher) defines the header bytes and the associated fields; the payload may be defined within *DP v1.4* (and higher) or by other standards organizations for specific feature support.

The VSC_EXT_VESA SDP is mainly intended for carrying non-CTA-defined header-related metadata that describes the header stream content attributes; however, the same framework can be used for other purposes when large payload data needs to be transported.

A DP Source device may transmit other SDPs, such as Audio_Stream SDPs, in between the VSC_EXT_VESA SDP(N) and VSC_EXT_VESA SDP($N + 1$). The same rule applies to the VSC_EXT_CTA SDP.

Figure 2-43 describes the VSC_EXT_VESA SDP chaining and metadata transport framework. The framework is composed of a flag that indicates whether any additional VSC_EXT_VESA SDPs are to follow as part of the SDP header bytes. The VSC_EXT_VESA SDP header bytes also include a flag indicating whether the header's Packet Sequence field is being sequentially incremented, starting from 0, as part of the VSC_EXT_VESA SDP chaining framework. The metadata transport framework also allows the DP Sink device to expose supported payload types and associated setup time mandates, explicitly or implicitly, in DisplayID or legacy EDID. The DP Source device shall transmit the entirety of the chained VSC_EXT_VESA SDPs, thereby ensuring that the DP Sink device setup time mandate is met.

If the entirety of the chained VSC_EXT_VESA SDPs are not received in time (i.e., the chained SDP with bit 7 of HB2 equal to 0 is not received in time), the DP Sink device shall discard the incomplete chained SDPs. The same policy mandate applies to the VSC_EXT_CTA SDPs, described in Section 2.2.5.10.

As illustrated in Figure 2-43, within a single DP frame, the VSC_EXT_VESA SDP framework allows Frame *N*'s metadata to be transported as early as the first horizontal blank after BE of Frame *N* – 1 and till the setup time before the start of active for Frame *N*.

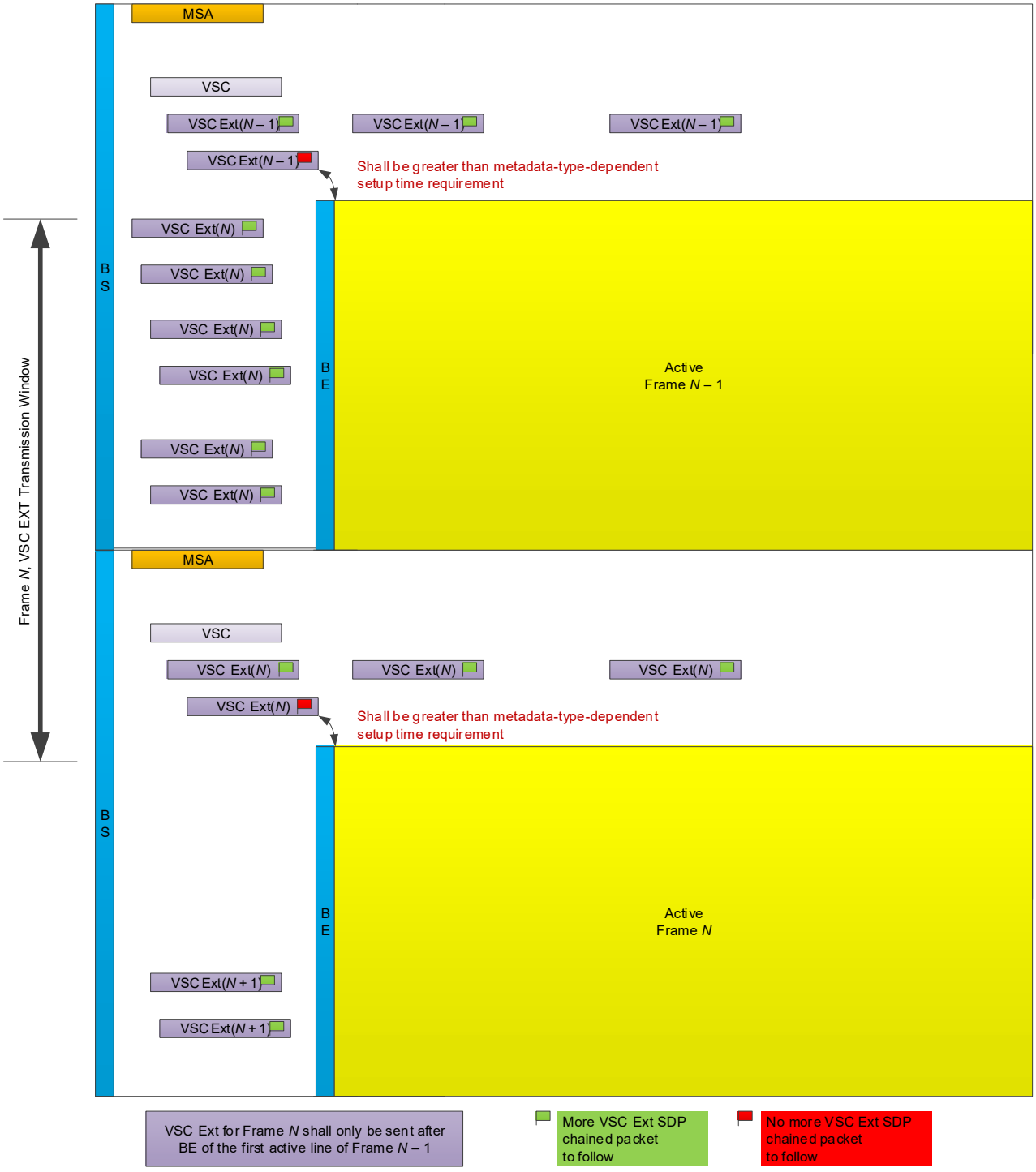


Figure 2-43: VSC_EXT_VESA SDP Framework

When a DP Sink device has DPCD r1.4 (or higher) and its VSC_EXT_VESA_SDP_SUPPORTED bit in the DPRX_FEATURE_ENUMERATION_LIST register (DPCD Address 02210h, bit 4) is set to 1, a DP Source device may transmit stream metadata using a single VSC_EXT_VESA SDP framework for the supported payload type exposed in DisplayID and/or legacy EDID by the DP Sink device.

If a DP Sink device, in addition to setting the VSC_EXT_VESA_SDP_SUPPORTED bit, also sets the VSC_EXT_VESA_SDP_CHAINING_SUPPORTED bit in the DPRX_FEATURE_ENUMERATION_LIST register (DPCD Address 02210h, bit 5) to 1, a DP Source device may transmit stream metadata using multiple VSC_EXT_VESA SDPs that use the chained-SDP framework for the supported payload type exposed in DisplayID and/or legacy EDID by the DP Sink device.

A DP Sink device that supports VSC_EXT_VESA SDP chaining shall support chaining of up to 64 SDPs equal to 2KB in size. A DP Sink device that supports the chaining of VSC_EXT_VESA SDPs beyond 64 shall indicate the number (count) that exceeds 64 in the VSC_EXT_VESA_SDP_MAX_CHAINING_COUNT field in the VSC_EXT_VESA_SDP_MAX_CHAINING register (DPCD Address 02212h, bits 7:0). For example, if a DP Sink device supports the chaining of 96 SDPs (maximum), the device shall program the VSC_EXT_VESA_SDP_MAX_CHAINING register to 32 decimal (20h).

2.2.5.9.1 VSC_EXT_VESA and VSC_EXT_CTA SDP Header and Payload Bytes

Table 2-120 defines the VSC_EXT_VESA and VSC_EXT_CTA SDP header bytes. Table 2-121 defines the VSC_EXT_VESA and VSC_EXT_CTA SDP payload bytes (actual payload is dependent on the payload type).

VSC_EXT_VESA and VSC_EXT_CTA SDPs follow the same lane mapping as the VSC SDP illustrated in Figure 2-38.

Table 2-120: VSC_EXT_VESA and VSC_EXT_CTA SDP Header Bytes

Byte #	Bit #	Content
HB0	7:0	**Secondary-data Packet ID** Specific to stream (usually 00h).
HB1	7:0	**Secondary-data Packet Type** 20h = VESA. 21h = CTA.
HB2	1:0	**VSC_EXT_VESA SDP Framework Version** Cleared to all 0s.
	5:2	**RESERVED** Read all 0s.
	6	**VARIABLE_PACKET_SEQUENCE_NUMBER** 0 = Packet Sequence field is fixed. 1 = Packet Sequence field is incremented with chained packets.
	7	**MIDDLE_OF_CHAINING** 0 = No chained packets to follow. 1 = Chained packet(s) to follow.
HB3	4:0	**Packet Sequence** Range is from 0 to 31. Shall be cleared to 0 on the first SDP of a new VSC_EXT packet sequence. When bit 6 of HB2 is set to 1, this field shall increment by 1 on each subsequent chained packet. This counter rolls over to 0 when it exceeds 31.
	7:5	**RESERVED** Read all 0s.

Table 2-121: VSC_EXT_VESA and VSC_EXT_CTA SDP Payload Bytes – DB0 through DB31

Byte #	Bit #	Content
DB0	7:0	**Payload Byte 1**
DB1	7:0	**Payload Byte 2**
DB2	7:0	**Payload Byte 3**
…	…	**…**
DB30	7:0	**Payload Byte 31**
DB31	7:0	**Payload Byte 32**

2.2.5.10 Video_Stream_Configuration Extension CTA SDP

Support for Video_Stream_Configuration Extension CTA (VSC_EXT_CTA) is new to *DP v1.4*.

VSC_EXT_CTA SDP shall be used for future CTA INFOFRAMEs that have more than 28 bytes of payload. A CTA INFOFRAME whose payload size is 28 or fewer bytes shall be encapsulated in the INFOFRAME SDP described in Section 2.2.5.12.

The SDP Type value for a VSC_EXT_CTA SDP is 21h (see Table 2-120). The VSC_EXT_CTA SDP's specification is identical to that of a VSC_EXT_VESA SDP. (See Section 2.2.5.9.)

When a DP Sink device has DPCD r1.4 (or higher) and its VSC_EXT_CTA_SDP_SUPPORTED bit in the DPRX_FEATURE_ENUMERATION_LIST register (DPCD Address 02210h, bit 6) is set to 1, a DP Source device may transmit stream metadata using a single VSC_EXT_CTA SDP framework for the supported payload type exposed in DisplayID and/or legacy EDID by the DP Sink device.

If a DP Sink device, in addition to setting the VSC_EXT_CTA_SDP_SUPPORTED bit, also sets the VSC_EXT_CTA_SDP_CHAINING_SUPPORTED bit in the DPRX_FEATURE_ENUMERATION_LIST register (DPCD Address 02210h, bit 7) to 1, a DP Source device may transmit stream metadata using multiple VSC_EXT_CTA SDPs that chain framework for the supported payload type exposed in DisplayID and/or legacy EDID by the DP Sink device.

A DP Sink device that supports VSC_EXT_CTA SDP chaining shall support the chaining of up to 64 SDPs equal to 2KB in size. A DP Sink device that supports the chaining of VSC_EXT_CTA SDPs beyond 64 shall indicate the number (count) that exceeds 64 in the VSC_EXT_CTA_SDP_MAX_CHAINING_COUNT field in the VSC_EXT_CTA_SDP_MAX_CHAINING register (DPCD Address 02213h, bits 7:0). For example, if a DP Sink device supports the chaining of 96 SDPs (maximum), the device shall program the VSC_EXT_CTA_SDP_MAX_CHAINING register to 32 decimal (20h).

2.2.5.10.1 CTA Extended INFOFRAME Transmission with Dynamic VSC_EXT_CTA SDP

New to *DP v1.4a*.

This section describes how to carry and map a CTA Extended INFOFRAME (see *CTA-861-G*) over DisplayPort using the dynamic VSC_EXT_CTA SDP.

For the VSC_EXT_CTA SDP, HB1 shall be programmed to 21h to indicate that the payload consists of the Extended INFOFRAME defined by CTA. The Extended INFOFRAME's payload is carried in the SDP payload data bytes, starting from the Extended INFOFRAME Type Code and followed by the Length of Extended INFOFRAME and Data Bytes. Other fields of the VSC_EXT_CTA SDP header byte shall be populated as per Section 2.2.5.9.1.

Table 2-122 lists the detailed mapping of the VSC_EXT_CTA SDP's Extended INFOFRAME fields. The Extended INFOFRAME Type LSB field shall be Payload Byte 0 of the first VSC_EXT_CTA SDP. The Extended INFOFRAME Type MSB shall be Payload Byte 1 of the first VSC_EXT_CTA SDP and so forth. After the first VSC_EXT_CTA SDP is filled (i.e., payload Byte 31 is filled), the next byte of the Extended INFOFRAME byte is situated in Payload Byte 0 of the second VSC_EXT_CTA SDP, as listed in Table 2-123.

Table 2-122: Extended INFOFRAME Payload Mapping of the First VSC_EXT_CTA SDP Payload Bytes – DB0 through DB31

Byte #	Bit #	Content
DB0	7:0	**Payload Byte 1 – Extended INFOFRAME Type LSB**
DB1	7:0	**Payload Byte 2 – Extended INFOFRAME Type MSB**
DB2	7:0	**Payload Byte 3 – Length of Following Extended INFOFRAME Data LSB**
DB3	7:0	**Payload Byte 4 – Length of Following Extended INFOFRAME Data MSB**
DB4	7:0	**Extended INFOFRAME Data Byte 1**
…	…	**…**
DB30	7:0	**Extended INFOFRAME Data Byte 27**
DB31	7:0	**Extended INFOFRAME Data Byte 28**

Table 2-123: Extended INFOFRAME Payload Mapping of the Second VSC_EXT_CTA SDP Payload Bytes – DB0 through DB31

Byte #	Bit #	Content
DB0	7:0	**Extended INFOFRAME Data Byte 29**
DB1	7:0	**Extended INFOFRAME Data Byte 30 (If Applicable)**
…	…	**…**
DB30	7:0	**Extended INFOFRAME Data Byte 59 (If Applicable)**
DB31	7:0	**…**

As described earlier, the setup time mandate shall be implicitly or explicitly defined and is metadata-type-dependent. For Extended INFOFRAME Metadata Type 0x0001 to 0x0004, which pertain to HDR Dynamic Meta types, the DP setup time mandate is defined as 200us.

2.2.5.11 Adaptive-Sync SDP

Support for the Adaptive-Sync SDP is new to *DP v1.4a*.

An Adaptive-Sync SDP allows a DP protocol converter to forward Adaptive-Sync video, with minimal buffering overhead within the protocol converter. Figure 2-44 illustrates the timing of an Adaptive-Sync SDP transmission.

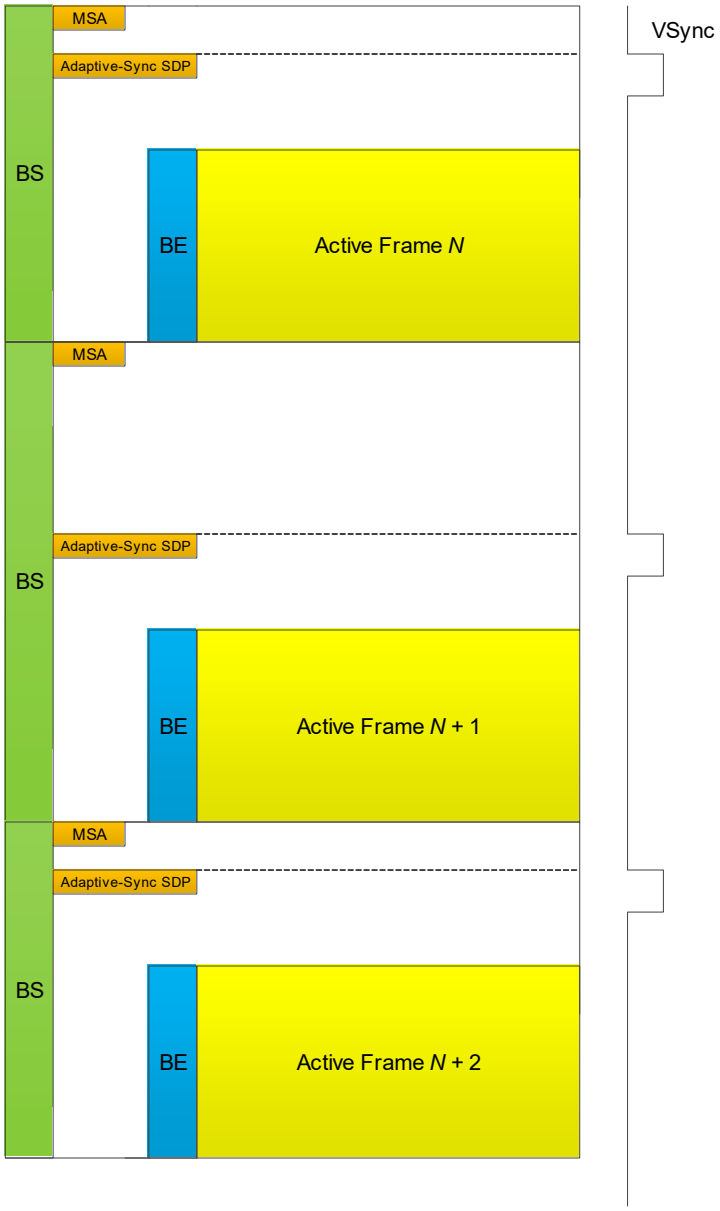


Figure 2-44: Adaptive-Sync SDP Transmission Timing

An Adaptive-Sync-capable DP protocol converter shall indicate Adaptive-Sync SDP support by setting the ADAPTIVE_SYNC_SDP_SUPPORTED bit in the ADAPTIVE_SYNC_CAPABILITY register (DPCD Address 02214h, bit 0) in addition to setting the MSA_TIMING_PAR_IGNORED bit in the DOWN_STREAM_PORT_COUNT register (DPCD Address 00007h, bit 6).

An Adaptive-Sync-capable DP protocol converter shall support SDP splitting in SST and MST modes, and indicates its splitting capability by setting the SST_SPLIT_SDP_CAP bit in the DPRX_FEATURE_ENUMERATION_LIST register (DPCD Address 02210h, bit 1).

An Adaptive-Sync-capable DP Source device may enable an Adaptive-Sync video transmission to a plugged DP protocol converter only after verifying the following:

- Plugged DP protocol converter has both the MSA_TIMING_PAR_IGNORED bit and ADAPTIVE_SYNC_SDP_SUPPORTED bit set
- Stream sink plugged to the DP protocol converter indicates support for the Adaptive-Sync refresh rate range in DisplayID or legacy EDID

As is always the case with Adaptive-Sync video transmission, an Adaptive-Sync-capable DP Source device shall use an AUX write transaction to write 1 to the MSA_TIMING_PAR_IGNORE_EN bit in the DOWNSPREAD_CTRL register (DPCD Address 00107h, bit 7) prior to enabling an Adaptive-Sync video transmission. When the plugged DP device has the ADAPTIVE_SYNC_SDP_SUPPORTED bit set, a DP Source device shall transmit an Adaptive-Sync SDP before enabling an Adaptive-Sync video transmission.

When transmitting an Adaptive-Sync SDP, a DP Source device shall do the following:

- Ensure that the start and end of the Adaptive-Sync SDP transmission occur within the 1st half of the line (marked by BS symbol sequences) that corresponds to the start of the VSync pulse
- Transmit valid HTotal[15:0], HStart[15:0], HSyncPolarity[0] (HSP), HSyncWidth[14:0] (HSW), VStart[15:0], VSyncPolarity[0] (VSP), and VSyncWidth[14:0] (VSW) while transmitting an Adaptive-Sync SDP, as well as valid HWidth[15:0] and VHeight[15:0]

That is, an Adaptive-Sync-capable DP protocol converter shall ignore only VTotal[15:0] while receiving an Adaptive-Sync SDP.

2.2.5.11.1 Adaptive-Sync SDP Header Bytes

Table 2-124 describes the Adaptive-Sync SDP header bytes. Adaptive-Sync SDP payload and parity bytes shall be cleared to 0.

Table 2-124: Adaptive-Sync SDP Header Bytes

Byte #	Bit #	Content
HB0	7:0	**Secondary-data Packet ID** Specific to stream (usually 00h).
HB1	7:0	**Secondary-data Packet Type** 22h = Adaptive-Sync.
HB2	4:0	**Revision Number** 01h = Initial revision, with no payload byte definition. The SDP's presence marks the VSync location for protocol converter timing output.
	7:5	**RESERVED** Read all 0s.
HB3	4:0	**Number of Valid Data Bytes** 00h = For Revision Number value of 01h, no data byte is defined. All payload bytes shall be cleared to 0.
	7:5	**RESERVED** Read all 0s.

An Adaptive-Sync SDP shall follow the same lane mapping as other SDPs depicted in Section 2.2.5 (e.g., Figure 2-45 illustrating INFOFRAME SDP lane mapping).

2.2.5.12 INFOFRAME SDP

Figure 2-45 illustrates both an INFOFRAME SDP v1.2 and v1.3 (see Section 2.2.5.12.1 and Section 2.2.5.12.2, respectively) over the Main-Link. Section 2.2.6 explains the construction of the parity bytes (PBs) that are illustrated in Figure 2-45. INFOFRAME SDP v1.2 shall be used to convey Audio INFOFRAME (non-Basic Audio) control information, as specified in *CTA-861-G*. Other INFOFRAME coding types, as specified in *CTA-861-G*, *Table 5*, shall use INFOFRAME SDP v1.3.

4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 0
SS	SS	SS	SS	SS	SS	SS
HB0	HB1	HB2	HB3	HB0	HB1	HB0
PB0	PB1	PB2	PB3	PB0	PB1	PB0
DB0	DB4	DB8	DB12	HB2	HB3	HB1
DB1	DB5	DB9	DB13	PB2	PB3	PB1
DB2	DB6	DB10	DB14	DB0	DB4	HB2
DB3	DB7	DB11	DB15	DB1	DB5	PB2
PB4	PB5	PB6	PB7	DB2	DB6	HB3
DB16	DB20	DB24	DB28	DB3	DB7	PB3
DB17	DB21	DB25	DB29	PB4	PB5	DB0
DB18	DB22	DB26	All 0s	DB8	DB12	DB1
DB19	DB23	DB27	All 0s	DB9	DB13	DB2
PB8	PB9	PB10	PB11	DB10	DB14	DB3
SE	SE	SE	SE	DB11	DB15	PB4
				PB6	PB7	DB4
				DB16	DB20	DB5
				DB17	DB21	DB6
				DB18	DB22	DB7
				DB19	DB23	PB5
				PB8	PB9	…
				DB24	DB28	DB24
				DB25	DB29	DB25
				DB26	All 0s	DB26
				DB27	All 0s	DB27
				PB10	PB11	PB10
				SE	SE	DB28
						DB29
						All 0s
						All 0s
						PB11
						SE

where:

- HB*xx* = Header Byte
- PB*xx* = Parity Byte
- DB*xx* = Data Byte

Figure 2-45: INFOFRAME SDP v1.2 and v1.3 Mapping over Main-Link

2.2.5.12.1 INFOFRAME SDP v1.2

A DP device shall comply with *CTA-861-G* when using the INFOFRAME SDP as an Audio INFOFRAME.

The DB1 ~ DB*N* (Data Byte 1 ~ Data Byte *N*), as specified in *CTA-861-G*, are mapped to SDP DB0 ~ DB[*N* – 1]. Unused bytes shall be zero-padded.

In use cases for coding types other than One Bit or DST audio, certain control information such as the audio stream's Sampling Frequency, Sample Bits, and Coding Type can be set through Audio INFOFRAME or Stream header bits. When the Stream header case is used, the Audio INFOFRAME shall be cleared to all 0s to indicate "Refer to Stream Header" so that the control information can be passed to the receiver through *IEC 60958* or *IEC 61937* Stream header bits. (See *IEC 60958-3* for stream header bit field programming mandates.)

In use cases for the One Bit audio coding type, Sampling Frequency, and in the case of 8-channel One Bit audio, Speaker Mapping, shall be set through the Audio INFOFRAME (CA, DM_INH, LSV, and LFEPBL). The Audio INFOFRAME sample size is **not** valid for 2- or 8-channel One Bit audio. Channel Count and Coding Type shall be programmed in the Audio_Stream SDP header, leaving the matching Audio INFOFRAME fields cleared to all 0s to indicate "Refer to Stream Header."

In use cases for the DST audio coding type, Sampling Frequency shall be set through the Audio INFOFRAME. Coding Type shall be set in the Audio_Stream SDP header. Programming the Channel Count in the Audio_Stream SDP header is **not** applicable for DST audio because the number of DST Audio channels is carried within the audio payload stream itself. This leaves the matching Audio INFOFRAME CC and CT fields cleared to all 0s to indicate "Refer to Stream Header." Audio INFOFRAME Sample Size and Channel Allocation are **not** valid for DST audio.

Although some parameters are available in the Audio_Stream and Audio INFOFRAME SDPs, the values of those in the Audio_Stream SDP take precedence.

Other audio packing formats may be added in a future revision of this Standard while maintaining the consistent secondary-data mapping specification described in this Standard.

INFOFRAME SDPs shall be transmitted once per frame during the main video stream's vertical blanking period. For the transport of an Audio INFOFRAME SDP without a main video stream, see Section 2.2.5.2.7. For further details regarding audio transport over DisplayPort, see Appendix A.

Table 2-125 summarizes the header bytes of an INFOFRAME SDP v1.2. Table 2-126 describes payload byte mapping of INFOFRAME SDP v1.2.

Table 2-125: INFOFRAME SDP v1.2 Header Bytes

Byte #	Bit #	Content
HB0	7:0	**Secondary-data Packet ID** Audio INFOFRAME SDP, Audio_TimeStamp SDP, Audio_Stream SDP, Audio_CopyManagement SDP, and ISRC SDP shall have the same Packet ID when they are associated with the same audio stream. • When only one audio stream per main video stream is being transmitted, the value shall be 00h • When multiple audio streams per main video stream are being transmitted, this SDP ID value is used to distinguish one audio stream from the others
HB1	7:0	**Secondary-data Packet Type** 80h + Audio INFOFRAME Type value (04h).
HB2	7:0	**Least Significant Eight Bits of (Data Byte Count – 1)** 1Bh (i.e., Data Byte Count = 28 bytes). Unused bytes shall be zero-padded.
HB3	1:0	**Most Significant Two Bits of (Data Byte Count – 1)**
	7:2	**INFOFRAME SDP Version Number** 12h.

Table 2-126: INFOFRAME SDP v1.2 Payload Data Bytes – DB0 through DB31

Byte #	Bit #	Content
DB0	7:0	**CTA Payload Byte 1**
DB1	7:0	**CTA Payload Byte 2**
DB2	7:0	**CTA Payload Byte 3**
…	…	**…**
DB27	7:0	**CTA Payload Byte 28** ***Note:*** *For a CTA Payload size that is less than 28 bytes, non-existent payload bytes are zero-padded.*
DB28	7:0	**Zero Padding**
DB29	7:0	**Zero Padding**
DB30	7:0	**Zero Padding**
DB31	7:0	**Zero Padding**

2.2.5.12.2 INFOFRAME SDP v1.3

Table 2-127 describes how to populate INFOFRAME SDP Header v1.3. Table 2-128 describes payload byte mapping of INFOFRAME SDP v1.3 that shall be used for non-audio CTA INFOFRAME encapsulation.

Table 2-127: INFOFRAME SDP v1.3 Header Bytes

Byte #	Bit #	Content
HB0	7:0	**Secondary-data Packet ID** Shall be 00h for non-Audio INFOFRAME.
HB1	7:0	**Secondary-data Packet Type** 80h + Non-audio INFOFRAME Type value.
HB2	7:0	**Least Significant Eight Bits of (Data Byte Count – 1)** 1Dh (i.e., Data Byte Count = 30 bytes). Unused bytes shall be zero-padded.
HB3	1:0	**Most Significant Two Bits of (Data Byte Count – 1)** Clear to 00b.
	7:2	**INFOFRAME SDP Version Number** 13h.

Table 2-128: INFOFRAME SDP v1.3 Payload Data Bytes – DB0 through DB31

Byte #	Bit #	Content
DB0	7:0	**CTA Header Byte 2 (INFOFRAME Version Number)**
DB1	7:0	**CTA Header Byte 3 (INFOFRAME Length)**
DB2	7:0	**CTA Payload Byte 1**
DB3	7:0	**CTA Payload Byte 2**
DB4	7:0	**CTA Payload Byte 3**
…	…	**…**
DB29	7:0	**CTA Payload Byte 28** ***Note:*** *For a CTA Payload size that is less than 28 bytes, non-existent payload bytes are zero-padded.*
DB30	7:0	**Zero Padding**
DB31	7:0	**Zero Padding**

2.2.5.13 SDP Splitting in SST Mode

Note: *Support for SDP splitting in MST mode is defined in Section 2.6.3.3.2.*

The DP Source device has an option of when it shall use the SDP splitting capability. In SST mode, the capability for a DP Sink device to reconstruct a split SDP is indicated by setting the SST_SPLIT_SDP_CAP bit in the DPRX_FEATURE_ENUMERATION_LIST register (DPCD Address 02210h, bit 1) to 1. This bit shall always be set to 1 (supported) in all new designs.

SDP splitting in SST and MST modes shall be supported for a DP Sink/Branch device.

SDP splitting is the process of splitting SDPs with a main video stream that includes the BS/BE symbol sequence, associated data (VB-ID/Mvid[7:0]/Maud[7:0]), and MSA packet, as illustrated in Figure 2-46.

Only one level of splitting is allowed. SDP splitting by another SDP is prohibited. The SDP stream may be interrupted at any time, and may additionally be interrupted more than once (e.g., such as when the HBlank period is short and the SDP length is long). In SST implementations, SDP interruption and resumption can occur at any individual symbol boundary.

Note: *In MST implementations, interruption and resumption of the SDP shall occur at the 4-symbol sequence boundary.*

SDP splitting can occur during HBlank and VBlank periods. SDP splitting can also occur while IDLE_PATTERN is being transmitted (no main video stream pixel data is transmitted).

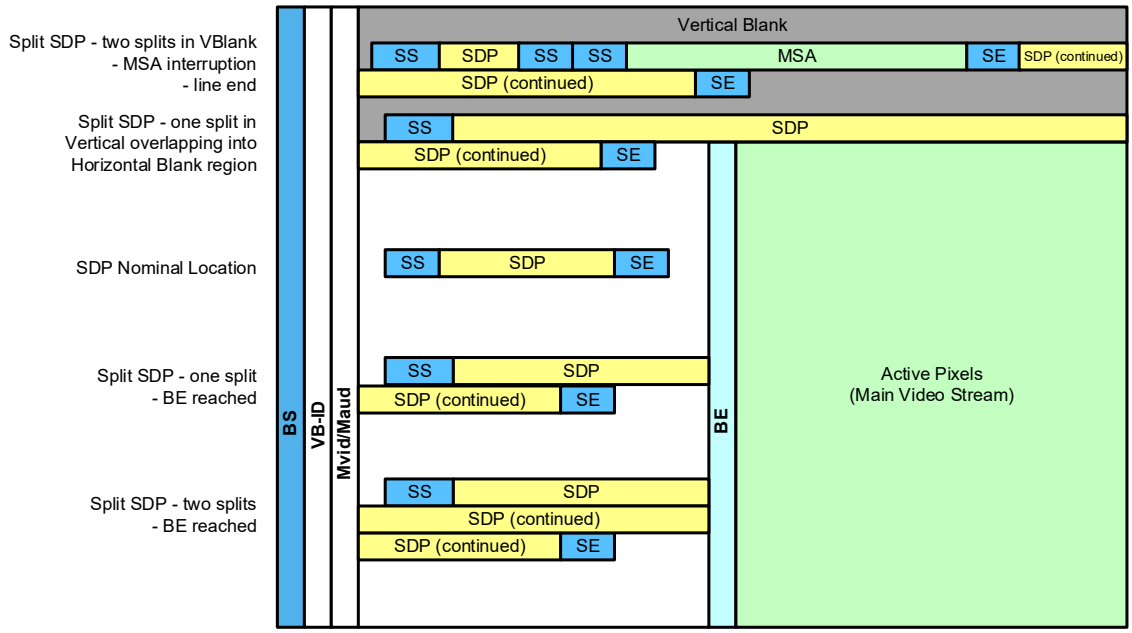


Figure 2-46: SDP Splitting in SST Mode Examples

2.2.6 ECC for SDP

All SDPs shall be protected by way of ECC. (DP Main-Link Attributes data is protected by way of redundancy.)

The SDP shall consist of a 4-byte header protected by four bytes of parity, followed by a payload consisting of a multiple of 8 bytes of data protected by the same multiple of 2 bytes of parity (i.e., 8 packet body bytes have 2 bytes of parity, 16 packet body bytes have 4 bytes of parity, etc.). The SDP shall end with a parity byte. SDPs constructed with fewer than 8 bytes of data shall use zero padding to fill the remaining data positions.

2.2.6.1 ECC Based on RS(15, 13)

DisplayPort uses RS(15, 13), with a symbol size of one nibble (four bits) in the ECC block.

The basic principle of error correcting encoding is to find the remainder of the message divided by a generator polynomial G(x).

The encoder works by simulating a Linear Feedback Shift Register with a degree equal to G(x), and feedback taps with the coefficients of the generating polynomial of the code. In general, the generator polynomial G(x) for any number of parity, configurable as the number of parity (NPAR), shall be as follows:

$$G(x) = (x - \alpha^0)(x - \alpha^1)(x - \alpha^2)(x - \alpha^3)(x - \alpha^4) \ldots (x - \alpha^{NPAR-1})$$

Because RS(15, 13) with a symbol size of one nibble is chosen, the second-degree generator polynomial is used as follows:

$$G(x) = (x - \alpha^0)(x - \alpha^1) = x^2 - g_1 \times x + g_0$$

Note: *Subtraction is equivalent to addition in binary fields.*

Therefore:

$$G(x) = x^2 + g_1 \times x + g_0$$

where:

- $g_1 = \alpha^4$
- $g_0 = \alpha$

With encoding of the base field GF (2^4), "α" is equal to (0, 0, 1, 0), which gives α^4 = (0, 0, 1, 1).

The logic equations for implementing g_1 and g_0 multiplications are listed below (where c[3:0] is a 4-bit nibble being multiplied by g_1 or g_0):

$$g_1 \times c[3:0] = \{c[3]\hat{}[2], c[2]\hat{}[1], c[3]\hat{}[1]\hat{}[0], c[3]\hat{}[0]\}$$

$$g_0 \times c[3:0] = \{c[2], c[1], c[3]\hat{}[0], c[3]\}$$

The following three messages show the outputs of ECC for input data, with parity nibbles listed as ***underlined, bolded, italicized*** numbers:

- Transmitted Message:
  f, e, d, c, b, a, 9, 8, ***2, 2***
- Transmitted Message:
  9, 8, 3, 2, 1, 7, 5, 4, ***8, f,***
- Transmitted Message:
  7, 6, 5, 9, 8, 1, 3, 2, ***7, 2,***

2.2.6.2 ECC g_1 and g_0 C-code (Informative)

Figure 2-47 illustrates the block diagram of an RS(15, 13) encoder with a symbol size of nibble.

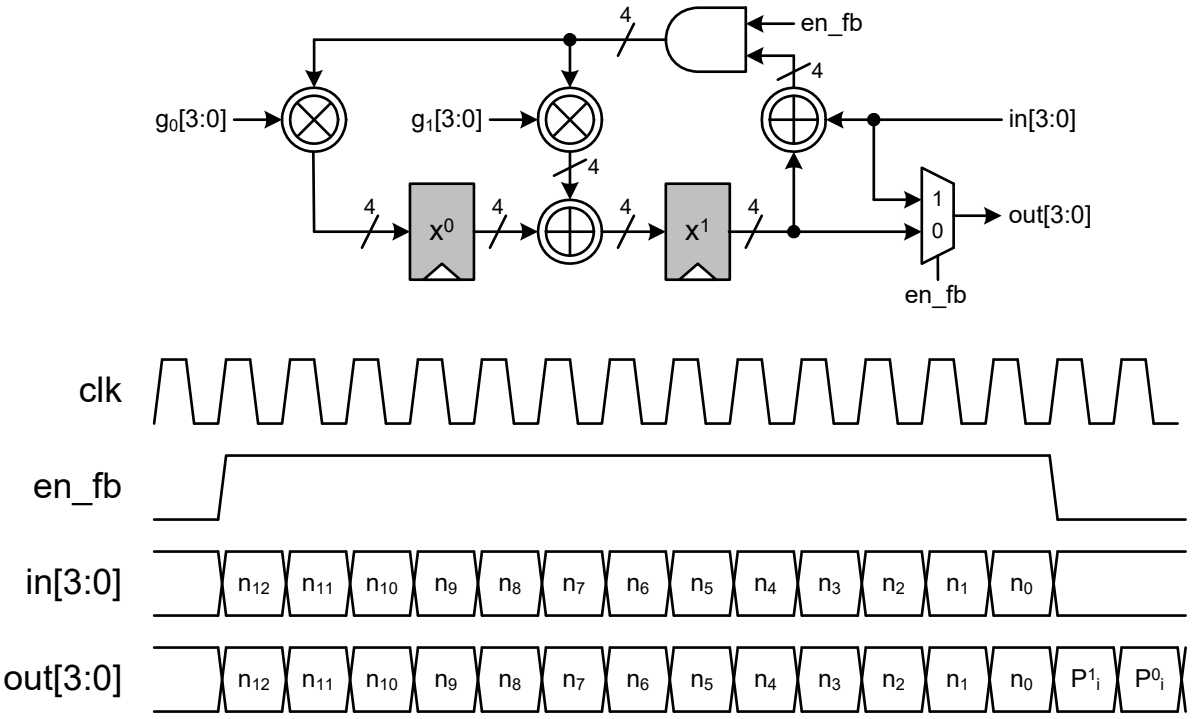


Figure 2-47: RS(15, 13) Encoder Block Diagram

The following example illustrates ECC g_1 and g_0 use in C code.

```
//-------------------------------------------------
//c * a^1
//-------------------------------------------------
unsigned char gfmul_1( unsigned char ) ;
unsigned char gfmul_1( a );
unsigned char a ;
{
int i ;
unsigned char c[8], gf_mul[8], r ;
 for ( i=0; i< 4; i++) {  /* Convert to single bit array for multiply */
 c[i] = a & 0x01 ;
 a = a >> 1 ;
}

gf_mul[0] = c[3] ;
gf_mul[1] = c[0] ^ c[3] ;
gf_mul[2] = c[1] ;
gf_mul[3] = c[2] ;
r = 0 ;
for ( i=0; i<4; i++) {
 r = ((gf_mul[i] & 0x01) << i) | r ;
}
return (r) ;
}
//-------------------------------------------------------
// c * a^4
//-------------------------------------------------------
unsigned char gfmul_4( unsigned char ) ;
unsigned char gfmul_4( a );
unsigned char a ;
{
int i ;
unsigned char c[8], gf_mul[8], r ;
 for ( i=0; i< 4; i++) {  /* Convert to single bit array for multiply */
 c[i] = a & 0x01 ;
 a = a >> 1 ;
}
gf_mul[0] = c[0] ^ c[3] ;
gf_mul[1] = c[0] ^ c[1]^ c[3] ;
gf_mul[2] = c[1] ^ c[2] ;
gf_mul[3] = c[2] ^ c[3] ;
r = 0 ;
for ( i=0; i<4; i++) {
 r = ((gf_mul[i] & 0x01) << i) | r ;
}
return (r) ;
}
//-----------------------------------------------------------
```

2.2.6.3 Nibble Interleaving

To further enhance the error correcting capability, the DP ECC block incorporates nibble interleaving after the incoming data packet is error-correcting encoded. Combining RS(15, 13) with the nibble interleaving, the ECC block is capable of correcting up to a 2-byte error within a 16-byte data block.

As illustrated in Figure 2-48 (for payload) and Figure 2-50 (for header), Lane 0 is interleaved with Lane 1, while Lane 2 is interleaved with Lane 3 for 4- and 2-lane Main-Link configurations. Figure 2-49 (for payload) and Figure 2-51 (for header) illustrate interleaving for a 1-lane Main-Link.

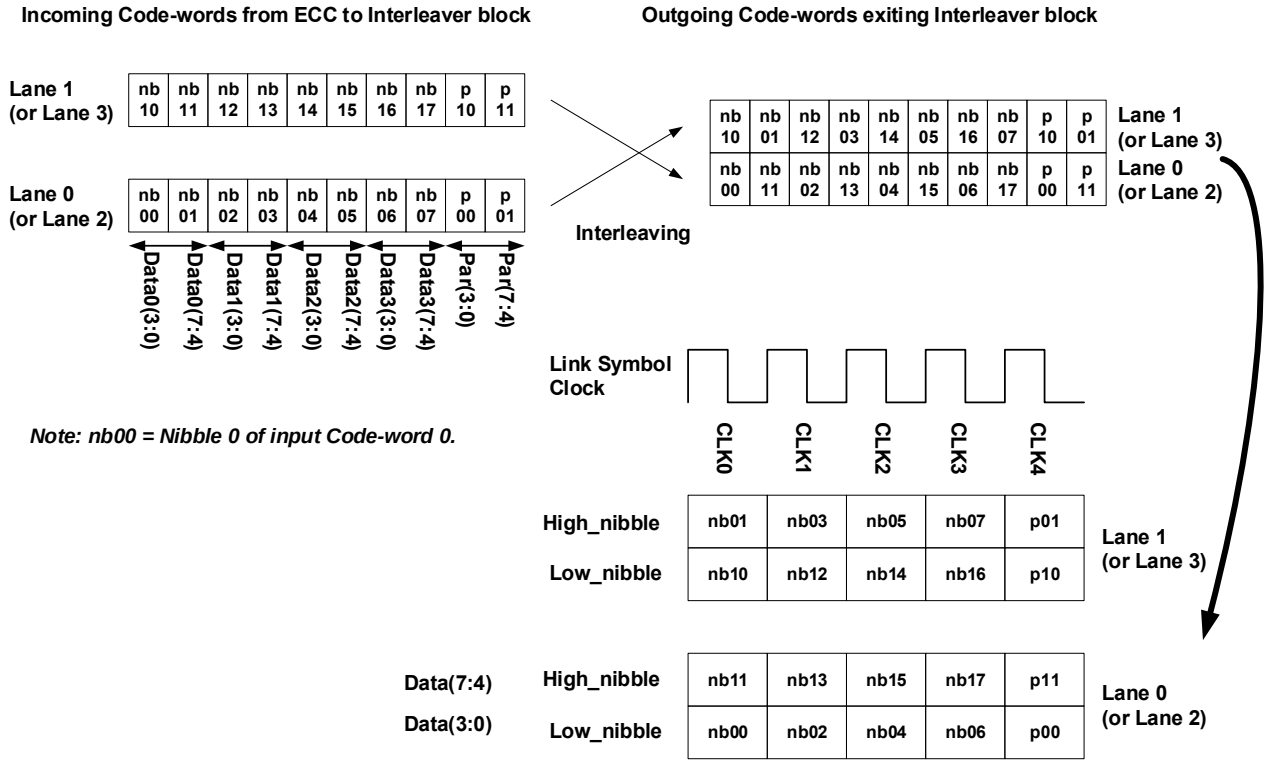


Figure 2-48: ECC Block Nibble-Interleaving for 4- and 2-Lane Main-Links (Payload)

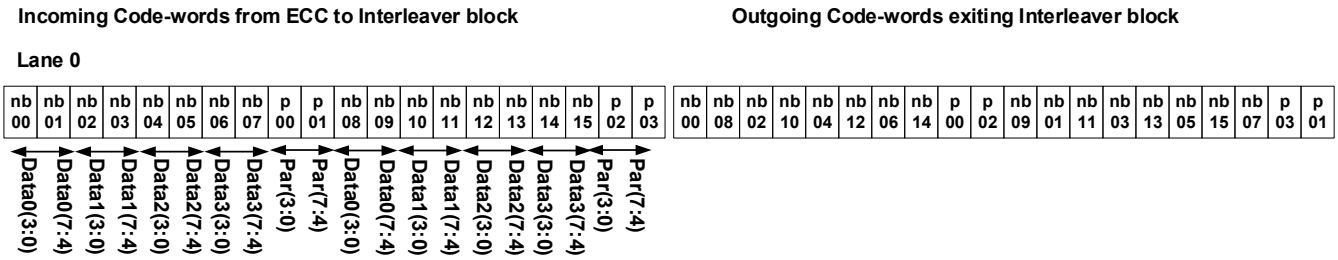


Figure 2-49: ECC Block Nibble-Interleaving for 1-Lane Main-Link (Payload)

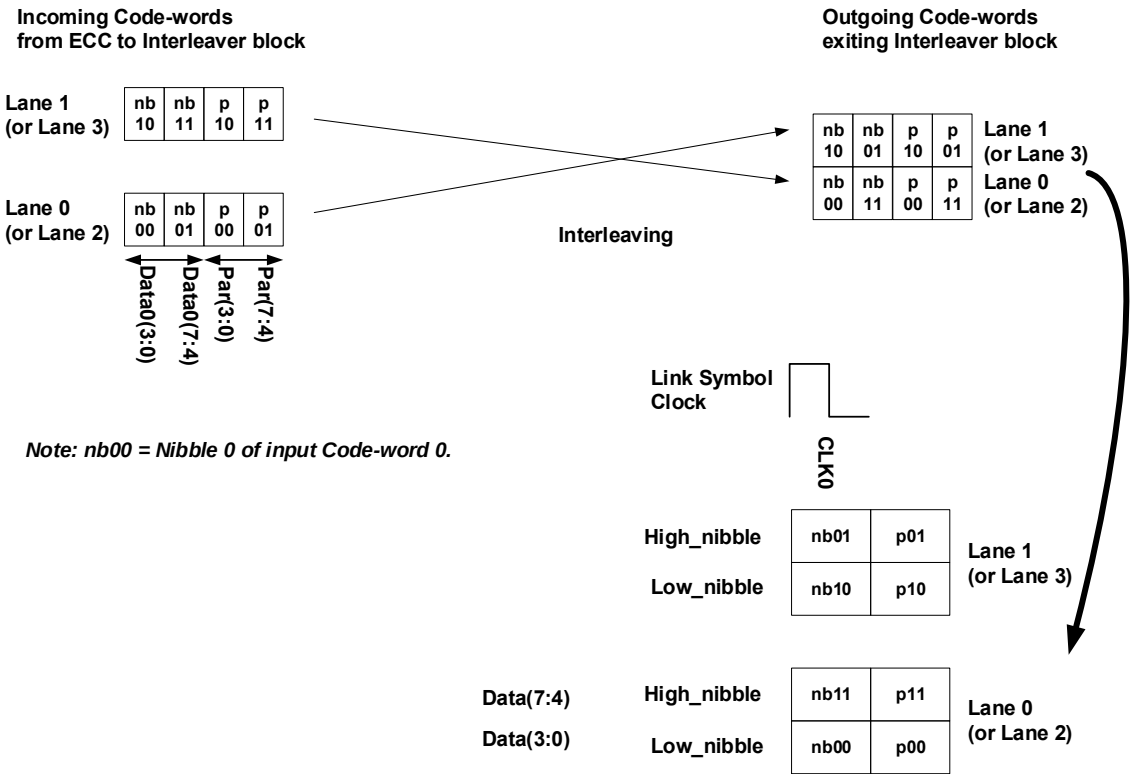


Figure 2-50: ECC Block Nibble-Interleaving for 4- and 2-Lane Main-Links (Header)

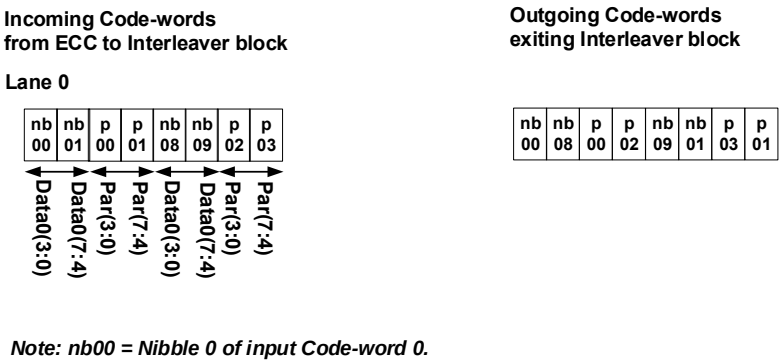


Figure 2-51: ECC Block Nibble-Interleaving for 1-Lane Main-Link (Header)

Note: *nb00 is the lowest nibble of HB0, nb01 is the highest nibble of HB0, nb08 is the lowest nibble of HB1, and nb09 is the highest nibble of HB1.*

Because the symbol size is a nibble (4 bits wide), the code-word length is 15 nibbles (= $2^4 - 1$) within the ECC block.

For packet payloads, two parity nibbles (or one byte) shall be generated for eight data nibbles (or four bytes) for the packet payload per lane, as illustrated in Figure 2-52. Only 10 nibbles consisting of eight data nibbles and two parity nibbles shall be used. The remaining most significant five nibbles shall be zero-padded, and shall **not** be transmitted over a DP link.

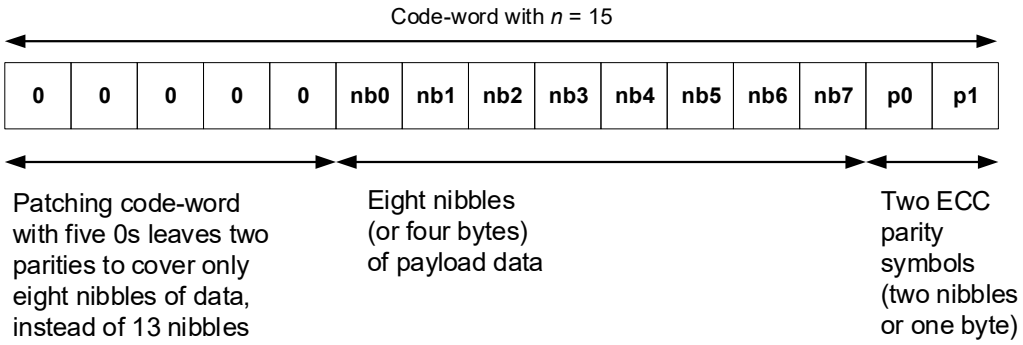


Figure 2-52: 15-nibble Code-word for Packet Payload

For the packet header, four of the 15 nibbles shall be used as illustrated in Figure 2-53. Those four nibbles consist of two data (i.e., packet header) nibbles and two parity nibbles. The remaining most significant 11 nibbles shall be zero-padded, and shall **not** be transmitted. With this protection, the ECC block is capable of correcting a 2-byte error within a 4-byte packet header.

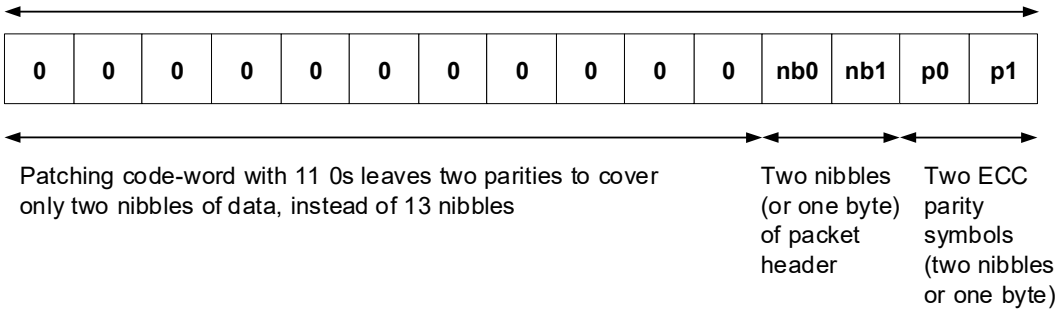


Figure 2-53: 15-nibble Code-word for Packet Header

2.2.6.4 Corrective Action in the Event of Three or More Symbol Errors (Informative)

The ECC method described above **cannot** correct the errors when there are three or more symbol errors. Corrective action by a Sink device in case such an error condition is encountered is an implementation-specific choice and beyond the scope of this Standard.

2.3 AUX_CH States and Arbitration

2.3.1 AUX_CH States Overview

The AUX_CH is a half-duplex, bidirectional channel. A DP device with a DPTX (e.g., a Source device) is the AUX_CH's master (referred to as an "AUX_CH Requester"). A DP device with a DPRX (e.g., a Sink device) is the AUX_CH's slave (referred to as an "AUX_CH Replier"). As the master, the Source device shall initiate a Request transaction, to which the Sink device shall respond with a Reply transaction.

Upon detecting the DPRX through the Hot Plug Detect mechanism, as described in Section 3.1.3.2, the DPTX shall place its AUX_CH in the AUX IDLE state, S2. (See Figure 2-54.) The DPRX shall also be in the AUX IDLE state, D1 (see Figure 2-55), when it asserts the HPD signal.

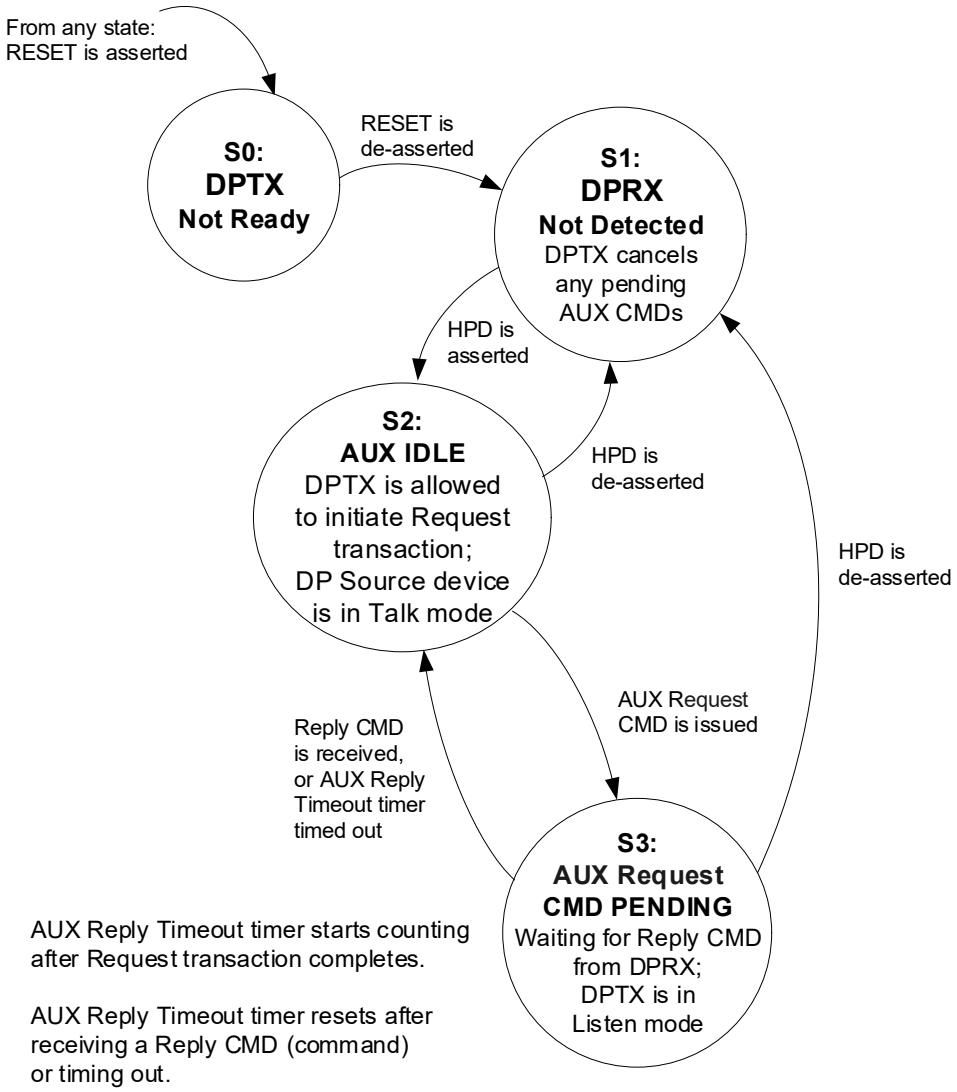
The Sink device may monitor for whether a DPTX is present. If the Sink device is monitoring for DPTX presence, the Sink device may enter the AUX IDLE state only when the DPTX is detected.

In state S2, the DPTX shall be in Talk mode and issue a Request command, as needed. The DPRX, in state D1, shall be in Listen mode, waiting for a Request command.

After issuing a Request transaction, the DPTX shall transition to state S3, the AUX Request CMD Pending state. In the S3 state, the DPTX shall be in Listen mode, waiting for the DPRX to reply. Upon receiving a Request transaction, the DPRX shall go to state D2, the AUX Reply CMD Pending state. Once in the D2 state, the DPRX shall be in Talk mode, ready to reply over the AUX_CH.

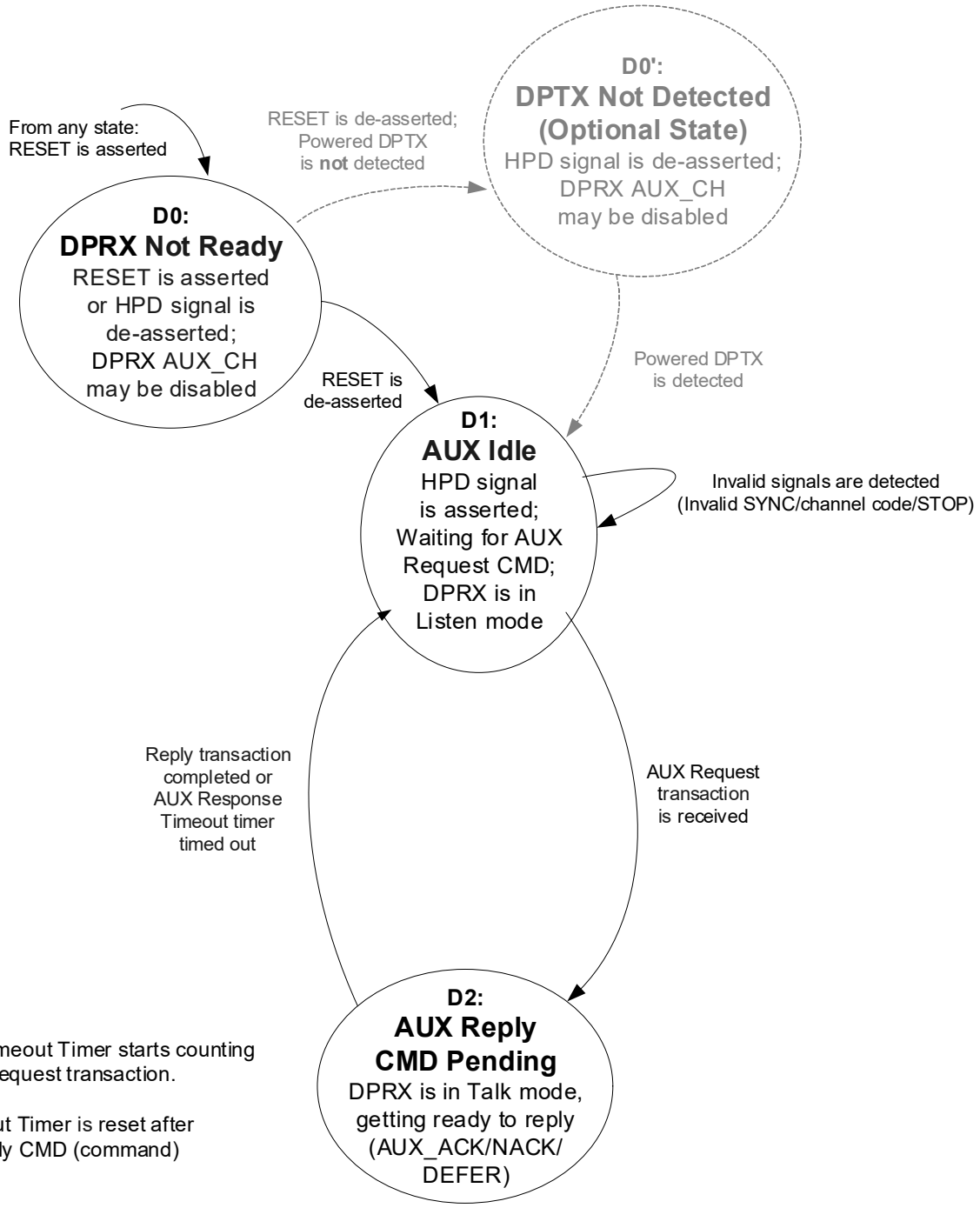
The DPRX shall reply within the maximum AUX Response Timeout timer period after receiving a Request transaction. If the DPRX is unable to reply within the AUX Response Timeout timer period, the DPRX shall return to the D1 state without replying. The DPTX shall wait for up to the maximum AUX Reply Timeout timer period after entering S3. If a reply is not received within the AUX Reply Timeout timer period, the DPTX shall return to S2 and be allowed to initiate a Request transaction, as needed. (See Section 2.11.2 for details regarding timeout timer periods.)

Transitions from D0 to D1 through the D0' state may be used by DPRXs that implement optional DPTX-detect functionality. In the D0' state, RESET is de-asserted from the DPRX; however, the DPTX is not detected.



Note: *The Policy Maker may disable the DPTX.*
After being re-enabled, the DPTX enters the S0 state.

Figure 2-54: DPTX AUX_CH State Diagram



AUX Response Timeout Timer starts counting after receiving a Request transaction.

AUX Reply Timeout Timer is reset after transmitting a Reply CMD (command) or timing out.

Note: *If the HPD signal is de-asserted, D0 shall always be the next state.*

Figure 2-55: DPRX AUX_CH State Diagram

2.3.1.1 DP Source Device DP_PWR State Rules

For cases in which the DP_PWR pin is enabled to supply power, Table 2-129 lists the DP_PWR state rules in conjunction with the DPTX AUX_CH state illustrated in Figure 2-54 for a DP Source device.

Table 2-129: DP Source Device DP_PWR State Rules

DP_PWR State	Rules
S0	Source device may disable DP_PWR: • Source device is either OFF (or reset) or not monitoring HPD • Source device may go to the S1 state at any time
S1	Source device shall enable DP_PWR: • Source device is monitoring HPD signal status • Source device goes to the S2 state when the HPD signal is present • Source device may go to the S0 state at any time
S2 and S3	Source device shall enable DP_PWR: • Source device is either transmitting or ready to transmit (after link training) bits over the Main-Link • Source device goes to the S1 state when the HPD signal is absent • Source device may go to the S0 state at any time

2.3.1.2 DP Sink Device DP_PWR State Rules

Table 2-130 lists the DP_PWR state rules in conjunction with the DPRX AUX_CH state illustrated in Figure 2-55 for a DP Sink device.

Table 2-130: DP Sink Device DP_PWR State Rules

DP_PWR State	Rules
D0	Sink device may disable DP_PWR: • Sink device is OFF (or reset) or not monitoring Source Detection signal • Sink device de-asserts HPD signal • Sink device may go to D1 state at any time • Sink device may go to D0' state if it supports Source Detect feature and Source device is not detected
D0'	Sink device shall enable DP_PWR (for a tethered Sink device, upon detecting DP_PWR Consumer): • Sink device de-asserts HPD signal, but monitors Source Detect status • Sink device goes to D1 when Source detected • Sink device may go to D0 state at any time
D1 and D2	Sink device shall enable DP_PWR (for a tethered Sink device, upon detecting DP_PWR Consumer): • Sink device asserts HPD signal • Sink device is either receiving or ready to receive bits over Main-Link • Sink device goes to D0' state when Source is absent • Sink device remains in D1 even when Source writes 010 to the SET_POWER_STATE field in the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h,bits 2:0) • Sink device may go to D0 state at any time

A Sink device may be in a power-saving state even in the D1 state when it is not receiving bits over the Main-Link. In a power-saving state, the Sink device may place itself in one of the following conditions:

- **Main-Link Receiver is disabled** – Different signals parked at V_{BIAS_RX}
- **AUX_CH Receiver is monitoring differential signals** – Sink device shall be ready to reply upon differential signal detection within 1ms

2.3.2 Link Layer Arbitration Control

As described above, the Source and Sink devices shall **not** be in Talk or Listen mode at the same time. Furthermore, the Sink device's AUX Response Timeout timer period shall be shorter than the Source device's AUX Reply Timeout timer period. If a timeout occurs, the Source and Sink devices shall both return to the AUX IDLE state (i.e., Talk mode for the Source device, and Listen mode for the Sink device). Therefore, contention and live lock shall be avoided.

2.3.3 Policy Maker AUX Services

There are multiple applications and services that initiate AUX transactions. Some examples are:

- AUX Link Services
  - Receiver capability read
  - Link configuration (training)
  - Link status read
- AUX Device Services
  - DisplayID or legacy EDID read
  - MCCS (Monitor Control Command Set) control

The AUX_CH shall **not** support nested transactions (i.e., one transaction shall end before another transaction can be initiated). The Policy Maker shall determine the order in which the multiple AUX Request transactions are executed per their priorities. The Link Layer shall merely initiate AUX transaction as it receives the request from the Policy Maker.

A request transaction may not end in full-completion. The Sink device may reply with NACK or DEFER when not ready for full-completion. The Policy Maker shall decide on the follow-up action if the Request transaction is replied to with a NACK or DEFER.

The amount of data transported over the AUX_CH per transaction shall be limited to 16 or fewer bytes (i.e., the burst size shall be 16 data bytes maximum). This limitation is set to prevent a single transaction from monopolizing the bus for an extended period of time. No transaction shall occupy the AUX_CH for more than 500us. If a given transaction needs to transport more than 16 bytes of data, the Policy Maker shall divide the transaction into multiple transactions, each of which shall be no larger than 16 bytes.

2.3.4 Detailed DPTX AUX_CH State and Event Descriptions

Table 2-131: DPTX AUX_CH State and Event Descriptions

State/Event	Description
S0: Reset	State S0 shall be entered from any state when RESET is asserted.
S1: AUX_CH Unplugged	The HPD signal is de-asserted (low state). Upon entry, the HPD signal level shall be passed up to the Link Policy Maker. The DPRX is either not connected or has not asserted the HPD signal. The AUX_CH is unavailable. Therefore, AUX_CH services such as DPCD, DisplayID or legacy EDID, etc., are **not** available.
S2: AUX_CH IDLE	The HPD signal is asserted (high). The DPRX is connected to either its main power supply or trickle power; however, the DPRX's power switch (if any) state is not specified. A message indicating that the AUX_CH is available shall be passed up to the Policy Maker. In this state, no AUX Command is pending and the AUX_CH is available for the Policy Maker to initiate request transactions. The Source device shall remain in Talk mode until a request transaction has completed according to the AUX_CH syntax specified in this section. After transmitting STOP, the last part of a request transaction, the DPTX shall transition to State S3, provided that HPD is still asserted.
S3: AUX Request CMD PENDING	Upon completion of an AUX request transaction, the DPTX AUX_CH shall enter State S3. In this state, the DPTX is waiting to receive a Reply message from the DPRX. The DPTX shall not issue commands in this state. The DPTX AUX_CH shall remain in Listen mode. After entering this state, the AUX Reply Timeout timer shall reset and start counting. (See Section 2.11.2 for AUX Reply Timeout timer period.) The DPTX AUX_CH shall exit from this state and enter State S2, AUX IDLE state, when it receives the Reply Command from the DPRX, or when the AUX Reply Timeout timer times out. If the AUX Reply Timeout timer times out, the DPTX shall retry at least three times because no reply may be due to the DPRX waking from a power-saving state, which may take up to 1ms.
Transition from any State to S0	Occurs when RESET is asserted.
Transition S0:S1	Occurs when RESET is de-asserted.
Transition S1:S2	Occurs upon Hot Plug Detection.
Transition S2:S1 or S3:S1	Occurs upon Hot Plug Detection.
Transition S2:S3	Occurs upon the completion of DPTX AUX Request Transaction.
Transition S3:S2	Occurs when the DPTX AUX_CH receives a Reply Command from the Sink device, –or– when the AUX Reply Timeout timer times out.

2.3.5 Detailed DPRX AUX_CH State and Event Descriptions

Table 2-132: DPRX AUX_CH State and Event Descriptions

State/Event	Description
D0: DPRX Not Ready	The DPRX shall transition to this state from any other state when RESET is asserted. In this state, the HPD signal is de-asserted. The DPRX AUX_CH may be disabled. Upon RESET de-assertion, the DPRX shall transition to the D1 state, unless DPTX detection is implemented, in which case the DPRX shall transition to the D0' state.
D0': DPTX Not Detected	Optional state in which a DPRX can monitor for DPTX presence. When RESET is de-asserted and HPD signal is asserted and the DPTX is not detected, this optional state may be entered. Upon detection of the DPTX, the DPTX shall transition to D1.
D1: AUX_CH Idle	In this state, the DPRX AUX_CH shall remain in Listen mode, waiting for the DPTX to transmit an AUX Request Command over the AUX_CH. The DPRX AUX_CH shall also remain in this state after an invalid signal (e.g., invalid SYNC, STOP, or channel code) is received. Upon receiving an AUX request transaction command from the DPTX, the DPRX AUX_CH shall transition to the D2 state and its AUX Response Timeout timer shall reset and start counting. In Listen mode, a DPRX shall either receive and decode the request transaction, –or– detect the presence of a differential signal input, even if the DPRX is in a power-saving state. If the DPRX is in a power-saving state and cannot reply within the AUX Response Timeout timer period, the DPRX shall exit the power-saving state within 1ms of detecting the presence of a differential signal input so that it can provide an AUX reply within three AUX transaction retries by the DPTX. (See Section 2.11.2 for AUX Response Timeout timer period.) A DPRX shall avoid not issuing a reply except when waking from a power-saving state.
D2: AUX Reply CMD Pending	In this state, the DPRX shall be in Talk mode, getting ready to reply to the DPTX. Upon completion of the reply transaction, the DPRX shall transition to the D1 state. If the AUX Response Timeout timer times out, the DPRX shall transition to the D1 state without initiating a reply transaction.
Transition of D0: D0' (Optional transition)	Occurs when RESET is de-asserted and HPD signal is asserted.
Transition of D0':D1 (Optional transition)	Occurs upon DPTX detect, after the optional D0' state is entered.
Transition of D0:D1	Occurs when RESET is de-asserted and when the DPRX has asserted the HPD signal and is ready to serve for services over the AUX_CH.
Transition of D1:D2	Occurs upon receiving an AUX Request transaction from the DPTX.
Transition of D2:D1	Occurs when the Sink device completes its reply to the DPTX, or the DPRX fails to reply before the AUX Response Timeout timer times out.

2.4 DP Multi-stream Isochronous Transport Service Overview

Note: *This section is applicable to both 8b/10b Link Layer and 128b/132b Link Layer.*

DP Isochronous Transport Service, based on micro-packet architecture, transports the audio and video streams from a Stream Source to a Stream Sink by way of DP link(s), as illustrated in Figure 2-56.

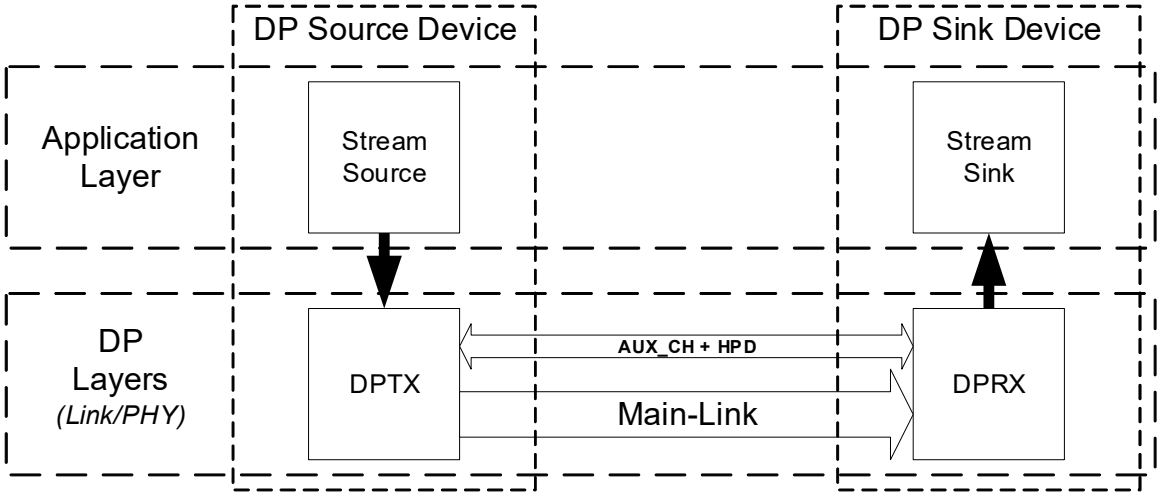


Figure 2-56: DP Data Transport Channels

This section provides an overview of the multi-stream Isochronous Transport Service extension. The multi-stream extension enables the transport of multiple streams from multiple stream Sources in one or more DP Source devices to multiple Stream Sinks in one or more DP Sink devices connected by way of DP Branch devices, as illustrated in Figure 2-57. This is in contrast with Single-Stream Transport (SST) mode, which is limited to transport of a single main video stream and optional SDP stream, as described in Section 2.2.

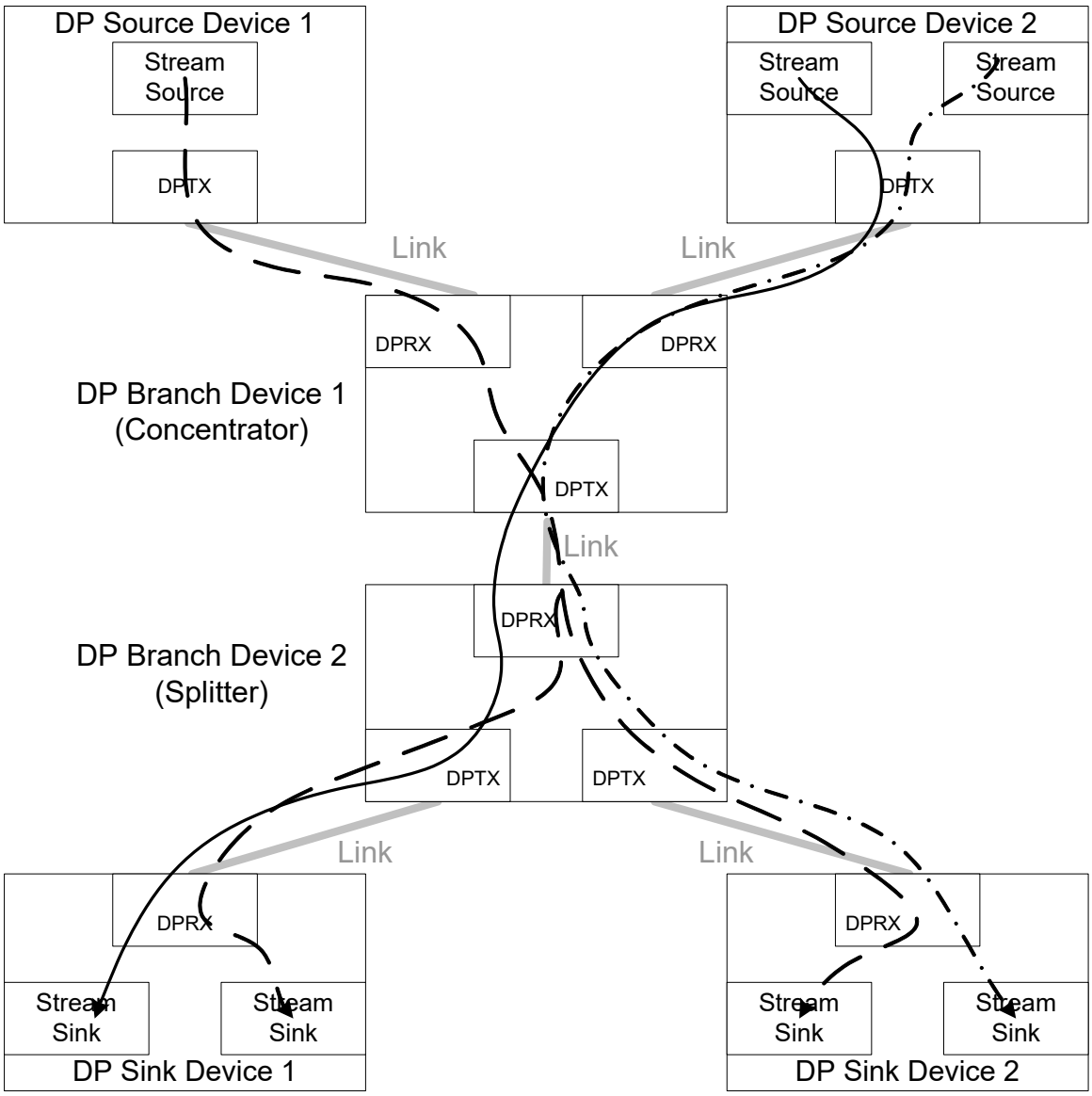


Figure 2-57: DP MST

2.4.1 Connection-oriented Transport

The DP Isochronous Transport Service is a connection-oriented transport providing for management of stream transfer from a Stream Source device to a Stream Sink device, independent of the actual underlying stream transport mechanisms.

Virtual Channel is an end-to-end, direct virtual connection between a Stream Source device and a Stream Sink device. On the underlying DP Layers level, multiple links (referred to as "path") may need to be traversed to achieve the Virtual Channel connection, as illustrated in Figure 2-58. Over each link, the Virtual Channel is mapped to a payload referred to as "VC Payload" of the micro-packet.

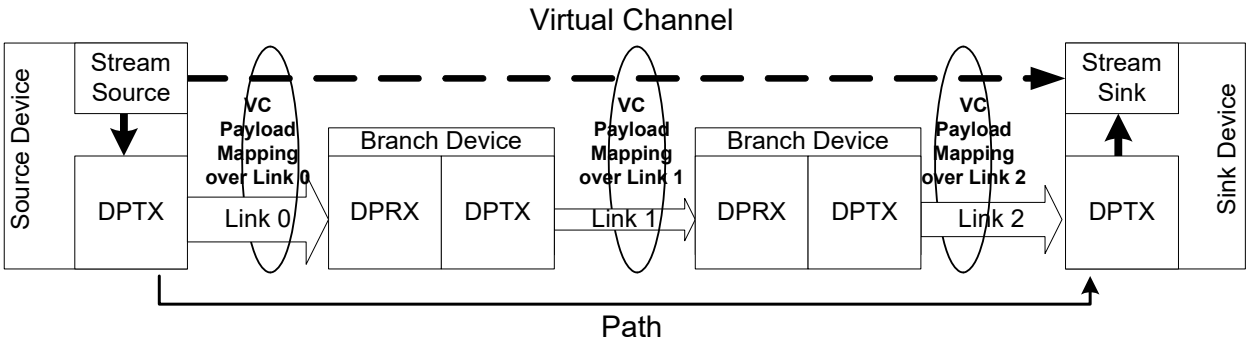


Figure 2-58: Illustration of Virtual Channel, Link, and Path

The end-to-end, direct-connection nature of Virtual Channel becomes more apparent when there are multiple Stream Sinks and multiple Stream Sources, as illustrated in Figure 2-59 and Figure 2-60. In the Dual Display Clone example illustrated in Figure 2-59, Link1 between the DP Source Device and DP Branch Device1 carries a single payload for the single Stream Source device. In the Extended Desktop example illustrated in Figure 2-60, Link1 between the DP Source Device with two Stream Sources and the DP Branch Device1 carries two payloads – one for Stream Source1 and the other for Stream Source2.

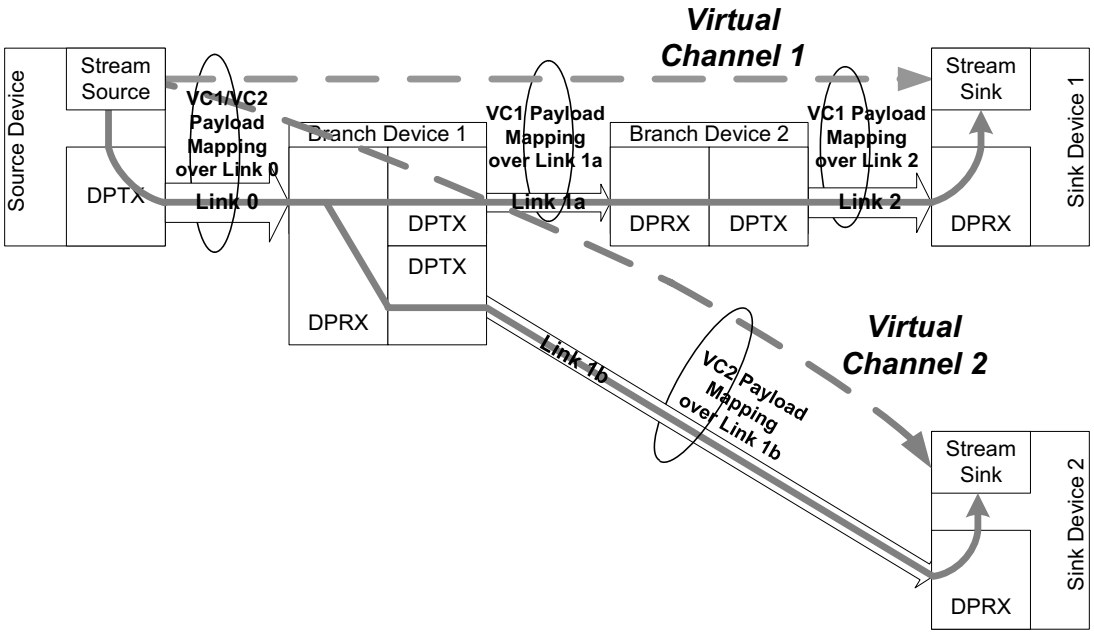


Figure 2-59: Single-Stream Source Device to Dual-Stream Sink Devices (Dual-Display Clone)

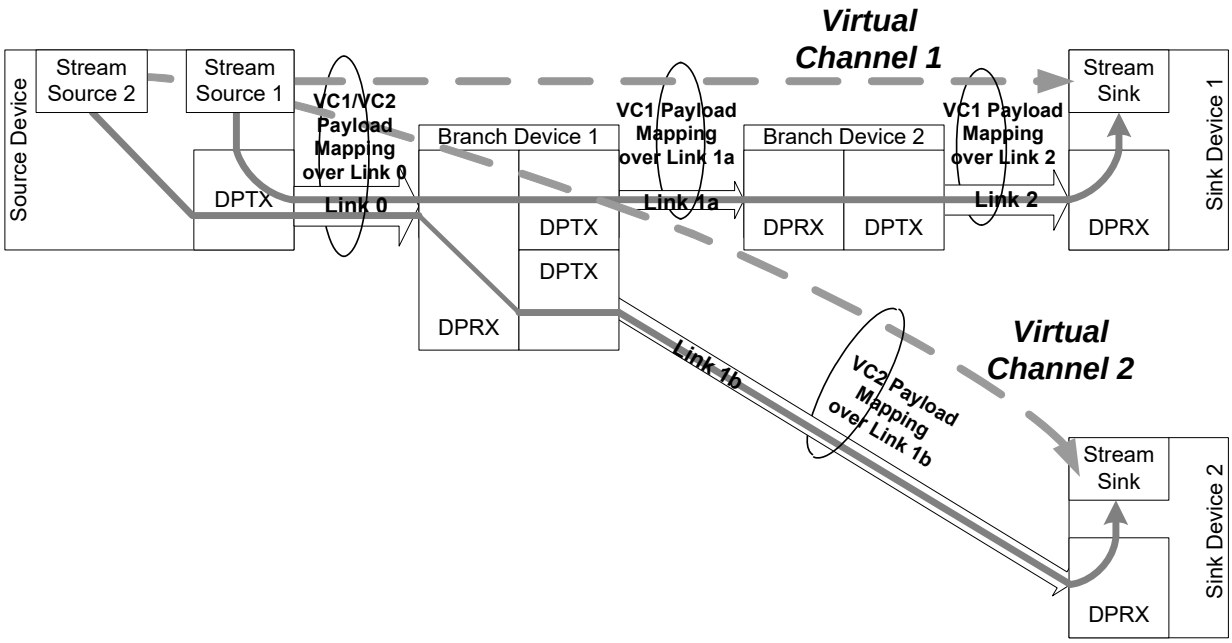


Figure 2-60: Dual-Stream Source Devices to Dual-Stream Sink Devices (Extended Desktop)

2.4.2 DP Isochronous Transport Service Layers

The Isochronous Transport Service uses the sideband communications over Sideband CH (AUX_CH and HPD) for managing the topology/virtual channel connection/Main-Link and performs Main-Link symbol mapping. The services provided within each layer differ between single-stream-only and multi-stream-capable devices, with multi-stream-capable devices generally providing a functionality superset.

The Single-stream-only and Multi-stream Isochronous Transport Service Layers are illustrated in Figure 2-61 and Figure 2-62, respectively, and briefly described in the remainder of this section.

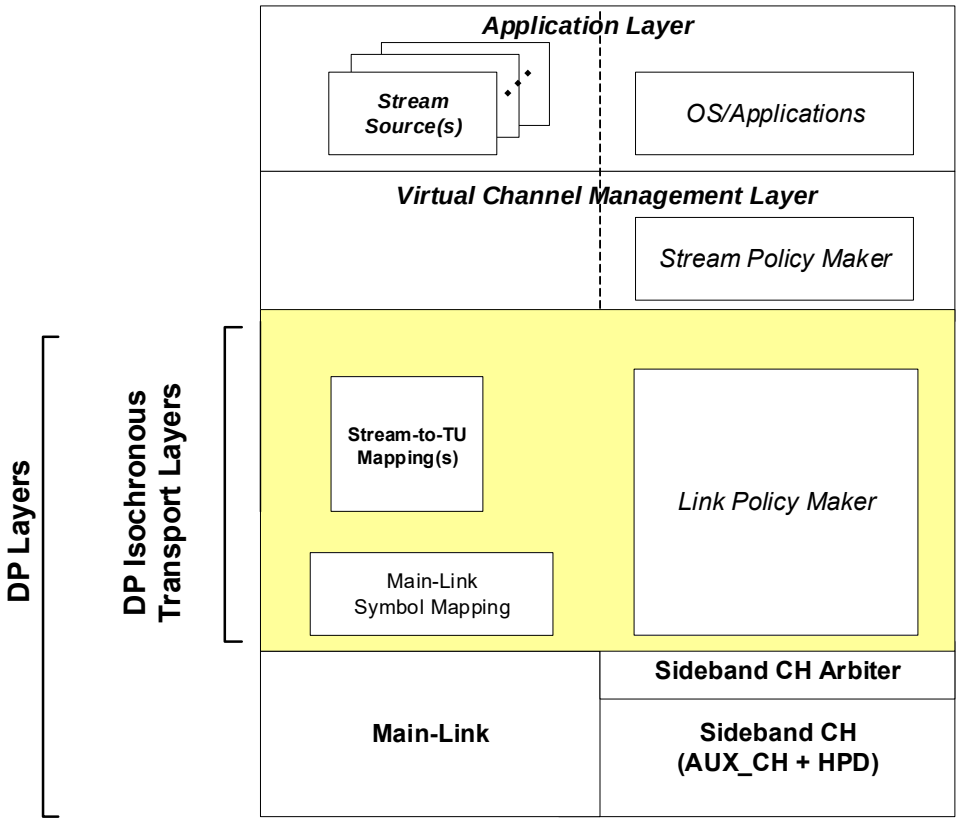


Figure 2-61: Single-stream-only Isochronous Transport Service Layers

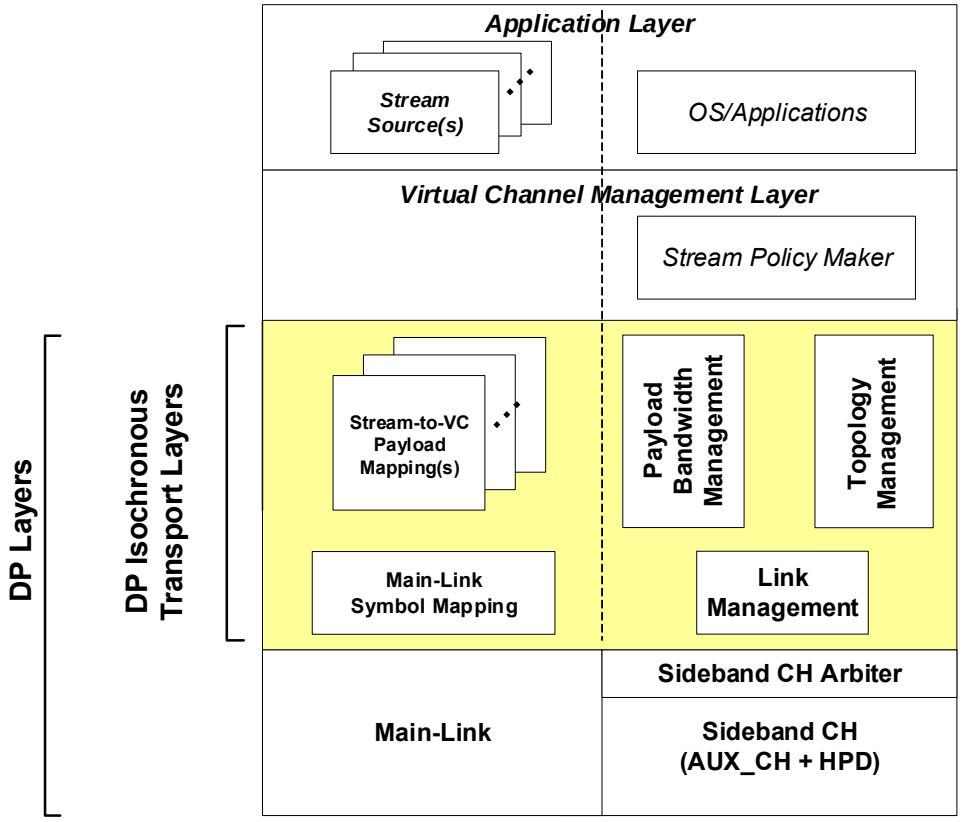


Figure 2-62: Multi-stream Isochronous Transport Service Layers

Layers above the DP Isochronous Transport Service Layers (i.e., Virtual Channel Management and Application Layers) are application-/implementation-specific, and are therefore beyond the scope of this Standard. This Standard refers to the implementation guidelines of the Stream/Link Policy Maker.

2.4.2.1 Topology Management Layer

- Present in every DP multi-stream device (i.e., a device that has a DPTX and/or DPRX, also referred to as a "DP node").
- Added for Multi-stream Isochronous Transport Service; not present in SST mode.
  A multi-stream-capable device transmitting in SST mode still provides for this function.
  - Topology Manager in a DP Source device discovers and maintains the topology by way of sideband communication.
  - Topology Assistant in a DP Branch device provides topology information to the Topology Manager by way of sideband communication.

2.4.2.2 Payload Bandwidth Management Layer

- Present in every DP multi-stream Source device and Branch device that has a DPTX.
- Added for Multi-stream Isochronous Transport Service; not present in SST mode. A multi-stream-capable device transmitting in SST mode still provides this function.
- Avoids the overflow of the buffer in the path from the stream source in a DP Source device to the Stream Sink in a DP Sink device.
  - Source Payload Bandwidth Manager in a DP Source device receives the stream bandwidth, calculates Payload Bandwidth Number (PBN) corresponding to the stream bandwidth, forwards the PBN value by way of sideband communication, and sets the VC Payload Bandwidth of its own downstream link by allocating sufficient time slots to the VC Payload.
  - Branch Payload Bandwidth Manager in a DP Branch device receives and forwards the PBN by way of sideband communication, and sets the VC Payload Bandwidth of its own downstream link by allocating sufficient time slots to the VC Payload.
  - Instructs the Main-Link Symbol Mapping Layer how many time slots to allocate to a VC Payload Allocation and when to enable/disable insertion of Stream symbols from VC Payload Mapping Layer into a VC Payload.

2.4.2.3 Link Management Layer

- Present in every multi-stream DPTX and DPRX.
- Present in MST and SST modes (referred to as “Link Policy Maker” in single-stream-only devices).
- Establishes and maintains Main-Link through link training and link maintenance.
  - DPTX’s Link Management Layer instructs the Main-Link Symbol Mapping Layer to transmit link training pattern sequences and, after link training is successful, to transmit micro-packets (referred to as “Multi-stream Transport Packets” (MTPs)) to keep the link enabled; also monitors the status of the DPRX that it is driving.
  - DPRX’s Link Management Layer provides for ADJUST_REQUEST for DPTX drive setting optimization during Link Training, and maintains up-to-date link status, generating an IRQ_HPD pulse when it needs the DPTX Link Management Layer’s attention.

2.4.2.4 Main-Link Symbol Mapping Layer

- Present in every DPTX and DPRX.
- Enhanced for Multi-stream Isochronous Transport Service.
  - Main-Link Symbol Mapping Layer of a DPTX transmits link training pattern sequences and MTP symbols, as instructed by the Link Management Layer; also allocates time slots to a VC Payload and controls the insertion of Stream Symbols coming from the VC Payload Mapping Layer, as instructed by the Payload Bandwidth Management Layer.
  - Main-Link Symbol Mapping Layer of DPRX receives Main-Link symbols and informs its Link Management Layer of the link quality; also keeps VC Payload allocation synchronized with that of the DPTX of the immediate upstream DP device and extracts Stream symbols from incoming MTP symbols.

2.4.2.5 VC Payload Mapping Layer

- Present per stream.
- Present in MST and SST modes (Stream-to-TU Payload Mapping Layer).
  - VC Payload Mapping Layer in a DP Source device receives the stream (both data and control) from a stream source and converts it to stream symbols inserted into VC Payload.
  - VC Payload Mapping Layer in a DP Sink device regenerates the stream from incoming stream symbols.
  - VC Payload Mapping Layer in a DP Branch device passes through incoming Stream symbols from its upstream DPRX to its downstream DPTX in a manner that is agnostic to stream data format/symbol type/lane count (i.e., no symbol parsing needed).
  - If the first (or most upstream) DP Branch device is receiving Main-Link symbols from a DP SST Source device, the VC Payload Mapping Layer of that DP Branch device shall perform more than stream symbol pass-through. How to perform the single-stream-to-multi-stream symbol conversion is implementation-specific.
    - If the last (or most downstream) DP Branch device is driving a DP SST Sink device, the VC Payload Mapping Layer of that DP Branch device shall perform more than stream symbol pass-through. How to perform the multi-stream-to-single-stream symbol conversion is implementation-specific.

2.4.3 Sideband CH Communications

As noted above, the Topology Management Layer, Payload Bandwidth Management Layer, and Link Management Layer use Sideband CH communications for management. Sideband CH Communications take place over the AUX_CH and HPD signal lines.

In addition to AUX Transaction between DP device pair across a single link, Message Transaction across any DP device pair over one or more links in the topology is available. Unlike AUX Transaction which is always initiated by an upstream DP device, Message Transaction is full-duplex bidirectional, and can be initiated either by an upstream or downstream DP device.

The Topology Management Layer and Payload Mapping Layer work across the topology, and therefore use Message Transactions for management as well as DPCD access by way of Native AUX Transactions. Link Management is across a single link between DPTX and DP Sink, and uses DPCD access only.

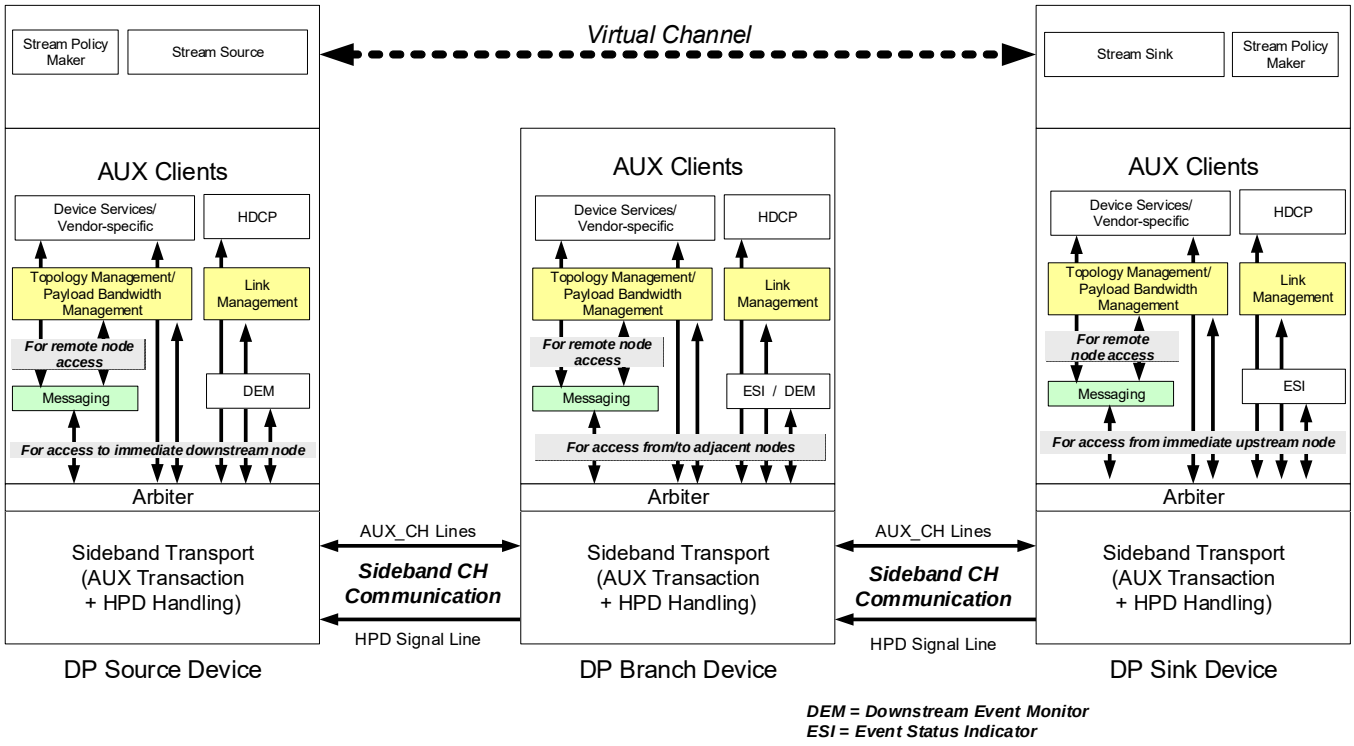


Figure 2-63: Sideband CH Communication Layers

2.5 Topology Management Layer

Note: *This section is applicable to both 8b/10b Link Layer and 128b/132b Link Layer.*

The Topology Management Layer using Messaging AUX Client, covered in Section 2.14, helps the Topology Manager in a DP Source device (optional in DP Sink device) determine what devices are in the topology.

This section consists of the following sub-sections:

- Section 2.5.1 – Primitives of Multi-stream DP Devices and Device Types

  Primitives of the DP multi-stream devices are DPTX, DPRX, branching unit, stream source, and stream sink. multi-stream DP Branch, Source, Sink, and Composite devices are composed of various combinations of these primitives.

- Section 2.5.2 – Multi-stream Topologies

  DP Branch devices of multi-stream topology need to be multi-stream devices supporting Topology Management while the “end” device (DP Source device, DP Sink device, and protocol converter) may be either a multi-stream or single-stream device.

- Section 2.5.3 – Multi-Stream Device Identification

  A multi-stream device with a branching unit is identified with Globally Unique Identifier (GUID) and Relative Address (RAD). An end device that does not have a branching unit is identified as a “peer device” connected to one of the ports of the multi-stream device with a branching unit. A DP device with a DPCD r1.2 (or higher) DPRX shall have the GUID register (DPCD Addresses 00030h through 0003Fh).

- Section 2.5.4 – Topology Manager and Topology Assistant

  Topology Management is conducted through the collaboration between Topology Manager in a DP multi-stream Source device (optionally in DP MST Sink device) and Topology Assistant in a multi-stream device with a branching unit.

- Section 2.5.5 – Topology Discovery

  Topology Manager obtains information about the topology by using Native AUX transactions and a LINK_ADDRESS message transaction messaging AUX client. (Messaging AUX Client is covered in Section 2.14.) The amount of information obtained about the topology and use of the information is Topology Manager implementation-specific.

- Section 2.5.6 – Topology Maintenance

  Topology Manager receives notifications when DP devices and legacy devices are connected and disconnected from the topology. These notifications are provided by Topology Assistants, using a CONNECTION_STATUS_NOTIFY message transaction messaging AUX client.

- Section 2.5.7 – Topologies with Single-stream-only Source devices

  Topology option with single-stream Source device is restricted.

- Section 2.5.8 – Loop Handling

  Multi-stream Topology Management feature provides for sufficient information for Topology Manager to properly handle a topology with a loop and/or a parallel path.

2.5.1 Primitives of Multi-stream DP Devices and Device Types

Primitives of DP devices are a DPTX, DPRX, branching unit, stream source, and stream sink.

The branching unit shall meet the following mandates:

- Have input and output ports, and be capable of VC Payload routing from the input ports to the output ports.
- Have at least one input port and one output port.
- Have no more than eight physical ports each of which is connected either to DPTX (output port) or DPRX (input port). The physical port numbers of a branching unit are from Port 0h up to Port 7h. The physical input ports, if present, are assigned smaller port numbers than those of the physical output ports.
- Have no more than eight logical ports that are internally connected (and therefore, not connected to a DPTX/DPRX). Logical port numbers of a branching unit are from Port 8h up to Port Fh. The logical input ports, if present, are assigned smaller port numbers than those of the logical output ports.

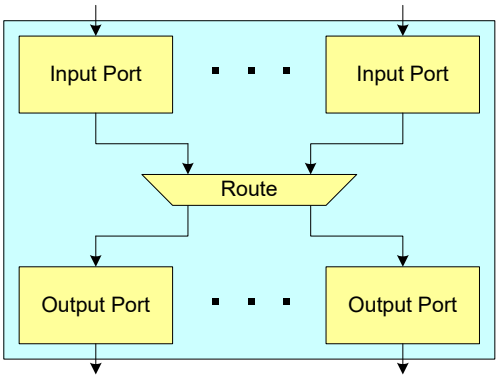


Figure 2-64: Branching Unit

Note: *A PHY Repeater that has only DPTX and DPRX PHY Layer circuits (i.e., DPTX_PHY and DPRX_PHY, respectively) is transparent in DP topology.*

2.5.1.1 Connection between Primitives: Physical Link and Logical Link

The connection between a DPTX and DPRX is referred to as a “physical link.” The connection between a branching unit and a stream source/stream sink/another branching unit is referred to as a “logical link.”

2.5.1.2 DP Source Device

A DP device that has one or multiple stream sources, has one or multiple DPTXs, but does not have a DPRX, is referred to as a "DP Source device."

A DP Source device that supports MST mode is referred to as a "DP multi-stream Source device." A multi-stream Source device shall support Topology Management to play the role of Topology Manager.

2.5.1.3 DP Sink Device

A DP device that has one or multiple stream sinks, has one or more DPRXs, but does not have a DPTX is referred to as a "DP Sink device." The following rules apply for the presence/ absence of a branching unit within a DP Sink device:

- DP Sink device either with single main video stream sinks or with a single main video stream sink and a single SDP stream does not have a branching unit inside.
- DP Sink device that has multiple main video stream sinks has a branching unit inside, whether each main video stream sink has SDP stream sinks. The output port number of the branching unit is assigned to Main/SDP Stream Router of each main video stream sink, as illustrated in Figure 2-65.
- DP Sink device that has a single video stream sink and multiple SDP stream sinks has a branching unit with one input port and one output port, as illustrated in Figure 2-66.
- DP Sink device that does **not** have a main video stream sink, but has multiple SDP stream sinks, has a branching unit with one input port and one output port, as illustrated in Figure 2-67.
- DP Sink device with a branching unit shall support Topology Management as the Topology Assistant. A DP Sink device can choose to play the role of Topology Manager.

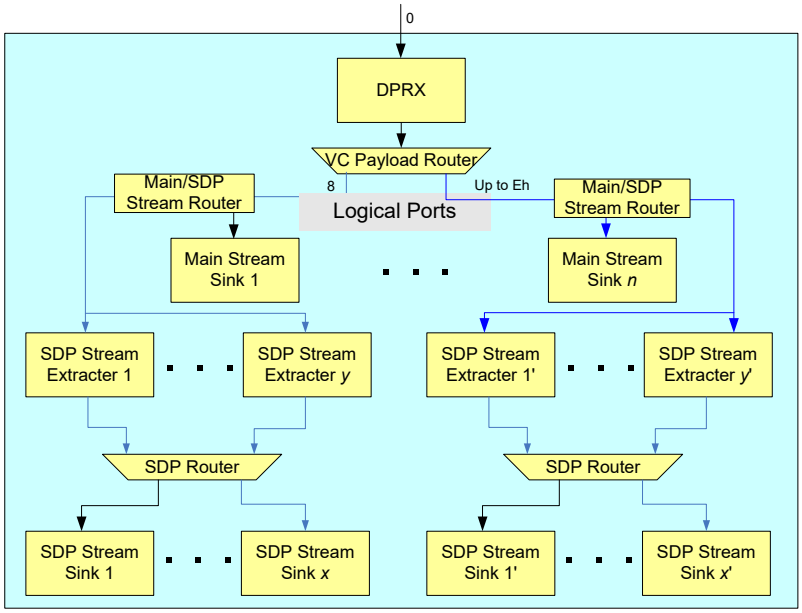


Figure 2-65: Multi-stream Multi-sink Device with Multiple Main Stream Sinks and SDP Sinks

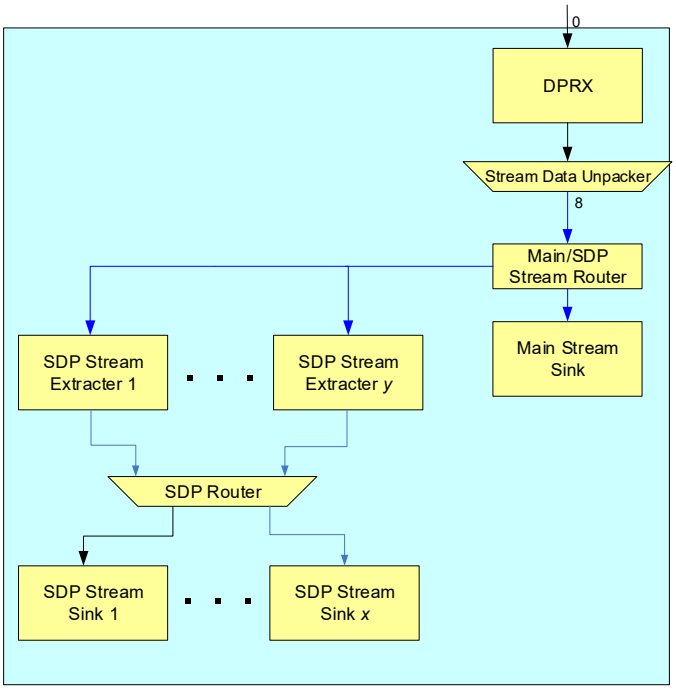


Figure 2-66: Multi-stream Sink Device with Single Main Stream Sink and Multiple SDP Sinks

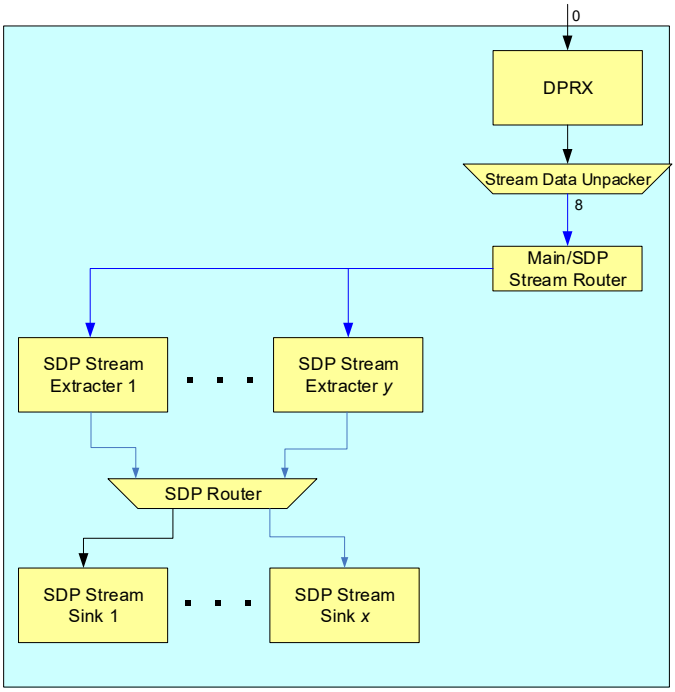


Figure 2-67: Multi-stream Audio-only Sink Device with SDP Sinks

2.5.1.4 DP Branch Device

A DP device that has a branching unit, at least one DPTX, and at least one DPRX, but does not have a stream source/sink is referred to as a "Branch device."

A DP Branch device that supports MST mode is referred to as a "multi-stream Branch device." A multi-stream Branch device shall support Topology Management as the Topology Assistant.

2.5.1.5 DP Composite Device

A DP Branch device with either stream source(s) or stream sink(s) is referred to as a "DP Composite device." The DP Composite device shall support Topology Management as the Topology Assistant.

2.5.2 Multi-stream Topologies

This Standard supports interconnections of DP multi-stream and single-stream devices into topologies. The Branch devices of the multi-stream topology shall be multi-stream Branch devices. Single-stream devices are allowed within the topology only as end devices, such as DP single-stream Source devices and Sink devices.

Topology Management is a multi-stream feature; therefore, Topology Management is **not** supported by single-stream devices. A single-stream device is identified by the Multi-Stream Topology Management Layer as a peer device connected to a multi-stream Branch device.

The maximum number of links between a Stream Source to a Stream Sink shall be 15 or fewer. Of these, the maximum number of physical links is limited to seven. Figure 2-68 illustrates an example multi-stream topology where all DP Source and Branch devices are multi-stream devices that support Topology Management and all DP Sink devices are those that have no branching unit.

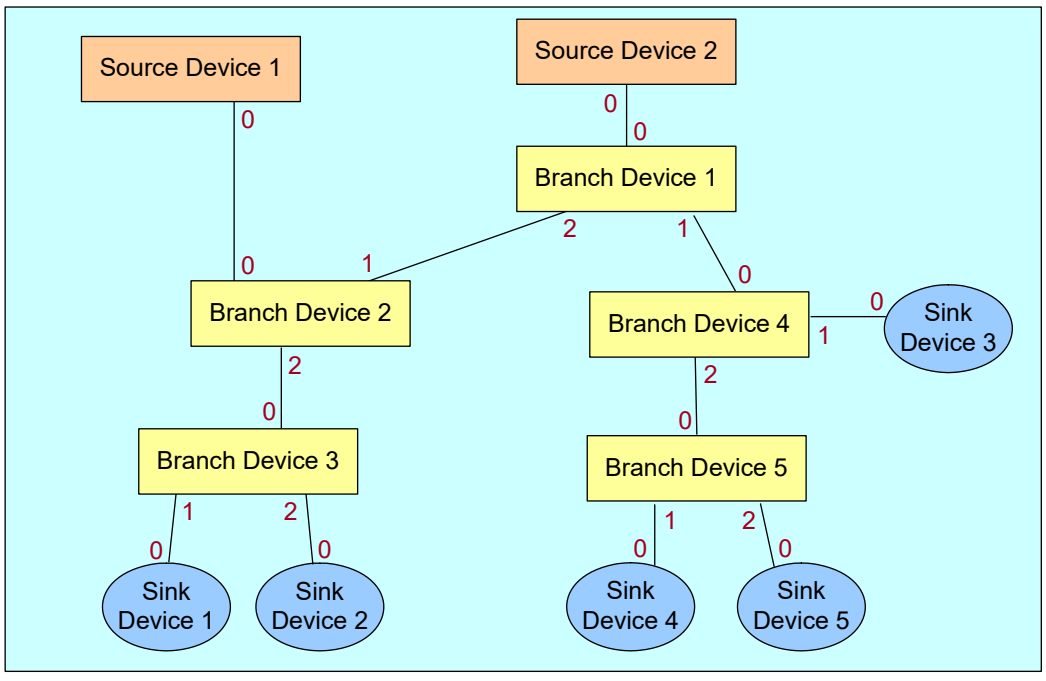


Figure 2-68: Multi-stream Topology Example

2.5.3 Multi-Stream Device Identification

The Topology Management Layer uses GUID and RAD to uniquely identify each DP multi-stream device that has a branching unit within the topology. DP multi-stream devices that do not have a branching unit and single-stream devices and therefore do **not** support Topology Management are thereby identified as peer devices connected to the multi-stream devices' ports with a branching unit.

2.5.3.1 Global Unique Identifier

DP multi-stream devices may perform more than one function. For example, a DP multi-stream Sink device may contain an USB hub. In such cases, the system needs to know that both functions are within the same physical unit.

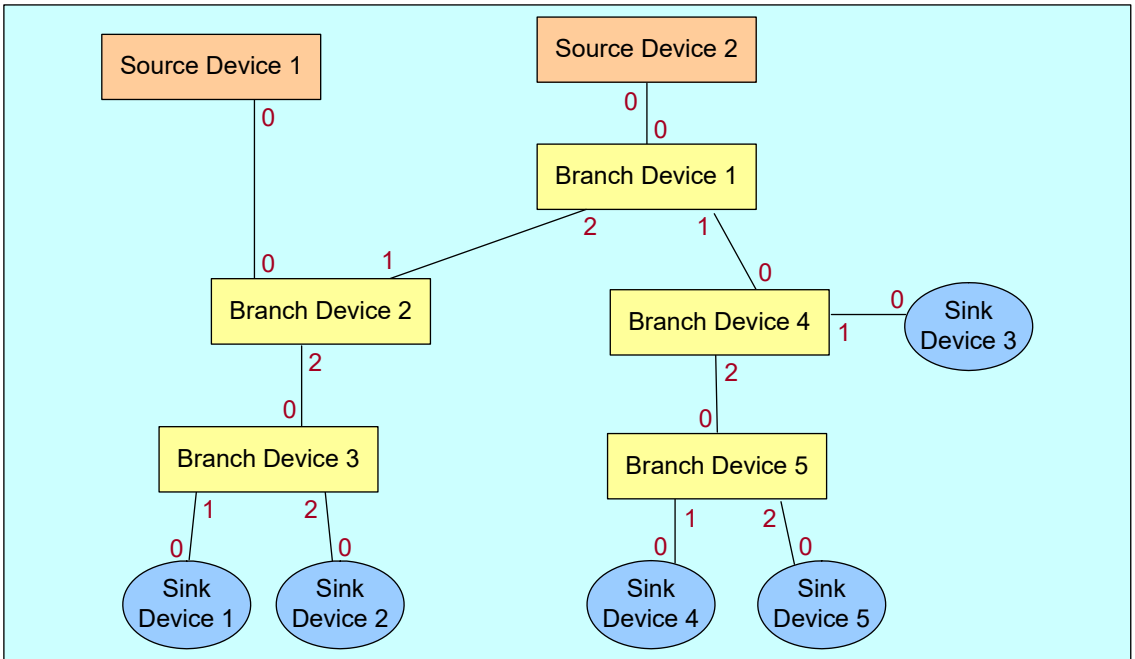
Depending on the topology, it is possible for a single physical device to be accessed through multiple paths. In such situations, the Topology Manager shall be able to infer that the physical device is the same, thereby reducing user confusion within the user interface. The 16-byte GUID, accessible through DPCD access, is used for these identification purposes.

All devices with a DPCD r1.2 (or higher) DPRX shall have the GUID register (DPCD Addresses 00030h through 0003Fh). For devices that have their own unique GUID, the GUID register is Read Only. For devices with DPCD r1.2 (or higher), but the GUID register is all 0s as the power-on reset value, the GUID register is both writable and readable.

In case there is an integrated USB or USB hub device, the GUID shall match the GUID in the Container Descriptor of the integrated USB device or hub. All functions within the physical DP multi-stream device shall report the same GUID.

2.5.3.2 Relative Address

Each DP multi-stream device port is addressable using a relative address. The RAD is relative to the DP multi-stream device. Each RAD is a sequence of port numbers. For visual purposes, each port number is separated by a decimal, “.”. In the example topology in Figure 2-69, Sink 1’s RAD relative to Source 2 is 0.2.2.1. A message from Source 1 shall be transmitted from Port 0 of Source 1, Port 2 of Branch 2, and Port 1 of Branch 3 to reach Sink 1. The RAD of Source 1 relative to Sink 1 is 0.0.0. A message from Sink 1 shall be transmitted from Port 0 of Sink 1, Port 0 of Branch 3, and Port 0 of Branch 2 to reach Source 1. The RAD for all the Sink devices relative to the Source devices in Figure 2-69 is provided in its table.



Relative Address of Devices Accessible from Source Device 1

Device	Relative Address
Branch Device 2	0
Branch Device 3	0.2
Sink Device 1	0.2.1
Sink Device 2	0.2.2

Relative Address of Devices Accessible from Source Device 2

Device	Relative Address
Branch Device 1	0
Branch Device 2	0.2
Branch Device 3	0.2.2
Sink Device 1	0.2.2.1
Sink Device 2	0.2.2.2
Branch Device 4	0.1
Sink Device 3	0.1.1
Branch Device 5	0.1.2
Sink Device 4	0.1.2.1
Sink Device 5	0.1.2.2

Figure 2-69: Example Topology with RAD of Devices Relative to Source Devices

2.5.4 Topology Manager and Topology Assistant

The Topology Management Layer in a multi-stream Source device (or optionally in a multi-stream Sink device) is referred to as the "Topology Manager." The Topology Management Layer in a multi-stream device with a branching unit is referred to as the "Topology Assistant."

2.5.4.1 Topology Manager

The Topology Manager shall generate and maintain the "DP device to RAD" table. The Topology Manager uses local Native AUX transactions and Message Transactions to build and maintain the table. How the Topology Manager builds and maintains the table is described in the subsequent sections.

2.5.4.2 Topology Assistant

The Topology Assistant is the name of the Topology Management Layer in a multi-stream device with a branching unit. The Topology Assistant uses local Native AUX transactions to gather information regarding peer devices connected to it and provides for the information as requested by the Topology Manager. The information provided by Topology Assistants is described in Section 2.5.5.2 and Section 2.5.6.2.

2.5.5 Topology Discovery

The goal of Topology Discovery is Stream Policy Maker implementation-specific. The goal may be to find the closest DP Sink device, build a DP Sink device to RAD table, –or– graphically display the topology showing each device and its associated interconnections.

2.5.5.1 Topology Manager

The Topology Manager uses Native AUX transactions and Message Transactions to implement its Topology Discovery algorithm. At power up, the Topology Manager monitors the connection status of its local DFPs by way of each port's HPD signal. When a device is connected to one of its DP ports, the Topology Manager reads the capabilities of the immediate downstream DP device using Native AUX transactions. The device capabilities include the device type and whether Messaging is supported. If the connected device (i.e., peer device) is a multi-stream device with a branching unit, the Topology Manager can instruct the Messaging AUX Client to transmit a LINK_ADDRESS message transaction request to the device to determine the device GUID, the number of input and output ports and the type and capabilities of devices connected to the device's input and output ports (referred to as "Peer_Device Types"). The Topology Manager, using the information obtained from the LINK_ADDRESS message transaction response, can further transmit LINK_ADDRESS messages to other DP multi-stream devices that contain branching units until the goal of its Topology Discovery is met.

2.5.5.2 Topology Assistant

During the Topology Discovery procedure, the Topology Assistant in a multi-stream device with a branching unit shall reply to the LINK_ADDRESS Request Message Transaction with its capabilities and the Peer Device Type of each DP device connected to its DPTX and DPRX ports (either physical or logical). The Topology Manager gathers the information of the peer devices using Native AUX transactions.

2.5.6 Topology Maintenance

Topology Maintenance is the continual monitoring for DP device connection or removal from the topology. The Topology Assistant within each DP multi-stream Branch/Composite device shall detect and notify the Topology Managers when devices are connected and/or removed. What the Topology Manager does with this notification is implementation-specific.

2.5.6.1 Topology Manager

During Topology Maintenance, the Topology Manager may receive CONNECTION_STATUS_NOTIFY Broadcast Request Message transactions when DP multi-stream Branch devices are connected to or disconnected from the topology. The following information is provided with the CONNECTION_STATUS_NOTIFY Broadcast Request Message transaction:

- GUID of the multi-stream device where the connection change was detected
- Port number on the device and whether the port is an input or output where the connection change was detected
- New connection status for the port where the connection change was detected
- Peer device type if a new DP device was connected
- Whether the newly connected DP device supports Messaging

How the Topology Manager uses this information is implementation-specific. The notification may be ignored if notification is not needed.

2.5.6.2 Topology Assistant

After a DP multi-stream device with a branching unit powers on, the device continually monitors the connection status of each of its input and output ports using the connection mechanism associated with the corresponding port type, HPD for DPTX ports and cable termination for DPRX ports. All internal DP Sinks of a logical branch device are connected by default. When the connection status of any DP port changes, the new status is broadcast out to all connected DPTX and DPRX ports using the CONNECTION_STATUS_NOTIFY Broadcast Request Message transaction. The Topology Assistant continues monitoring its DPTX and DPRX ports for connection changes. The Topology Assistant may receive one or more LINK_ADDRESS Message Transaction requests. Each LINK_ADDRESS request shall be handled the same as during the Topology Discovery procedure.

2.5.7 Topologies with Single-stream-only Source devices

When a topology contains one or more DP single-stream-only Source devices, the DP multi-stream Branch device connected to the DP single-stream-only Source devices shall perform the single-stream-only Topology Management function. The DP multi-stream Branch device recognizes the upstream device as the single-stream-only device when the upstream device keeps the UP_REQ_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 1) cleared to 0. A multi-stream upstream device may function and be treated as a single-stream-only device by **not** setting the UP_REQ_EN bit to 1.

The single-stream-only Topology Management function is a basic input to output port selection. The DP multi-stream Branch device connected to a single-stream-only Source device functions as a single-stream-only Branch device as described in Section 5.3. A multi-stream Branch device functioning as a single-stream-only Branch device shall **not** convert single-stream input to multi-stream output.

A DP multi-stream Source device's DPTX may choose to transmit in SST mode (i.e., keeps the MST_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 0) of the downstream device cleared to 0) while setting the UP_REQ_EN bit to 1, as long as it performs the role of Topology Manager and Source Payload Bandwidth Manager and originates Message Transactions for virtual channel management prior to single-stream transmission. After the DP multi-stream Source device establishes the virtual channel, using Message Transactions, and transmits in SST mode, the DP multi-stream Branch device shall convert the single-stream input to multi-stream output.

2.5.8 Loop Handling

While DP multi-stream topologies should be constructed without loops or parallel paths, the Topology Manager shall be able to handle the case where loops or parallel paths exist.

The GUID obtained from the LINK_ADDRESS Message Transaction request and the RAD of the DP device queried provide for sufficient information to determine whether a loop or parallel path in the topology exists. The path chosen to access a DP device accessible through multiple paths is Topology Manager implementation-specific, including the handling of a topology that has a loop and/or a parallel path. An example topology with a loop and a parallel path is illustrated in Figure 2-70 along with the GUID and RAD for the loop and parallel path.

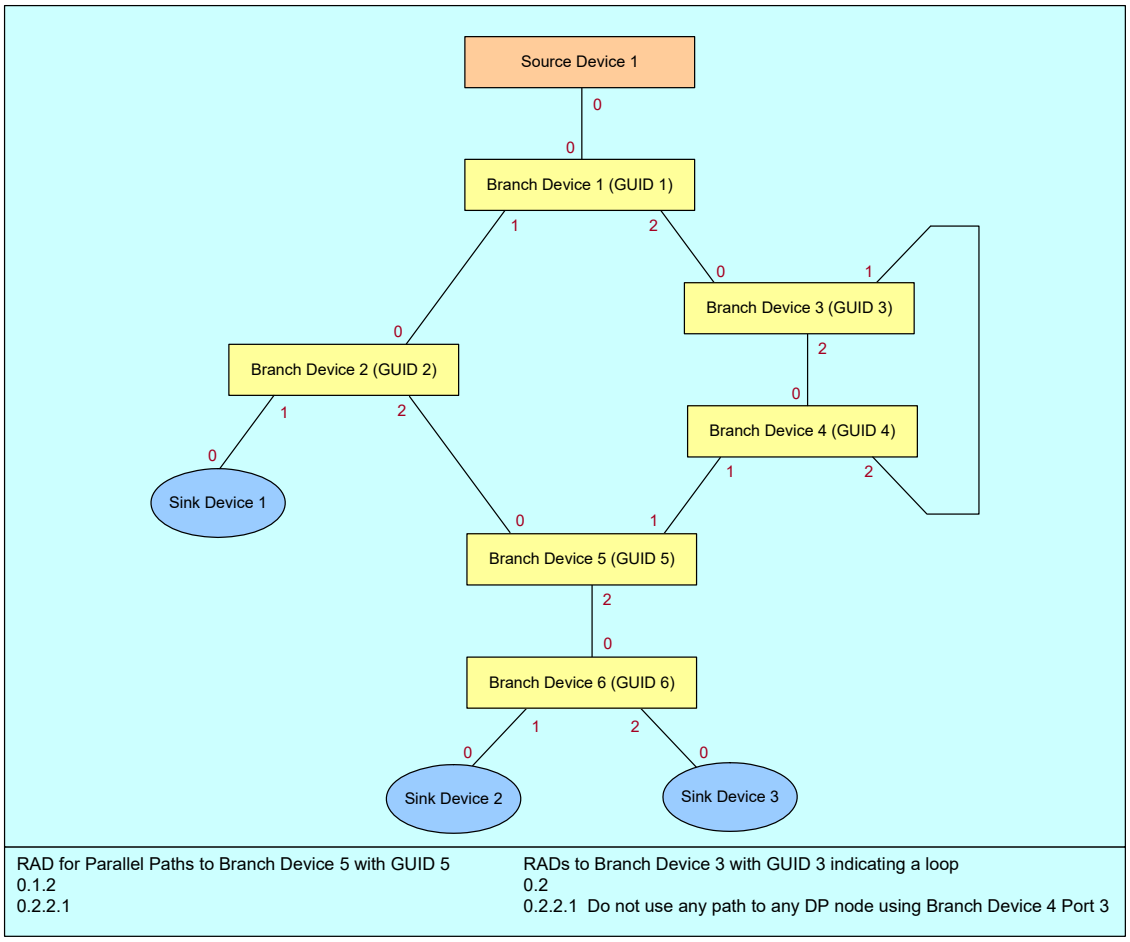


Figure 2-70: Multi-stream Topology with a Loop and a Parallel Path

Section 2.14 defines the procedure that the Messaging AUX client uses for handling Broadcast Message Transaction when loops are present.

2.6 MST Mode 8b/10b Link Layer Operation

The Multi-Stream Transport (MST) Extension Specification described in this section achieves the following features:

- Transport of multiple streams that are asynchronous with one another and de-coupled from the link timing, with the packetizing overhead as small as 1.6%
- Addition or deletion of a stream without affecting the other streams being transported
- Symbol Stream Sequence pass-through of DP Branch devices in the path (except those performing the conversion between MST and SST symbol mapping) is agnostic to symbol types, data types/format, and Main-Link lane count
- Robust link; predictable link timing and redundancy in VC Payload symbol transmission (regardless of the lane count)

DP devices that support MST mode shall support SST mode as well.

Stream Policy Maker is the entity that decides the audio and/or video streams to be transported. Stream Policy Maker makes use of the Payload Bandwidth Manager and the Topology Manager to achieve this task. To decide on the specific stream to use, Stream Policy Maker optionally determines the various audio and/or video modes that could be set at that moment based on various constraints and capabilities along the path.

This section focuses on the enumeration of path constraints within the Stream Policy Maker, the Main-Link Symbol Management Layer, Payload Bandwidth Management Layer and VC Payload Mapping Layer (see Figure 2-71) and consists of the summarized sub-sections that follow.

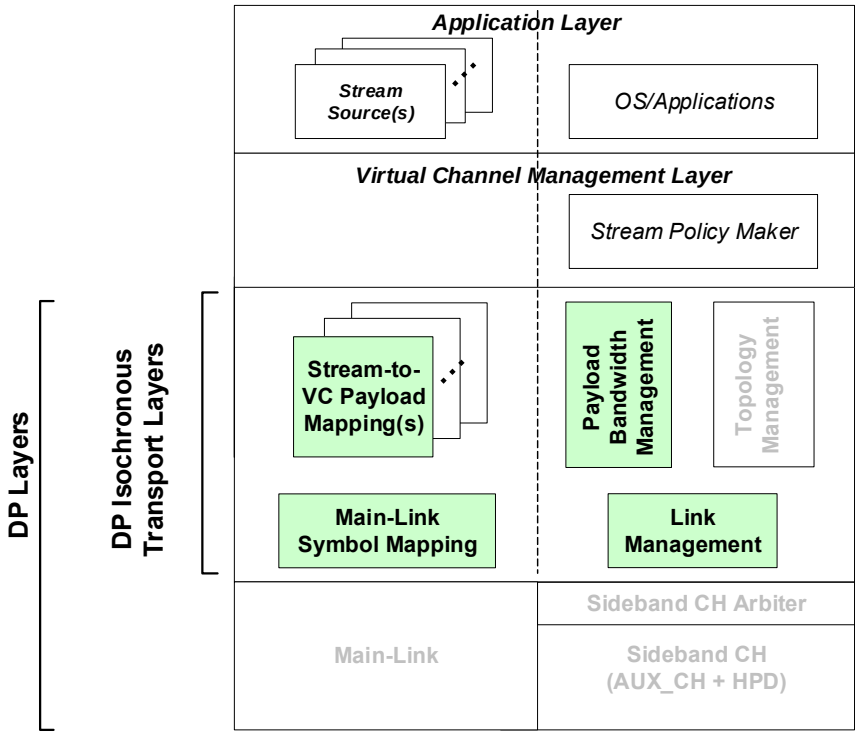


Figure 2-71: Layers Discussed in this Section

- Section 2.6.1 – Path Constraint Enumeration
  - Stream Policy Maker optionally determines the various audio and/or video modes that could be set at the moment based on various constraints and capabilities along the path.
- Section 2.6.2 – Link Timing Generation Based on MST Packet
  - The timing is self-generated by Main-Link Symbol Manager, rather than dictated by the timing of the stream being transported.
- Section 2.6.3 – Symbol Sequence Mapping into VC Payload
  - Symbol sequence mapped into VC Payload consists of 4-symbol sequence units, regardless of the Main-Link lane count.
  - Only a DP Source device generates Stream Symbol sequence, while a DP Branch device forwards the Stream Symbol sequence.
  - VC Payload Fill (VCPF) Symbol sequence is inserted by Main-Link Symbol Manager in the absence of Stream symbols. Stream Symbol sequence mapped by VC Payload Mapper replaces VCPF Symbol sequence when streams are transported.
  - VC Payload Symbol generation method in MST mode enables pass-through of Stream symbols by the intermediate DP Branch devices.
- Section 2.6.4 – Time Slot Count Allocation to VC Payload
  - Source Payload Bandwidth Manager and Branch Payload Bandwidth Managers collaborate to ensure that a stream be transported in the VC Payloads established for the stream over the path without causing overflow. Source Payload Bandwidth Manager calculates Payload Bandwidth Number (PBN) for a stream and passes the PBN value to the downstream Branch devices to let the Branch Payload Bandwidth Managers determine the VC Payload size in time slot count per MTP.
  - Source and Branch Payload Bandwidth Managers ensure that the VC Payloads are set to the smallest possible size so that the maximum number of streams may be transported simultaneously. A Source device performs the rate governing and evenly distributes the number of Stream symbols over multiple MTPs by throttling the Stream Symbol sequence insertion rate.
- Section 2.6.5 – VC Payload Allocation Synchronization Management
  - VC Payload is managed by synchronizing the VC Payload ID tables between the DPTX and DPRX and also by synchronizing the VC Payload allocation over the Main-Link to the table.
- Section 2.6.6 – ALLOCATE_PAYLOAD Timing Sequence
  - ALLOCATE_PAYLOAD message transaction maintains VC Payload synchronization over multiple links between a stream source and stream sink.
- Section 2.6.7 – Impacts of Various Events on VC Payload ID Table
  - Some events such as unplug event and loss of link affect the VC Payload ID tables.
- Section 2.6.8 – Robustness Mandate
  - Certain actions are necessary for a DPRX to make the link as robust as possible by taking advantage of the self-generated link timing and MST DPTX VC Payload symbol-generating methods.

- Section 2.6.9 – Control Functions, Control Link Symbols, and K-code Assignment
  - Control link symbols are mapped to 8b/10b K-codes. Most of the control link symbols, as well as all the data symbols, are scrambled.
- Section 2.6.10 – Conversion between MST and SST Symbol Mapping
  - Simple pass-through does **not** apply to DP Branch devices that convert from MST-to-SST-mapped symbols (or vice versa).
  - Switching between MST mode and SST mode interrupts stream transport.
- Section 2.6.11 – MTPH Usages for CP Extension in MST Mode
  - Some MTPHs are used for Content Protection purposes.

Figure 2-72, Figure 2-73, and Figure 2-74 illustrate the logic block diagrams of a DP MST Source, Sink, and Branch device, respectively. These diagrams are zoomed in and described in Section 2.6.2 and Section 2.6.3.

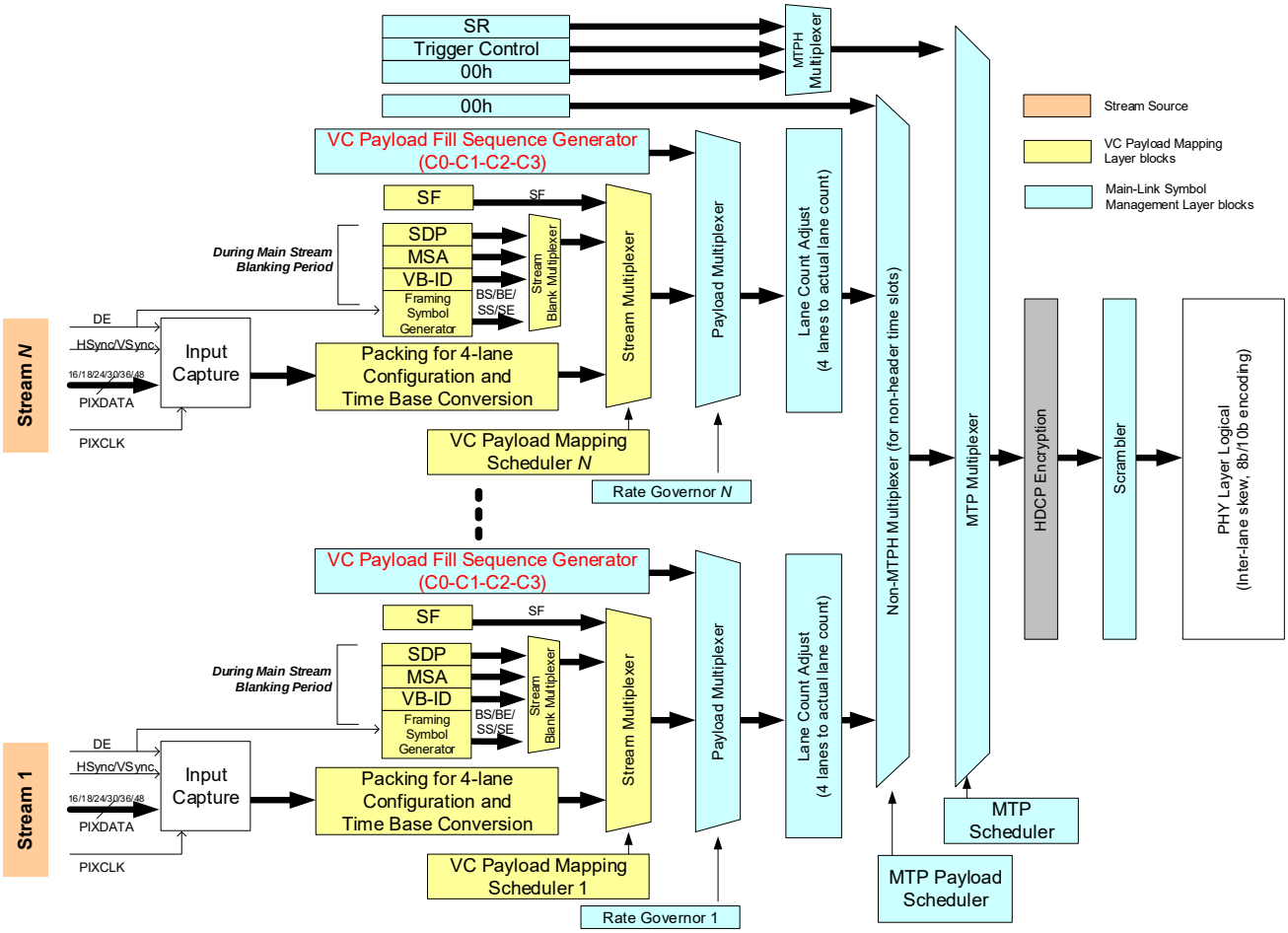


Figure 2-72: DP MST Source Device Logic Block Diagram

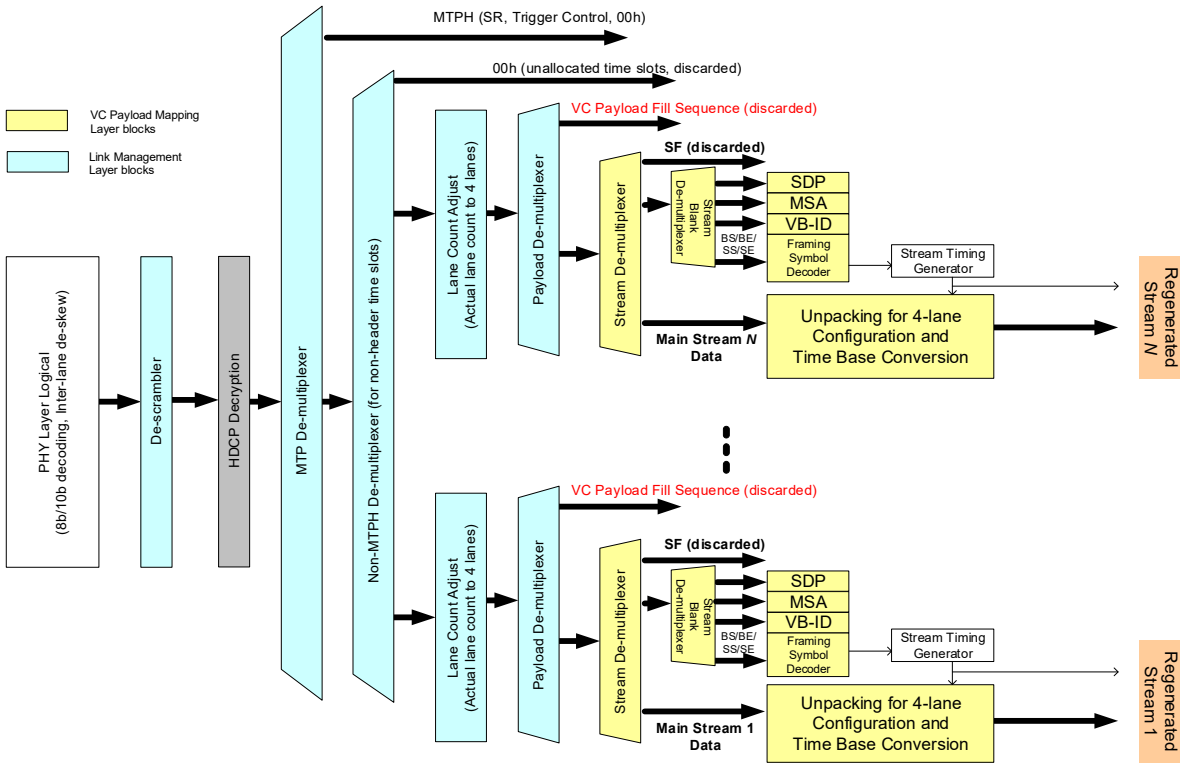


Figure 2-73: DP MST Sink Device Logic Block Diagram

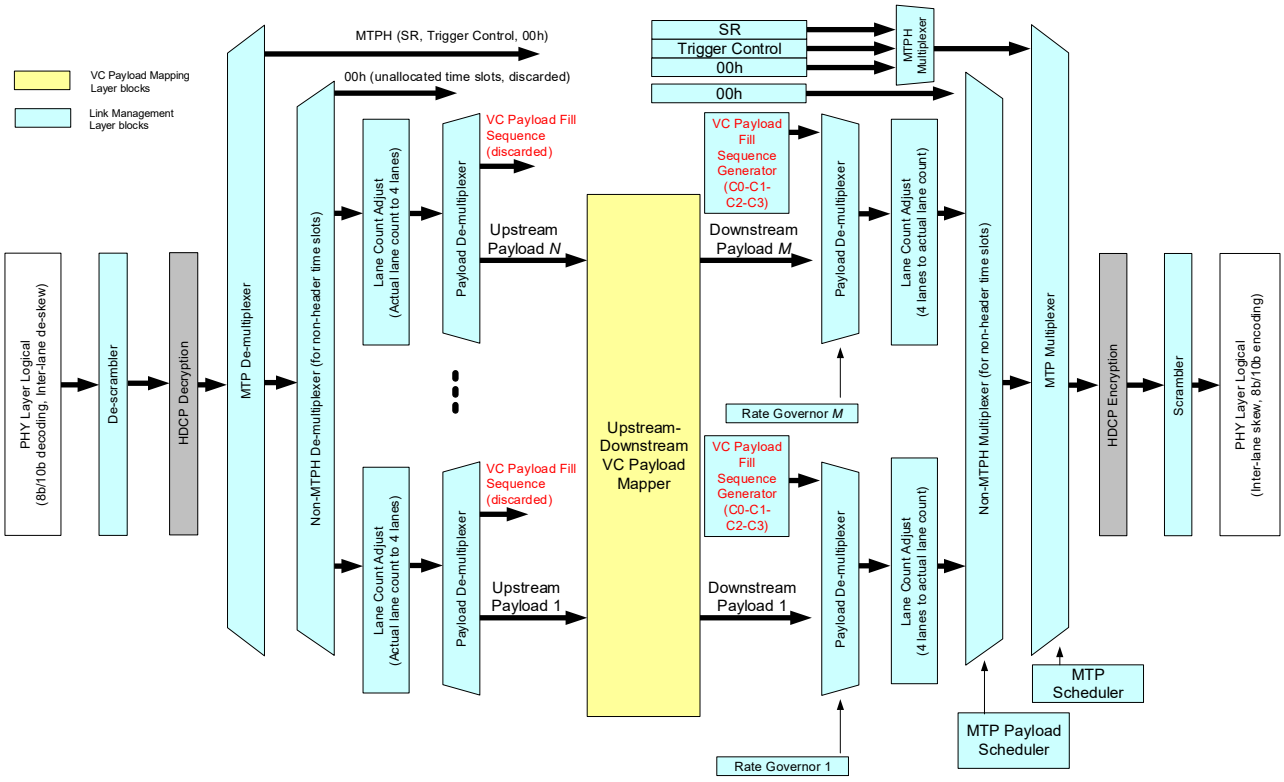


Figure 2-74: DP MST Branch Device Logic Block Diagram

Figure 2-75 and Figure 2-76 illustrate the logic block diagrams of DP SST Source and Sink devices, respectively, for reference purposes. These diagrams, when compared to Figure 2-72 and Figure 2-73, illustrate the similarity of VC Payload Mapping Layer blocks between SST in 4-lane configuration and MST.

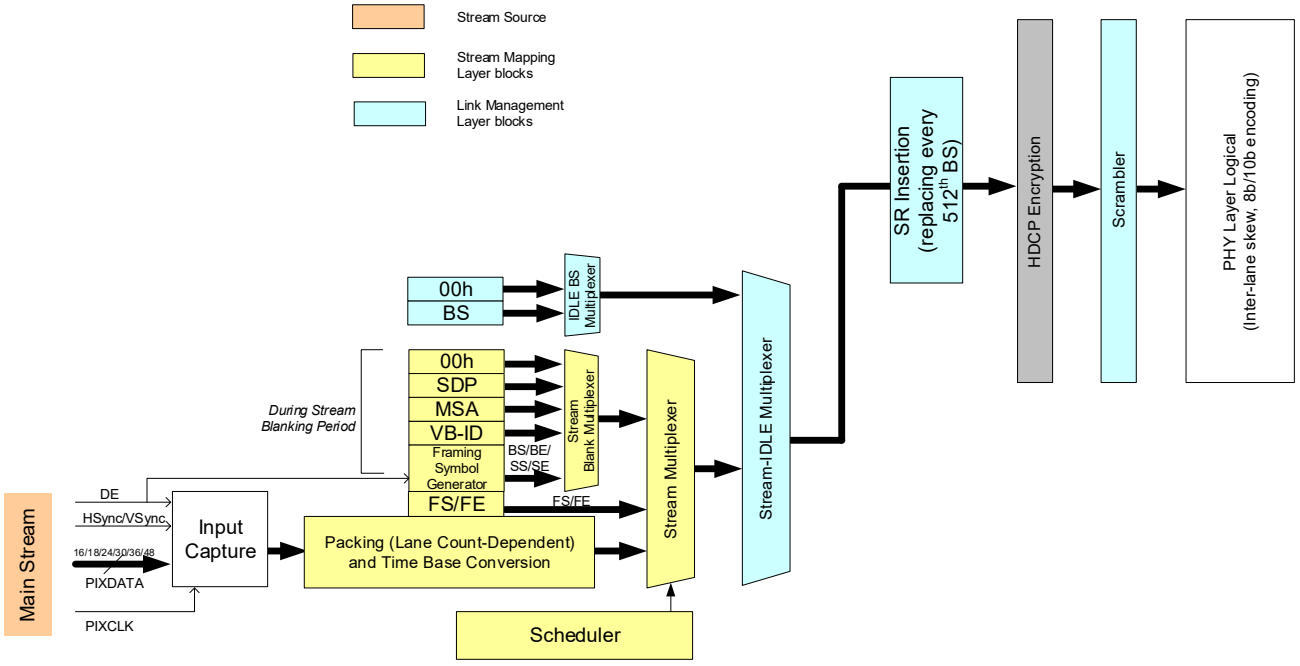


Figure 2-75: DP SST Source Device Logic Block Diagram

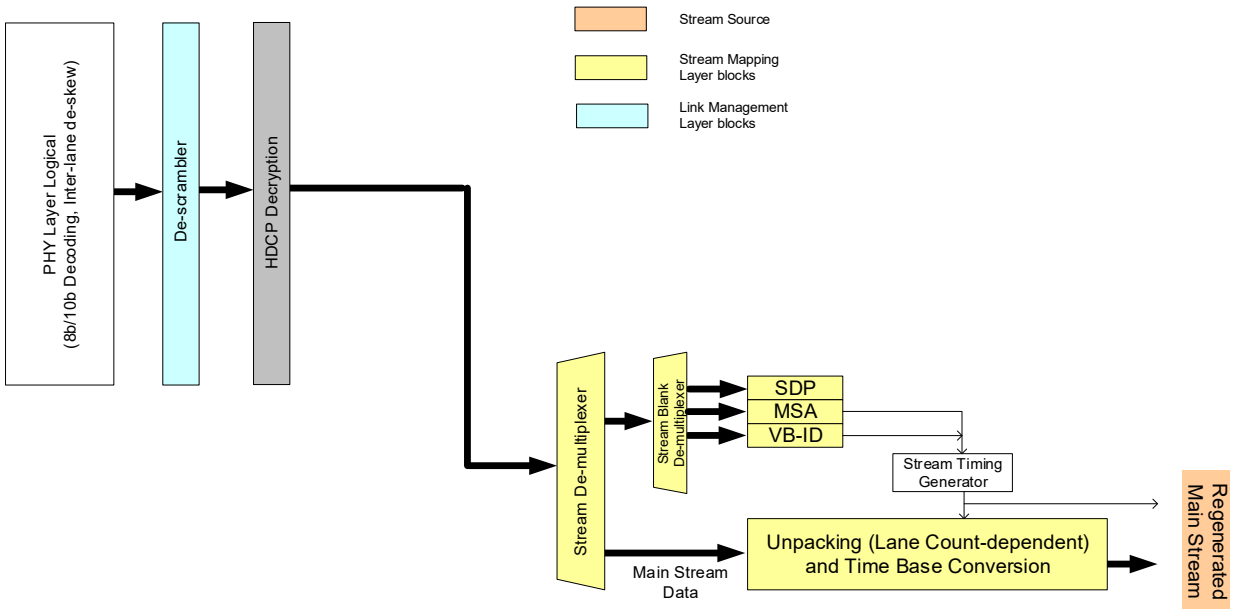


Figure 2-76: DP SST Sink Device Logic Block Diagram

2.6.1 Path Constraint Enumeration

An MST Source device uses a combination of LINK_ADDRESS and ENUM_PATH_RESOURCES Message Transactions to determine resource constraints on a given path. LINK_ADDRESS returns a Current_Capabilities_Structure (CCS), as defined in Table 2-133 and Table 2-134, indicating static device capabilities. ENUM_PATH_RESOURCES returns dynamic path resources (currently only the available link bandwidth) on a path through the Available PBN parameter.

Table 2-133: Current_Capabilities_Structure Syntax

Syntax	# of Bits
Current_Capabilities_Structure	
Max Frame Height	16
Max Frame Width	16
Max Frame Size	24
Max Frame Rate	10
RESERVED	6
Color Depth Supported RGB	8
Color Depth Supported YCbCr	16
Max Pixel Clock	16
S3D Formats Supported	16
Max Streams Supported	7
Other Unspecified Capability Exists	1

Table 2-134: Current_Capabilities_Structure Field Definitions

Field	Description
Max Frame Height	Maximum Active Height of the video frame that the device supports.
Max Frame Width	Maximum Active Width of the video frame that the device supports.
Max Frame Size	Maximum Active Frame Size of the video frame that the device supports. Specified in number of MacroBlocks (16 pixels by 16 pixels). This field can further refine the Max Frame Height and Max Frame Width constraints.
Max Frame Rate	Maximum rate at which the device can consume frames. Specified in terms of number of frames per second.
Color Depth Supported RGB	Indicates the color depth value that the device supports for RGB, Luma, and Chroma, The bit field values are defined in Table 2-136. Color Depth Supported RGB uses one instance of Table 2-136.
Color Depth Supported YCbCr	Indicates the color depth value that the device supports for RGB, Luma, and Chroma, The bit field values are defined in Table 2-136. Color Depth Supported YCbCr uses two instances of Table 2-136, with the table for Luma preceding the table for Chroma.
Max Pixel Clock	Maximum pixel clock that the device supports on the DFP used by the input path under characterization. Value is conveyed in units of MHz.

Table 2-134: Current_Capabilities_Structure Field Definitions (Continued)

Field	Description
S3D Formats Supported	Indicates support for various S3D formats, as defined in Table 2-135.
Max Streams Supported	Maximum number of streams that the device supports.
Other Unspecified Capability Exists	Indicates presence of a vendor-specific constraint. The Source device discovers this constraint in a vendor-specific manner.

Table 2-135: Bit Field Definition for S3D Capabilities

Bit Field Value	Meaning
0h	No S3D support
1h	Frame/Field Sequential, Value 0x0
2h	Frame/Field Sequential, Value 0x1
4h	Frame/Field Sequential, Value 0x2
8h	RESERVED
10h	Stacked Frame: Left-eye view is on top, right-eye view is on bottom
20h	RESERVED
40h	Pixel Interleaved, Value 0x0
80h	Pixel Interleaved, Value 0x1
100h	Pixel Interleaved, Value 0x2
200h	Pixel Interleaved, Value 0x3
400h	Pixel Interleaved, Value 0x4
800h	RESERVED
1000h	Side-by-side, Value 0x0
2000h	Side-by-side, Value 0x1
4000h	Top-to-bottom, Value 0x0
8000h	Top-to-bottom, Value 0x1

Table 2-136 defines color depths associated with the bits identified in Table 2-133.

Table 2-136: Bit Field Definition for Color Depth Indication for RGB, Luma, and Chroma

Bit Field Value	Meaning
1h	6bpc
2h	8bpc
4h	10bpc
8h	12bpc
10h	16bpc
All other values	RESERVED

2.6.1.1 Multi-function DP MST Branch Device Enumeration

New to *DP v1.4*.

A basic MST Branch device contains an MST Branching Unit (BU) capable of the following operations:

- DP MST-in, DP MST-out VC Payload routing as an intermediate MST Branch device
- DP MST-to-DP SST conversion as the last MST Branch device

A multi-function MST Branch device, as the last MST Branch device, is capable of performing one or more of the following operations in addition to the basic MST Branch device capabilities listed above:

- Protocol conversion
- Horizontal Blanking Expansion
- Ignore-MSA handling for Adaptive-Sync support
- Pixel encoding format conversion (e.g., YCbCr4:4:4-to-YCbCr4:2:0)
- Display Stream Compression (DSC) decompression

A multi-function MST Branch device may contain local stream sinks to constitute a multi-function MST Branch-Sink device.

2.6.1.1.1 Virtual DP Peer Device with DPCD Registers

A multi-function MST Branch or Branch-Sink device shall enumerate those multi-function DFPs connected to SST devices, both DP and non-DP transport DFPs, and local stream sinks with virtual DP peer devices equipped with DPCD registers. (See Section 2.6.1.1.2 for details regarding Virtual DP Peer Device DPCD registers.) A virtual DP peer device with DP output shall set the MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0) to 1 to provide accessibility of the DPCD registers of the downstream DP SST device to the DP MST Source device.

A multi-function MST Branch or Branch-Sink shall have unique GUID values in the UFP DPCD and virtual DPCD registers (mapped to DPCD Addresses 00030h through 0003Fh). Virtual DPCD registers shall have the common non-zero value for GUID_2 (DPCD Addresses 00040h through 0004Fh). For UFP DPCD registers, GUID_2 shall be all 0s.

Figure 2-77 illustrates an example of a multi-function MST Branch-Sink device with one MST-capable DPTX port, two MST-capable DP++ TX ports, one HDMI TX port, and one local stream sink. DP++ TX Port 1 has neither a downstream device nor level-shifting dongle connected in this example.

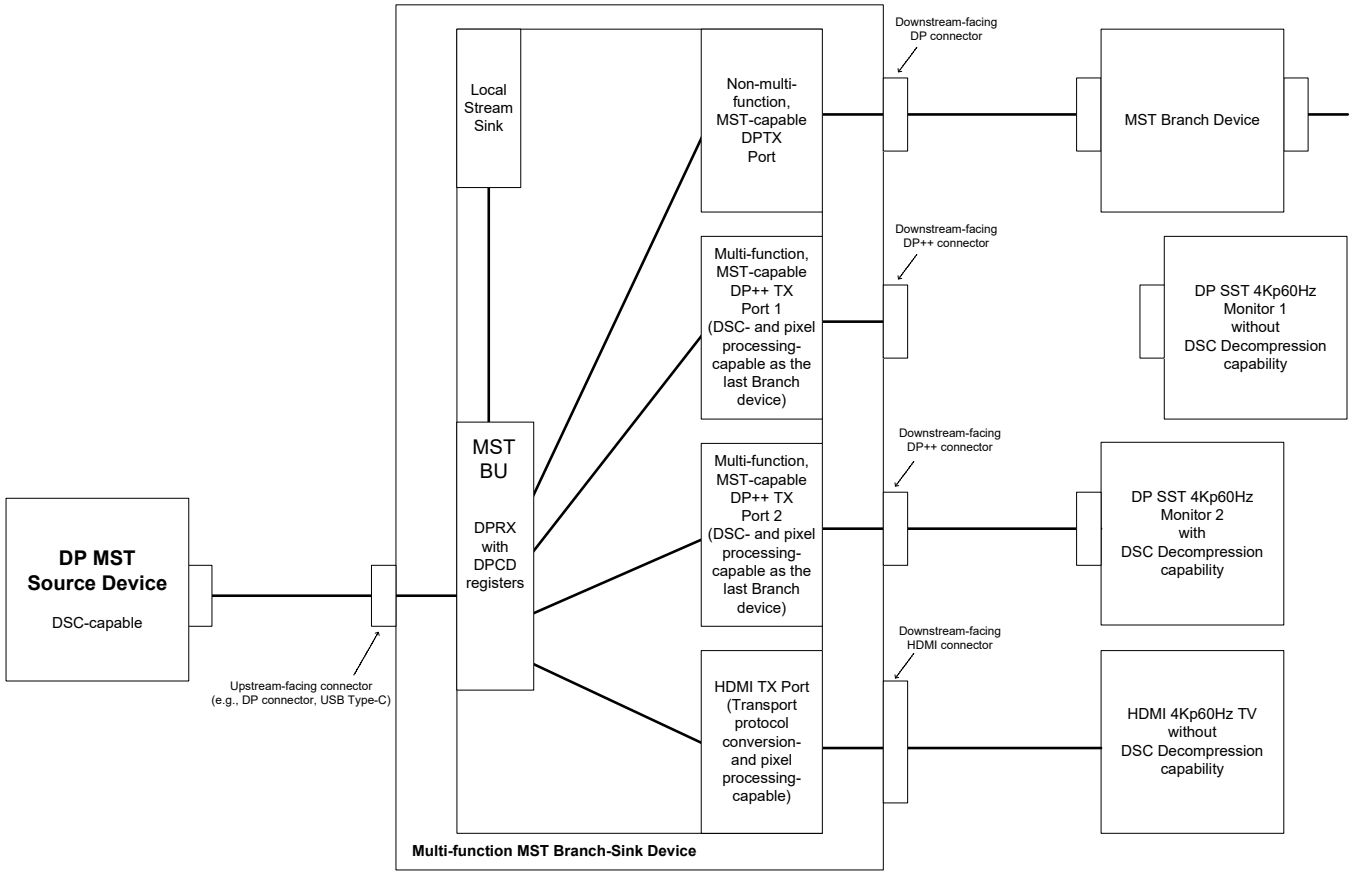


Figure 2-77: Multi-function Branch-Sink Device Example

Figure 2-78 illustrates how this multi-function MST Branch-Sink device enumerates the following topology to the DP MST Source device:

- DP++ TX Port 2 with a DP SST monitor connection enumerated as a virtual DP-to-DP peer device with a Virtual DPCD register set
- HDMI TX Port enumerated as a virtual DP-to-HDMI protocol converter peer device with a Virtual DPCD register set
- Local stream sink enumerated as a Virtual DP Sink peer device with a Virtual DPCD register set

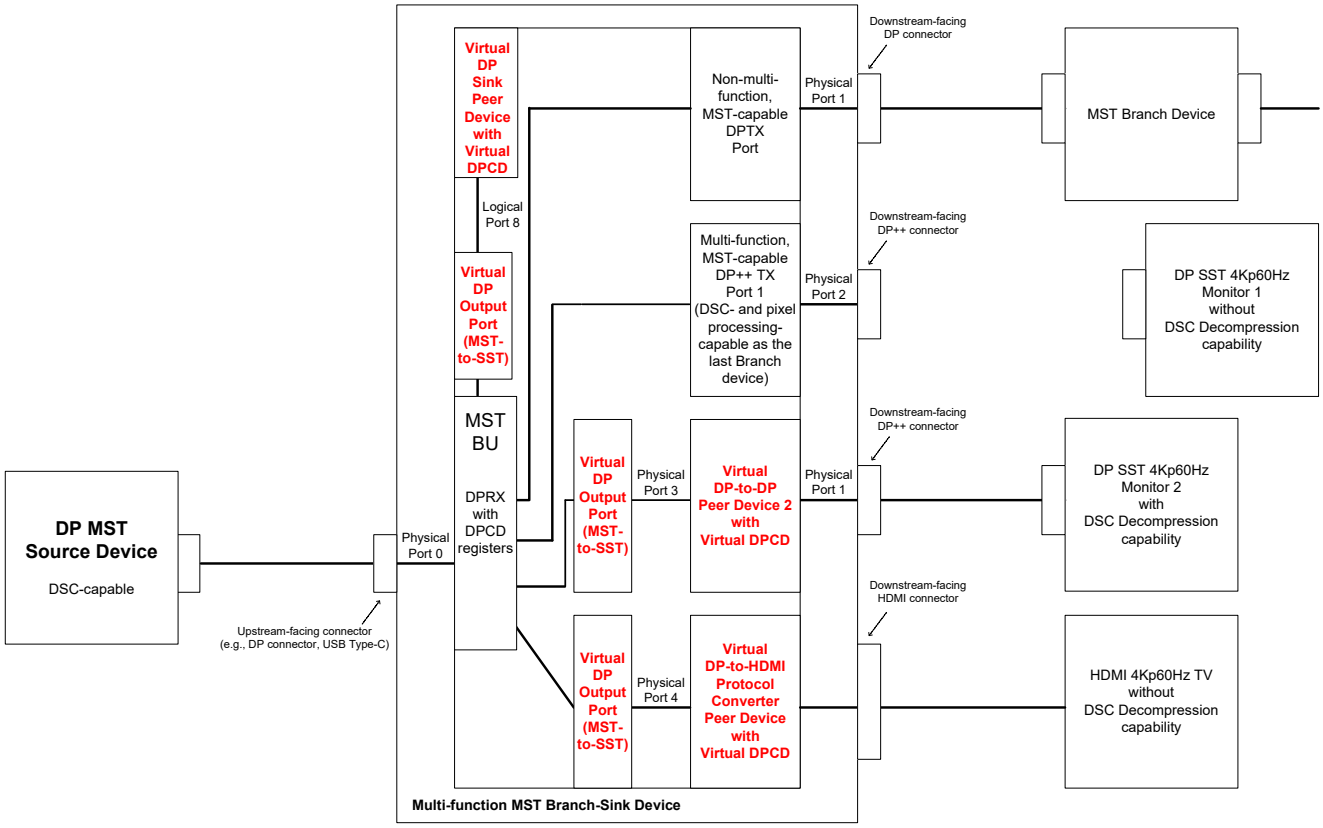


Figure 2-78: Multi-function MST Branch-Sink Device Enumeration Example

Figure 2-79 illustrates the enumeration after DP SST Monitor 1 is plugged to DP++ TX Port 1. After the plugging of a DP SST device, the multi-function MST Branch-Sink device changes DP++ TX Port 1 to a Virtual DP-to-DP peer device with a Physical DPTX Port that has a DP SST peer device, and then issues a Connection Status Notify (CSN) message transaction to the DP MST Source device.

If a level-shifting dongle had been plugged to the DP++ TX Port 1, the multi-function MST Branch-Sink device would have changed DP++ TX Port 1 to a Virtual DP-to-HDMI peer device.

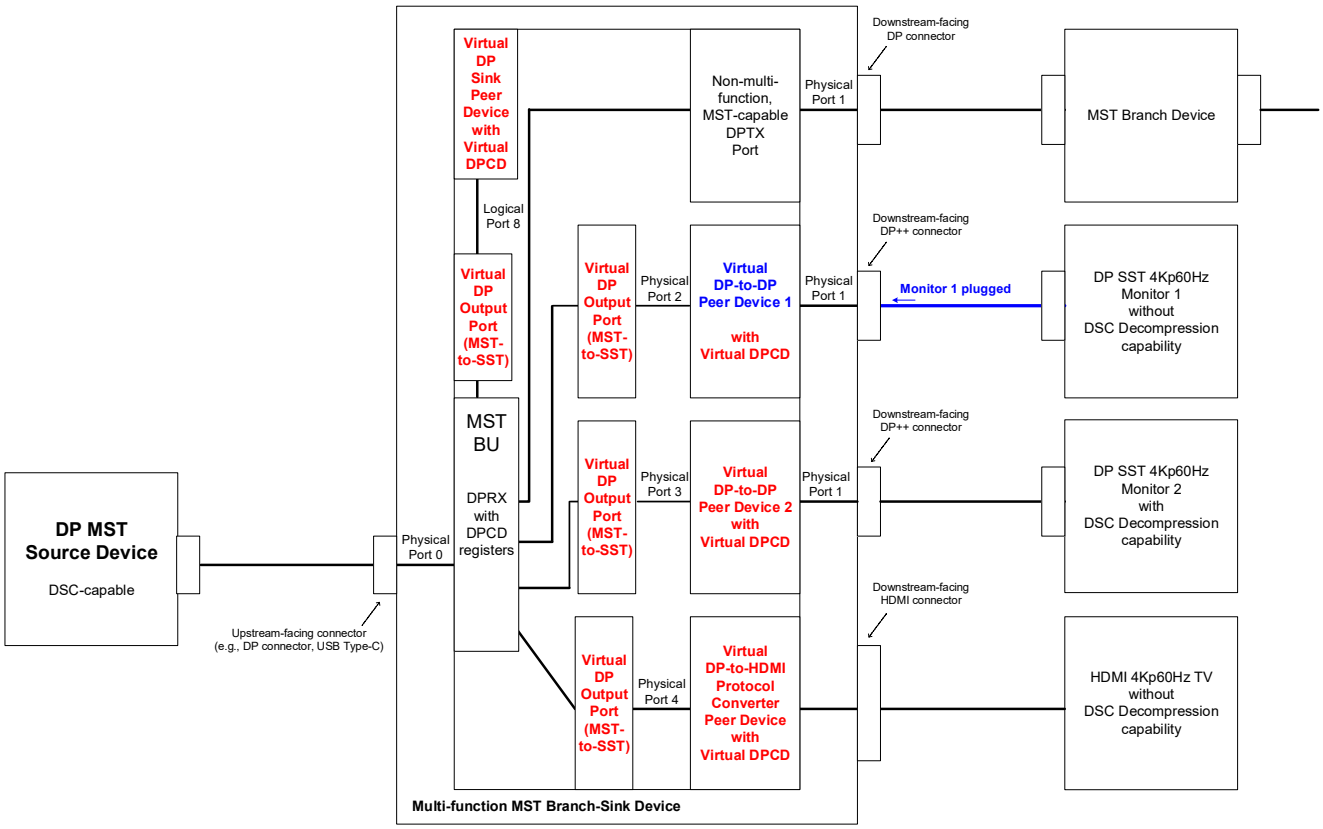


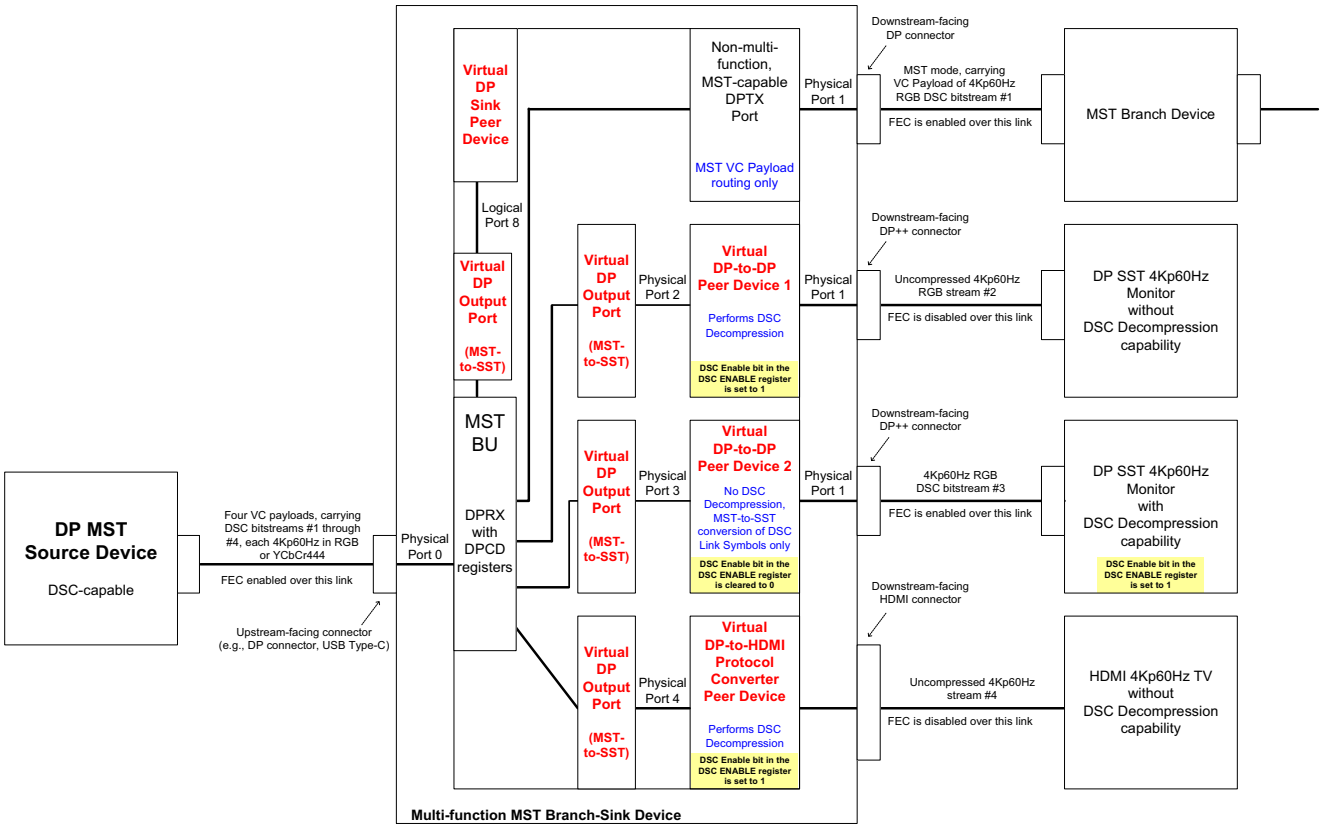
Figure 2-79: Enumeration after DP SST Monitor 1 Is Plugged

078165468884The DP MST Source addresses each of the virtual peer devices and connected downstream DP devices (which are physical DP peer devices) using RAD, as defined in Section 2.5.3.

For example, a DP MST Source device may simultaneously do the following:

- Enable DSC Decompression capability of Virtual DP-to-DP Peer Device #1 (because the DP SST device connected to it is **not** DSC Decompression-capable),
- Disable DSC Decompression capability of Virtual DP-to-DP Peer Device #2, and
- Enable DSC Decompression capability of its downstream DP SST device

Such control granularity by the DP MST Source device is possible by setting both the virtual and physical DPCD register bits by way of REMOTE_DPCD_READ and REMOTE_DPCD_WRITE message transactions, as illustrated in Figure 2-80.



Note: *DSC Enable bit = DPCD Address 00160h, bit 0.*

Figure 2-80: DSC Decompression Operation Control by way of Virtual/Physical DPCD Register Setting

2.6.1.1.2 DPCD Registers Used with Virtual DP Peer Devices

Table 2-137 lists the DPCD registers that are used with virtual DP peer devices. (For complete register descriptions, see Table 2-183, Table 2-184, and Table 2-194.) For the remaining DPCD registers, a multi-function MST Branch device shall reply with the DPCD register values of its MST BU's DPRX.

Table 2-137: DPCD Registers Used with Virtual DP Peer Devices

DPCD Address	Bit #	Definition	Read/Write over AUX_CH
00005h	**DOWN_STREAM_PORT_PRESENT**		Read Only
	0	**DFP_PRESENT** 0 = Device is a virtual DP Sink peer device and does not have DFP(s). 1 = Device is another type of virtual DP peer device and has DFP(s).	
00007h	**DOWN_STREAM_PORT_COUNT**		Read Only
	3:0	**DFP_COUNT** 0h for a virtual DP Sink peer device. 1h for other virtual DP peer devices.	
	6	**MSA_TIMING_PAR_IGNORED** Virtual DP peer devices that support the Ignore MSA option shall set this bit as described in Section 2.2.4.1.1.	
00008h	**RECEIVE_PORT0_CAP_0** Virtual DP peer devices that support Horizontal Blanking Expansion shall program this register as described in Section 2.2.4.1.2.		Read Only
00009h	**RECEIVE_PORT0_CAP_1** Virtual DP peer devices that support Horizontal Blanking Expansion shall program this register as described in Section 2.2.4.1.2.		Read Only
00021h	**MSTM_CAP** Virtual DP peer device with DP output shall set the MST_CAP bit (bit 0) to 1.		Read Only
00060h through 0006Fh	**DSC Capabilities**		Read Only
00080h through 00083h	**Detailed Capabilities Info** Detailed capabilities information for the DFP(s) of the virtual DP peer device.		Read Only
000A0h through 000A2h	**DSC Capability Branch Decoder Overall Throughput and Line Buffer Width**		Read Only
00107h	**DOWNSPREAD_CTRL**		Read/Write
	7	**MSA_TIMING_PAR_IGNORE_EN** Can be set to 1 only when the MSA_TIMING_PAR_IGNORED bit in the DOWN_STREAM_PORT_COUNT register (DPCD Address 00007h, bit 6) is set to 1.	

Table 2-137: DPCD Registers Used with Virtual DP Peer Devices (Continued)

DPCD Address	Bit #	Definition	Read/Write over AUX_CH
00160h		**DSC ENABLE**	Read/Write
00200h (and 02002h)		**SINK_COUNT** Used by virtual DP-to-non-DP peer device to indicate connection of the non-DP downstream device.	Read Only
0020Fh (and 02011h)		**DSC STATUS**	Read/Write
00240h through 00245h		**TEST_CRC-related registers**	Read Only
03030h through 03034h		**Downstream HDMI Link Status Reporting-related registers**	Read Only
03050h through 03053h		**DVI/HDMI Mode Configuration and Pixel Processing Configuration-related registers**	Read/Write
03054h and 03055h		**OUTPUT_HTOTAL** Used with Horizontal Blanking Expansion, as described in Section 2.2.4.1.2.	Read/Write
03056h and 03057h		**OUTPUT_HSTART** Used with Horizontal Blanking Expansion, as described in Section 2.2.4.1.2.	Read/Write
03058h and 03059h		**OUTPUT_HSP_HSW** Used with Horizontal Blanking Expansion, as described in Section 2.2.4.1.2.	Read/Write

2.6.1.1.3 DSC Resource Management of DSC-capable Multi-function DP MST Branch Device

A multi-function DP MST Branch device may have multiple virtual DP peer devices that have DSC decompression capability. This section describes the policy of DSC resource management among multiple virtual DP peer devices that have DSC decompression capability.

The DSC engine capability (consisting of one or more DSC decoder units) is exposed in the following registers (see Section 2.8 for details):

- Peak DSC throughput at DPCD Address 0006Bh
- DSC slice capabilities at DPCD Addresses 00064h and 0006Dh
- DSC maximum slice width at DPCD Address 0006Dh

A DP Branch device with DSC decompression may expose additional capability limitations of its DSC engine (composed of one or more DSC decoder units) in the following registers (see Section 2.10.1.1 for details):

- Peak DSC overall throughput at DPCD Addresses 000A0h and 000A1h
- DSC maximum line buffer width at DPCD Address 000A2h

A multi-function DP MST Branch device with multiple virtual DP peer devices that have DSC capability shall expose fixed DSC capability when a Sink device is connected. The fixed DSC capability persists for the connection's duration. The multi-function DP MST Branch device shall manage the DSC unit resource and assign DSC units to a DSC engine when a port is connected based on its own policy. A multi-function Branch device with flexible DSC resource sharing capability should be used to keep the DSC resource partitioning information within the device's non-volatile memory, to maintain policy consistency after the device power cycles.

An upstream DP MST DSC Source device shall rely on the DSC capability exposed by the multi-function DP MST Branch device in the DSC capability DPCD registers listed above.

2.6.2 Link Timing Generation Based on MST Packet

The DPTX enables an MST mode by setting the MST_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 0) to 1 by way of a Native AUX write after having verified that its downstream DPRX has the MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0) set to 1.

In SST mode, Main-Link timing is governed by the timing of the main video stream that it is transporting. This is because the BS/SR symbol insertion interval is dictated by the main video stream's horizontal period. The TU, the vessel of micro-packets in SST mode, is transported only during the main video stream's active period. In MST mode, Main-Link timing is self-generated and is not governed by the timing of transported streams. The vessel of micro-packets is referred to as a "Multi-Stream Transport Packet" (MTP). The MTP is 64 link symbol cycles (i.e., 64 time slots) long, starting with MTP Header (MTPH) in the first time slot (or Time Slot 0), and is constantly transported, regardless of the presence/absence of streams.

The Main-Link Symbol Manager of the DPTX inserts an SR control link symbol to the MTPH time slot every 1024th MTP as a Link Frame boundary marker, resulting in an SR insertion interval of 2^{16} time slots, as illustrated in Figure 2-81.

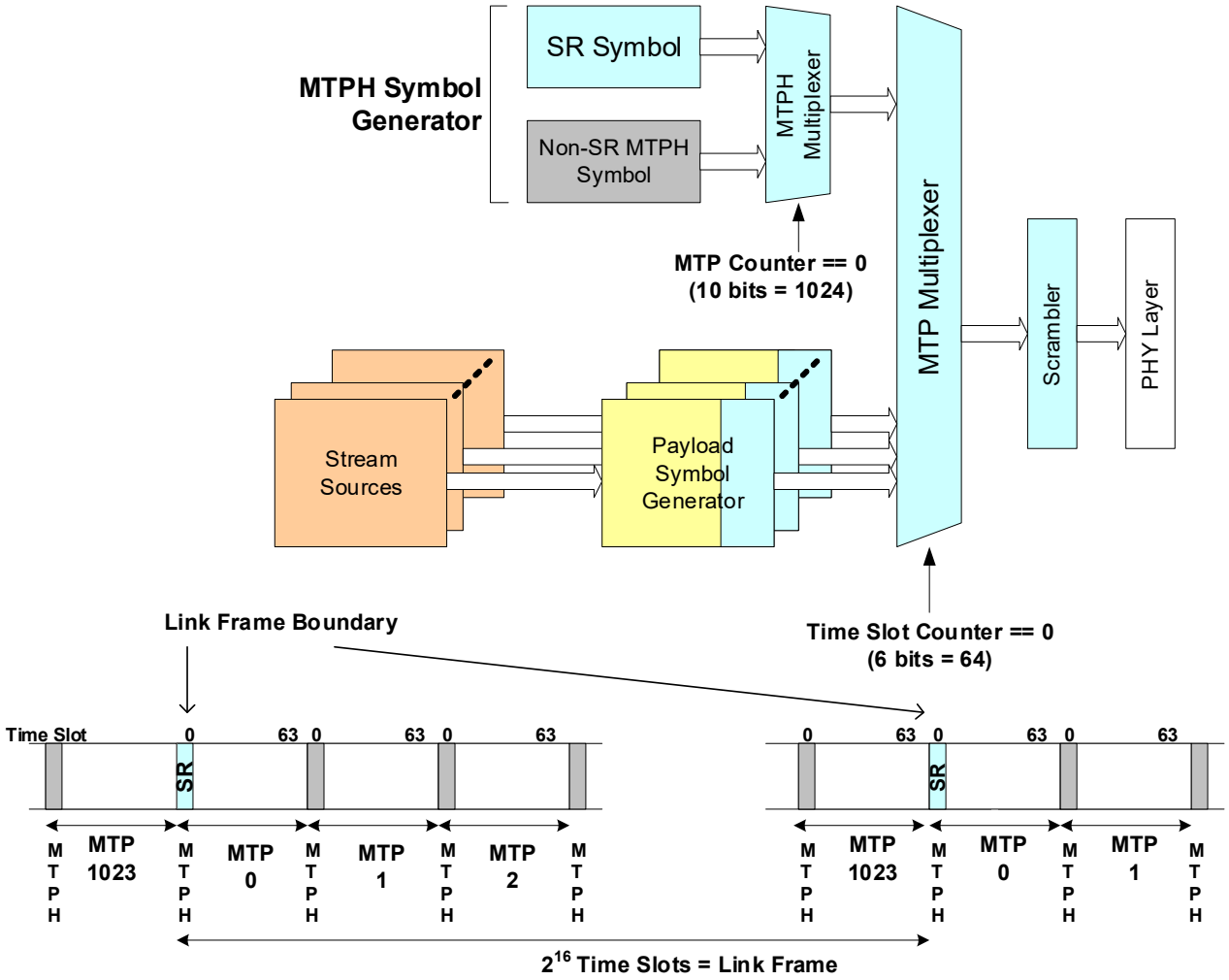


Figure 2-81: Link Timing Generation in MST Mode

2.6.2.1 MST Link Timing Generation with FEC Encoding/Decoding Enabled

New to *DP v1.4*.

When FEC encoding/decoding is enabled (see Section 3.5.1.5), a DPTX Link Layer shall insert FEC_PARITY_PH and FEC_PM link symbols, as follows:

- **4- and 2-lane configurations**
  - Six FEC_PARITY_PH link symbols inserted after 250 Link Layer link symbols
  - Every 256th set of six FEC_PARITY_PH link symbols, followed by an FEC_PM link symbol
- **1-lane configuration**
  - 12 FEC_PARITY_PH link symbols inserted after 500 Link Layer link symbols
  - Every 128th set of 12 FEC_PARITY_PH link symbols, followed by an FEC_PM link symbol

FEC_PARITY_PH and FEC_PM Link Layer symbol insertion is strictly periodic and is agnostic to Link Layer link symbol transmission being interrupted by the inserted FEC parity symbols.

Link Layer link symbol transmission timing, including SR symbol transmission timing, is skewed due to FEC_PARITY_PH and FEC_PM link symbol insertion.

2.6.3 Symbol Sequence Mapping into VC Payload

The Payload Bandwidth Manager of each DPTX in the path from a DP Source to a target Sink device allocates time slots within the MTP to a VC Payload to establish the virtual channel for transporting a stream.

When no time slot is allocated for any VC Payload, all 63 non-MTPH time slots are filled with data 0x00 (before data scrambling), as illustrated in Figure 2-82.

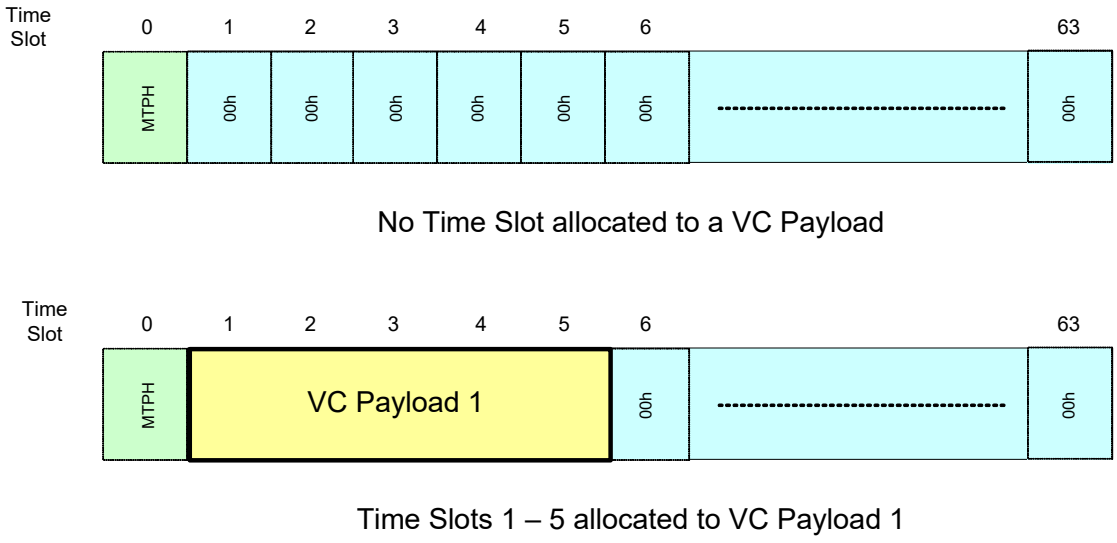


Figure 2-82: Time Slot Allocation to VC Payload

Two types of symbol sequences are mapped to the VC Payload time slots:

- Stream Symbol sequence generated by VC Payload Mapper of a DP Source device
- VC Payload Fill (VCPF) Symbol sequence generated by Main-Link Symbol Manager of a DP Source device and DP Branch devices

A Stream Symbol sequence generator is present only in a DP Source device. A DP Branch device generates VCPF Symbol sequence, but does not generate a Stream Symbol sequence. Rather, the DP Branch device forwards the Stream Symbol sequence received from the upstream DP device. When there is no Stream Symbol Sequence to forward, the Branch device transmits the VCPF Symbol sequence it generates.

Both symbol sequences consist of a unit of four symbols, regardless of lane count, as illustrated in Figure 2-83.

Upon the establishing a new VC Payload, a DPTX transmits VCPF Symbol sequence as the default symbol sequence for at least 16 MTPs before starting the transmission of Stream Symbol sequences. When there is no Stream Symbol sequence to insert, the DPTX continues transmitting the VCPF Symbol sequence.

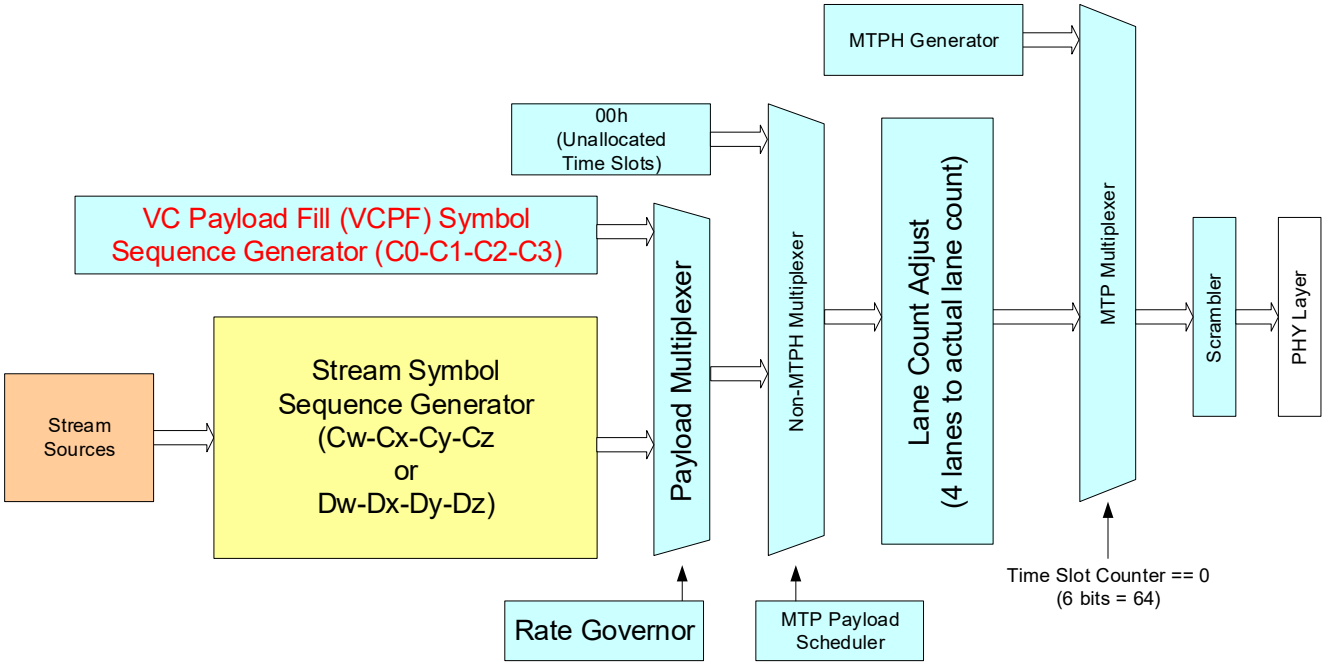


Figure 2-83: VC Payload Symbol Generator of a DP Source Device

When a DPTX is driving four lanes, the 4-symbol sequence unit – Sym_w, Sym_x, Sym_y, and Sym_z (Sym = C for control link symbol, and D for data symbol) – is mapped into the single time slot in the VC Payload time slots. For 1- and 2-lane configurations, the 4-symbol sequence unit is sequentially mapped, as illustrated in Figure 2-84.

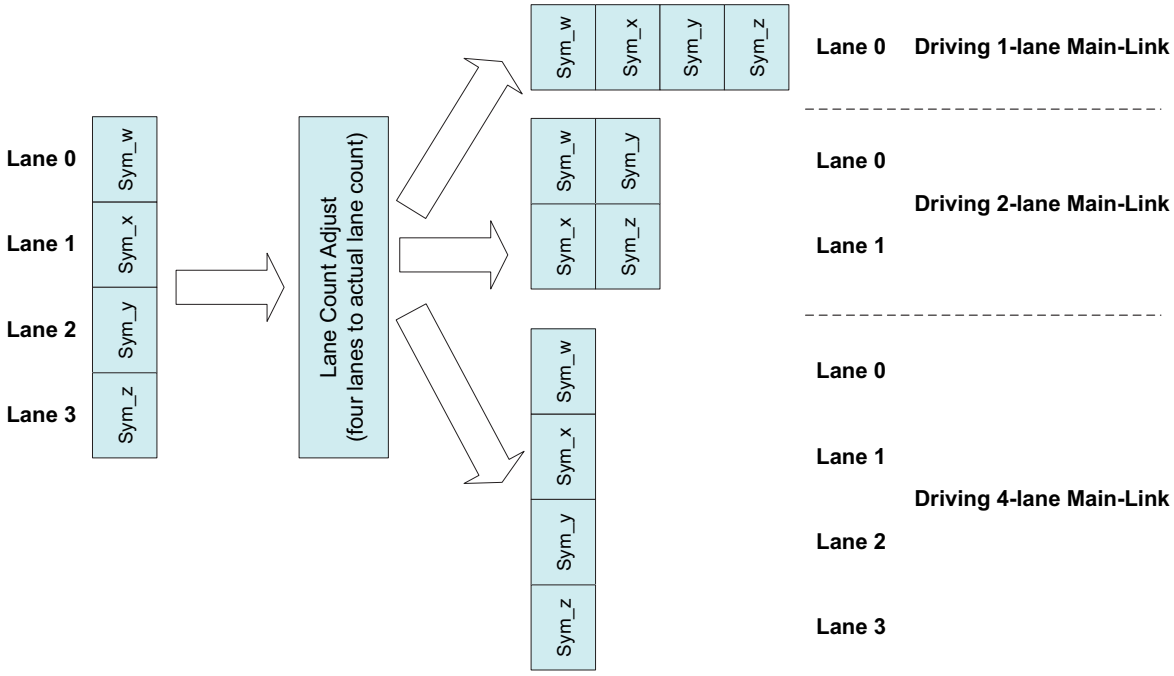


Figure 2-84: 4-Symbol Sequence Unit Mapping to Main-Link Lanes

The 4-symbol sequence unit pattern repeats itself when the VC Payload for a given stream is concatenated, as illustrated in Figure 2-85. As can be seen in the diagram, the 4-symbol sequence unit may straddle the VC Payload boundary of a given stream within an MTP.

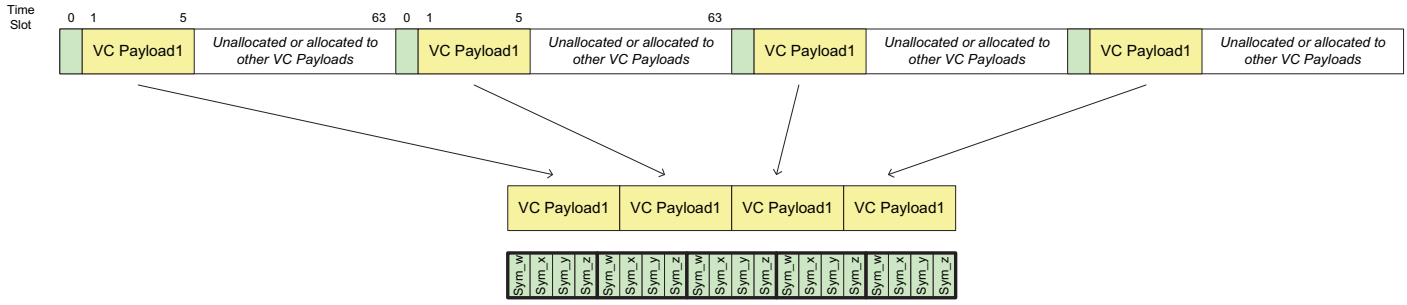


Figure 2-85: Repetition of 4-Symbol Sequence Unit Example for 1-Lane Main-Link

Table 2-138 summarizes the VC Payload control link symbol sequences.

Table 2-138: Summary of VC Payload Control Link Symbol Sequence

VC Payload Control Link Symbol Sequence[a]	Symbol Name	Control Code Sequence
VC Payload Fill Control	VCPF	C0-C1-C2-C3[b]
Stream Control		
Stream Framing Control	BS	C0-C0-C0-C0
	BE	C1-C1-C1-C1
	SS	C3-C3-C3-C3
	SE	C6-C6-C6-C6
Stream Fill Control	SF	C4-C4-C4-C4

a. VCPF symbols are generated either by a DP Source device for rate governing, or a DP Branch device when there is no stream symbol from the upstream device to forward to the downstream link. Stream symbols are generated by a DP Source device, not a DP Branch device.

b. C0, C1, C2, and C3 correspond to Sym_w, Sym_x, Sym_y, and Sym_z, respectively, in Figure 2-84.

Section 2.6.9 defines the control code to 8b/10b K-code mapping.

2.6.3.1 VC Payload Fill Symbol Sequence

The VC Payload Fill (VCPF) Symbol sequence inserted by Main-Link Symbol Manager is composed of four control link symbols, as listed in Table 2-138.

When there are no stream symbols to transmit while the link is enabled, the DPTX re-transmits the VCPF Symbol sequence.

The VCPF Symbol sequence is the only control sequence designed to allow for robust detection of the correct phase in the presence of bit errors. A single, isolated bit error **cannot** convert a non-VCPF Symbol sequence into a false VCPF Symbol sequence. With all other control sequences, a single bit error could cause a phase detection error. DPRXs shall use only the VCPF Symbol sequence to detect the phase of the 4-symbol sequence unit mapping to Main-Link lanes in the 2- and 1-lane cases. DPRXs shall continuously implement phase error correction to ensure recovery from any loss of 4-symbol sequence phase lock.

2.6.3.2 Stream Symbol Sequence

Stream symbols consist of data symbols and control link symbols.

2.6.3.2.1 Control Link Symbols

- BS, BE, SS, and SE Stream Framing control link symbols
- Stream Fill control link symbols
  - SF symbols are inserted when the Rate Governor in a DP Source device selects the Stream Symbol sequence generator side of Payload multiplexer (see Figure 2-83), but VC Payload Mapper does not have a meaningful Stream Symbol sequence to insert.
  - During the main video stream's blanking period, SF symbols are inserted by a DP Source device by default as there are no meaningful Stream Symbol sequences to insert. Those SF symbols during the blanking period are replaced with Stream Framing control link symbols, a VB-ID packet (composed of VB-ID, Mvid[7:0], and Maud[7:0], immediately following the BS control link symbol sequence), an MSA packet, and SDPs.
  - VB-ID, MSA packets, and SDPs shall **not** contain SF symbols (i.e., after the start of these packet types, SF symbols shall **not** be inserted until the complete packet has been transmitted; the only exception is for SF within an active video line during nested SDP transmission because SDP transmission does not resume until after BS/VB-ID transmission).

Table 2-138 lists the Stream control link symbol Control Code sequence.

In SST mode, every 512th BS is replaced with SR for scrambler reset. In other words, BS is used not only as a Stream Framing control link symbol (blanking start, corresponding to Display Enable falling edge of the main video stream), but also as a Link Timing control link symbol (i.e., SR as the Link Frame boundary and BS as the Link Line boundary). To enhance BS and SR control link symbol error immunity, Enhanced Framing Symbol sequence shall be used for BS and SR in SST mode, as described in Section 2.2.1.2.

In MST mode, the Link Frame boundary (SR, inserted once in 2^{16} time slots) is completely de-coupled from the timing of the stream the link is transporting. The BS symbol sequence is used only as a Stream Framing control link symbol and is never replaced with SR. The BS symbol sequence consists of four symbols, regardless of the lane count.

Note: *There is no control link symbol that marks the Link Line boundary in MST mode. It should be noted, however, that a notion of a Link Line may be established for any upper layer protocol that needs a Link Line boundary. This can be done by setting the Link Line boundaries relative to the Link Frame boundary, which is fixed to 2^{16} time slots. For example, there are 32 Link Lines per Link Frame if the Link Line interval is set to 32 MTPs.*

2.6.3.2.2 Data Symbols

- Main Stream data symbols
- VB-ID packet (VB-ID/Mvid[7:0]/Maud[7:0])
- MSA packet data symbols
- SDP data symbols, including Parity byte symbols

Stream data symbol mapping of MST mode is identical to that of SST mode in the 4-lane Main-Link configuration.

The AV stream is mapped into the VC Payload time slots of the stream, as illustrated in Figure 2-86 in MST mode, regardless of the Main-Link lane count that the DPTX is driving. In case the lane count is one or two lanes, the Lane Count Adjust block (see Figure 2-83) sequentially maps to the lane count, as illustrated in Figure 2-84.

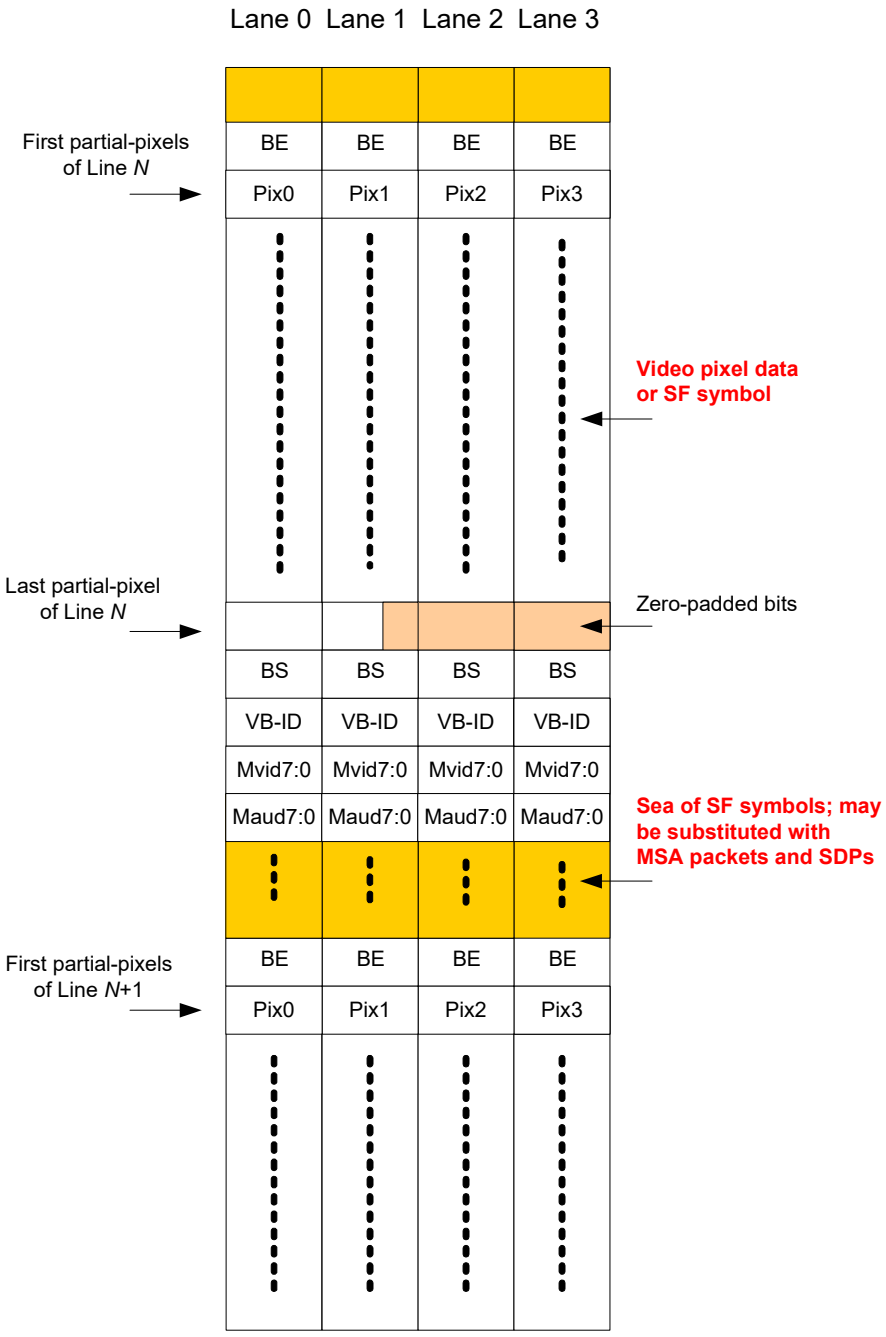


Figure 2-86: AV Stream Mapping in MST Mode After VC Payloads for a Given Main Video Stream are Concatenated and VC Payload Fill Symbol Sequences Removed

2.6.3.3 SDP Transport in MST Mode

Figure 2-87, Figure 2-88, and Figure 2-89 illustrate the logic block diagrams of Stream-to-VC Payload Mapping Layer of DP Source, Sink, and Branch devices, respectively.

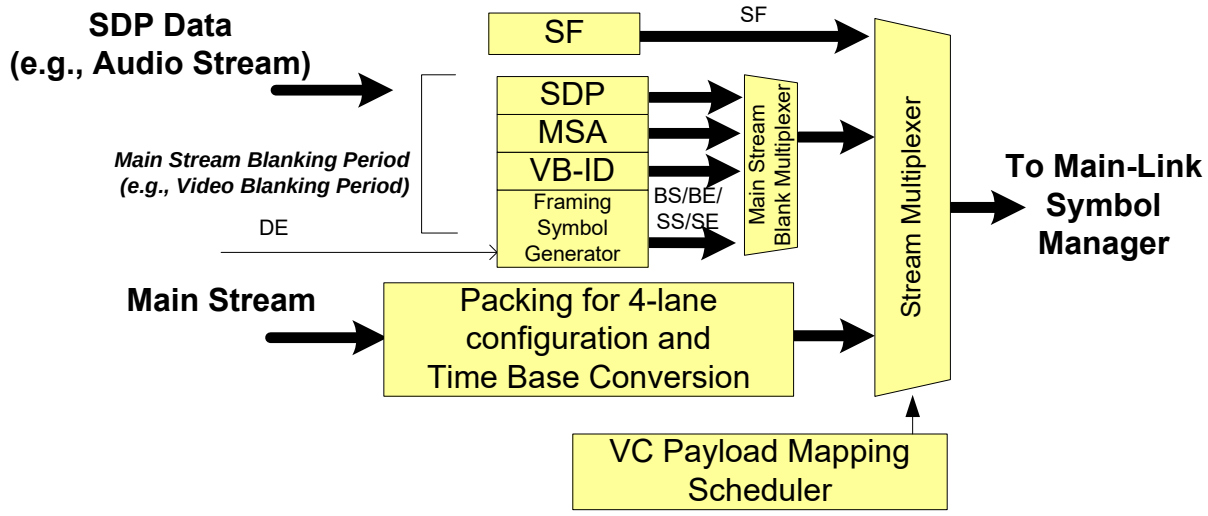


Figure 2-87: DP Source Device VC Payload Mapping Logic Block Diagram

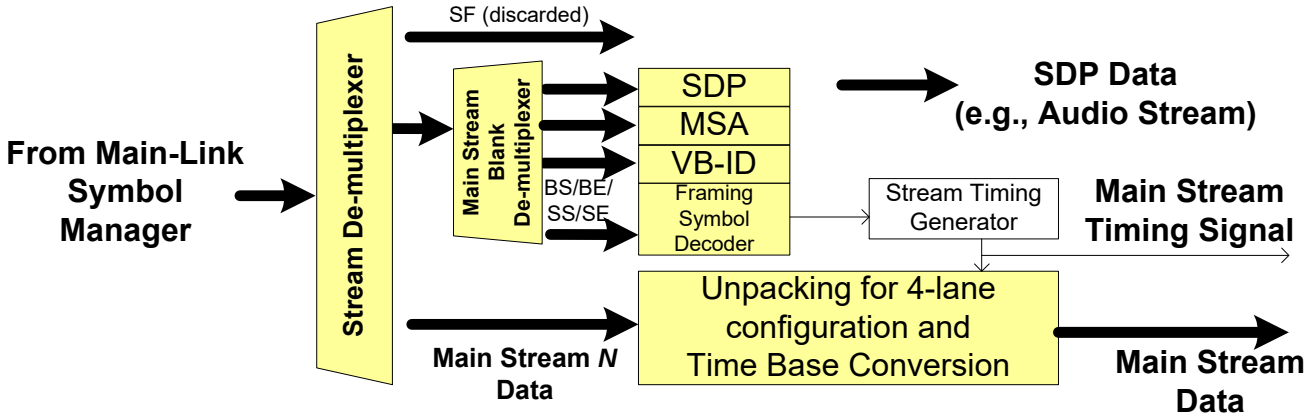


Figure 2-88: DP Sink Device VC Payload Mapping Logic Block Diagram

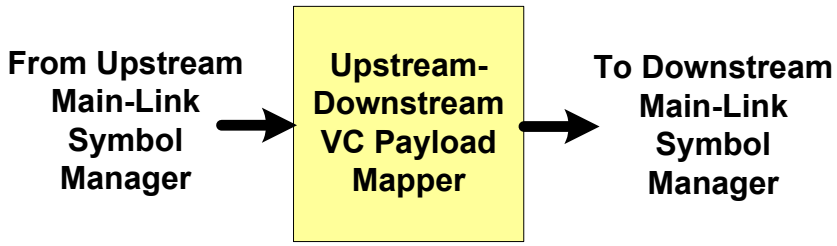


Figure 2-89: Pass-through DP Branch Device VC Payload Mapping Logic Block Diagram

From a stream interface standpoint, the VC Payload Mapping Layer is analogous to the Stream-to-Link Symbol Mapping Layer of SST mode. MST mode extension de-couples the transport from the stream generation, but re-uses the part of the Stream-to-Link Symbol Mapping Layer structure in SST mode to allow for commonality in MST and SST system implementation. As is the case with Stream-to-Link Symbol Mapping Layer in SST mode, the VC Payload Mapping Layer can receive a main video stream and one or more SDP streams.

There are three notable differences between MST and SST modes concerning SDP transport:

- Number of time slots available for SDP transport
- Support for SDP splitting – normative feature for MST-capable DP Branch/Sink devices
- Transport of SDP-only without a main video stream

2.6.3.3.1 Number of Data Symbols Available for SDP Transport (Informative)

In MST mode, a DPTX's Main-Link Symbol Mapper reads symbols from VC Payload Mapper in a DP Source device on every link symbol clock edge when the Rate Governor selects the Stream Symbol sequence generator side of Payload multiplexer during the VC Payload time slots for the stream. When there is no MSA data and VB-ID packet/MSA packet to transmit, an SDP may be transported.

This sub-section is informative because the number of SDP payloads to be transported is dependent on how the Source device packs the SDP. In this section, the example provided is an SDP payload size that is fixed to 32 bytes. Concatenating the payloads within a single SDP reduces the time slot usage overhead for SDP header and SE symbol insertion, and thus increases the data symbols that are available for SDP payload transport.

The number of MTPs per main video stream horizontal blanking period (MtpCntPerHBlank) is:

$$MtpCntPerHBlank = \frac{t\_HBlank}{64 \times t\_TimeSlot}$$

where:

- t_HBlank is the main video stream horizontal blanking period
- t_TimeSlot is the link time slot period (i.e., the Link Symbol Clock period)

The number of Stream symbols per t_HBlank (StrmSymblCntPerHBlank) is:

$$StrmSymblCntPerHBlank = MtpCntPerHBlank \times Throttled\_VCP\_Size \times LaneCnt$$

where:

- LaneCnt is the lane count of the Main-Link

During t_HBlank, a BS, VB-ID packet, and BE symbol sequence shall be transmitted, resulting in 20 StrmSymblCntPerHBlanks used for these symbols. Therefore, the number of Stream symbols available for SDP is as follows:

$$StrmSymblCntForSdpPerHBlank = StrmSymblCntPerHBlank - 20$$

SDP data has an overhead of SS, SE, Header, and Parity. Therefore, SdpDataEfficiency is:

$$SdpDataEfficiency = \frac{SdpDataSize}{SdpDataSize + SdpOverhead}$$

When the SDP data size is 32 bytes, for example, the total overhead is 24 bytes. Therefore, SdpDataEfficiency becomes:

$$SdpDataEfficiency = \frac{32}{32 + 24} = \frac{4}{7}$$

The number of symbols available for SDP Data per t_HBlank (SdpDataSmbCnt) is:

$$SdpDataSmbCnt = StrmSymblCntForSdpPerHBlank \times SdpDataEfficiency$$

The resulting SdpDataRate is:

$$SdpDataRate = SdpDataSmbCnt / t\_HPeriod$$

The SdpDataRate shall be greater than or equal to the peak data rate of the stream packed into the SDPs.

2.6.3.3.2 SDP Splitting in MST Mode

Note: *Support for SDP splitting in SST mode is defined in Section 2.2.5.13.*

In MST mode, a DP Source device has an option of SDP splitting. SDP splitting is the process of splitting SDPs with a main video stream including a BS/BE symbol sequence, associated data (VB-ID/Mvid[7:0]/Maud[7:0]), and MSA packet, as illustrated in Figure 2-90.

Only one level of splitting is allowed. SDP splitting by another SDP is prohibited. The SDP stream may be interrupted at any time, and may additionally be interrupted more than once (e.g., such as when the HBlank period is short and the SDP length is long). SDP interruption and resumption shall occur at the 4-symbol sequence boundary.

A DP MST Sink device shall be capable of reassembling the nested SDP.

SDP splitting in SST and MST modes shall be supported for a DP Sink/Branch device.

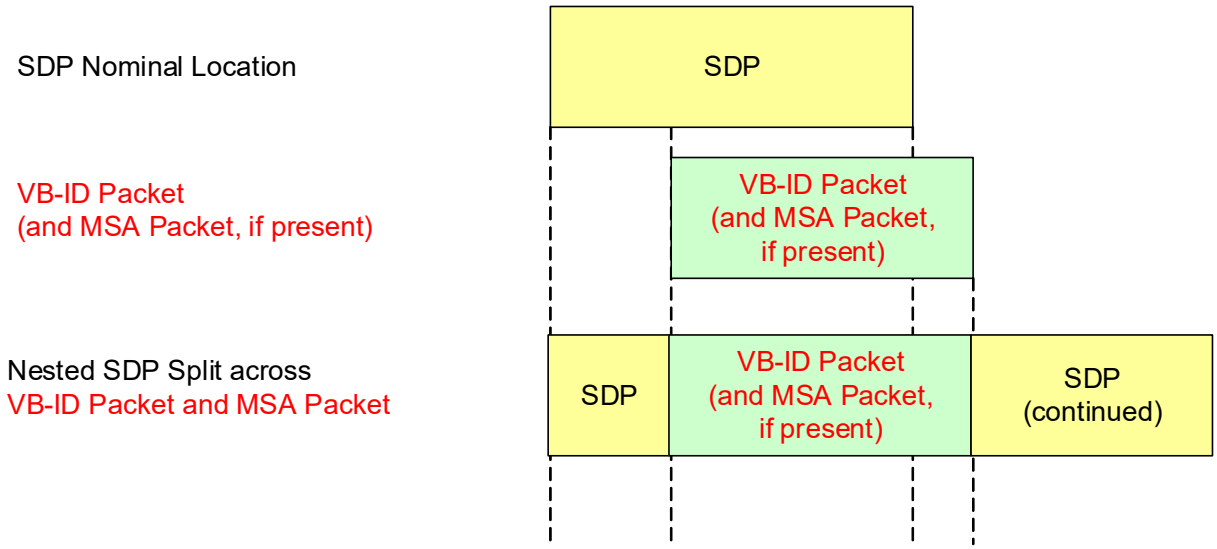


Figure 2-90: SDP Splitting in MST Mode

2.6.3.3.3 SDP-only Transport without Main Video Stream

MST mode, as is the case with SST mode, supports the transport of an SDP-only stream that does not have a main video stream (e.g., an audio-only stream that does not have a main video stream). In this condition, a BS control link symbol sequence followed by a VB-ID packet is inserted every 1024th time slot of the VC Payload where the SDP is transported.

2.6.3.3.4 No SDP/Main Stream

Regardless of whether a main video stream or SDP stream is being transmitted, the BS control link symbol sequence followed by a VB-ID packet is inserted every 1024th time slot of the VC Payload replacing SF symbol sequences as long as the DP Source device sets the Rate Governing block to select the Stream symbol generator side of the VC Payload Multiplexer. The DP Source device may stop the insertion of stream symbols by always selecting the VCPF symbol sequence (which is done by setting the TARGET_Average_StreamSymbolTimeSlotsPerMTP to 0.0, as defined in Section 2.6.4).

2.6.4 Time Slot Count Allocation to VC Payload

Aside from the MTPH time slot, the remaining 63 time slots of the MTP are available for allocation to one or multiple VC Payloads. The layer that manages the allocation of the time slots to VC Payloads is the Payload Bandwidth Manager.

There are two types of Payload Bandwidth Managers:

- One in a DP MST Source device, referred to as the “Source Payload Bandwidth Manager”
- One in DP MST Branch devices, referred to as the “Branch Payload Bandwidth Manager”

Working together, Source and Branch Payload Bandwidth Managers ensure the following:

- Allocate sufficient bandwidth to the VC Payloads constituting the virtual channel from the Source device to the target Sink device for transporting a stream without causing overflow of buffers in the path
- Minimize the VC Payload bandwidth allocation overhead so that the number of streams transported over the DP links can be maximized

Source Payload Bandwidth Manager has the following responsibilities:

- Determine the peak bandwidth of a stream it needs to transport
- From the peak stream bandwidth, calculates the Payload Bandwidth Number (PBN) value for the stream to be transported and passes the PBN value to the downstream Branch devices by way of an ALLOCATE_PAYLOAD message transaction
- Calculate the VC Payload size in time slot count of the link it is driving and throttles the Stream Symbol sequence insertion rate so that transmission of the Stream Symbol sequence is evenly distributed over multiple MTPs

Branch Payload Bandwidth Manager has the following responsibility:

- Upon receiving the PBN value, calculates the smallest possible VC Payload size in time slot count of the link it is driving that provides for sufficient bandwidth for the PBN value

Figure 2-91 illustrates the interaction between the DP Source and Branch Device Payload Bandwidth Managers.

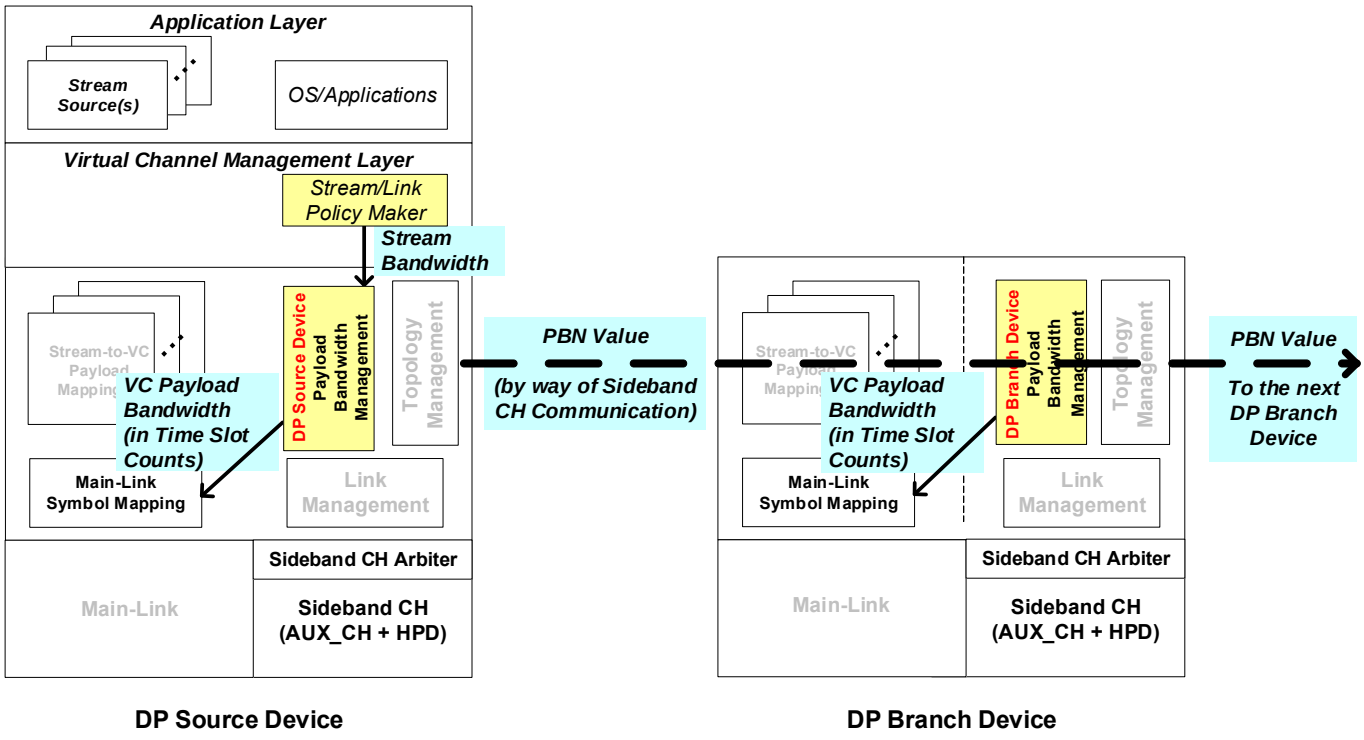


Figure 2-91: Bandwidth Management by Payload Bandwidth Manager

2.6.4.1 PBN Value Calculation by a Source Device Payload Bandwidth Manager

The PBN is an integer number calculated by the Source device Payload Bandwidth Manager, representing a peak bandwidth of a stream to be transported in a VC Payload. The PBN value has the unit of 54/64MBps.

Note: *The unit of 54/64MBps is an arbitrary unit, based on a common multiplier to render an integer PBN for all link rate/lane counts combinations.*

The Source Payload Bandwidth Manager calculates a PBN value using a peak stream bandwidth value. The calculated value is likely to have a fraction. The Source Payload Bandwidth manager adds a 0.6% margin to the calculated fractional PBN value and rounds it up to the closest integer. This integer PBN value is the value that the Source Payload Bandwidth Manager passes to downstream Branch devices.

The 0.6% margin accounts for the deviation of the link rate driven by a downstream DP Branch device (as small as nominal link rate minus 5300ppm, or 0.53%, including link rate down spreading), as well as the link rate driven by the DP Source device itself (as large as nominal link rate plus 300ppm, or 0.03%).

The following example illustrates how the PBN value is determined for a pixel stream with a pixel rate of 154MP/s (i.e., WUXGA, 1920x1200 at 60Hz of vertical frame rate with reduced horizontal blanking) and pixel data size of 30bpp (or 3.75 bytes per pixel).

$$
\begin{aligned}
PeakPixelBandwidth &= 154MHz \times 30BitsPerPixel / 8BitsPerByte \\
&= 577.5MBps \\
&= 577.5MBps \times \frac{1}{54/64MBps / PBN} \\
&= 684.444PBN \\
&\quad ADDITION\_OF\_0.6\%\_MARGIN \\
&\quad \texttt{CEIL(}684.444 \times 1.006\texttt{)} = 689PBN
\end{aligned}
$$

2.6.4.1.1 PBN Value Calculation with FEC Encoding/Decoding Enabled

New to *DP v1.4*.

FEC overhead of 2.4%, down-spreading overhead of 0.5%, and MST Branch device link reference clock difference of up to 0.06% (= 600ppm) add up to approximately 3% total overhead.

A DP MST Source device shall use the following equation to calculate the effective PBN value to be communicated to the downstream devices by way of ENUM_PATH_RESOURCES and ALLOCATE_PAYLOAD message transactions from the native PBN value derived from the pixel rate and pixel bit depth.

$$PBN\_EFFECTIVE = PBN\_NATIVE \times 100 / (100 - 3)$$

The DP MST Source device shall evenly distribute the additional valid pixel data symbols across its VC Payload time slots, per MTP, to account for the time slots occupied by FEC_PARITY_PH and FEC_PM Link Layer symbols.

To avoid the 2.4% FEC overhead, the DP Source device may choose to not use FEC by clearing the FEC_READY bit in the FEC_CONFIGURATION register (DPCD Address 00120h, bit 0) to 0 prior to link training. If the DP Source device needs to use FEC at a later time, the device shall first set the FEC_READY bit, initiate link training, and then enable FEC encoding after link training completes.

2.6.4.2 VC Payload Size Determination by Branch Payload Bandwidth Manager

The unit of the PBN value simplifies the task of determining the VC Payload size in time slot count for the Branch Payload Bandwidth Manager. The Branch Payload Bandwidth Manager determines the VC Payload size (in time slot count per MTP), as follows:

$$VCPayload\_Size\_Branch = CEIL(PBN\_Value / VCPayload\_Bandwidth\_for\_OneTimeSlotPer\_MTP\_Allocation)$$

For example, a 4-lane Main-Link at RBR (1.62Gbps) has a link bandwidth of 648MBps. When the Branch Payload Bandwidth Manager allocates one time slot per MTP to a VC Payload, the resulting VC Payload Bandwidth is 648MBps × 1 time slot/64 time slots, which is equal to 12 × 54 / 64MBps or 12 PBN.

For the above pixel stream with the PBN value of 689, the Branch Payload Bandwidth Manager driving its downstream Main-Link at RBR over four lanes sets the VC Payload size in time slot count per MTP, as follows:

$$VCPayload\_Size\_Branch = CEIL(689PBN / 12PBN / TimeSlotsPerMTP = 58TimeSlots/MTP)$$

A Branch device's DPTX may be driving the link at a rate that is lower than the nominal link rate due to down spread (0.5% maximum from the nominal) and the reference clock variation (±300ppm or ±0.03% from the nominal). As noted earlier, the Source device Payload Bandwidth Manager adds a 0.6% margin when it calculates to account for those deviations.

Table 2-139 defines the VC Payload bandwidths (in PBN) when one time slot is allocated per every MTP for various link configurations.

Table 2-139: VC Payload Bandwidth for One Time Slot per MTP Allocation for Various Link Configurations

Link Type	# of Lanes	Nominal Link Bandwidth (Excluding 8b/10b Link Layer Overhead) (MBps)	VC Payload Bandwidth When One Time Slot Per Every MTP Is Allocated (PBN)
HBR3	1	810	15
	2	1620	30
	4	3240	60
HBR2	1	540	10
	2	1080	20
	4	2160	40
HBR	1	270	5
	2	540	10
	4	1080	20
RBR	1	162	3
	2	324	6
	4	648	12

2.6.4.3 VC Payload Size Determination by a Source Payload Bandwidth Manager

As noted earlier, it is only a DP Source device that generates Stream Symbol sequences. The Source Payload Bandwidth Manager calculates the average Stream Symbol time slots per MTP over the link it is driving (i.e., between the Source device and the first device with a Branching Unit), as follows:

$$Average\_Strea,SymbolTimeSlotsPerMTP = PeakStreamBandwidth / LinkBandwidth \times 64$$

The Source Payload Bandwidth Manager rounds up the Average_StreamSymbolTimeSlotsPerMTP to set the VCPayload_Size_Source, as follows:

$$VCPayload\_Size\_Source = CEIL(Average\_StreamSymbolTimeSlotsPerMTP = PeakStreamBandwidth / LinkBandwidth \times 64)$$

The Source Payload Bandwidth Manager throttles Stream Symbol insertion rate so that the average of Stream Symbol time slots per MTP is evenly distributed to TARGET_Average_StreamSymbolTimeSlotsPerMTP:

$$TARGET\_Average\_StreamSymbolTimeSlotsPerMTP = TS\_INT + TS\_FRAC\_enum / TS\_FRAC\_denom$$

where:

- TS_INT is an integer
- TS_FRAC_enum / TS_FRAC_denom is a simplified fraction

The TARGET_Average_StreamSymbolTimeSlotsPerMTP value shall not be smaller than the Average_StreamSymbolTimeSlotsPerMTP. The TARGET_Average_StreamSymbolTimeSlotsPerMTP may be higher than the Average_StreamSymbolTimeSlotsPerMTP, as long as the following condition is met:

$$Maximum\_TARGET\_Average\_StreamSymbolTimeSlotsPerMTP \leq PBN\_Value\_to\_DownstreamBranchDevices / (LinkBandwidth\_Source \times 54)$$

where:

- LinkBandwidth_Source is the bandwidth of the link that is being driven by the Source device

For 4-lane Main-Link, the number of Stream Symbol time slots per MTP fluctuates between TS_INT and [TS_INT + 1] over the TS_FRAC_denom MTPs. TS_FRAC_enum MTPs have [TS_IN + 1] Stream Symbol time slots and [TS_FRAC_denom - TS_FRAC_enum] MTPs have TS_INT Stream Symbol time slots. Those TS_FRAC_enum MTPs with [TS_INT + 1] Stream Symbol time slots shall be evenly distributed over TS_FRAC_denom MTPs.

For 1- and 2-lane Main-Link configurations, the fact that symbol sequences are 4-symbol multiples affects how the Stream Symbols insertion rate gets throttled. Over the [TS_FRAC_denom × 4 / LaneCount] MTPs, the stream symbols per MTP shall be evenly distributed to TARGET_Average_StreamSymbolTimeSlotsPerMTP value.

When the PeakStreamBandwidth is 577.5MBps and when the bandwidth of the link Source device is driving is 1080MBps (i.e., 4-lane HBR):

$$Average\_StreamSymbolTimeSlotsPerMTP = 577.5MBps / 1080MBps \times 64 = 34.222$$

Therefore, the Source Payload Bandwidth Manager sets the VCPayload_Size_Source to 35 time slots. The maximum allowed TARGET_Average_StreamSymbolTimeSlotsPerMTP is:

$$Maximum\_Target\_Average\_StreamSymbolTimeSlotsPerMTP = 689 \times 64 \times (54 / 64) / 1080 = 34.45$$

Thus, the Source Payload Bandwidth Manager may set the TARGET_Average_StreamSymbolTimeSlotsPerMTP to 34.25 (i.e., TS_INT = 34, TS_FRAC_enum = 1, TS_FRAC_denom = 4).

One out of four MTPs has 35 Stream Symbol time slots with 0 VCPF Symbol time slots within the VC Payload. Three out of four MTPs have 34 Stream Symbol time slots with 1 VCPF Symbol time slot.

2.6.4.3.1 Maximum Allowed Rate Governing Deviation from Target Average for a Source Device

A DP Source device shall throttle the Stream Symbol insertion rate so that the accumulation of transmitted stream symbol count is in the following range at the beginning of any MTP:

$$ACTUAL\_AccumulatedSymbolCount > TARGET\_AccumulatedSymbolCount - 8$$

$$ACTUAL\_AccumulatedSymbolCount \leq TARGET\_AccumulatedSymbolCount$$

The remainder of this sub-section describes the rationale behind the maximum allowed rate governing deviation above and should be regarded as informative.

For each MTP, the target number of transmitted stream symbols for a given VC Payload is *M*:

$$M = LaneCount \times (TS\_INT + TS\_FRAC\_enum / TS\_FRAC\_denom$$

For each MTP, the actual number of transmitted stream symbols is *N*:

$$N = \sum_{\substack{TimeSlots \\ inVCPayload}} (LaneCount - RG)$$

where:

- RG = 4, if the time slot is occupied by the first VCPF code (VCPF0, or C0), –or–
- RG = 0, otherwise

Note: *VCPF symbols occupy 4/LaneCount time slots; therefore, N's temporary decrease for a 2- or 1-lane LANE_COUNT represents that a decision to introduce VCPF0 on a given time slot shall cause subsequent time slot(s) to be occupied by the remaining VCPF codes (C1, C2, and C3). Additionally, insertion of VCPF symbols in a VC Payload within one MTP may span to the VC Payload of the next MTP in a 2- or 1-lane Main-Link.*

Calculate the delta *D* accumulation between the target and actual number of transmitted symbols:

$$D = \sum_{MTPs} (N - M)$$

The *D* value is per MTP, not per time slot in a given MTP.

Insert VCPF0 (the first code of the VCPF Symbol sequence) **only when** D shall otherwise exceed 0.

Summarizing:

$$D = \left(\sum_{MTPs} \left(\sum_{\substack{TimeSlots \\ inVCPayload}} (LaneCount - RG) - LaneCount * (TS\_INT + TS\_FRAC\_ENUM / TS\_FRAC\_DENOM) \right) \right)$$

where:

- RG = 0 or 4

The limit on the variability of D is determined by the following factors:

- Because symbols are inserted in sets of four and the constraint $D \leq 0$ shall be met, the VCPF insertion algorithm shall insert VCPF symbol **only when** the D value on the current time slot would be less than four with a VCPF symbol inserted. The resulting variability is $-4 < Delta1 \leq 0$.
- Because VCPF symbols are inserted in sets of four, in the 1-lane case a decision to insert VCPF0 shall result in VCPF1 through VCPF3 in the next three allocated time slots. The resulting variability is $-3 \leq Delta2 \leq 0$. In the 2-lane case, only the next allocated time slot after the start of VCPF Symbol Sequence shall contain VCPF symbol, and in the 4-lane case, each VCPF Symbol Sequence is transmitted completely within the single time slot.

Adding up *Delta*1 and *Delta*2, $-7 < Delta1 + Delta2 \leq 0$, determines the minimum possible variability range for D. For simplicity (because all symbols are managed in sets of four at the Stream to VC Payload Mapping Layer), the range of D (when measured at the start of an MTP) is constrained to:

$$-8 < D \leq 0$$

Thus, the contribution to the rate variability observed at the DPRX due to rate governing in the Source device is eight symbols.

2.6.4.3.2 Rate Governing Sample Pseudo-Code (Informative)

The following pseudo-code is provided to illustrate how rate governing could be implemented with a simple state machine.

Note: *This example implementation is for reference purposes only.*

RG Parameters:

```
   D // range of D is -256 to 0 so 8 integer (no sign) bits are required; number
of fractional bits is equal to number of bits of Y value
   X.Y // X.Y calculated by multiplying
TARGET_Average_StreamSymbolTimeSlotsPerMTP by Lane Count. X is an 8-bit value in
the range 0 to 252, Y is implementation-dependent but should be at least 2 bits
and ideally more
```

Other Parameters (not specifically for rate governing but referenced below):

```
  PHASE // 2-bit value to represent the four phases in the single-lane case,
or two phases in two-lane case
  LANE_COUNT // 2-bit value; 1 = 1-lane, 2 = 2-lane, 0 = 4-lane
```

Initial condition and no time slot allocated to a VC Payload:

```
  Set D = 0
  Set X.Y = 0
  Set PHASE=0
```

At least sixteen symbols after ACT for new VC Payload time slot allocation, and at any time for existing or reallocated VC Payload:

```
  Update X.Y to nonzero value (new X.Y automatically takes effect on next MTPH)
If MTPH Time Slot
{
  D = D - X.Y
}
else if VC Time Slot
{
  if PHASE = 0  // Only decide whether to start RG or VC data on phase zero since
both are transmitted in sets of four
  {
    if D <= -4  // Ensures that four Stream Symbols cannot cause D > 0
    {
     Read (from VC Payload Mapper) and start transmitting set of four
Stream Symbols
     D <= D + 4  // Decrement D by amount of data that will be transmitted
(some may be in subsequent time slots)
    }
    else
    {
      start Rate Governing  // Don't update D since no data was transmitted
    }
  else
  {
     continue previously started 4-symbol sequence (VCPF Symbols or Stream
Symbols)  // Don't update D since the change in D (if any) in the PHASE=0 case
was already accounted for
  }
  PHASE = PHASE + LANE_COUNT
}
```

2.6.5 VC Payload Allocation Synchronization Management

Prior to starting a stream transfer from a stream Source to a stream Sink, a Stream Policy Maker, based on the topology map information provided by the Topology Manager, establishes the virtual channel connection between the stream Source and Sink with the help of Payload Bandwidth Managers in the DP Source and Branch devices in the path. The Payload Bandwidth Manager maps the virtual channel to a VC Payload on a DP link.

The Payload Bandwidth Manager establishes and maintains VC Payloads it is receiving and transmitting/forwarding by managing the VC Payload ID Table. The Payload Bandwidth Manager:

- Keeps its VC Payload ID Table synchronized with that of the downstream device's DPRX that it is driving through Native AUX transactions
- Keeps the VC Payload time slot allocation over the Main-Link synchronized with the VC Payload ID Table through an ACT sequence inserted into MTPH time slots

Each DPTX and DPRX of an MST-capable device has a VC Payload ID Table. The table within the DPRX is mapped to the DPCD Address space, as listed in Table 2-140. Reading of the DPRX's VC Payload ID Table by the immediate upstream DPTX's Payload Bandwidth Manager shall **not** be required for normal operation. When to read this table (e.g., for debugging purposes) is an implementation-specific choice for DP Source and Branch device developers.

Though it is possible for an upstream device to update the VC Payload ID Table of a remote downstream device by way of a REMOTE_DPCD message transaction, the remote update of a VC Payload ID Table is prohibited. Only the immediate upstream device is allowed to update the VC Payload ID Table of the downstream device because only the immediate upstream device is capable of initiating the ACT sequence over the Main-Link.

Table 2-140: 8b/10b Channel Coding VC Payload ID Table of DPRX Mapped to DPCD Address Space

DPCD Address	Time Slot	VC Payload ID (7-bit value RO)[a]
002C1h, Bits 6:0	1	1
002C2h, Bits 6:0	2	1
002C3h, Bits 6:0	3	1
002C4h, Bits 6:0	4	1
002C5h, Bits 6:0	5	1
002C6h, Bits 6:0	6	3
002C7h, Bits 6:0	7	3
002C8h, Bits 6:0	8	3
002C9h, Bits 6:0	9	3
002CAh, Bits 6:0	10	3
002CBh, Bits 6:0	11	3
002CCh, Bits 6:0	12	3
002CDh, Bits 6:0	13	3
002CEh, Bits 6:0	14	4
002CFh, Bits 6:0	15	4
002D0h, Bits 6:0	16	4
002D1h, Bits 6:0	17	4
002D2h, Bits 6:0	18	4
002D3h, Bits 6:0	19	4
002D4h, Bits 6:0	20	4
002D5h, Bits 6:0	21	4
002D6h, Bits 6:0	22	5
002D7h, Bits 6:0	23	5
002D8h, Bits 6:0	24	5
002D9h, Bits 6:0	25	5
002DAh, Bits 6:0	26	5
002DBh, Bits 6:0	27	0
002DCh, Bits 6:0	28	0
002DDh, Bits 6:0	29	0
002DEh, Bits 6:0	30	0
…	…	…
002FFh, Bits 6:0	63	0

*a. This table illustrates an example in which VC Payload ID #2 has been deleted. Time slots with VC Payload ID value 0 are **not** allocated.*

The VC Payload ID assignment is uniquely managed by each Payload Bandwidth Manager of a DP device with a DPTX. The Payload Bandwidth Manager of a DP Branch device shall maintain the mapping of the VC Payload Mapping Tables of its DPRXs to those of its DPTXs.

The VC Payload ID Table of a DPRX is updated by the Payload Bandwidth Manager of the immediate upstream device, by way of Native AUX transactions to the DPCD addresses described in Table 2-141.

Table 2-141: 8b/10b Channel Coding DPCD Address Map for VC Payload Table Update and ACT Status Verification[a]

DPCD Address	Bit #	Definition	Read/Write over AUX_CH
001C0h	**PAYLOAD_ALLOCATE_SET** Writing 00h, 00h, and 3Fh to DPCD Addresses 001C0h, 001C1h, and 001C2h, respectively, clears the entire VC Payload ID table. When this occurs, the DPRX immediately ignores the incoming VC Payloads (if any) without waiting or ACT on the Main-Link.		Write/Read
	6:0	**VC Payload ID to Be Allocated** ID of 0 indicates that the time slots are unallocated.	
001C1h	**PAYLOAD_ALLOCATE_START_TIME_SLOT**		Write/Read
	5:0	**Starting Time Slot of VC Payload ID in DPCD Address 002C0h**	
001C2h	**PAYLOAD_ALLOCATE_TIME_SLOT_COUNT**		Write/Read
	6:0	**Time Slot Count of VC Payload ID in DPCD Address 002C0h**	
002C0h	**PAYLOAD_TABLE_UPDATE_STATUS**		Clearable Read Only
	0	**VC Payload ID Table Updated** 0 = Not updated since the last time that this bit was cleared. 1 = Updated, cleared to 0 when the DP Source device writes 1.	
	1	**ACT Handled** 0 = ACT is not handled since the last time that this bit was read. 1 = ACT is handled, cleared to 0 when the VC Payload ID Table Updated bit (bit 0) is set to 1.	

a. This table duplicates DPCD Address information for the registers described here, from Table 2-184 (DPCD Addresses 001C0h through 001C2h) and Table 2-185 (DPCD Address 002C0h). Only non-RESERVED register bits are listed.

The Payload Bandwidth Manager writes the VC Payload ID, its start location and size in time slot count, by way of a Native AUX write transaction to DPCD Addresses 001C0h, 001C1h, and 001C2h, respectively.

To delete a VC Payload, the Payload Bandwidth Manager writes the VC Payload ID to be deleted to DPCD Addresses 001C0h, its start location before deletion to DPCD Addresses 001C1h, and a value of 00h to DPCD Addresses 001C2h. Clearing the ID to 00h, the start location to 00h, and programming the size to 3Fh clears the DPRX's entire VC Payload ID Table.

After the Payload Bandwidth Manager verifies that the VC Payload ID Table is updated (VC Payload ID Table Updated bit in the PAYLOAD_TABLE_UPDATE_STATUS register (DPCD Address 002C0h, bit 0) is set to 1), the Payload Bandwidth Manager shall trigger the VC Payload allocation over the Main-Link by inserting an ACT sequence into four consecutive MTPH time slots, as illustrated in Figure 2-92. The ACT sequence is always preceded by the 32 MTPH time slot Encryption Control Field (ECF), as described in Section 2.6.11. The ACT sequence shall **not** be inserted in the following MTPH time slots:

- 36 to 5 MTPH time slots prior to Link Frame boundary SR
- Time slot for SR
- 1 to 34 MTPH time slots following SR

Furthermore, the ACT sequence shall not straddle the above keep-out MTPH time slots.

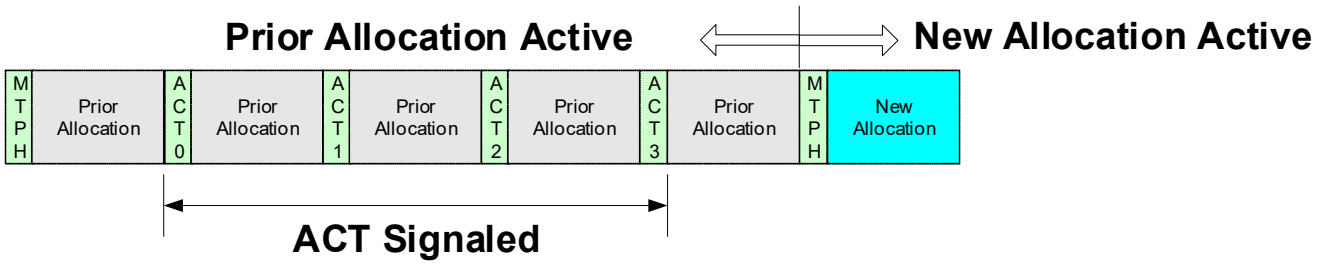


Figure 2-92: ACT Sequence

The Payload Bandwidth Manager then confirms the successful handling of ACT sequence by the downstream DPRX by reading the ACT Handled bit in the PAYLOAD_TABLE_UPDATE_STATUS register (DPCD Address 002C0h, bit 1, is set to 1).

Using the Native AUX transactions and ACT sequence described above, Payload Bandwidth Manager may add a new VC Payload (new allocation), change a VC Payload size (decrease/ increase), or delete a VC Payload (de-allocation). In any event, a Branch device's Payload Bandwidth Manager shall eliminate any unallocated time slots in between VC Payloads, as illustrated in Figure 2-93.

When a DPRX receives an ACT sequence without any change to values at DPCD Addresses 001C0h through 001C2h, the DPRX shall not make any changes to the VC Payload allocation.

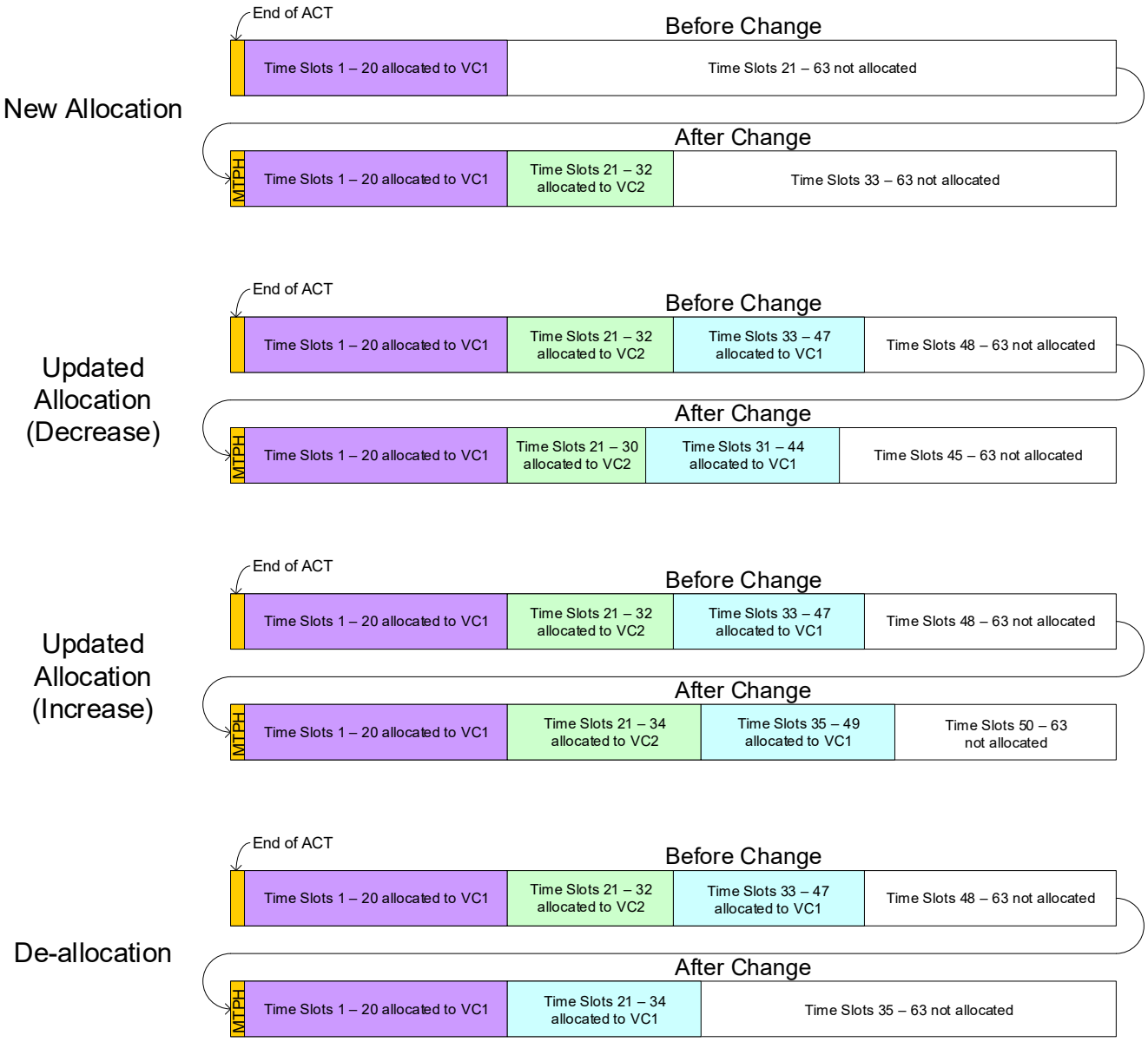


Figure 2-93: VC Payload Allocation Change

2.6.6 ALLOCATE_PAYLOAD Timing Sequence

To synchronize the VC Payload time slot allocation change across the multiple links of the path, Payload Bandwidth Manager issues an ALLOCATE_PAYLOAD Message Transaction. This section describes the timing sequence of interactions among the Payload Bandwidth Manager, Main-Link Symbol Manager, and VC Payload Mapper surrounding an ALLOCATE_PAYLOAD Message Transaction.

An ALLOCATE_PAYLOAD Message Transaction uses the VC Payload ID and PBN values as the variables of this transaction. Optionally, the DP MST Source device may execute an ENUM_PATH_RESOURCES Message Transaction to check the path's available PBN value before executing an ALLOCATE_PAYLOAD Message Transaction.

An MST Source device targets both ENUM_PATH_RESOURCES and ALLOCATE_PAYLOAD at the last MST device with a branching unit driving a stream sink. In other words, the Payload Bandwidth Manager of a DP Source device sets the Relative Address (RAD) field of the header of the Message Transaction to point to the last MST device with a branching unit. The port number (either physical or logical) of the branching unit to which the Sink device is plugged to is included in the body of the Message Transaction.

When transporting an SDP stream (e.g., an audio stream), the Payload Bandwidth Manager of a DP Source device specifies the SDP stream sink number in the body of the ALLOCATE_PAYLOAD Message Transaction.

Figure 2-94 illustrates a timing sequence for adding a new payload. The Payload Bandwidth Manager of each DPTX in the path, upon receiving ALLOCATE_PAYLOAD message transaction, updates the VC Payload ID Table and VC Payload time slot allocation, using the procedures described in Section 2.6.5. Once successful, it forwards the message transaction to its downstream DP device in the path.

When DP Source device's Payload Bandwidth Manager verifies that the ACT sequence has been successfully handled by the downstream device's DPRX, the manager may set the Throttled_VCP_Size (i.e., X.Y) value to the non-zero value to start the Stream Symbol Sequence insertion at least 16 MTPs after the new VC Payload is established.

The Payload Bandwidth manager of a DP Branch device, upon verifying the successful handling of the ACT, waits for 16 MTPs after the new VC Payload is established and starts forwarding Stream Symbol Sequence from the upstream DP device.

Figure 2-95 illustrates a timing sequence for adding a new payload that results in error. Upon receiving NAK Reply Message to ALLOCATE_PAYLOAD message transaction it has initiated, the Payload Bandwidth Manager of the DP Source device issues another ALLOCATE_PAYLOAD with PBN value cleared to 0 to delete the VC Payloads from the links on which the VC Payload allocations have just been completed.

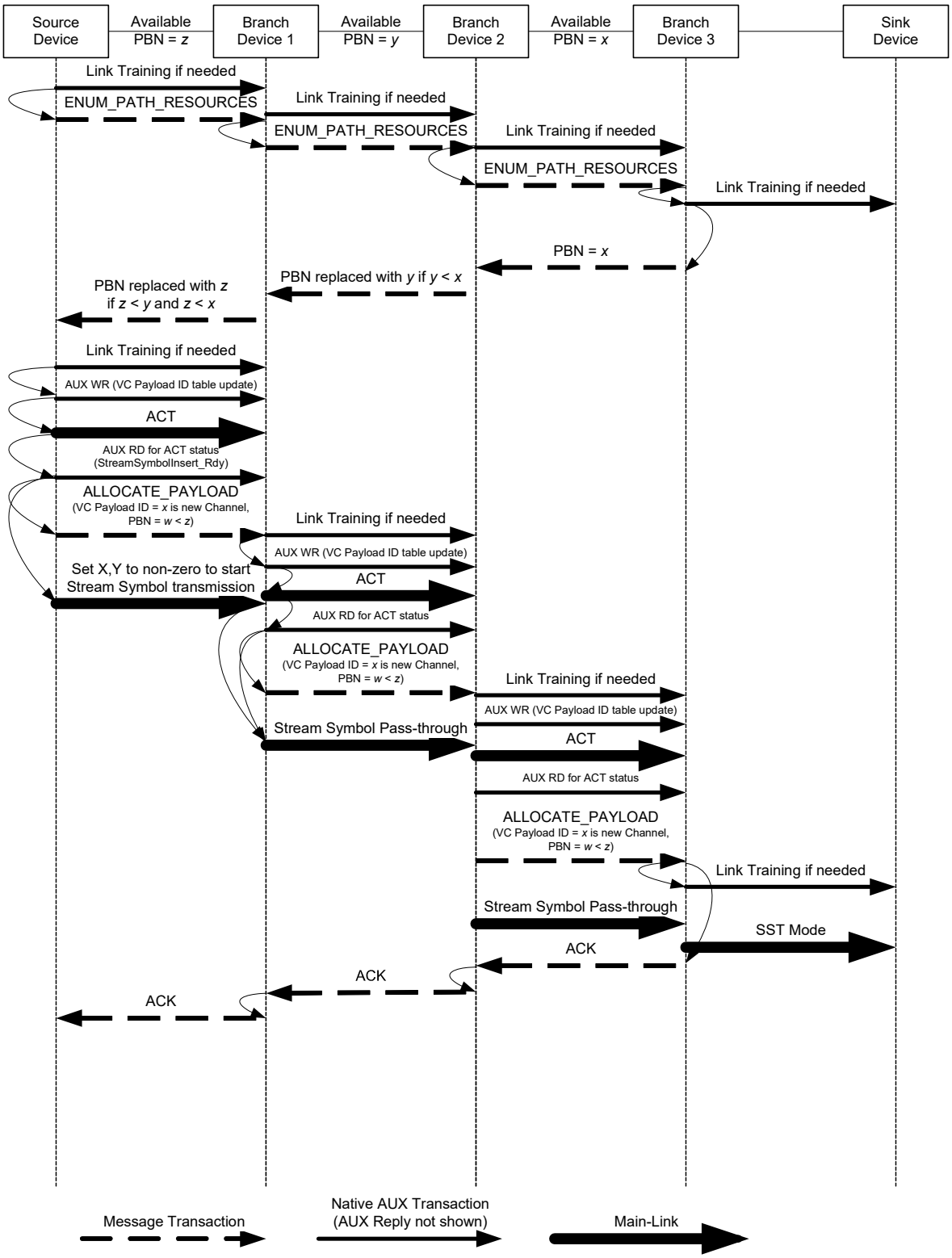


Figure 2-94: Time Sequence for Adding a New Payload Example

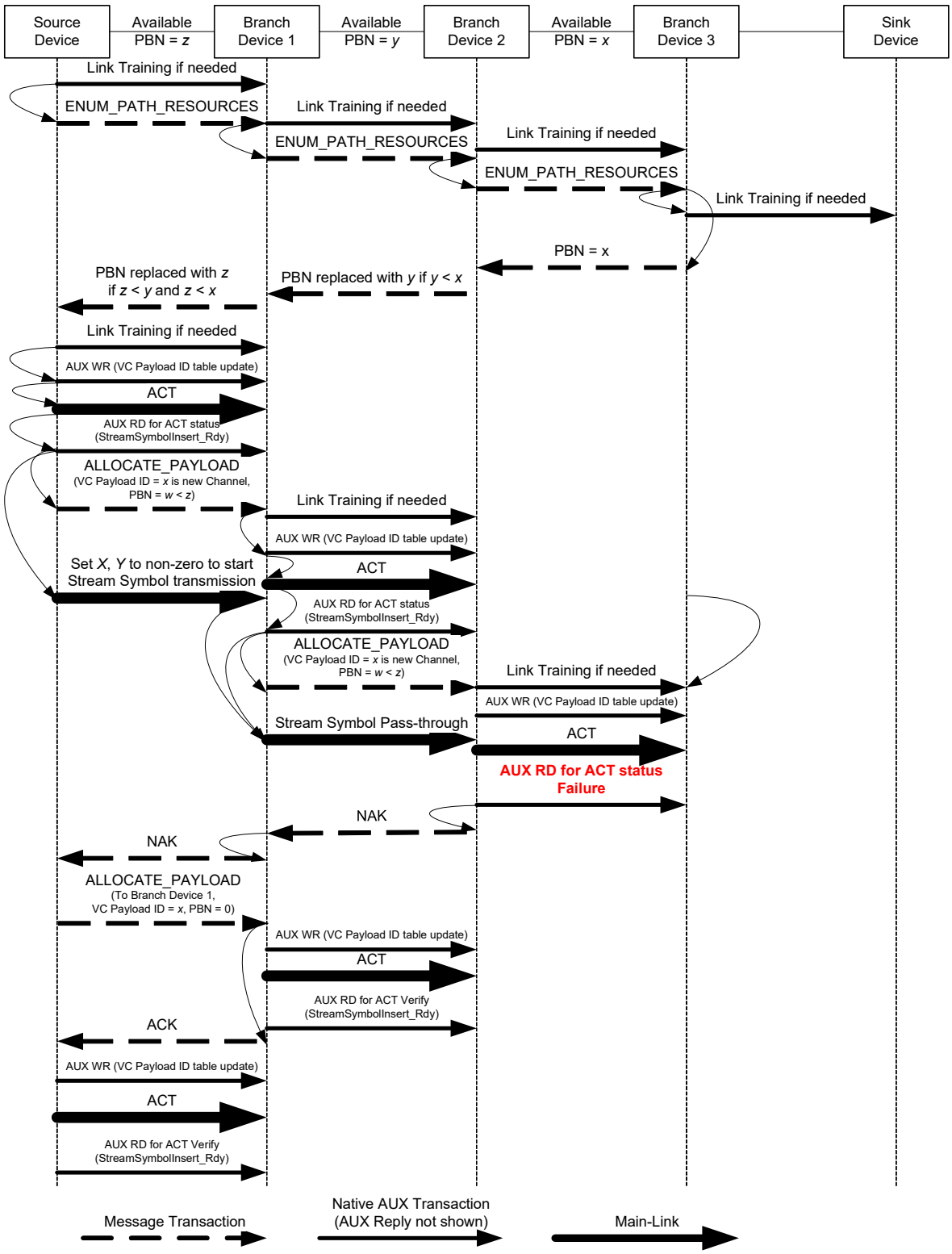


Figure 2-95: Timing Sequence for Adding a New Payload with Error

Figure 2-96 illustrates a timing sequence for successfully deleting a payload.

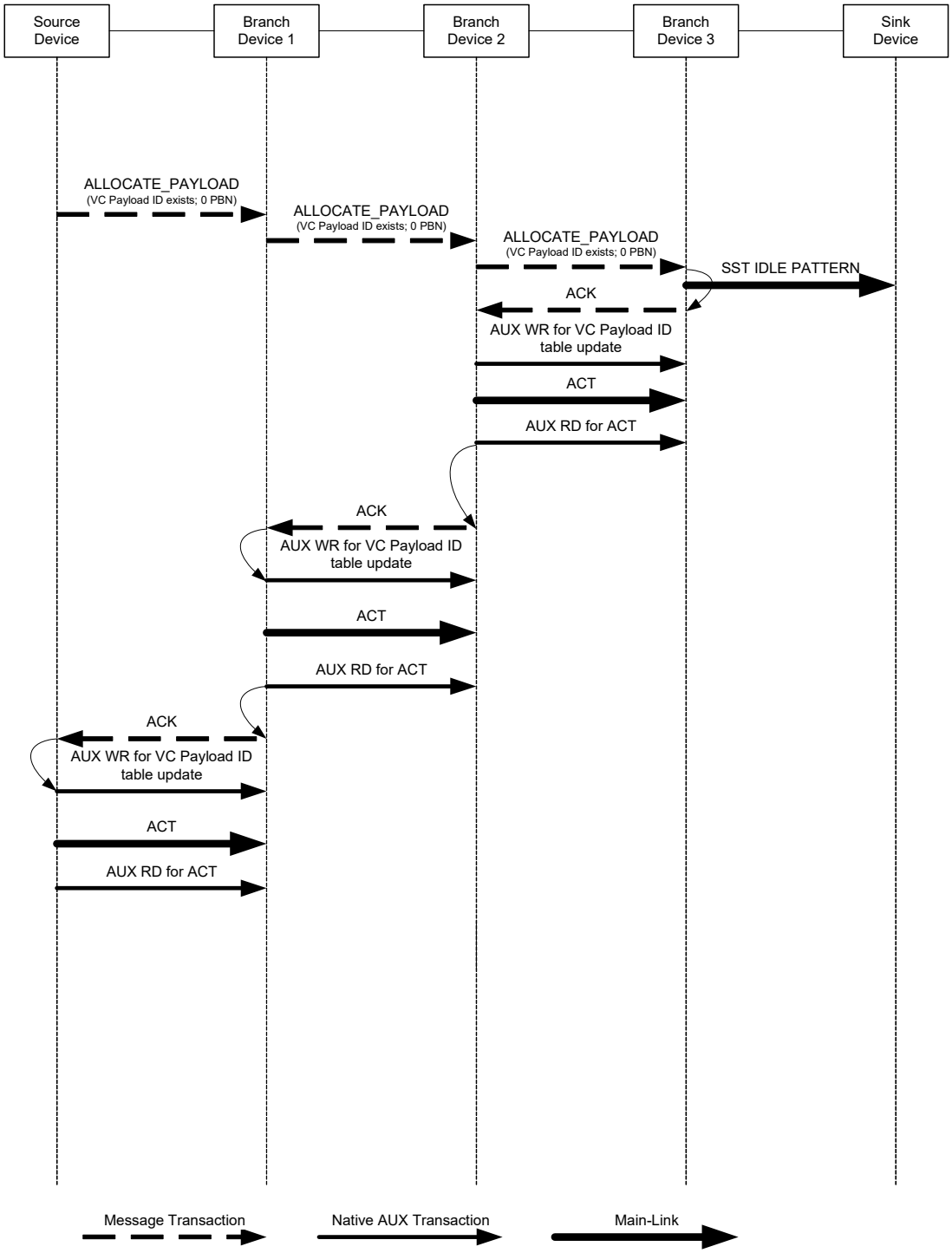


Figure 2-96: Timing Sequence for Deleting a Payload

Figure 2-97 illustrates a timing sequence for deleting a payload that has an error. The DP Branch device that has experienced an error in allocation change on the link it is driving shall first retry to resolve the error condition.

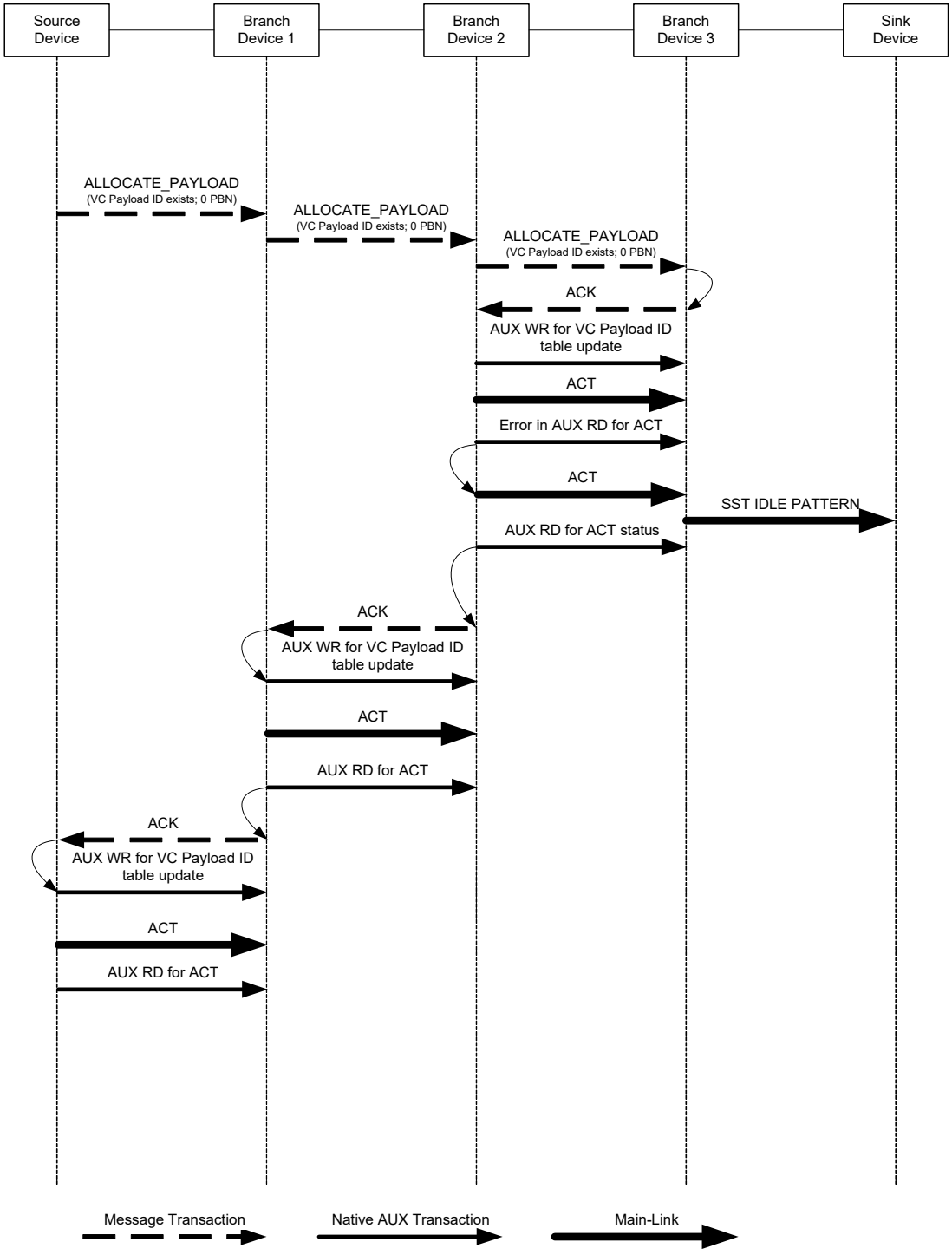


Figure 2-97: Timing Sequence for Deleting a Payload with an Error

Figure 2-98 illustrates a timing sequence for deleting a payload that has an error that is not locally recoverable by the DP Branch device. The DP Branch device shall clear the entire VC Payload ID Table and reply with NAK to the DP Source device.

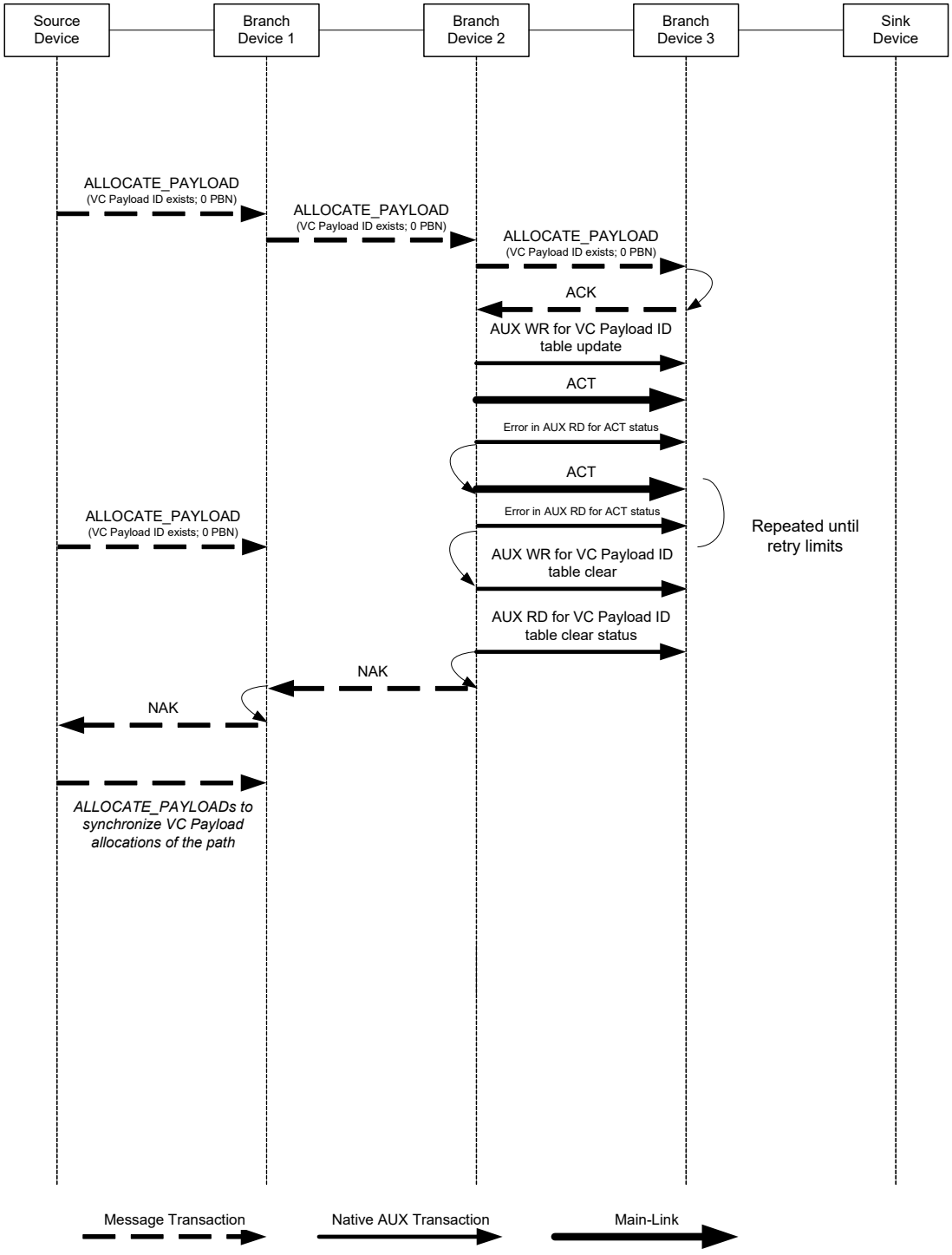


Figure 2-98: Timing Sequence for Deleting a Payload with Locally Unrecoverable Error

Figure 2-99 illustrates a timing sequence for reducing the VC Payload time slot allocation. The DP Source device shall reduce the Throttled_VCP_Size value prior to this operation to avoid the overflow in the path. As a result of the Throttled_VCP_Size reduction, the VC Payload transmits more VCPF Symbol Sequences until the VC Payload Size is reduced following an ACT sequence.

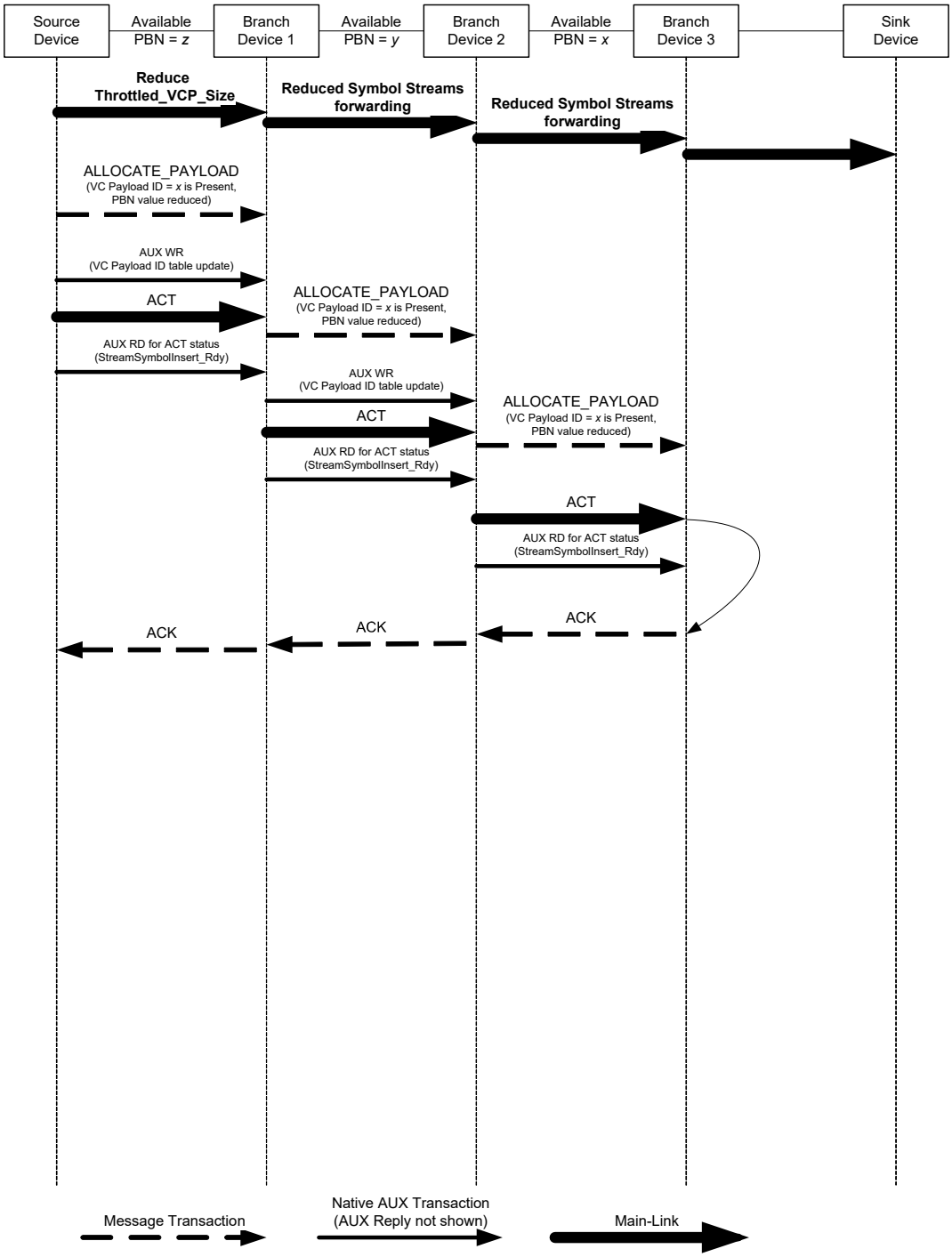


Figure 2-99: Timing Sequence for Reducing the VC Payload Allocation

Figure 2-100 illustrates a timing sequence for increasing the VC Payload time slot allocation. The DP Source device shall wait, receiving the ACK Reply Message, before increasing the Throttled_VCP_Size value to avoid the overflow in the path.

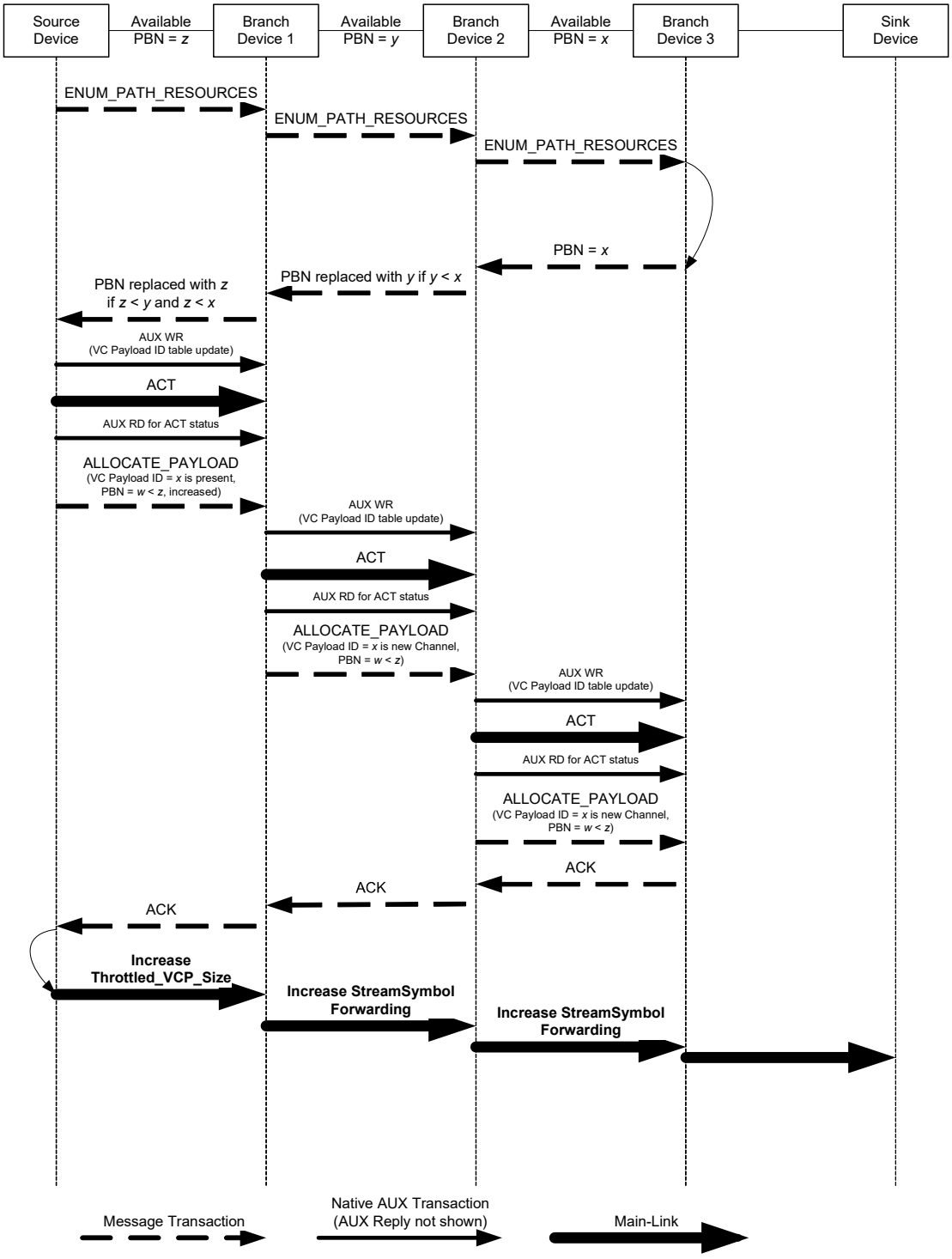


Figure 2-100: Timing Sequence for Increasing the VC Payload Allocation

2.6.7 Impacts of Various Events on VC Payload ID Table

Table 2-142 defines various events and their impact on the VC Payload ID Table.

Table 2-142: Various Events and Impacts on VC Payload ID Table

Events	Results
ALLOCATE_PAYLOAD, with a new VC Payload ID	Time slots allocated at the end of the VC Payload ID Table to support the requested PBN.
ALLOCATE_PAYLOAD, with an existing VC Payload ID and with the same PBN value	No change in Payload Allocation table.
ALLOCATE_PAYLOAD, with an existing VC Payload ID, but with a new, non-zero PBN value	Number of time slots allocated to VC Payload ID is adjusted to support the new PBN value. Higher-numbered time slots are moved up to make room if the new PBN is larger than the original PBN. Higher-numbered time slots are moved down to remove the gap of unused time slots after the number of time slots was reduced due to the new PBN value.
ALLOCATE_PAYLOAD, with an existing VC Payload ID, but with the PBN value cleared to 0	Time slots numbered higher than the last time slot used by the VC Payload ID are moved down to the first time slot used by the VC Payload ID, essentially removing the VC Payload ID from the table.
Loss of Stream within a DP Source device	No change in VC Payload ID table. When the rate governing value X.Y is non-zero, the Main-Link Symbol Mapper transmits Stream Fill symbols when the Stream Symbols are selected by VC Payload multiplexer. When Payload Bandwidth Manager sets X.Y to 0.0, transmits only Rate Governing symbols.
Loss of incoming Stream Symbols or loss of VC Payload symbol sequence phase lock for a DP Branch device	No change in VC Payload ID table. DP Branch device transmits Rate Governing symbols in these conditions.

Table 2-142: Various Events and Impacts on VC Payload ID Table (Continued)

Events	Results
Loss of link followed by link training	The DP device whose DPRX has detected the link loss (Device D) generates IRQ_HPD to notify the upstream DPTX of "link-lost" status and clears the ACT Handled bit in the PAYLOAD_TABLE_UPDATE_STATUS register (DPCD Address 002C0h, bit 1) while keeping the VC Payload ID table intact on the DFP's DPTX and UFP's DPRX. On its DFP's DPTX, Device D fills the VC Payloads that have been affected by the loss of link with Rate Governing symbol sequence. If there is no subsequent link training to recover the link by the upstream DPTX for extended period (e.g., for a few seconds), the DP device: • Clears the DPRX port's VC Payload ID table, and • Initiates ALLOCATE_PAYLOAD with PBN value cleared to 0, to delete those VC Payloads that were coming from the port. The DP device whose DPTX has conducted the link training for link maintenance (Device U) first reads the registers at DPCD Addresses 002C0h through 002FFh of the downstream device (Device D). If the registers at DPCD Addresses 002C0h through 002CFh are all cleared to 00h, that is an indication that Device D has cleared the VC Payload ID table. Device U notifies its upstream devices of this event by way of a RESOURCE_STATUS_NOTIFY message transaction. ***Note:*** *Device U does not need to read all the registers at DPCD Addresses 002C0h through 002FFh; reading of DPCD Addresses 002C0h through 002CFh is sufficient.* If the registers at DPCD Addresses 002C0h through 002CFh retain the values previously set by Device U, that is an indication that Device D has retained the VC Payload ID table and Device U attempts for a local recovery. For the local recovery, Device U performs Native AUX write transactions to the PAYLOAD_ALLOCATE_SET, PAYLOAD_ALLOCATE_START_TIME_SLOT, and PAYLOAD_ALLOCATE_TIME_SLOT_COUNT registers (DPCD Addresses 001C0h, 001C1h, and 001C2h, respectively), followed by ACT on Main-Link and Native AUX read transaction for ACT status flag verification to restore time slot allocations to VC Payloads in the same order they existed before link training was needed. The time slot allocation stops when there is an insufficient number of time slots remaining for any subsequent VC Payloads. Device U initiates ALLOCATE_PAYLOAD with PBN value cleared to 0 to delete those VC Payloads that have lost the time slots as the result of the link training. In case the link cannot be re-established, it deletes all the VC payloads. After the local recovery, Device U issues RESOURCE_STATUS_NOTIFY message transaction, in case the link bandwidth has changed as the result of the link training.

Table 2-142: Various Events and Impacts on VC Payload ID Table (Continued)

Events	Results
Unplug event or receipt of CONNECTION_STATUS_NOTIFY	The DP device whose DPRX has detected the disconnect event (Device D) clears the following registers and bits, as appropriate: • MSTM_CTRL (DPCD Address 00111h) • PAYLOAD_ALLOCATE_SET (DPCD Address 001C0h) • PAYLOAD_ALLOCATE_START_TIME_SLOT (DPCD Address 001C1h) • PAYLOAD_ALLOCATE_TIME_SLOT_COUNT (DPCD Address 001C2h) • ACT Handled and VC Payload ID Table Updated bits in the PAYLOAD_TABLE_UPDATE_STATUS (DPCD Address 002C0h, bits 1:0, respectively) The DP device also clears the VC Payload ID table of the disconnected DPRX, then initiates ALLOCATE_PAYLOAD with the PBN value cleared to 0 to delete those VC Payloads that were coming from the disconnected port. The DP device whose DFP's DPTX detected the unplug event (Device U) then deletes the VC Payloads that were being transmitted from the unplugged port. Device U deletes those VC Payloads from the VC Payload ID table of the unplugged DPTX port, and then issues a CONNECTION_STATUS_NOTIFY message transaction to its upstream devices. DP Source devices, upon receiving CONNECTION_STATUS_NOTIFY, delete all the VC Payloads transmitted through Device U with ALLOCATE PAYLOAD with PBN = 0. (CLEAR_PAYLOAD_ID_TABLE (see Section 2.14.9.2) may be used in case all the VC Payloads are to be deleted.)
POWER_UP_PHY and POWER_DOWN_PHY	VC Payload ID tables are preserved. Loss of link, when it is preceded by POWER_DOWN_PHY, does not result in clearing of VC Payload ID tables.

Notes: *A DP Branch device receiving a POWER_DOWN_PHY executes on it (i.e., write 02h to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h)) of the downstream DPRX) only when either none of the VC Payloads on its downstream link is carrying Stream Symbols or there is no VC Payloads. Upon receiving ALLOCATE_PAYLOAD for VC Payload allocation through the link on which POWER_DOWN_PHY has been executed, the DP Branch device shall execute POWER_UP_PHY (i.e., write 01h to the SET_POWER & SET_DP_PWR_VOLTAGE register).*

Power cycling of the DPTX of an upstream DP device is detected by the downstream DP device's DPRX as a loss of link without preceding POWER_DOWN_PHY and is handled as such.

Power cycling of the DPRX of a downstream DP device is detected by the upstream DP device's DPTX as an unplug event and is handled as such.

2.6.8 Robustness Mandate

There are four aspects to MST mode robustness:

- Link timing robustness through predictable, self-generated link timing
- Trigger Control Sequence robustness in MTPH time slots
- VC Payload 4-symbol sequence phase locking
- VC Payload symbol robustness through redundancy in symbol transmission, regardless of the lane count

This section describes the DPRX implementation mandates for using the above aspects to improve link robustness.

2.6.8.1 Link Timing Robustness

The DPTX shall maintain the 2^{16} symbol interval of SR in MST mode, following the establishment of the Main-Link by way of link training.

The DPRX shall validate the SR interval's consistency before using the SR symbol as the link timing reference point. Besides, the DPRX shall disregard the appearance of SR symbol at an unexpected time slot that may result from an intermittent symbol error over the Main-Link.

The DPRX shall wait for four consecutive SRs with 2^{16} time-slot intervals before switching to an SR location that is different from the original location.

2.6.8.2 Trigger Control Sequence Robustness in MTPH Time Slots

Because the location of the Trigger Control Sequence (such as ACT sequence) is unpredictable, other than it is inserted in MTPH time slots, the DPTX transmits 4-symbol sequence per lane on four consecutive MTPH time slots.

The DPRX shall use this 4-symbol sequence redundancy to properly detect the Trigger Control Sequence, even when only two of the four control link symbols have errors.

2.6.8.3 VC Payload 4-symbol Sequence Boundary Establishment

The DPRX shall establish the 4-symbol sequence boundary and shall correct symbols that do not match the Stream Control Link Symbol Sequence/Rate Governing Symbol Sequence rule.

2.6.8.4 Stream Framing Symbol Sequence Robustness

Each BS, BE, SS, and SE Stream Framing symbol sequence consists of four consecutive, identical Control Codes. Majority voting after 8b/10b decoding shall be used for robustness. The DPRX shall pick the Control Code that appears in two or more symbols within the 4-symbol sequence.

2.6.9 Control Functions, Control Link Symbols, and K-code Assignment

Control Functions consist of sets of defined control link symbols or sequences, and are used in the Main-Link Symbol Management and VC Payload Mapping Layers. To improve link integrity, MST uses 4-symbol sequences to identify all the data symbols and those control link symbols that appear in VC Payload time slots. To minimize emission effects of these 4-symbol codes, the underlying K-codes used are selected using a scrambled index scheme. To maximize error robustness, the remaining control functions inserted into MTPH time slots are directly mapped to 1-symbol K-codes.

2.6.9.1 Control Functions

Table 2-143 defines control function codes used in the MTPH time slots. Table 2-144 defines control function codes that may appear within the MTP data payload time slots.

Table 2-143: MTPH Control Functions

Control Function	Control Link Symbol	Code/Control Link Symbol Sequence[a]	Comment
Scrambler Reset	SR	K28.5	Comma character; Link Frame Indicator.
RESERVED	–	K28.1	Not used.
Active Video Fill (Dummy Pixel Indication)	–	K28.7	Not used, to avoid coding complications.
RESERVED	–	K28.4	Not used, for EMI reduction purposes.
Allocation Change Trigger	ACT	C0-C1-C1-C0	Trigger to downstream device indicating change in allocation on local link. ACT sequence is unique from others; its 4-code control link symbol sequence spans four consecutive MTPH time slots).

a. Cx indicates an indexed control link symbol, as defined in Section 2.6.9.2.

Table 2-144: MTP Payload Control Functions

Control Function	Control Link Symbol	Control Link Symbol Sequence (C*w*, C*x*, C*y*, C*z*)
Virtual Channel Payload Fill	VCPF	C0-C1-C2-C3
Blank Start	BS	C0-C0-C0-C0
Blank End	BE	C1-C1-C1-C1
End of Chunk	EOC	C2-C2-C2-C2
Secondary Start	SS	C3-C3-C3-C3
Stream Fill	SF	C4-C4-C4-C4
RESERVED	–	C5-C5-C5-C5
Secondary End	SE	C6-C6-C6-C6
Active Video Fill (Dummy Pixel Indication)	–	C7-C7-C7-C7

2.6.9.2 Control Link Symbol Index Scrambling

In control link symbol index scrambling, for each control link symbol Cx, “x” defines a (pre-scrambled) index integer value between 0 and 7. A scrambled index is then calculated using the current contents of the Main-Link data scrambling LFSR as follows:

Scrambled Index = Index ^ {LFSR[13], LFSR[14], LFSR[15]}

Finally, this scrambled index determines the actual K-code selected, using the mapping provided in Table 2-145.

Table 2-145: Scrambled Index to K-Code Map

Scrambled Index	K-Code
0	K23.7
1	K27.7
2	K28.0
3	K28.2
4	K28.3
5	K28.6
6	K29.7
7	K30.7

2.6.9.3 Data Symbol Scrambling

The data symbol scrambling is identical between MST mode and SST mode. All data symbols are scrambled.

2.6.10 Conversion between MST and SST Symbol Mapping

All DP devices that support MST mode shall also support SST mode. This mandate ensures interoperation between MST and SST devices.

A DPRX capable of supporting MST mode sets the MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0). An MST-capable DPTX shall first verify whether the downstream DPRX has the MST_CAP bit set, by way of a Native AUX read. If the bit is set to 1 and the DPTX chooses to enable MST mode, the DPTX sets the MST_EN bit to 1 in the MSTM_CTRL register (DPCD Address 00111h, bit 0), by way of a Native AUX write of the downstream DPRX.

For a DP Source and Sink device, whether to enable MST mode is a policy-making choice. A DP Branch device shall always set the MST_CAP bit to 1 on its DPRX, and set the MST_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 0) of the downstream DP device's DPRX to 1, as long as the downstream device has the MST_CAP bit set to 1.

For DP Branch devices that are converting SST to MST symbol mapping or MST to SST symbol mapping, the simple pass-through described in Section 2.6.3.3 does **not** apply.

2.6.10.1 Last Branch Device

The last Branch device receiving MST-mapped symbols and driving an SST-only mode DPRX should first regenerate the receiving stream, and then map the regenerated stream into SST-mapped symbols including Mvid/Nvid, Maud/Naud, and ECC parity generation. Because the reference clock of the last Branch device and that of the DP Source device sourcing streams are asynchronous with one another, Asynchronous Clocking mode shall be used for Mvid/Nvid and Maud/Naud (i.e., the Nvid and Naud values shall be programmed to 8000h). The last Branch device shall generate Mvid and Maud with ±0.1% accuracy.

DP Sink device receiving streams from the last Branch device shall use Mvid and Maud as hints for stream clock regeneration, as is the case with stream clock regeneration with link rate down spreading enabled in SST mode.

Note: *Intermediate DP Branch devices pass-through the Stream Symbols Sequence without parsing the contents. Therefore, those intermediate DP Branch devices pass-through Mvid/Nvid, Maud/Naud, and SDP ECC parity as is.*

There may be ways to simplify the conversion from MST to SST symbol mapping; however, it is an implementation-specific choice and beyond the scope of this Standard.

2.6.10.1.1 Enablement of Enhanced Framing Symbol Sequence by the Last Branch Device

The last Branch device driving the downstream SST device shall enable the Enhanced Framing Symbol Sequence as long as the downstream device supports the sequence.

2.6.10.2 First Branch Device

The first Branch device receiving SST-mapped symbols from an SST-only mode Source device shall forward the stream to the downstream link in SST mode with the same link configuration as the upstream link.

When an upstream Source device is MST-capable, but chooses to transmit in SST mode, the MST Source device shall initiate ALLOCATE_PAYLOAD message transaction to establish the virtual channel to the target Sink device. In this case, the first Branch device converts incoming SST-mapped symbols into MST-mapped symbols including Mvid/Nvid, Maud/Naud, and ECC parity generation. Because the reference clock of the last Branch device and that of the DP Source device sourcing streams are asynchronous with one another, Asynchronous Clocking Mode shall be used for Mvid/Nvid and Maud/Naud.

There may be ways to simplify this conversion, but it is an implementation-specific choice and beyond the scope of this Standard.

2.6.10.2.1 Enhanced Framing Symbol Sequence support by the First Branch Device

The first Branch device shall support the Enhanced Framing Symbol Sequence in SST mode.

2.6.10.3 Mode Switching between MST and SST Modes

The DPTX and DPRX capable of MST mode shall support SST mode to interoperate with SST-only mode DP devices.

Switching between MST and SST modes results in interruption of the transport of stream(s) because the DPTX shall stop the stream transport and FEC activity prior to this mode switch. The DPTX re-initiates Link Training, and come out of the Link Training with Idle Pattern in SST mode or no-VC Payload (i.e., empty MTP) pattern in MST mode.

2.6.11 MTPH Usages for CP Extension in MST Mode

Two additional usages of MTPH time slots are defined for the CP extension in MST mode – Encryption Control Field and Link Verification Pattern (LVP).

2.6.11.1 Encryption Control Field

The Encryption Control Field (ECF) consists of a 64-bit data word contained within an 8-data symbol sequence spanning eight consecutive MTPHs. Each data symbol contains one byte of the 64-bit data word, starting with the LSB (i.e., ECF0 = Data[7:0], ECF1 = Data[15:8], …, ECF7 = Data[63:56]). The data symbol sequence is identical per-lane, regardless of the lane count. The ECF is repeated four consecutive times, resulting in a total sequence length of 32 MTPs. The DPRX shall apply majority voting on the repeated ECFs for error correction.

How the ECF is used is specific to the Content Protection system ported onto the DP MST link and is therefore beyond the scope of this Standard.

The DPTX shall transmit four consecutive ECFs at least once per Link Frame, starting exactly 36 MTPHs prior to the Link Frame boundary SR signal.

The ECF may be transmitted by DPTX anywhere beyond the keep-out area. When the ECF is transmitted beyond the fixed location, starting from the 36 MTPH time slots prior to SR, the ECF shall be immediately followed by an ACT sequence.

Besides this fixed location, the DPTX may transmit four consecutive ECFs anywhere immediately prior to the ACT sequence that spans four consecutive MTPH time slots.

Neither the four consecutive ECFs nor the ACT sequence shall straddle the SR and Link Verification Pattern (described in Section 2.6.11.2).

The DPRX shall monitor both the fixed four consecutive ECFs' location and 32 MTPH time slots prior to ACT sequence and take proper encryption action.

Figure 2-101 illustrates the timing relationships of these fields for the link frame boundary case.

Figure 2-102 illustrates the timing relationship of four consecutive ECFs and ACT sequence. Note that the MTP*N* + 4 in Figure 2-102 may optionally occur at MTP0 (the link frame boundary), in which case MTPH*N* + 5 and MTPH*N* + 6 shall contain the LVP, as illustrated in Figure 2-101. Also, the MTP*N* – 32 may optionally occur at MTP3 after the link frame boundary, in which case MTPH*N* containing the first ACT sequence starts on MTP36 immediately after the reserved time slots illustrated in Figure 2-101.

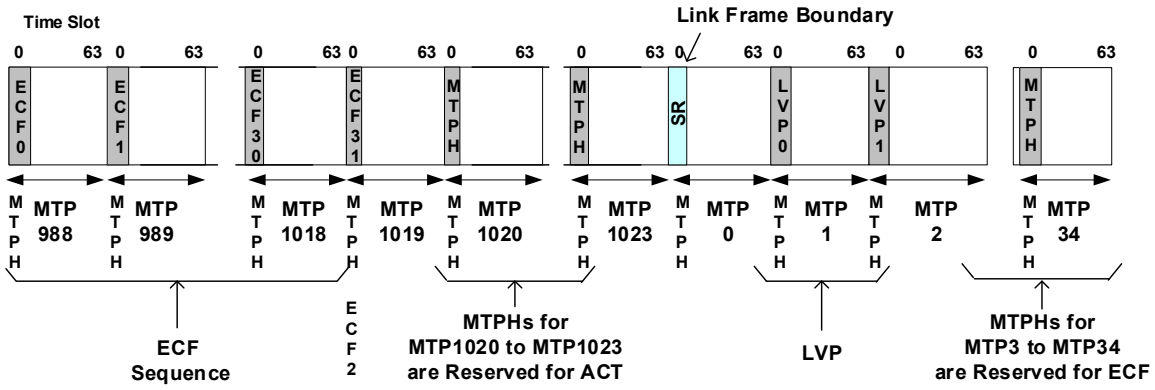


Figure 2-101: MSTM ECF and LVP Signaling at Link Frame Boundary

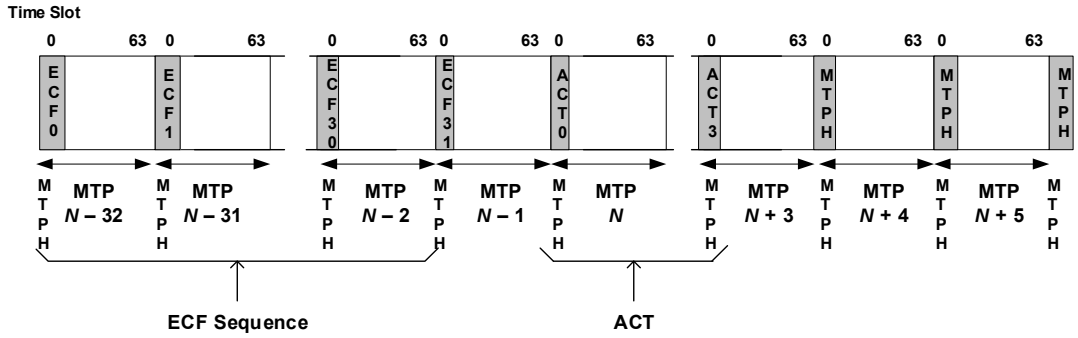


Figure 2-102: ECF Immediately prior to ACT Sequence

2.6.11.2 Link Verification Pattern

The two consecutive MTPH time slots immediately following the Link Frame boundary SR signal are used for transporting the 16-bit LVP, the least significant byte (bits 7:0) transmitted first and the most significant byte (bits 15:8) last.

In SST mode, the HDCP SYNC DETECT bit in the VB-ID (bit 5) is used to sequentially transport the 16-bit Link Verification Pattern. In MST mode, bit 5 becomes “don’t care.”

2.6.11.3 MTPH Time Slot Encryption

The data symbols transported in those MTPH time slots for ECFs shall **not** be encrypted. LVP shall be encrypted. The decision of whether to encrypt other MTPH time slots is up to the policy of the content protection system running over the DP MST link.

2.7 Stream Data-to-Link Symbol Mapping with 128b/132b Link Layer

New to *DP v2.0*.

This section defines the 128b/132b Link Layer (**yellow** boxes in Figure 2-103).
(For 128b/132b PHY Logical Sub-layer capability discovery and configuration through AUX transactions, see Section 3.5.2.)

Figure 2-103 illustrates the 128b/132b Link Layer-capable DP Source and Sink device connection, highlighting the Link Layer blocks.

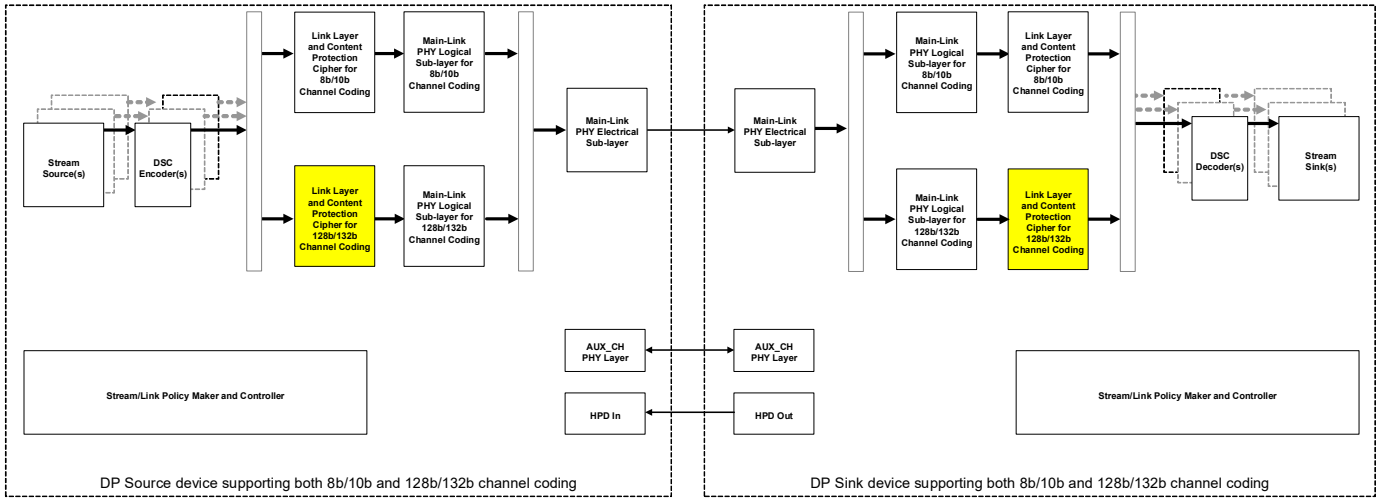


Figure 2-103: 128b/132b Link Layer-capable DP Source and Sink Device Connection, Highlighting Link Layer Blocks

The 128b/132b Link Layer protocol is based on the MST protocol defined in Section 2.6. Modifications to that protocol are defined in the sub-sections that follow. All Section 2.6 mandates apply to 128b/132b Link Layer, except when stated otherwise within this section. Section 2.6.9 and Section 2.6.11 do **not** apply to 128b/132b Link Layer.

Table 2-146 compares 128b/132b Link Layer (applied for UHBR bit rates, *DP v2.0* and higher) to 8b/10b Link Layer (applied for HBR3/HBR2/HBR/RBR bit rates), as defined in Section 2.2. Section 2.4, and Section 2.6. Only mapping for the 4-lane Main-Link configuration is relevant because 128b/132b Link Layer always operates on four Main-Link lanes (i.e., the Link Layer Main-Link lane count is always four), which is also the case for MST 8b/10b Link Layer.

Note: *For stream data mapping to DP link symbols, including pixel data, MSA packet, VB-ID, and SDPs, see Section 2.2.*

Table 2-146: 128b/132b vs. 8b/10b Channel Coding Comparison

Attributes	128b/132b Channel Coding	8b/10b Channel Coding	
		SST	MST
***DP Standard* Version**	• Added in *DP v2.0*	• Defined in *DP v1.4a*	
Single Stream vs. Multiple Streams	• Common format is used for both	• Single stream	• Multiple streams
Link Rates (Bit Rates)	• 20Gbps/lane (UHBR20) • 13.5Gbps/lane (UHBR13.5) • 10Gbps/lane (UHBR10)	• 8.1Gbps/lane (HBR3) • 5.4Gbps/lane (HBR2) • 2.7Gbps/lane (HBR) • 1.62Gbps/lane (RBR)	
Data Bandwidth Efficiency[a]	• 96.71% with FEC enabled for single stream and multiple streams	• 80% with FEC disabled • 78.13% with FEC enabled	• 78.75% with FEC disabled • 76.90% with FEC enabled
Per-lane Data Bandwidths	• UHBR20 • 19.34Gbps/lane • UHBR13.5 • 13.05Gbps/lane • UHBR10 • 9.671Gbps/lane	• HBR3, with/without FEC • 6.48Gbps/lane without • 6.33Gbps/lane with • HBR2, with/without FEC • 4.32Gbps/lane without • 4.22Gbps/lane with • HBR, with/without FEC • 2.16Gbps/lane without • 2.11Gbps/lane with • RBR, with/without FEC • 1.30Gbps/lane without • 1.27Gbps/lane with	• HBR3, with/without FEC • 6.30Gbps/lane without • 6.22Gbps/lane with • HBR2, with/without FEC • 4.25Gbps/lane without • 4.15Gbps/lane with • HBR, with/without FEC • 2.13Gbps/lane without • 2.08Gbps/lane with • RBR, with/without FEC • 1.28Gbps/lane without • 1.25Gbps/lane with
Link Symbol Data Size	• 32 bits	• 8 bits	
Micro-packet Type and Size	• MTP, 64 link symbol cycles (time slots) per Link Layer lane	• TU, 32 to 64 link symbol cycles (time slots) per Link Layer lane	• MTP, 64 link symbol cycles (time slots) per Link Layer lane
Micro-packet Header	• Condensed in LLCP packet	• N/A	• 1st link symbol cycle of MTP
Rate Governing	• VC Payload time slot allocation prior to the start of stream transmission plus VCPF insertion	• Fill symbols inserted into TU	• VC Payload time slot allocation prior to the start of stream transmission plus VCPF insertion
Link Layer Lane Count[b]	• Four	• Same as physical lane count	• Four

Table 2-146: 128b/132b vs. 8b/10b Channel Coding Comparison (Continued)

Attributes	128b/132b Channel Coding	8b/10b Channel Coding	
		SST	MST
Content Protection Lane Count[b]	• Four	• Same as physical lane count	
Physical Lane Count	• Four, two, or one	• Four, two, or one	
Link Layer Frame Timing vs. Main Video Stream Timing	• Agnostic to main video stream timing	• Depends on main video stream timing	• Agnostic to main video stream timing
Link Layer Frame Boundary	• LLCP packet	• Scrambler Reset (SR) symbol	
SDP Parity	• Zero-padded	• Populated with RS(15, 13) parity nibbles	
Stream Rates Indication	• Absolute stream rate values in VFREQ and AFREQ fields	• Mvid/Nvid and Maud/Naud fields indicate ratio between stream and link symbol rates	• Mvid/Nvid and Maud/Naud are meaningful only when a DP Sink device is directly plugged to a DP Source device

*a. Includes overhead from the Link Layer and PHY Logical Sub-layer; however, down spreading overhead (0.25%) is **not** included.*

b. For 128b/132b Link Layer, the conversion to physical lane count in a DPTX occurs in the PHY Logical Sub-layer. For MST 8b/10b Link Layer, the conversion to physical lane count in a DPTX occurs in the content protection cipher block.

The link symbol data size increases from 8 to 32 bits to reduce the link symbol rate from 1/8 of the serial bit rate to 1/32, which is from 2500 to 625Msymbols/sec/lane for a 20-Gbps/lane serial bit rate.

Figure 2-104, Figure 2-105, and Figure 2-106 illustrate the informative, logical views of 128b/132b Link Layer for DP Source, Sink, and Branch devices, respectively. The three figures correspond to Figure 2-72, Figure 2-73, and Figure 2-74, respectively, which illustrate the logical views of 8b/10b Link Layer, as described in Section 2.6.

Note: *An alternate approach to the following place holder method can be found in Appendix M. The resulting bitstream from both approaches will be identical.*

Because Figure 2-104 through Figure 2-106 are informative, the actual implementation may be different from those illustrated. For example, the figures show place holder symbols inserted in the Link Layer that are replaced with PHY sync symbol and 128b/132b channel coding overhead (i.e., insertion of CDI field, RS FEC symbol, etc.) in the PHY Logical Sub-layer. An implementation that does not insert place holder symbols is feasible, as described and illustrated in Appendix M. What needs to be ensured is that the serial bit patterns that are transmitted by the 128b/132b DPTX meet the normative specification requirement. A DPTX implementer shall compare the serial bit patterns of the implementation to that defined in Section 3.5.2.17 to verify an exact match.

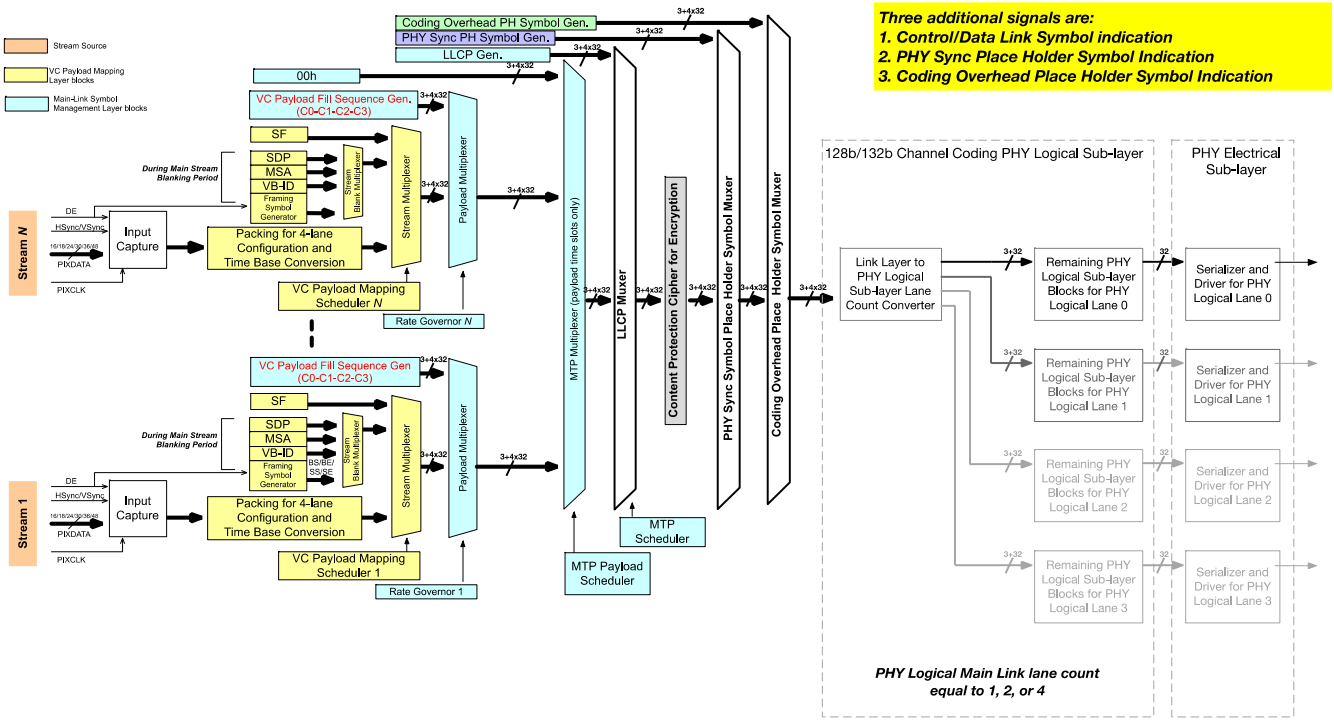


Figure 2-104: DP Source Device 128b/132b Link Layer Logical View (Informative)

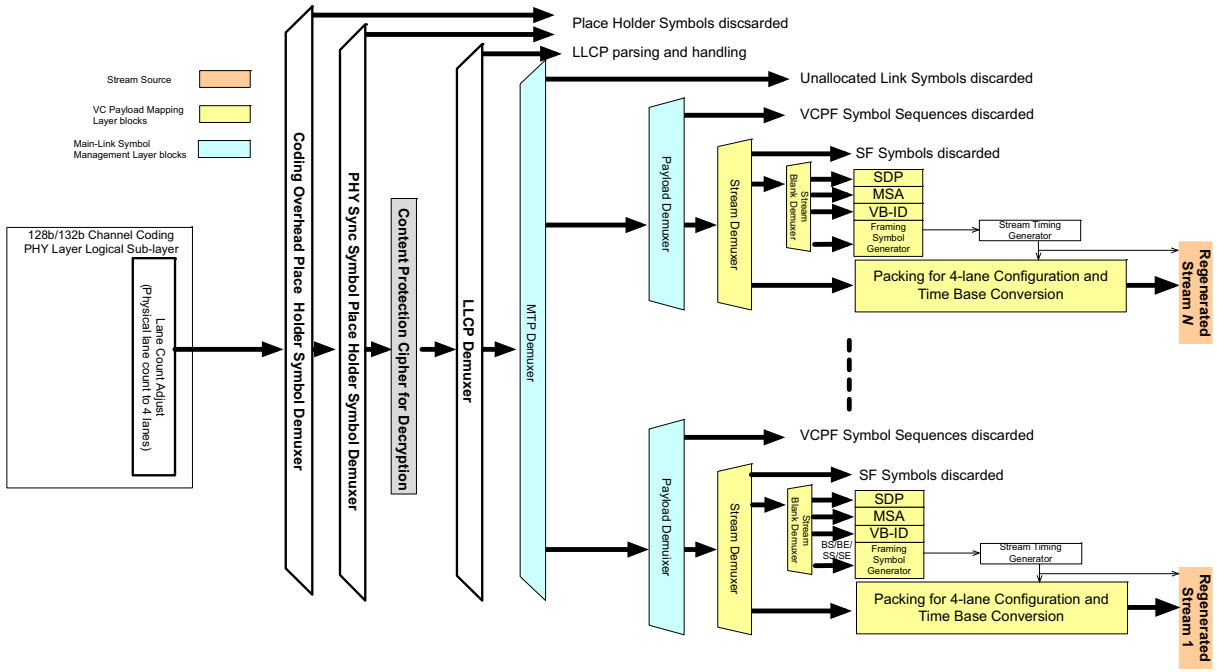


Figure 2-105: DP Sink Device Logical View for 128b/132b Link Layer (Informative)

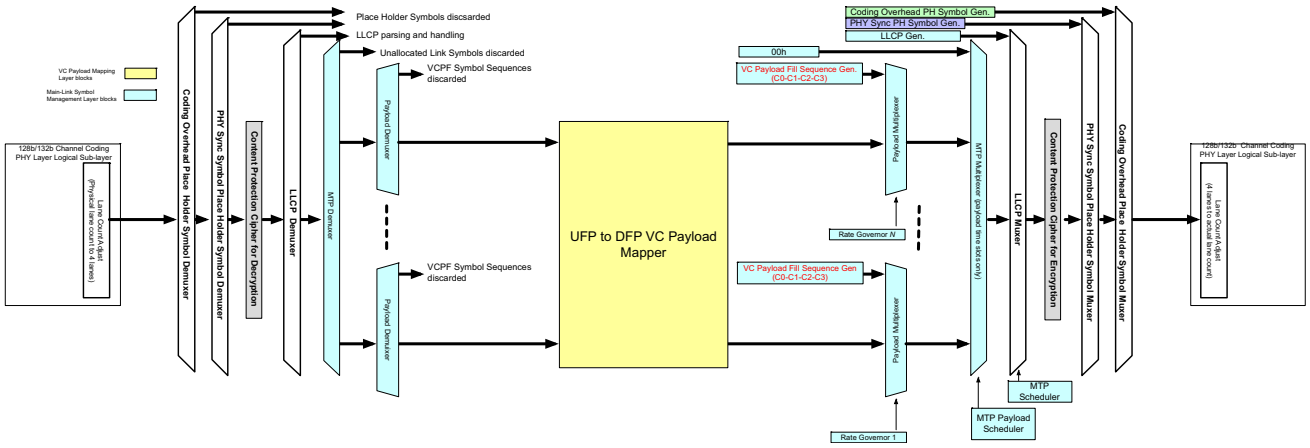


Figure 2-106: DP Branch Device Logical View for 128b/132b Link Layer (Informative)

2.7.1 32-bit Link Symbols

This section describes 32-bit link symbol generation of the 128b/132b Link Layer. 128b/132b Link Layer always operates on four Main-Link lanes. Link symbols are either data link or control link symbols. For any link symbol cycle, all four lanes carry the same link symbol type.

2.7.1.1 Data Link Symbols

Figure 2-107 illustrates how 32-bit data link symbols are constructed, using 8-bpc pixel data into 32-bit symbol mapping at the start of horizontal active video as an example.

For each lane, four of 8-bit data are cascaded into 32-bit data. The first eight bits of the 32-bit data that would be transmitted for 8b/10b Link Layer is mapped to the least significant eight bits (i.e., Byte 0), and the last eight bits to the most significant eight bits (i.e., Byte 3).

The last pixel data link symbols of each horizontal video active line are immediately followed by a BS control link symbol. Bits within the last pixel data link symbol that are **not** carrying pixel data shall be zero-padded.

Lane 0		**Lane 1**		**Lane 2**		**Lane3**	
BE		BE		BE		BE	
Lane 0 Pixel Data Link Symbol 0 of Video Horizontal Active Line *N*	Byte 0 = R0-7:0	Lane 1 Pixel Data Link Symbol 0 of Video Horizontal Active Line *N*	Byte 0 = R1-7:0	Lane 2 Pixel Data Link Symbol 0 of Video Horizontal Active Line *N*	Byte 0 = R2-7:0	Lane 3 Pixel Data Link Symbol 0 of Video Horizontal Active Line *N*	Byte 0 = R3-7:0
	Byte 1 = G0-7:0		Byte 1 = G1-7:0		Byte 1 = G2-7:0		Byte 1 = G3-7:0
	Byte 2 = B0-7:0		Byte 2 = B1-7:0		Byte 2 = B2-7:0		Byte 2 = B3-7:0
	Byte 3 = R4-7:0		Byte 3 = R5-7:0		Byte 3 = R6-7:0		Byte 3 = R7-7:0
Lane 0 Pixel Data Link Symbol 1 of Video Horizontal Active Line *N*	Byte 0 = G4-7:0	Lane 1 Pixel Data Link Symbol 1 of Video Horizontal Active Line *N*	Byte 0 = G5-7:0	Lane 2 Pixel Data Link Symbol 1 of Video Horizontal Active Line *N*	Byte 0 = G6-7:0	Lane 3 Pixel Data Link Symbol 1 of Video Horizontal Active Line *N*	Byte 0 = G7-7:0
	Byte 1 = B4-7:0		Byte 1 = B5-7:0		Byte 1 = B6-7:0		Byte 1 = B7-7:0
	Byte 2 = R8-7:0		Byte 2 = R9-7:0		Byte 2 = R10-7:0		Byte 2 = R11-7:0
	Byte 3 = G8-7:0		Byte 3 = G9-7:0		Byte 3 = G10-7:0		Byte 3 = G11-7:0

Figure 2-107: Pixel Data to 32-bit Link Symbol Mapping Example

2.7.1.2 Control Link Symbols

Table 2-147 defines the eight 32-bit control link symbols that are used for 128b/132b Link Layer, and how they map to 8b/10b Link Layer.

Table 2-147: 8b/10b Link Layer-to-128b/132b Link Layer Control Link Symbol Mapping

8b/10b Link Layer Control Link Symbols	128b/132b Link Layer Control Link Symbols[a]	Comment
BE	BE	
BF	–	BS-BF-BF-BS sequence replaced with 32-bit BS control link symbol.
BS	BS	
CP	–	Encryption Control Field (ECF) in the LLCP. Used for encryption status indication, same as in MST 8b/10b Link Layer.
EOC	EOC	
FE	–	Unallocated time slots populated with 0s, same as in MST 8b/10b Link Layer.
FS	–	
PM	–	RS FEC parity bytes mapped to 32-bit RS parity symbol.
SE	SE	
SF	SF	
SR	–	32-bit PHY Layer sync symbol used to reset scrambler LFSR.
SS	SS	
VCPF	VCPF	
–	LLCP_MARKER	First control symbol of the four-symbol Link Layer control packet (LLCP).

a. See Table 3-21 for the bit mapping of these eight control link symbols.

2.7.2 Mapping to MTPs and Link Layer Frames

128b/132b Link Layer MTPs have 64 link symbol cycles. The Link Layer frame is composed of an LLCP that is followed by 1024 MTPs, as illustrated in Figure 2-108.

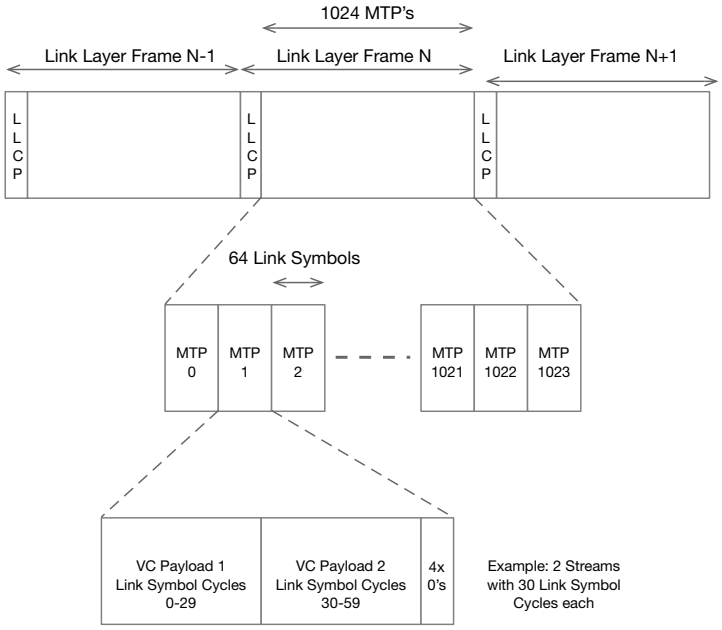


Figure 2-108: 128b/132b Link Layer MTPs and Link Layer Frames

2.7.3 Link Layer Control Packet

Table 2-148 defines the LLCP's bit mapping, consisting of four symbols per Link Layer lane that are composed of four 32-bit link symbols. Because the ACT bit, HDCP Encryption Indicator bit, and ECF field are located within the LLCP, an allocation trigger change and content protection change may occur only at the Link Layer frame boundary in 128b/132b Link Layer. If an ACT is transmitted in the LLCP in Link Layer Frame *N*, the new allocation takes effect in MTP0 of Link Layer Frame *N*.

Table 2-148: LLCP Bit Mapping

Link Symbol Number	128b/132b Link Layer Symbol Type	Bit #	Description	
0	LLCP_MARKER Control Link Symbol	31:0		
1	Data Link Symbol 0	0	Allocation Change Trigger (ACT).	
		1	HDCP Encryption Indicator.	
		15:2	RESERVED; read all 0s.	
		31:16	64-bit Encryption Control Field (ECF).	ECF[15:0].
2	Data Link Symbol 1	31:0		ECF[47:16].
3	Data Link Symbol 2	15:0		ECF[63:48].
		31:16	16-bit Link Verification Pattern (LVP).	

2.7.4 MSA Packet and VB-ID Mapping to 32-bit Link Symbols

This section describes MSA packet and VB-ID mapping to 32-bit link symbols.

2.7.4.1 MSA Packet Mapping to 32-bit Link Symbols

Figure 2-109 illustrates MSA packet mapping to 32-bit link symbols. The Mvid[23:0] and Nvid[23:0] fields used in 8b/10b Link Layer are replaced with the VFREQ[47:0] field.

Lane 0		Lane 1		Lane 2		Lane 3	
Lane 0 Symbol *N*	SS	Lane 1 Symbol *N*	SS	Lane 2 Symbol *N*	SS	Lane 3 Symbol *N*	SS
Lane 0 Symbol *N* + 1	SS	Lane 1 Symbol *N* + 1	SS	Lane 2 Symbol *N* + 1	SS	Lane 3 Symbol *N* + 1	SS
Lane 0 Symbol *N* + 2	All 0s	Lane 1 Symbol *N* + 2	All 0s	Lane 2 Symbol *N* + 2	All 0s	Lane 3 Symbol *N* + 2	VFREQ[47:40]
	All 0s		All 0s		All 0s		VFREQ[39:32]
	All 0s		All 0s		All 0s		VFREQ[31:24]
	HTotal[15:8]		HStart[15:8]		HWidth[15:8]		VFREQ[23:16]
Lane 0 Symbol *N* + 3	HTotal[7:0]	Lane 1 Symbol *N* + 3	HStart[7:0]	Lane 2 Symbol *N* + 3	HWidth[7:0]	Lane 3 Symbol *N* + 3	VFREQ[15:8]
	VTotal[15:8]		VStart[15:8]		VHeight[15:8]		VFREQ[7:0]
	VTotal[7:0]		VStart[7:0]		VHeight[7:0]		MISC0[7:0]
	HSP[0] | HSW[14:8]		VSP[0] | VSW[14:8]		All 0s		MISC1[7:0]
Lane 0 Symbol *N* + 4	HSW[7:0]	Lane 1 Symbol *N* + 4	VSW[7:0]	Lane 2 Symbol *N* + 4	All 0s	Lane 3 Symbol *N* + 4	All 0s
	All 0s		All 0s		All 0s		All 0s
	All 0s		All 0s		All 0s		All 0s
	All 0s		All 0s		All 0s		All 0s
Lane 0 Symbol *N* + 5	SE	Lane 1 Symbol *N* + 5	SE	Lane 2 Symbol *N* + 5	SE	Lane 3 Symbol *N* + 5	SE

Figure 2-109: MSA Packet Mapping to 32-bit Link Symbols

2.7.4.2 Pixel Rate Indication with VFREQ Field

The VFREQ[47:0] field shall carry the absolute pixel rate in units of Hz. A DP Source device shall set the 48-bit value to within ±1% accuracy. As is the case with 8b/10b Link Layer, a DPRX that performs pixel rate regeneration shall use the 48-bit field value as a hint.

2.7.4.3 VB-ID Mapping to 32-bit Link Symbols

Figure 2-110 illustrates VB-ID mapping to 32-bit link symbols. A DPTX shall map the 8-bit VB-ID to the lowest significant 8 bits of the 32-bit link symbol; the DPTX shall **not** map Mvid[7:0] or Maud[7:0]. In 128b/132b Link Layer, because the LVP field in the LLCP takes its place, the HDCP SYNC DETECT bit in the VB-ID (bit 5) is "don't care," the same as with MST 8b/10b Link Layer.

Lane 0		Lane 1		Lane 2		Lane 3	
Lane 0 Symbol *N*	VB-ID[7:0]	Lane 1 Symbol *N*	VB-ID[7:0]	Lane 2 Symbol *N*	VB-ID[7:0]	Lane 3 Symbol *N*	VB-ID[7:0]
	All 0s		All 0s		All 0s		All 0s
	All 0s		All 0s		All 0s		All 0s
	All 0s		All 0s		All 0s		All 0s

Figure 2-110: VB-ID Mapping to 32-bit Link Symbols

2.7.5 SDP Mapping to 32-bit Link Symbols

Note: *For mapping to SDP with 8b/10b channel coding that has 8-bit symbols, see Section 2.2.5.*

With 128b/132b channel coding, which has a symbol size of 32 bits, groups of four 8-bit symbols form a 32-bit symbol for each lane, such that the first 8-bit symbol in the group that would be transmitted for 8b/10b Link Layer is mapped to the lsbs (i.e., Byte 0 = Symbol[*x*][7:0]) and the last 8-bit symbol in the group is mapped to the msbs (i.e., Byte 3 = Symbol[*x*][31:24]), as illustrated in Figure 2-111.

Because 8-bit RS(198, 194) protects all 32-bit link symbols that are used in 128b/132b Link Layer, RS(15, 13) for SDPs is deprecated; thus, an SDP's RS(15, 13) parity nibble locations shall be zero-padded. Therefore, parity nibble interleaving is **not** applicable to 128b/132b Link Layer.

When the 8-bit symbols do **not** fully map to 32-bit symbols at the end of the payload, the unoccupied 8 bits are zero-padded.

Lane 0		Lane 1		Lane 2		Lane 3	
Lane 0 Symbol *N*	SS	Lane 1 Symbol *N*	SS	Lane 2 Symbol *N*	SS	Lane 3 Symbol *N*	SS
Lane 0 Symbol *N* + 1	HB0	Lane 1 Symbol *N* + 1	HB1	Lane 2 Symbol *N* + 1	HB2	Lane 3 Symbol *N* + 1	HB3
	All 0s		All 0s		All 0s		All 0s
	DB0		DB4		DB8		DB12
	DB1		DB5		DB9		DB13
Lane 0 Symbol *N* + 2	DB2	Lane 1 Symbol *N* + 2	DB6	Lane 2 Symbol *N* + 2	DB10	Lane 3 Symbol *N* + 2	DB14
	DB3		DB7		DB11		DB15
	All 0s		All 0s		All 0s		All 0s
	DB16		DB20		DB24		DB28
Lane 0 Symbol *N* + 3	DB17	Lane 1 Symbol *N* + 3	DB21	Lane 2 Symbol *N* + 3	DB25	Lane 3 Symbol *N* + 3	DB29
	DB18		DB22		DB26		DB30
	DB19		DB23		DB27		DB31
	All 0s		All 0s		All 0s		All 0s
Lane 0 Symbol *N* + 4	SE	Lane 1 Symbol *N* + 4	SE	Lane 2 Symbol *N* + 4	SE	Lane 3 Symbol *N* + 4	SE

Figure 2-111: SDP Mapping to 32-bit Link Symbols

2.7.5.1 Audio_TimeStamp SDP AFREQ Field

In 128b/132b Link Layer, the Maud and Naud fields are combined to form a 48-bit field, AFREQ[47:0] (as illustrated in Figure 2-112). AFREQ[47:0] shall carry the rate (in Hz) of the absolute master audio clock, which is 512 times the audio sample frequency. A DP Source device shall set the 48-bit value to within ±1% accuracy. As is the case with 8b/10b Link Layer, a DPRX that performs master audio clock regeneration shall use the 48-bit field value as a hint.

Lane 0		**Lane 1**		**Lane 2**		**Lane 3**	
Lane 0 Symbol *N*	SS	Lane 1 Symbol *N*	SS	Lane 2 Symbol *N*	SS	Lane 3 Symbol *N*	SS
Lane 0 Symbol *N* + 1	HB0	Lane 1 Symbol *N* + 1	HB1	Lane 2 Symbol *N* + 1	HB2	Lane 3 Symbol *N* + 1	HB3
	All 0s		All 0s		All 0s		All 0s
	AFREQ[47:40]		AFREQ[47:40]		AFREQ[47:40]		AFREQ[47:40]
	AFREQ[39:32]		AFREQ[39:32]		AFREQ[39:32]		AFREQ[39:32]
Lane 0 Symbol *N* + 2	AFREQ[31:24]	Lane 1 Symbol *N* + 2	AFREQ[31:24]	Lane 2 Symbol *N* + 2	AFREQ[31:24]	Lane 3 Symbol *N* + 2	AFREQ[31:24]
	All 0s		All 0s		All 0s		All 0s
	All 0s		All 0s		All 0s		All 0s
	AFREQ[23:16]		AFREQ[23:16]		AFREQ[23:16]		AFREQ[23:16]
Lane 0 Symbol *N* + 3	AFREQ[15:8]	Lane 1 Symbol *N* + 3	AFREQ[15:8]	Lane 2 Symbol *N* + 3	AFREQ[15:8]	Lane 3 Symbol *N* + 3	AFREQ[15:8]
	AFREQ[7:0]		AFREQ[7:0]		AFREQ[7:0]		AFREQ[7:0]
	All 0s		All 0s		All 0s		All 0s
	All 0s		All 0s		All 0s		All 0s
Lane 0 Symbol *N* + 4	SE	Lane 1 Symbol *N* + 4	SE	Lane 2 Symbol *N* + 4	SE	Lane 3 Symbol *N* + 4	SE

Figure 2-112: Audio_TimeStamp SDP Mapping to 32-bit Link Symbols

2.7.6 Time Slot Allocations

2.7.6.1 DP Sink Device Directly Plugged to DP Source Device

In 128b/132b Link Layer, regardless of the number of streams that the device transmits, a DP Source device shall use Time Slot Allocation AUX write transactions to the following registers:

- PAYLOAD_ALLOCATE_SET register (DPCD Address 001C0h)
- PAYLOAD_ALLOCATE_START_TIME_SLOT (DPCD Address 001C1h)
- PAYLOAD_ALLOCATE_TIME_SLOT_COUNT register (DPCD Address 001C2h)

A DPRX indicates ACT detection and time slot allocation status in the following registers and bits, as appropriate:

- ACT Handled and VC Payload ID Table Updated bits in the PAYLOAD_TABLE_UPDATE_STATUS register (DPCD Address 002C0h, bits 1:0, respectively)
- VC Payload ID table registers:
  - VC_PAYLOAD_ID_SLOT0_6 bit in the VC_PAYLOAD_ID_SLOT1 register and VC_PAYLOAD_ID_SLOT0_5:0 field in the PAYLOAD_TABLE_UPDATE_STATUS register (DPCD Address 002C1h, bit 7, and DPCD Address 002C0h, bits 7:2, respectively)
  - VC_PAYLOAD_ID_SLOT*x* registers (where *x* is 1 through 63, DPCD Addresses 002C1h through 002FFh, respectively)

Table 2-149 provides an example VC Payload ID Table of a 128b/132b channel coding DPRX. In contrast to the equivalent 8b/10b channel coding table, Table 2-140, 128b/132b channel coding has a Time Slot 0.

Table 2-149: 128b/132b Channel Coding VC Payload ID Table of DPRX Mapped to DPCD Address Space

DPCD Address	Time Slot	VC Payload ID (7-bit value RO)[a]
002C1h, Bit 7 and 002C0h, Bits 7:2	0	1
002C1h, Bits 6:0	1	1
002C2h, Bits 6:0	2	1
002C3h, Bits 6:0	3	1
002C4h, Bits 6:0	4	1
002C5h, Bits 6:0	5	1
002C6h, Bits 6:0	6	3
002C7h, Bits 6:0	7	3
002C8h, Bits 6:0	8	3
002C9h, Bits 6:0	9	3
002CAh, Bits 6:0	10	3
002CBh, Bits 6:0	11	3
002CCh, Bits 6:0	12	3
002CDh, Bits 6:0	13	3
002CEh, Bits 6:0	14	4
002CFh, Bits 6:0	15	4
002D0h, Bits 6:0	16	4
002D1h, Bits 6:0	17	4
002D2h, Bits 6:0	18	4
002D3h, Bits 6:0	19	4
002D4h, Bits 6:0	20	4
002D5h, Bits 6:0	21	4
002D6h, Bits 6:0	22	5
002D7h, Bits 6:0	23	5
002D8h, Bits 6:0	24	5
002D9h, Bits 6:0	25	5
002DAh, Bits 6:0	26	5
002DBh, Bits 6:0	27	0
002DCh, Bits 6:0	28	0
002DDh, Bits 6:0	29	0
002DEh, Bits 6:0	30	0
…	…	…
002FFh, Bits 6:0	63	0

a. This table illustrates an example in which VC Payload ID #2 has been deleted. Time slots with VC Payload ID value 0 are ***not*** *allocated.*

2.7.6.2 DP Sink Device(s) Plugged to DP Source Device by way of DP Branch Device(s)

When one or more DP Sink devices are connected to a DP Source device by way of a multi-stream-capable DP Branch device, AUX message transactions (as defined in Section 2.14) are needed in addition to a Time Slot Allocation AUX transaction for VC Payload time slot allocation(s). As described in defined in Section 2.6, the following DPCD registers are relevant:

- MSTM_CAP register (DPCD Address 00021h)
  - DPRX sets the register's MST_CAP bit (bit 0) to 1 to indicate the DPRX's ability to handle transporting of multiple streams and Sideband MSGs
  - DPRX sets the register's SINGLE_STREAM_SIDEBAND_MSG_SUPPORT bit (bit 1) to 1 to indicate the following:
    - DPRX's ability to handle Sideband MSGs
    - DPRX's inability to handle multiple streams
- MSTM_CTRL register (DPCD Address 00111h)
  - Takes effect only for a DPRX that has the MST_CAP bit set to 1
    - DPTX sets the register's MST_EN bit (bit 0) to 1 to indicate its intention of transmitting multiple streams
    - DPTX sets the register's UP_REQ_EN bit (bit 1) to 1 to enable Sideband MSG handling of the DPRX
  - Takes effect only for a DPRX that has the MST_CAP bit cleared to 0 and the SINGLE_STREAM_SIDEBAND_MSG_SUPPORT bit set to 1
    - DPTX sets the UP_REQ_EN bit to 1 to enable Sideband MSG handling of the DPRX

2.7.6.3 PBN Values

As defined in Section 2.6.4, a multi-stream DP Source device and multi-stream DP Branch device indicate the available link data bandwidth as a PBN value in ENUM_PATH_RESOURCES and ALLOCATE_PAYLOAD AUX message transactions (as defined in Section 2.14.9.4 and Section 2.14.9.1, respectively). One PBN is equal to 54/64MBps.

Table 2-150 defines the 128b/132b Link Layer per-time-slot PBN values. The listed PBN values take Link Layer and PHY Logical Sub-layer overhead into account; however, the values do **not** take link rate down spreading into account. The DP Source device's Payload Bandwidth Manager shall add a 0.6% margin, as defined in Section 2.6.4.1.

Table 2-150: 128b/132b Link Layer Per-time-slot PBN Values

128b/132b Link Rate (Bit Rate)	Physical Lane Count	Nominal Data Bandwidth, Excluding Down Spreading, but Including Link Layer and PHY Logical Sub-layer (MBps)	VC Payload Bandwidth When One Time Slot/MTP Is Allocated (PBN)
20Gbps/lane (UHBR20)	4	9671.1	179.09
	2	4835.5	89.55
	1	2417.8	44.77
13.5Gbps/lane (UHBR13.5)	4	6527.9	120.89
	2	3264.0	60.44
	1	1632.0	30.22
10Gbps/lane (UHBR10)	4	4835.5	89.55
	2	2417.8	44.77
	1	1208.9	22.39

2.7.7 32-bit Link Symbol Content Protection

128b/132b Link Layer supports content protection by using a 128-bit key stream that does **not** periodically re-key, such as *HDCP to DP r2.3*.

The *HDCP to DP r2.3* cipher generates 128 bits of key stream every cipher cycle. The cipher is stalled on cycles that carry Place Holder symbols in place of link symbols (see Figure 2-104, Figure 2-105, and Figure 2-106 for DP Source, Sink, and Branch devices, respectively).

128b/132b Link Layer carries 128 bits of link symbol (= 32 bits/symbol/Link Layer lane × 4 Link Layer lanes) every Link Symbol cycle. 128 bits of key stream is XOR'd with 128 bits of link symbols (i.e., encrypted) with the following exceptions:

- Control link symbols are **not** XOR'd with the key stream
- Some of the data link symbol bits in the LLCP are **not** XOR'd with key stream, as defined in Table 2-151 and Table 2-152
- MTP time slots in which the corresponding ECF bits are 0 are not XOR'd with a key stream

Table 2-151: Mapping of 128-bit Cipher Key Stream to 128b/132b Link Layer Lanes

Link Layer Lane	Cipher Key Stream Bits	128b/132b Link Symbol
3	127:96	Lane 3 Link Symbol Cycle *N*
2	95:64	Lane 2 Link Symbol Cycle *N*
1	63:32	Lane 1 Link Symbol Cycle *N*
0	31:0	Lane 0 Link Symbol Cycle *N*

Table 2-152: XOR'ing/Non-XOR'ing of LLCP with Key Stream

LLCP Link Symbol Number[a]	Symbol Type	Bit #	Comments
0	LLCP_MARKER Control Link Symbol	31:0	Marks the LLCP, **not** XOR'd.
1	Data Link Symbol 0	0	ACT, **not** XOR'd.
		1	HDCP Encryption Indicator, **not** XOR'd.
		15:2	RESERVED, reads all 0s, **not** XOR'd.
		31:16	ECF[15:0], **not** XOR'd.
2	Data Link Symbol 1	31:0	ECF[47:16], **not** XOR'd.
3	Data Link Symbol 2	15:0	ECF[63:48], **not** XOR'd.
		31:16	LVP, XOR'd.

a. The LLCP is transmitted on all four Link Layer lanes.

The HDCP Encryption Indicator bit indicates whether HDCP Encryption over a 128b/132b DP link is enabled or disabled, as illustrated in Figure 2-113. The ECF field value takes effect from the MTP that immediately follows the LLCP.

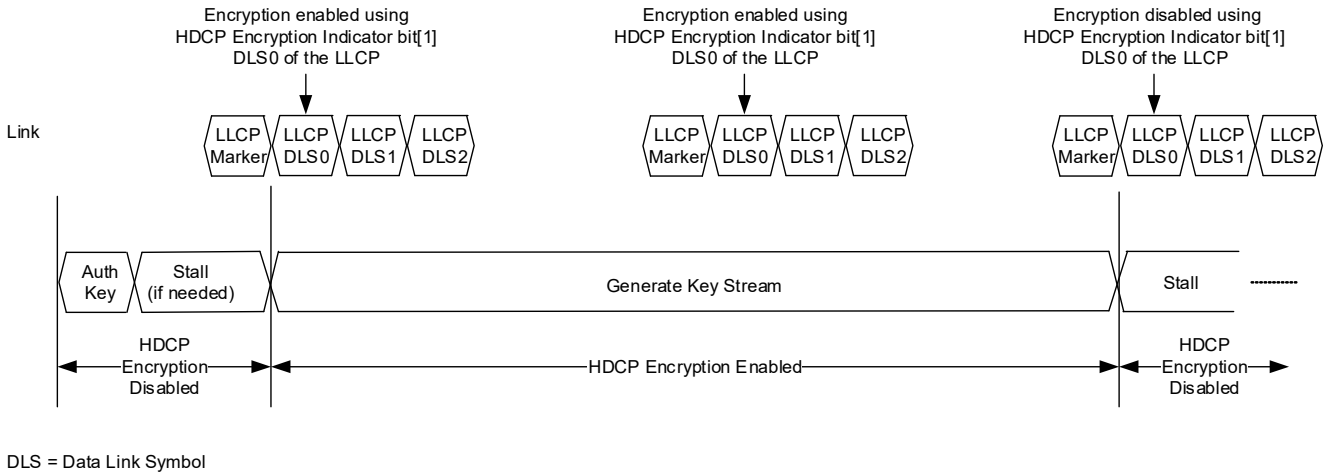


Figure 2-113: 128b/132b DP Link HDCP Encryption Status Signaling

2.7.8 Place Holder Symbol Insertion

Note: *The place holder symbols used in 128b/132b channel coding are* ***not*** *link symbols.*

As described in Section 3.5.2.13.2, a PHY sync symbol is transmitted as the Symbol[44] location, the 1st symbol of the last super symbol of the last RS block of the PHY Logical Frame consisting of 384 symbols. Additionally, 128b/132b PHY Logical Sub-layer has an overhead of 4 bits for every 128 information bits within the PHY Logical Sub-layer.

To account for PHY sync symbol insertion and 128b/132b PHY Logical Sub-layer overhead, 128b/132b Link Layer inserts place holder symbols, as follows:

- Insert one PHY sync place holder symbol for every 383 link symbols
- Insert one coding overhead place holder symbol for one of the following:
  - Every one PHY sync place holder symbol plus 31 link symbols, –or–
  - Every 32 link symbols

Figure 2-114 illustrates an example of DPTX 128b/132b Link Layer place holder symbol insertion for each of the four Link Layer lanes.

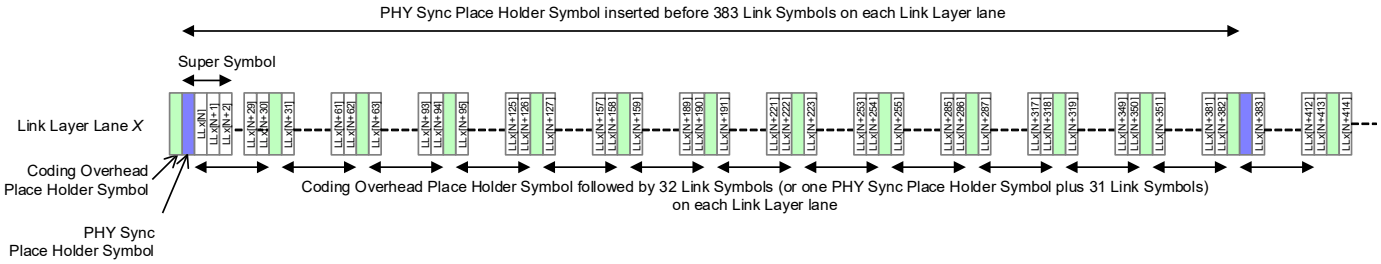


Figure 2-114: DPTX 128b/132b Link Layer Place Holder Symbol Insertion (Informative)

Note: *An alternate approach to the place holder method can be found in Appendix M. The resulting bitstream from both approaches will be identical.*

2.8 Compressed Display Stream Transport Services

DisplayPort may transport a bitstream as per *DSC Standard*. Display Stream Compression (DSC) may be supported for DP Source, Sink, and Branch devices. When DSC is enabled, FEC shall also be enabled.

DP DSC maps to a new Stream Compression Layer, logically located below the Stream Layer and above the Transport Layer in the DP Layer Architecture Model, as illustrated in Figure 2-115. The DSC algorithm, described in *DSC Standard*, is logically separate from the transport services. This logical separation is neither intended to imply nor restrict an implementation.

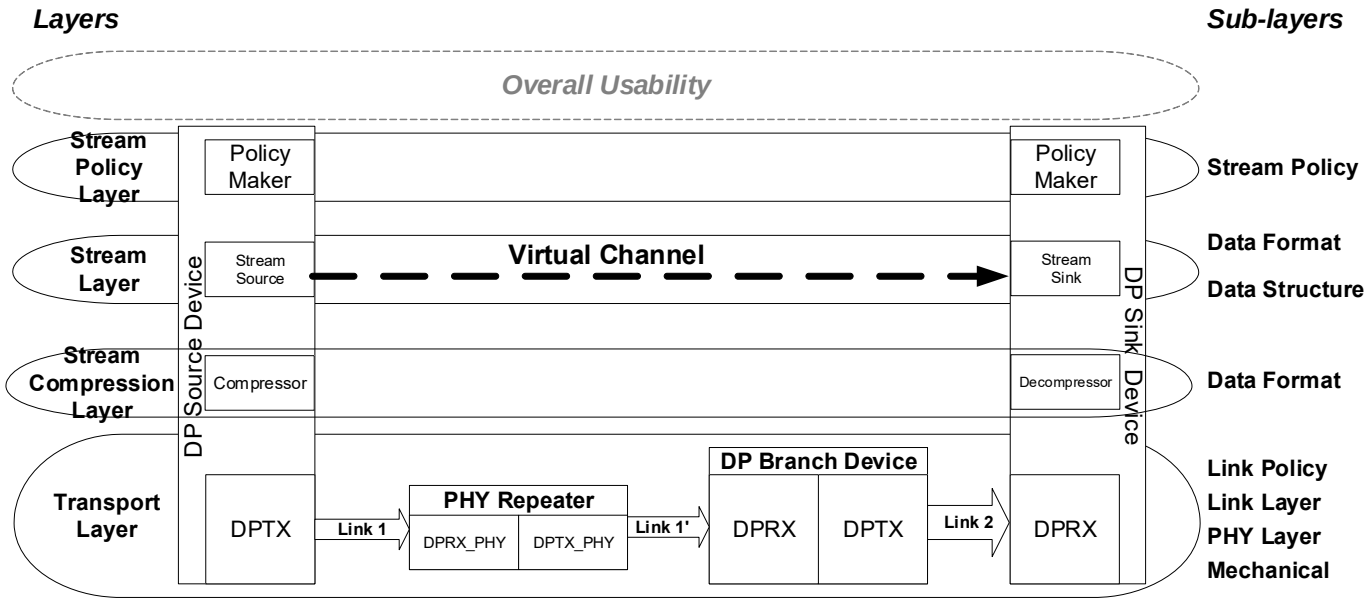


Figure 2-115: DP Layer Architecture Model with Compression

2.8.1 Transport Buffer Model

Figure 2-116 illustrates an architectural view of the compression elements and transport buffers. A downstream frame buffer may be included with the compressed data before the Decompressor, or with the reconstructed data after the Decompressor. System designers should see *DSC Standard* for rate buffer size mandates for any combination of pixel stream and the bitstream rate.

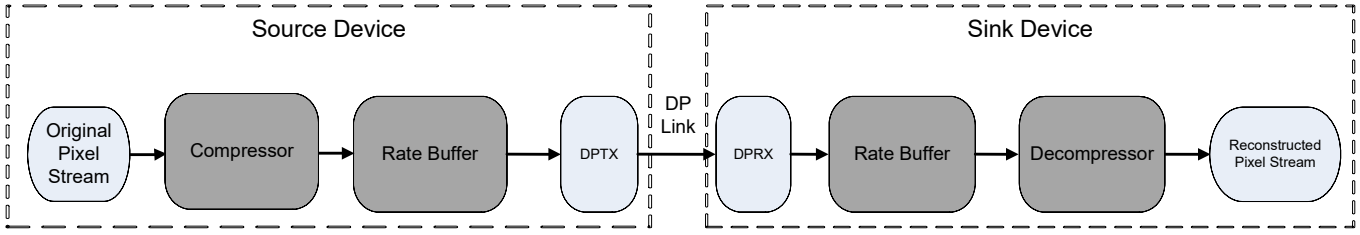


Figure 2-116: High-Level Compression Architectural Elements

2.8.2 DSC Bitstream Transport over DP SST/MST Link

Each SST or MST virtual channel may carry a single independent DSC bitstream. DSC bitstreams on separate virtual channels are considered independent and shall be decoded without information from other virtual channels. The PPS transmitted on a virtual channel applies only to the DSC bitstream transmitted on that virtual channel.

Figure 2-117 illustrates an example SST topology that transmits a single DSC bitstream with 16 vertical slices. Figure 2-118 illustrates an example MST topology that transmits four DSC bitstreams over four virtual channels, each with four vertical slices. Although both examples include only a single DSC encoder and decoder per bitstream, other encoder/decoder implementations are possible.

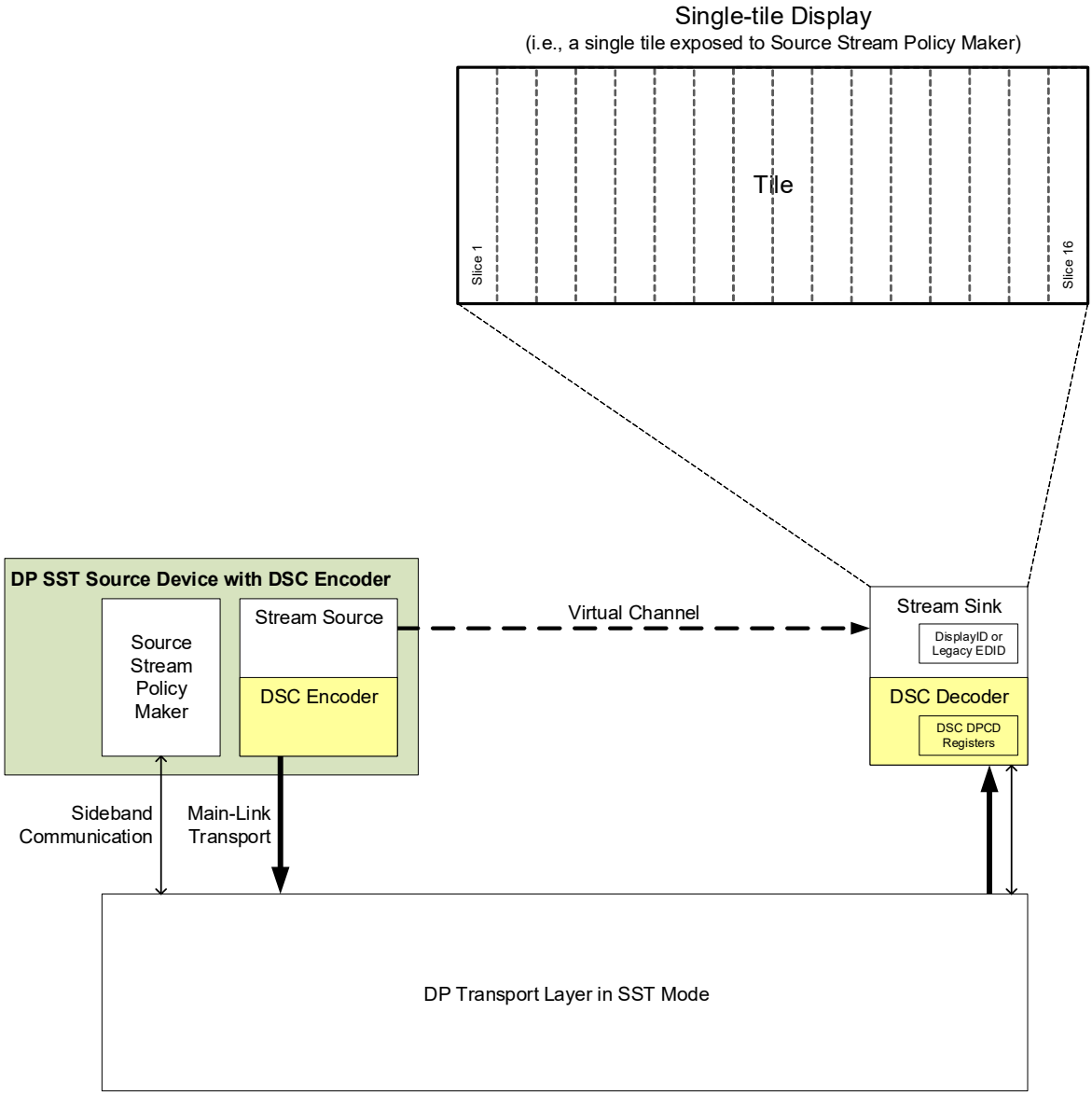


Figure 2-117: Single DSC Bitstream DP SST Display Example

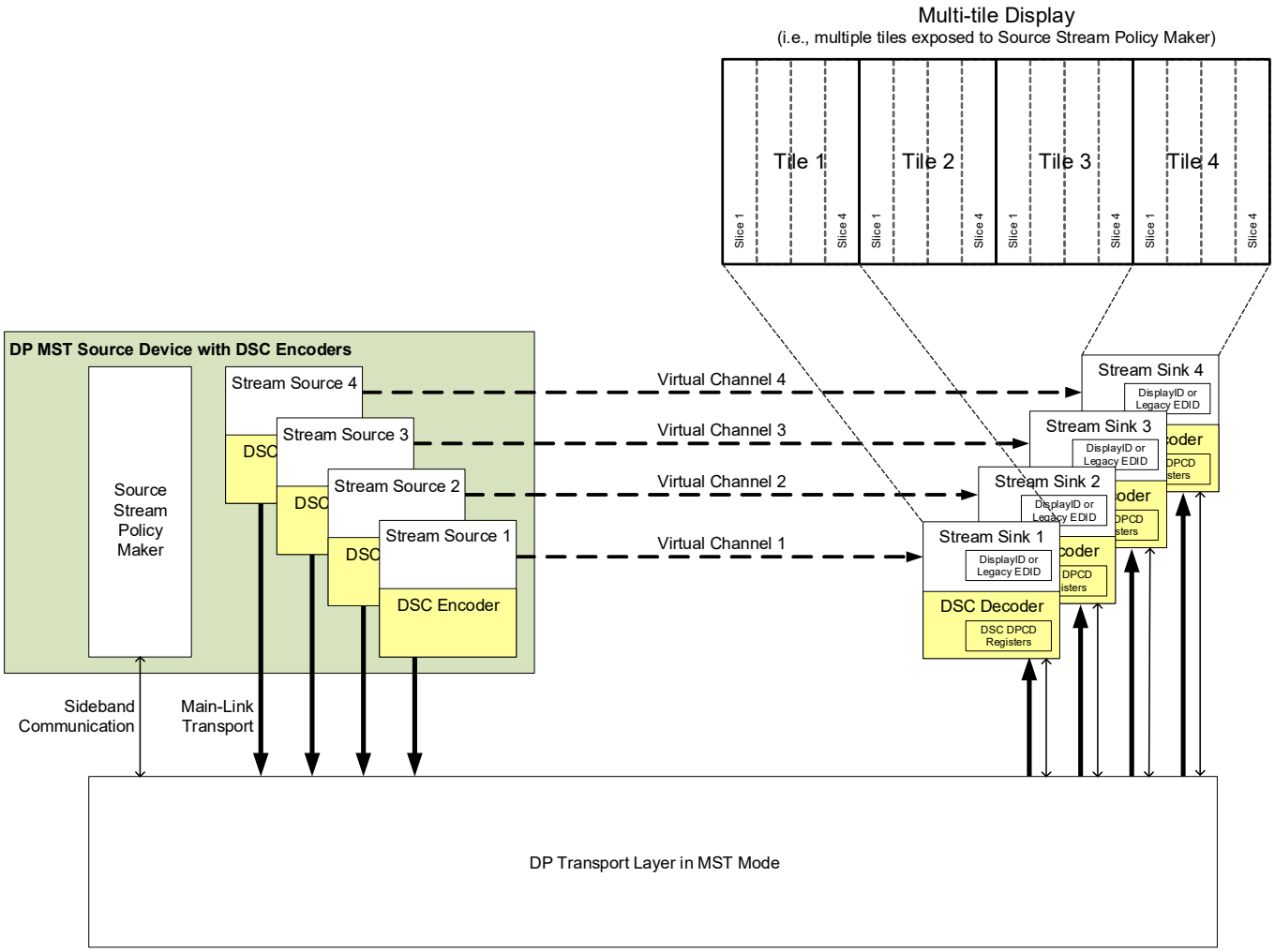


Figure 2-118: Multiple DSC Bitstream DP MST Display Example

2.8.3 DSC Configuration – Discovery, Enabling, and Disabling

This section describes the policy of DP DSC transport discovery, enabling, and disabling for DSC-capable DP devices.

2.8.3.1 DP DSC Sink Device Configuration

Updated in *DP v2.0*.

A DSC decompression-capable DP device is referred to as a "DP DSC Sink device." A DP DSC Sink device may be either a DP Sink or Branch device that is DSC decompression-capable. A device shall declare its decompression capability in the DSC Capability DPCD registers (DPCD Addresses 00060h through 0006Fh, 000A0h through 000A2h, and 02260h through 0226Fh).

The DP DSC Sink device shall support the compression bit rate range listed in the **Mandatory Bit Rate Range Support** column of Table 2-153 for each DSC pixel encoding format and component bit depth (bits/component, bpc) that it reports to support in the DSC DECODER PIXEL ENCODING FORMAT CAPABILITY registers (DPCD Addresses 00069h and 02269h). The device shall support the range, in increments, with the bits/pixel increment precision (1bpp or smaller) reported in the INCREMENT OF ***bits_per_pixel SUPPORTED BY THE DECOMPRESSOR*** field in the DSC_MAX_BPP_DELTA_AND_BPP_INCREMENT registers (DPCD Addresses 0006Fh and 0226Fh, bits 2:0).

There is a range of possible supported target bits/pixel values between the highest values provided in the **Mandatory Bit Rate Range Support** column, and the **Maximum Allowed Bit Rate** column in Table 2-153. The maximum decompressor-supported bits/pixel shall be reported in the DSC_MAX_BPP_DELTA_AND_BPP_INCREMENT registers (DPCD Addresses 0006Eh and 0006Fh, and 0226Eh and 0226Fh) with the MAX_BPP_DELTA_AVAILABILITY bit in the MAXIMUM ***bits_per_pixel SUPPORTED BY THE DECOMPRESSOR*** registers (DPCD Addresses 00068h and 02268h, bit 7) set to 1. When the DSC_MAX_BPP_DELTA_AND_BPP_INCREMENT registers are cleared to all 0s, the maximum decompressor-supported bits/pixel values are as listed in the **Maximum Allowed Bit Rate** column in Table 2-153.

Table 2-153: DP DSC Sink Device Compressed Transport Bit Rate Range

DSC Pixel Encoding Format	Mandatory Bit Rate Range Support for 8, 10, or 12bpc Input (bpp)[a]	Maximum Allowed Bit Rate for 8, 10, or 12bpc Input (bpp)[a]
4:4:4 or Simple 4:2:2	$8 \le n \le 16$	3 × bpc
Native 4:2:2[b]	$7 \le n \le 16$	2 × bpc
Native 4:2:0[b]	$6 \le n \le 12$	1.5 × bpc

a. The "bpc" is the bits/component of the original video input to the DSC encoder.
b. Native 4:2:2 mode is supported only by DSC v1.2 (and higher). Native 4:2:0 mode is supported only by DSC v1.2a (and higher).

For a DP DSC Sink device that supports 128b/132b channel coding, changes in the DSC target bits/pixel between two compressed frames, such as could occur during network or link topology transitions, shall be handled without a noticeable visible glitch (see the following note). This is normative for both SST and MST streams, and also applies to 8b/10b channel coding for any DP Sink device that supports 128b/132b capabilities. This is **optional** but also recommended for devices that do **not** support 128b/132b channel coding. The Dynamic PPS Update Support – Compressed-to-Compressed bit in the DSC SUPPORT and DSC SUPPORT AND DSC DECODER COUNT registers (DPCD Addresses 00060h and DPCD Address 02260h, respectively, bit 2) shall be set to 1 when the capability is supported.

Note: *It is **not** possible to completely eliminate individual pixel changes because a frame compressed at a different compression level is expected to have minor changes in the reconstructed image. The intent is that frame-to-frame changes should be limited only to minor image differences from the compression-level adjustment. There should **not** be any user-visible glitches, corruption, or tearing.*

A DP DSC Sink device that can also support dynamic target bits/pixel changes between uncompressed and compressed frames, without a noticeable visible glitch shall set the Dynamic PPS Update Support – Uncompressed-to/from-Compressed bit in the DSC SUPPORT and DSC SUPPORT AND DSC DECODER COUNT register(s) (DPCD Address(es) 00060h and DPCD Address 02260h, respectively, bit 3). This shall apply for both 8b/10b and 128b/132b channel coding.

Examples of supported changes:

- **SST link in a hub topology with MST input** – The SST link may experience a change in DSC bits/pixel. This applies to DP DSC Sink devices that support only SST mode.
- **MST into a hub** – When a display is connected or disconnected from a hub, the other streams may experience a change in the DSC bits/pixel.

2.8.3.2 DP DSC Source Device Configuration

Updated in *DP v2.0*.

A DSC-capable DP Source device is referred to as a "DP DSC Source device." A DP DSC Source device shall read the DSC Capability DPCD registers (DPCD Addresses 00060h through 0006Fh, 000A0h through 000A2h, and 02260h through 0226Fh) to confirm whether the downstream DP device is capable of supporting decompression.

The DSC data structures of a DP DSC Sink device are held in the DSC DPCD register locations from DPCD Addresses 00060h through 0006Fh and 02260h through 0226Fh that are accessed through native AUX transactions. For MST devices, the DSC data structures are accessed through REMOTE_DPCD_READ message transactions to the virtual DP peer device. (See Section 2.6.1.1.)

A DP DSC Source device shall program the bit rate within the range of **Minimum Allowed Bit Rate** column in Table 2-154 and the maximum bit rate supported by the connected DP DSC Sink device (inclusive) enumerated in the MAXIMUM ***bits_per_pixel SUPPORTED BY THE DECOMPRESSOR*** registers (DPCD Addresses 00067h and 00068h, and 02267h and 02268h), and DSC_MAX_BPP_DELTA_AND_BPP_INCREMENT registers (DPCD Addresses 0006Eh and 0006Fh, and 0226Eh and 0226Fh). The DP DSC Source device may support this range, in increments of 1bpp or smaller. If a smaller increment is chosen, it shall not be smaller than the increment capability supported by the DP DSC Sink device, which is enumerated in the INCREMENT OF ***bits_per_pixel SUPPORTED BY THE DECOMPRESSOR*** field in the DSC_MAX_BPP_DELTA_AND_BPP_INCREMENT registers (DPCD Addresses 0006Fh and 0226Fh, bits 2:0).

Table 2-154: DP DSC Source Device Compressed Transport Bit Rate Range

DSC Pixel Encoding Format	Minimum Allowed Bit Rate for 8, 10, or 12bpc Input (bpp)
4:4:4 or Simple 4:2:2	8
Native 4:2:2[a]	7
Native 4:2:0[b]	6

a. Native 4:2:2 mode is supported only by DSC v1.2 (or higher). Native 4:2:0 mode is supported only by DSC v1.2a (or higher).

A DP DSC Source device that needs to change the bit rate, –or– transition from uncompressed display stream to DSC bitstream (or vice versa) at a video frame boundary, shall check whether the connected DP DSC Sink device is capable of handling the dynamic change without visual glitch. The DP DSC Sink device and any Branch device advertises this capability in the following Dynamic PPS Update Support-related bits in the DSC SUPPORT and DSC SUPPORT AND DSC DECODER COUNT registers (DPCD Addresses 00060h and DPCD Address 02260h, respectively):

- Dynamic PPS Update Support – Compressed-to-Compressed bit (bit 2)
- Dynamic PPS Update Support – Uncompressed-to/from-Compressed bit (bit 3)

For a DP adapter that is connected to a non-DP Sink device, at such time when DisplayID incorporates a new data block that enumerates a range of supported targeted bits/pixel rates for the stream sink, a DP DSC Source device shall take the supported bit rates into account when determining the link configuration and peak pixel rate for the DSC bitstream to be routed to the stream sink.

2.8.3.3 Enabling DP DSC Source Device Encoding

Figure 2-119 illustrates the initial DSC discovery, setup, and enable.

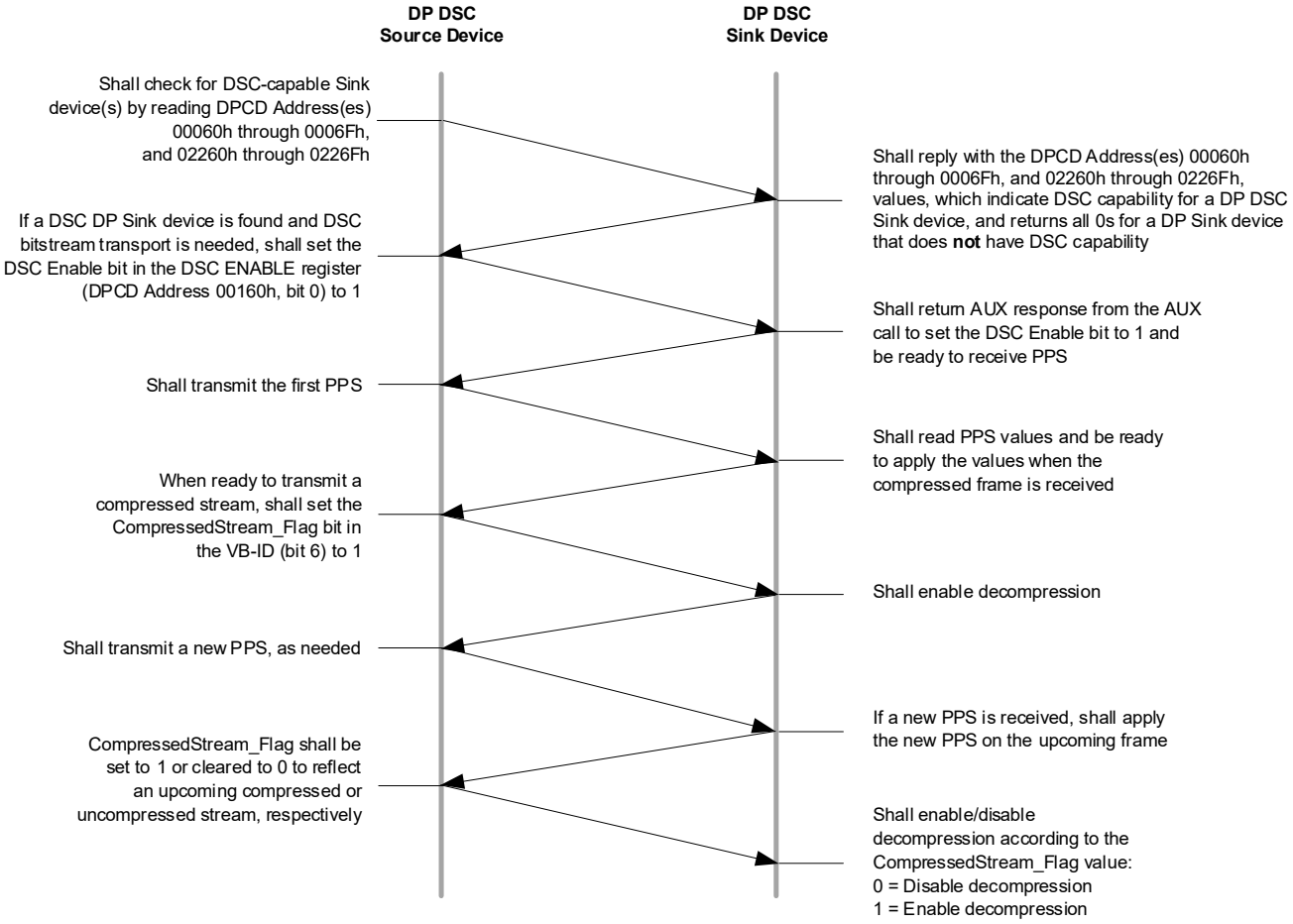


Figure 2-119: Initial DSC Discovery, Setup, and Enable

A DSC-capable device with a higher *DSC v1.sub-version number* (e.g., *v1.2*) shall be able of operating with any other DSC-capable device of the same or lower *DSC v1.sub-version number* (e.g., *v1.2* and *v1.1*). See *DSC Standard* for further details regarding interoperability between sub-versions.

If a DP DSC Sink device is discovered downstream, a DP DSC Source device may enable compression by setting the DSC Enable bit in the DSC ENABLE register (DPCD Address 00160h, bit 0) to 1. After the bit is set, the DP DSC Source device shall not clear DSC Enable bit to 0 while the CompressedStream_Flag bit in the VB-ID (bit 6) is set to 1.

After the DP DSC Source device receives an ACK from its setting of the DSC Enable bit, the DP DSC Source device shall transmit the Picture Parameter Set (PPS), as detailed in Section 2.2.5.8. Only after the PPS is transmitted shall the Source device set the CompressedStream_Flag bit in the VB-ID (bit 6) to indicate whether compression is enabled (flag state of 1) or disabled (flag state of 0), over each individual video frame following the VB-ID. The PPS value shall persist across the CompressedStream_Flag transitions. The PPS shall be transmitted, as follows:

- After the DSC Enable bit is set, and
- If a PPS parameter changes

See *DSC Standard* for further details.

If compression on a frame is enabled, the DP DSC Source device shall set the CompressedStream_Flag to 1 no later than one scan line prior to the active region. If compression on a frame is disabled, the DP DSC Source device shall clear the CompressedStream_Flag to 0 no later than one scan line prior to the active region. These timing mandates are illustrated in Figure 2-120, which defines these timings relative to events visible to a DPRX.

2.8.3.4 DP DSC Sink Device DSC Decoding Enabling

After transmitting an ACK response to the AUX write transaction (DP SST DSC Sink device) or REMOTE_DPCD_WRITE message transaction (DP MST DSC Sink device) to set the DSC Enable bit in the DSC ENABLE register (DPCD Address 00160h, bit 0) to 1, a DP DSC Sink device shall be ready to receive and process the PPS followed by the compressed stream, until the DP DSC Source device clears the DSC Enable bit to 0.

The DP DSC Sink device shall use any PPS transmitted from the DP DSC Source device only while the DSC Enable bit is set to 1. The device shall ignore any PPS that is received when the DSC Enable bit is cleared to 0.

The DP DSC Sink device shall monitor the CompressedStream_Flag bit in the VB-ID (bit 6), which indicates whether compression is enabled (flag state of 1) or disabled (flag state of 0), over each individual video frame.

The DP DSC Sink device shall ignore this flag state during the active region. These timing mandates are illustrated in Figure 2-120, which defines these timings relative to events visible on the DP link.

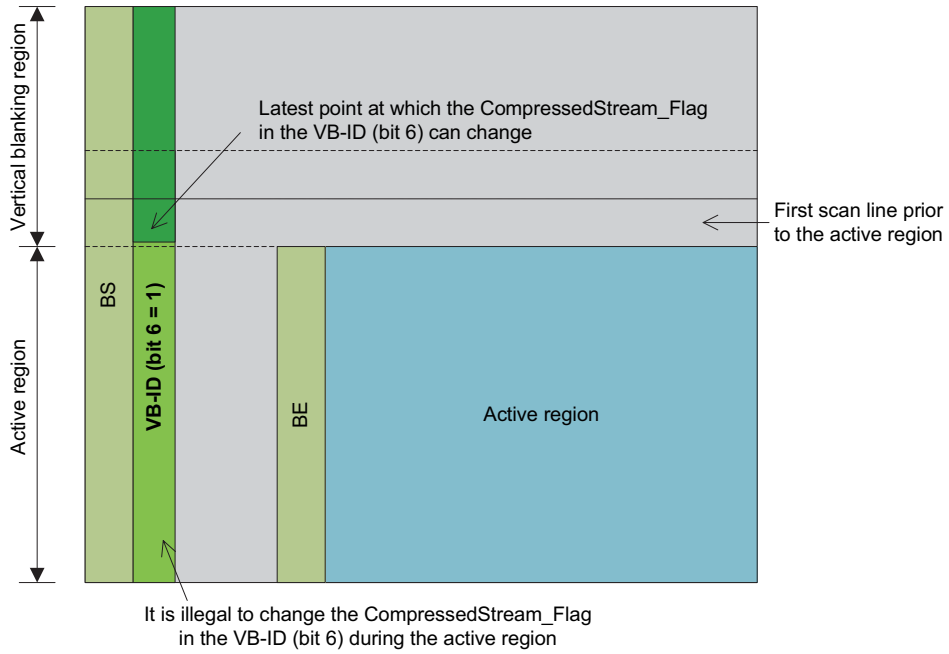


Figure 2-120: Compressed/Uncompressed Stream Indication in VB-ID

2.8.4 Minimum Slices/Display Line Mandate

Updated in *DP v2.0*.

A DSC-capable display device shall support, at a minimum, a configuration with a specific number of slices/display line for each of the display's supported video timing formats defined as a combination of resolution and refresh rate. Table 2-155 defines the number of slices/display line that are needed for various pixel throughput rates.

When a DP MST display is driven by more than one DSC bitstream, the display peak pixel rate (ppr) is the cumulative peak pixel rate of all the DSC bitstreams that are used for the display. The number of slices/display line is the sum of all slices for all DSC bitstreams that are used for the display. The slice width shall be the same for all DSC bitstreams used for the display. See Figure 2-118 for an example.

The supported number of slices per DP DSC Sink device that is declared in the following registers represents the slice count per DP DSC Sink device:

- DSC SLICE CAPABILITIES 1 register(s) (DPCD Address(es) 00064h and 02264h)
- DSC SLICE CAPABILITIES 2 register(s) (DPCD Address(es) 0006Dh and 0226Dh)

Each DP DSC Sink device decodes a single DSC bitstream.

For tiled displays whose tile count, when divided into the slice/display line mandate, does **not** provide a standard value as allowed in the DSC SLICE CAPABILITIES 1 and DSC SLICE CAPABILITIES 2 registers, the number of slices across a horizontal line per tile (per DP DSC Sink device) shall be increased to the next higher number that is allowed within the two registers.

See Appendix L for examples of how to use Table 2-155 with the mandates outlined within this section.

Table 2-155: Number of Slices Needed per Display Line[a]

Display Peak Pixel Rate (ppr) (MP/s)	Slice/Display Line Mandate[b]	Alternative Slice/Display Line Mandate[c]
ppr ≤ 340	1	1
340 < ppr ≤ 680	2	1
680 < ppr ≤ 1360	4	2
1360 < ppr ≤ 3200[d]	8[d]	4
3200 < ppr ≤ 4800	12	8
4800 < ppr ≤ 6400	16	8
6400 < ppr ≤ 8000	20	12
8000 < ppr ≤ 9600	24	12

a. *Table values are subject to different restrictions and/or limits. See the text within this section for rules specific to handling maximum slice width.*

b. *This column has mandates based on a DP DSC Source device at a 1-pixel/clock (DP DSC Sink device at 3 pixels/clock) throughput rate. The third ("**Alternative**") column addresses a DP DSC Source device at a 2-pixels/clock (DP DSC Sink device at 6 pixels/clock) throughput rate. See the text within this section for further details.*

c. ***For use with DSC v1.2 (and higher) Native 4:2:2 and DSC v1.2a (and higher) 4:2:0 modes only** – This column applies when both of the following conditions exist:*
   - *A given timing format is available only in the YCbCr4:2:2 and/or YCbCr4:2:0 format*
   - *DP DSC Sink device supports YCbCr Native 4:2:2 and/or YCbCr Native 4:2:0 (as indicated by the YCbCr Native 4:2:2 Support and YCbCr Native 4:2:0 Support bits in the DSC DECODER PIXEL ENCODING FORMAT CAPABILITY register(s) (DPCD Address(es) 00069h and 02269h, bits 3 and 4, respectively).*

d. *The ppr values in MP/s units that are greater than 2720 assume a DSC throughput capability of 400MP/s. The ppr values in MP/s units that are less than or equal to 2720 assume a DSC throughput capability of 340MP/s.*

If the slice size from the table needs a size greater than MaxSliceWidth (number of pixels/chunk, as specified by the DSC Maximum Slice Width register(s) (DPCD Address(es) 0006Ch and 0226Ch)), the next higher allowed slice count value shall be used in place of the table-supplied value. This adjustment repeats until the slice width is less than or equal to MaxSliceWidth.

For further details and usage examples, see Appendix L.

A DP DSC Source device shall be able to support all slice/display line combinations listed in Table 2-155, up to the highest display mode that the Source device supports.

A DP DSC Source device may set any slice/display line count that the DP DSC Sink device supports, as long as the slice width is less than or equal to MaxSliceWidth and does not violate the DP DSC Sink device's peak DSC throughput.

2.8.4.1 Additional Slice per DP DSC Sink Device Options

A DP DSC Sink device may support additional slice per DP DSC Sink Device configurations. All supported slice per DP DSC Sink Device configurations shall be declared in the following registers:

- DSC SLICE CAPABILITIES 1 register(s) (DPCD Address(es) 00064h and 02264h)
- DSC Peak Throughput (DSC Sink) register(s) (DPCD Address(es) 0006Bh and 0226Bh)

2.8.4.2 Additional DP DSC Sink Capabilities

If a DP DSC Sink device can support throughputs other than the default values (340 and 400MP/s in 3-pixels/clock mode; see Section 2.8.4) or slice widths greater than the default width of 2560 pixels, the device may declare its greater capabilities in the registers listed below. The DP DSC Source device may then use this information to identify possible additional supported configurations.

- DSC Peak Throughput (DSC Sink) register(s) (DPCD Address(es) 0006Bh and 0226Bh)
- DSC Maximum Slice Width register(s) (DPCD Address(es) 0006Ch and 0226Ch)

For example, a 4K (3840-pixel-wide) display that uses *CVT Standard* timings with reduced Blanking Timing v1 at a 90Hz refresh rate needs a maximum Peak Pixel rate of 811.44MP/s. As per Table 2-155, this shall be supported with 4 slices/display line; however, other configurations may be possible. A DP DSC Source device could choose to use 2 slices/display line if the DPCD registers report the following capabilities:

- Throughput Mode 0 reports a value of 450MP/s or greater (450MP/s is the smallest register value that would support a throughput of 811.44 / 2 = 405.72MP/s/slice)
- DSC Maximum Slice Width register(s) report a value of 1920 pixels (3840 / 2) or greater

An alternate throughput rate of 170MP/s (value of 15 for each mode) is defined in the DSC Peak Throughput (DSC Sink) register to allow for special test designs and custom uses. Use of this value will disqualify the DP Sink device from receiving DP DSC compliance certification.

DP Source devices should support this alternate throughput rate when sufficient slices are available.

A DP Source device that does not support the alternate throughput rate, –or– does not recognize the value of 15, should **not** enable DSC to the DP Sink. If the alternate throughput rate is supported but there are insufficient slices available for the desired configuration, the DP Source device has the option to either not enable DSC, –or– to choose a different resolution/slice count combination that would work.

A DP Branch device with DSC decompression may have additional restrictions on overall throughput and line buffer size because these are independent from the downstream Sink device's DisplayID or legacy EDID and **not** fully covered by the DP Branch device's per-slice DPCD capabilities. The DP DSC Branch device may report its limitations in the following capability registers:

- BRANCH DSC OVERALL THROUGHPUT MODE 0 register (DPCD Address 000A0h)
- BRANCH DSC OVERALL THROUGHPUT MODE 1 register (DPCD Address 000A1h)
- BRANCH DSC MAXIMUM LINE BUFFER WIDTH register (DPCD Address 000A2h)

If these capability registers are cleared to all 0s, no additional restrictions on overall throughput and line width shall be required, and the DP Source device shall assume that the overall limits are provided by per-slice limits multiplied by the number of reported slices.

For interoperability, the overall throughput and line width restrictions on a DP DSC Branch device shall **not** change the minimum per-slice mandates. A 4-slice DP DSC Branch device shall support a pixel throughput of at least (2 slices × 340MP/s/slice = 680MP), and a maximum line width of at least (2 slices × 2560 pixels/slice = 5120 pixels). The 4-slice DP DSC Branch may program its maximum pixel throughput to a setting below (4 slices × 340MP/s/slice = 1380MP) and/or its maximum line width to a setting below (4 slices × 2560 pixels/slice = 10240 pixels).

The DSC Capability registers located at DPCD Addresses 000A0h through 000A2h are valid for a DP Branch device that has a DSC decoder with more than two slices. On a DP multi-stream Branch device, the register values are applicable to both a native 4-slice decoder and a 4-slice decoder created by the aggregation of two 2-slice decoders. A DP Branch device that does **not** have a DSC decoder with more than two slices shall reply with all 0s when read. A 2-slice decoder shall meet the following mandates:

- **Overall peak throughput** – 340MP/s/slice
- **Line buffer width** – 2560 pixels/slice

A DP DSC Source device shall honor the mandates of a downstream DSC Branch device in the DSC Capability registers located at DPCD Addresses 000A0h through 000A2h for any streams that are decoded by that DP DSC Branch device.

2.8.4.3 RGB Color Conversion Bypass (Informative)

New to *DP v2.0*.

RGB Color Conversion Bypass mode can be used to improve compression results for head-mounted displays (HMDs) that do pre-correction for chromatic aberration distortions before the display stream is compressed. (HMDs are commonly used for augmented reality/virtual reality (AR/VR).) This **optional** mode is available only for *DSC v1.2a* (and higher) encoders and decoders and for RGB 4:4:4 input. RGB Color Conversion Bypass mode should **not** be used in any other configuration.

To support this mode, the following conditions shall exist:

- RGB components shall be able to map directly to the encoder's CrYCb channels
- Decoder's YCbCr channels shall be able to map directly to the GBR output components

Table 2-156 defines the mandatory color channel mapping.

Table 2-156: Color Channel Mapping for RGB Color Conversion Bypass Mode

Input to Encoder	YCbCr Channels		Decoder Output
Red	Cr	(U in YUV)	**Red**
Green	Y	(Y in YUV)	**Green**
Blue	Cb	(V in YUV)	**Blue**

If the decoder is capable of supporting RGB Color Conversion Bypass mode, the decoder shall set the RGB Color Conversion Bypass Support bit in the DSC FEATURE SUPPORT registers (DPCD Addresses 00066h and 02266h, bit 1) to 1.

A DP DSC Source device can enable RGB Color Conversion Bypass mode only when the DP DSC Source device detects that the RGB Color Conversion Bypass Support bit is set to 1. To enable RGB Color Conversion Bypass mode, the DSC PPS syntax elements listed in Table 2-157 shall be cleared to 0.

Table 2-157: DSC PPS Syntax Element Flags and Settings Needed for Enabling RGB Color Conversion Bypass Mode

PPS Syntax Element	Size (Bits)	Format	Maps To	Description
convert_rgb	1	Flag	PPS4[4]	0 = Do not convert RGB to/from YCoCg-R (CrYCb).[a]
simple_422	1	Flag	PPS4[3]	0 = RGB only.
native_420	1	Flag	PPS88[1]	0 = RGB only.
native_422	1	Flag	PPS88[0]	0 = RGB only.

a. DSC v1.2a says that the value of 0 = Color space is YCbCr.. This is the equivalent to what RGB Color Conversion Bypass mode is doing when it maps the RGB channels to the encoder's CrYCb channels and then back with the decoder.

At this point, the DP DSC Source device shall map its RGB channels to the DSC YCbCr channels, as per Table 2-156, without any color space conversion.

A DP DSC Sink device, upon seeing the DSC PPS parameters cleared as listed in Table 2-157, shall map its DSC YCbCr output channels directly to its RGB channels, without any color space conversion.

Note: *The codecs will treat the RGB input the same way that they treat YCbCr 4:4:4 input, neither with color space conversion. The only difference is that the DP DSC Source device is RGB 4:4:4 which, when not using this mode, would always be converted to/from YCbCr.*

2.8.4.3.1 Using the DSC Software Model with RGB Color Conversion Bypass Mode

For convenience, the DSC software model includes color conversion for RGB input/output. However, this color conversion is not part of *DSC v1.2a* and is expected to be supplied by the transport, as needed, when going into a DSC encoder and coming out of a DSC decoder.

Because the software model includes additional error checking, simply feeding in an RGB image and programming the configuration (.cfg) file to **not** do the conversion will be overridden by the software model, which considers this to be a user error.

To work around this error checking, a .dpx image file should be used, but with the R, G, and B samples mapped to the Cr, Y, and Cb components, respectively, before running the DSC software model. The .cfg file shall include the settings listed in Table 2-158 when in RGB Color Conversion Bypass mode.

The C model output shall need to have its Cr, Y, and Cb components re-mapped to the R, G, and B channels, respectively, before viewing or any further decoder output processing.

Table 2-158: DSC .cfg File Settings for RGB Color Conversion Bypass Mode

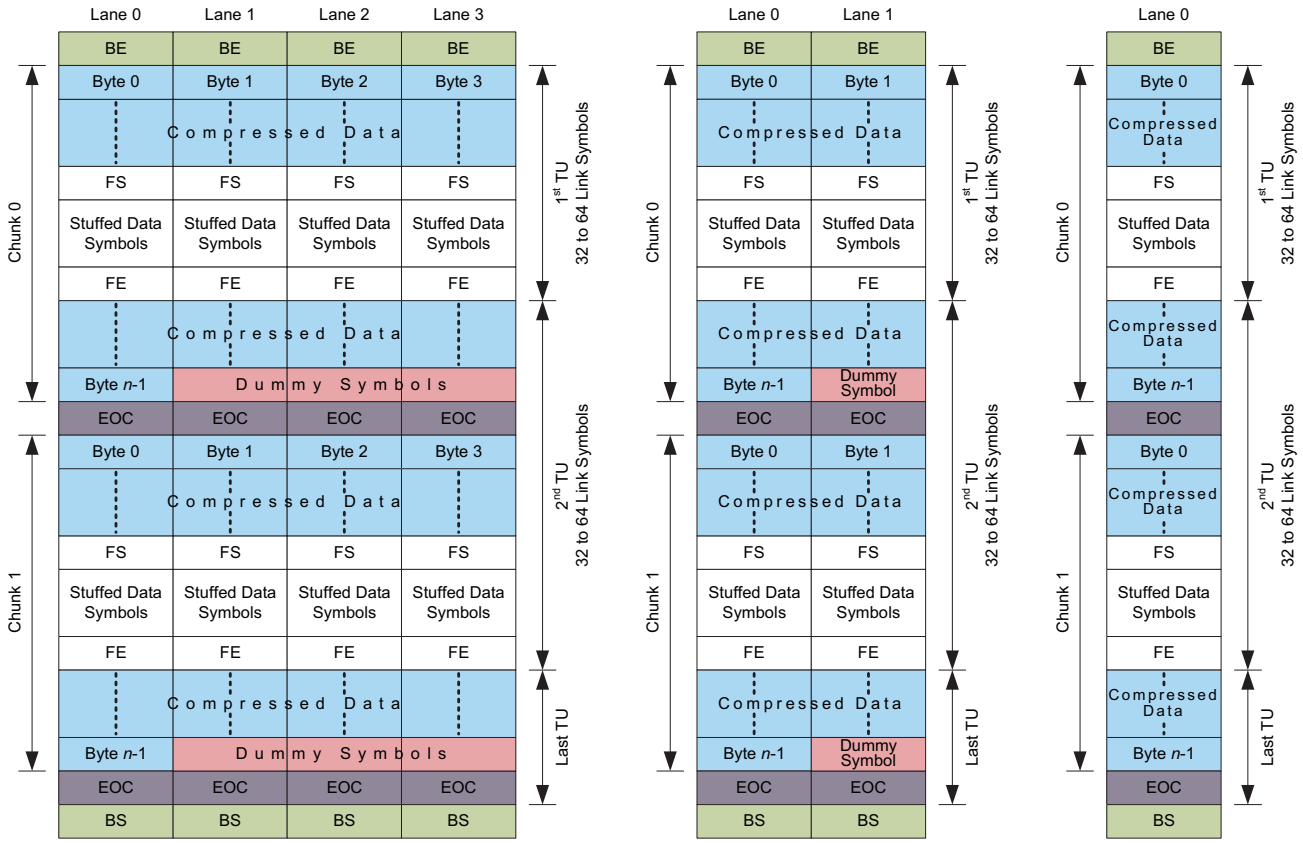
DSC .cfg File Parameter	Value	Description
USE_YUV_INPUT	1	Although the data format is really RGB, do **not** convert RGB to YCbCr in RGB Color Conversion Bypass mode.
SIMPLE_422	0	Input data is **not** 4:2:2.
NATIVE_422	0	Input data is **not** 4:2:2.
NATIVE_420	0	Input data is **not** 4:2:0.

2.8.4.4 Framing and Compressed Stream Mapping

This section describes the rules for transporting a compressed stream over the DP Main-Link.

When a Source device enables DSC, the DP DSC Source device shall transmit a DSC-encoded bitstream, instead of uncompressed raw pixel data, over the link during the active video period. The Source device shall maintain the video frame format. The definition of MSA remains unchanged.

The slice height shall be restricted such that the active video height is an integer multiple of this value. Compressed Display Stream data is transported (in chunks). The Source device shall insert an End of Chunk (EOC) after the transmission of each chunk. EOC shall be inserted in all lanes in the same LS_Clk (DP Main-Link Symbol Clock) cycle. Figure 2-121 illustrates EOC placement.



BS = Blank Start
BE = Blank End
EOC = End of Chunk
FS = Fill Start
FE = Fill End
TU = Transfer Unit
n = Number of bytes within a chunk

Figure 2-121: Packing DSC Data Bytes within a Video Frame Example

The bytes of the DSC bitstream are spread across the enabled lanes, starting with Byte 0 on Lane 0. If the bytes within a chunk are not a multiple of the number of lanes, dummy data shall be inserted as padding to make it a multiple of the number of lanes. The dummy data contents used for padding is TX implementation-specific. Note that normal data, rather than special K-codes, shall be chosen. The chunk, as well as any necessary padding, shall then be followed by an EOC. Table 3-9 and Table 2-144 define EOC control link symbol to 8b/10b special character mapping for SST and MST modes, respectively.

In SST and MST modes, the Source device shall transmit the BS symbol sequence after the device transmits the last chunk of the scan line and EOC, as described in Section 2.2.1.2. Compressed data transmission shall resume immediately after the next BE symbol. In MST mode, EOC control link symbols are inserted four times, regardless of the lane count (i.e., four consecutive time slots in 1-lane configuration, two consecutive time slots across two lanes in 2-lane configuration, and one time slot across four lanes in the 4-lane configuration), as is the case with the uncompressed video stream transport in MST mode described in Section 2.6.3.

If the number of bytes received for a chunk does **not** match the PPS-specified chunk size, the DP DSC Sink device shall report a Chunk Length error by performing the following tasks, in the order listed:

1 Set the Chunk Length Error bit in the DSC STATUS register(s) (DPCD Address(es) 0020Fh and 02011h, bit 2) to 1.

2 Set the DSC_ERROR_STATUS bit in the DEVICE_SERVICE_IRQ_VECTOR_ESI1 register (DPCD Address 02004h, bit 4) to 1.

3 Generate an IRQ_HPD.

The Sink device shall then report the following errors by setting their respective DSC STATUS register bits to 1:

- **RC Buffer Under-run error(s)** – RC Buffer Under-run bit (bit 0)
- **RC Overflow error(s)** – RC Buffer Overflow bit (bit 1)

The DP DSC Sink device shall then set the DSC_ERROR_STATUS bit to 1, and then generate an IRQ_HPD on the RC buffer under-run or overflow error(s), respectively. The Source device handles the error(s) in an implementation-specific manner.

If a DP Branch device receives a DSC error status notification by way of an IRQ_HPD (as described above), while passing through a DSC bitstream to its downstream DP DSC Sink, the DSC error status notification method used depends on whether the DP Branch device's UP_REQ_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 1) is set to 1:

- When the UP_REQ_EN bit is set to 1, the DP Branch device issues a SINK_EVENT_NOTIFY AUX message transaction with its Event_Identifier bit(s) that correspond to the DSC error set to 1
- When the UP_REQ_EN bit is cleared to 0, the DP Branch device sets the same DSC Status bits as the downstream DP DSC Sink, sets the DSC_ERROR_STATUS bit to 1, and then generates an IRQ_HPD

The DSC algorithm shall restrict artifacts resulting from errors in the received bitstream to the slices in which the errors occurred. Standard DP compressed stream transport services shall **not** provide additional error resiliency features beyond the FEC needed to mitigate the potential impact of bit-error-induced artifacts. Care should be taken during DP system design to account for this.

2.8.5 CRCs for DSC

New to *DP v1.4a*.

For validation/compliance certification of DSC compression and decompression engines, cyclic redundancy checks (CRCs) are used to verify the correctness of the compressed data stream and the reconstructed image.

The CRC calculation is performed on the entire display frame. A 16-bit CRC is generated for each of the three CRC engines. (See Section 2.8.5.2.) The CRC is based on the following polynomial:

$$f(x) = x^{16} + x^{15} + x^2 + 1$$

2.8.5.1 Source-side Compressor

DP devices that have a DSC compressor should generate a set of CRCs for individual display frames, using the compressed data stream that is transmitted over the link, as illustrated in Figure 2-122.

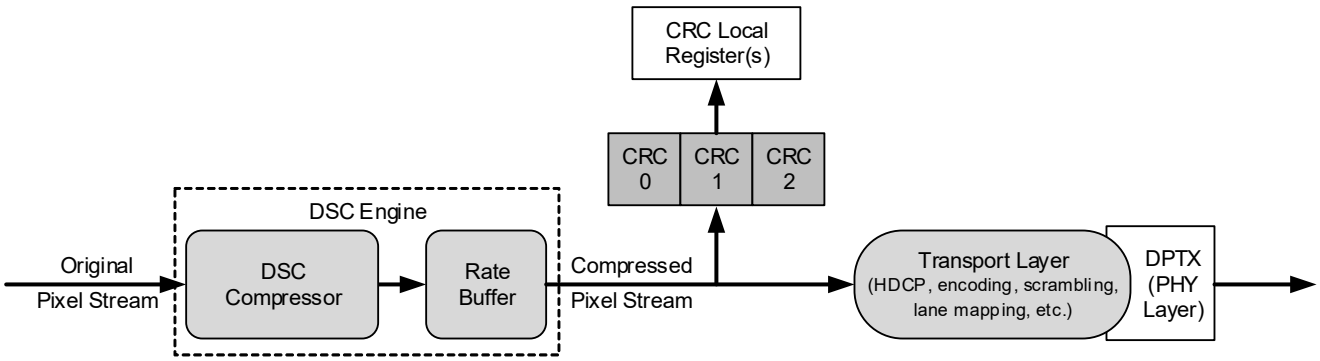


Figure 2-122: Source-side CRC Component Locations for the Compressed Data Stream

For DP Source devices that support CRC generation:

- CRCs shall be generated only on the data directly output from the compressor, before the compressed data stream enters the Transport Layer
- CRCs shall **not** include any transport-added dummy symbols for lane fitting or other transport modifications
- CRC calculations for each new display frame shall start with Byte 0 of the compressed data stream going to CRC Engine 0
- Calculated CRC values on the Source side should be stored in local registers that Source-side software drivers can access

2.8.5.2 Mapping the Compressed Data Stream to CRC Engines

The compressed data stream is spread over three 16-bit CRC engines to create three CRCs. Figure 2-123 illustrates the mapping of the compressed data stream bytes to the CRC engines for a compressed data stream comprised of *n* compressed data bytes.

CRC Engine 0		CRC Engine 1		CRC Engine 2	
[7:0]	[15:8]	[7:0]	[15:8]	[7:0]	[15:8]
Compressed Data Byte 0	Compressed Data Byte 3	Compressed Data Byte 1	Compressed Data Byte 4	Compressed Data Byte 2	Compressed Data Byte 5
Compressed Data Byte 6	Compressed Data Byte 9	Compressed Data Byte 7	Compressed Data Byte 10	Compressed Data Byte 8	Compressed Data Byte 11
⋮	⋮	⋮	⋮	⋮	⋮
Compressed Data Byte *n* – 6	Compressed Data Byte *n* – 3	Compressed Data Byte *n* – 5	Compressed Data Byte *n* – 2	Compressed Data Byte *n* – 4	Compressed Data Byte *n* – 1
n is the total compressed data bytes within the update region					

Figure 2-123: Mapping of Compressed Data Bytes to CRC Engines

For every six bytes of the compressed data stream:

- Bytes 3 and 0 will be the MSB and LSB, respectively, for CRC Engine 0 (CRC 0)
- Bytes 4 and 1 will be the MSB and LSB, respectively, for CRC Engine 1 (CRC 1)
- Bytes 5 and 2 will be the MSB and LSB, respectively, for CRC Engine 2 (CRC 2)

The last byte of the data stream may end up being mapped to CRC Engine 0, 1, or 2. At the end of the data stream, CRC engines that have only one byte (in the LSB) must pad the MSB with 0s to generate the CRC value. Padding is **not** needed in the other CRC engines. Each CRC engine may have a different number of bytes in its final CRC calculation.

2.8.5.3 Sink-side Decompressor

The Sink-side decompressor shall have two sets of CRC engines:

- First set calculates the CRC values for the compressed pixel stream coming into the DSC engine
- Second set calculates the CRC on the reconstructed pixel stream

The incoming compressed pixel stream is mapped into the three CRC engines in the same manner as the Source-side compressed pixel stream is mapped, as described in Section 2.8.5.2 and illustrated in Figure 2-123. The resulting values shall exactly match those calculated for the Source-side compressed pixel stream.

As each display frame completes, the DP Sink device writes the CRC engine's compressed pixel stream results to the DSC_CRC_*x* registers (DPCD Addresses 00262h through 00267h).

The reconstructed pixel stream shall map into a separate set of three CRC engines, one engine per color component (these are the same CRC engines that are used for test automation):

- R_Cr component maps to CRC Engine 0 (CRC 0)
- G_Y component maps to CRC Engine 1 (CRC 1)
- B_Cb component maps to CRC Engine 2 (CRC 2)

This CRC calculation is performed only on active pixels. The msb is shifted in first. For any colorimetry format that is less than 16bpc, the lsb is zero-padded.

The DP Sink device copies these reconstructed pixel stream CRC values to the TEST_CRC_R_Cr, TEST_CRC_G_Y, and TEST_CRC_B_Cb registers, respectively (DPCD Addresses 00240h and 00241h, 00242h and 00243h, and 00244h and 00245h, respectively). The TEST_SINK_MISC register (DPCD Address 00246h) is used for control, using the same mechanism as outlined in relevant *CTS* documentation.

Because the TEST_CRC_*x* registers for the CRC circuits and structure are required for DP Sink devices that support DSC decompression, the TEST_CRC_SUPPORTED bit in the TEST_SINK_MISC register (DPCD Address 00246h, bit 5) shall be set to 1.

Figure 2-124 describes the locations of CRC calculations within DP DSC Sink.

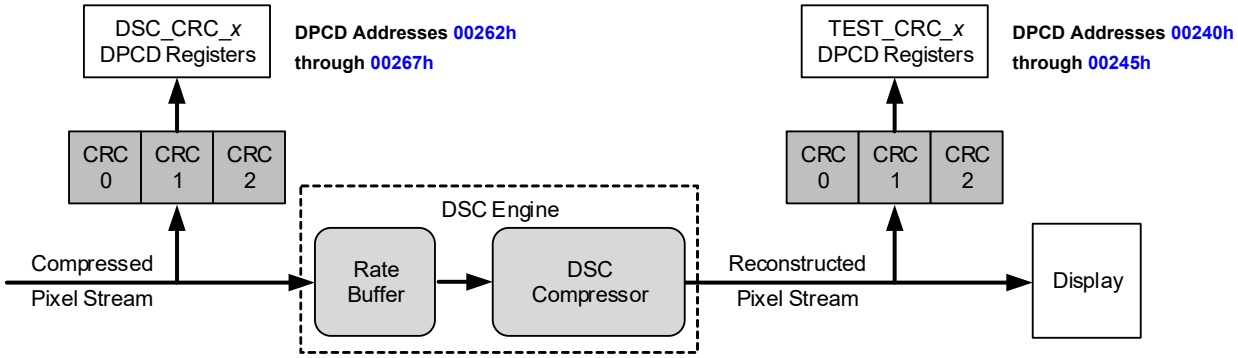


Figure 2-124: CRC Calculation Locations for the Reconstructed Image

2.8.6 DSC Bitstream Transport of 3D Stereo Video

New to *DP v1.4a*.

This section defines the rules for DP DSC bitstream transport of 3D stereo video.

2.8.6.1 Supported 3D Stereo Video Types

Table 2-159 describes the 3D stereo video interface modes that support DSC bitstream transport and the PPS/CRC rules. See Appendix H for details specific to 3D stereo video types over a DP link.

Table 2-159: 3D Stereo Video DP DSC Transport

VSC DB0, bits 3:0 (Stereo Interface Method Code)	DSC Supported?	PPS	CRC Calculation Method
1 (Frame/Field Sequential)	Yes	Same PPS for left- and right-eye view frames	• **Option 0** – CRC calculation starts at the beginning of each view frame and then completes at the end of the view frame[a] • **Option 1** – CRC calculation starts at the beginning of the top view frame, pauses on the ensuing vertical blanking lines, resumes at the beginning of the bottom view frame, and then completes at the end of the bottom view frame[b]
2 (Stacked Frame)	Yes		• **Option 0** – Not allowed when DSC encoding is enabled[a] • **Option 1** – CRC calculation starts at the beginning of the top view frame, pauses on the vertical space region (VSR) lines, resumes at the beginning of the bottom view frame, and then completes at the end of the bottom view frame[b]
3 (Pixel Interleaved)	No	Not applicable	• Not applicable
4 (Side-by-side)	Yes	Combined left- and right-eye view frames have a single PPS	• CRC is calculated for the combined left- and right-eye view frames[c]
5 (Top-to-bottom)	Yes		

a. CRC_3D_OPTION1_SELECT bit in the TEST_SINK register (DPCD Address 00270h, bit 1) is cleared to 0.
b. CRC_3D_OPTION1_SELECT bit is set to 1.
c. CRC_3D_OPTION1_SELECT bit value is "don't care."

2.8.6.2 Vertical Space Region Video Lines for Stacked Frame 3D Stereo Video

A DP DSC Source device shall **not** DSC-encode the 00h pixel data on the VSR video lines. Instead, DP DSC Source device shall insert the appropriate number of 00h symbols on the VSR video lines in micro-packets, replacing stream symbols, but not the symbols listed below:

- BE, BS, and EOC control link symbols
- Stuffing symbols (i.e., FS and FE symbols, as well as the symbols between FS and FE symbols in SST mode, and VCPF symbol sequences in MST mode)
- Dummy symbols

While the VSR video lines are not being DSC-encoded and therefore do not have actual slices, the EOC symbols shall be placed in the same manner as they are placed in the active lines of the left- and right-eye view frames. A way to visualize this placement is to say that the VSR active line (from BE to BS symbols) has the same number of virtual slices of the same width as in the left- and right-eye view frames. The EOC markers are placed accordingly on each VSR active line, as illustrated in Figure 2-125.

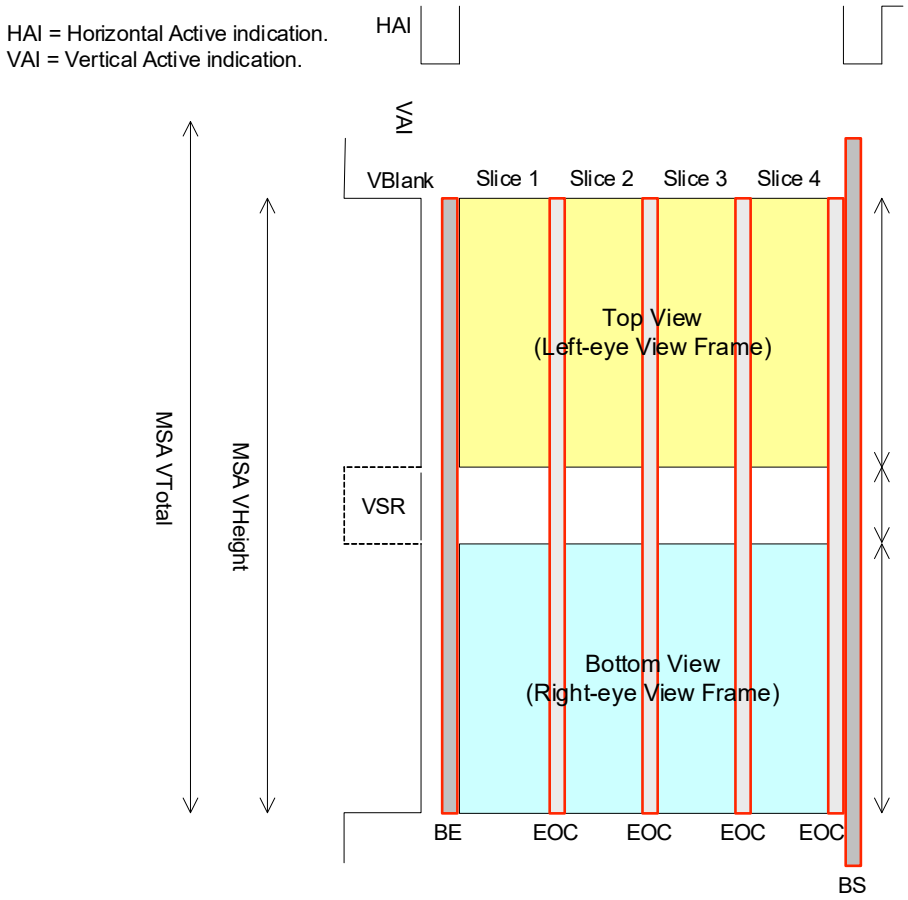


Figure 2-125: EOC Symbols on VSR Lines for 4-slice DSC Example Stacked Frame 3D Stereo Video

2.8.7 DSC Bitstream Mapping to 128b/132b Link Layer Link Symbols

New to *DP v2.0*.

As described in Section 2.7 and Section 3.5.4, 128b/132b Link Layer has a 32-bit link symbol size. Figure 2-126 illustrates the DSC bitstream bytes that are mapped to the VC Payload 1 (VCP1) link symbols.

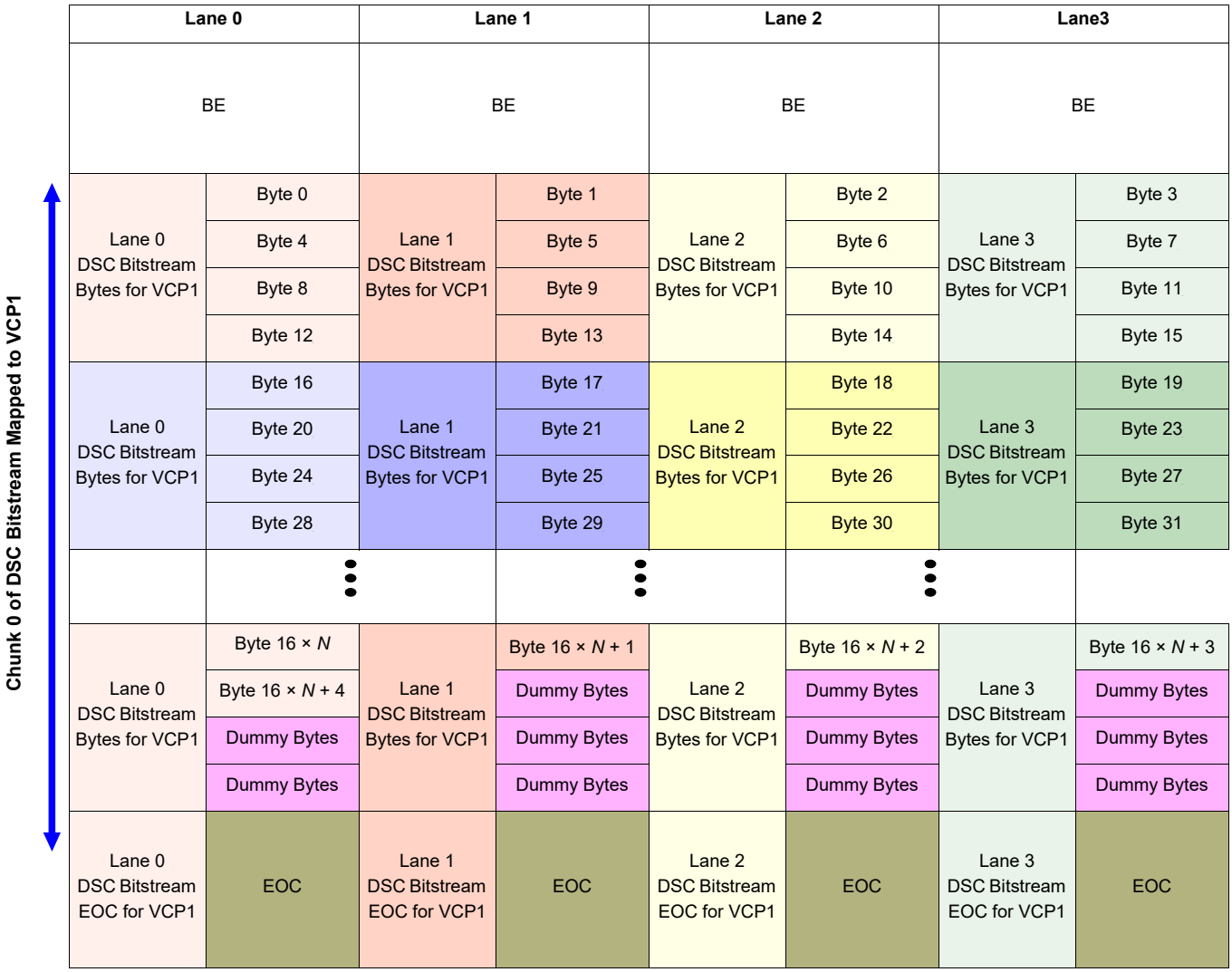


Figure 2-126: DSC Bitstream Mapping to 128b/132b Link Layer Link Symbols

2.8.8 DSC Bitstream Pass-through across a DP Branch Device

New to *DP v2.0*.

A DP DSC Source device may enable DSC bitstream pass-through of a DP Branch device, and have a stream sink device plugged to one of the DP Branch device's DFPs perform DSC decoding, when both of the following conditions exist:

- DP Branch device is DSC bitstream pass-through-capable when the DSC Pass-through Support bit in the DSC SUPPORT registers (DPCD Addresses 00060h and 02260h, bit 1) is set to 1
- Stream Sink device is DSC decoding-capable, as indicated by the DSC Support bit (bit 0) in the DSC SUPPORT registers, –or– by way of DisplayID or legacy EDID

For DSC bitstream pass-through, a DP DSC Source device shall configure the DSC bitstream based on the stream sink device's DSC decoder's decoding capability. A DP DSC Source device and DP Branch device shall both enable FEC on their DFP Main-Links before starting DSC bitstream transmission and pass-through.

Figure 2-127 illustrates the DSC bitstream pass-through enable sequence.

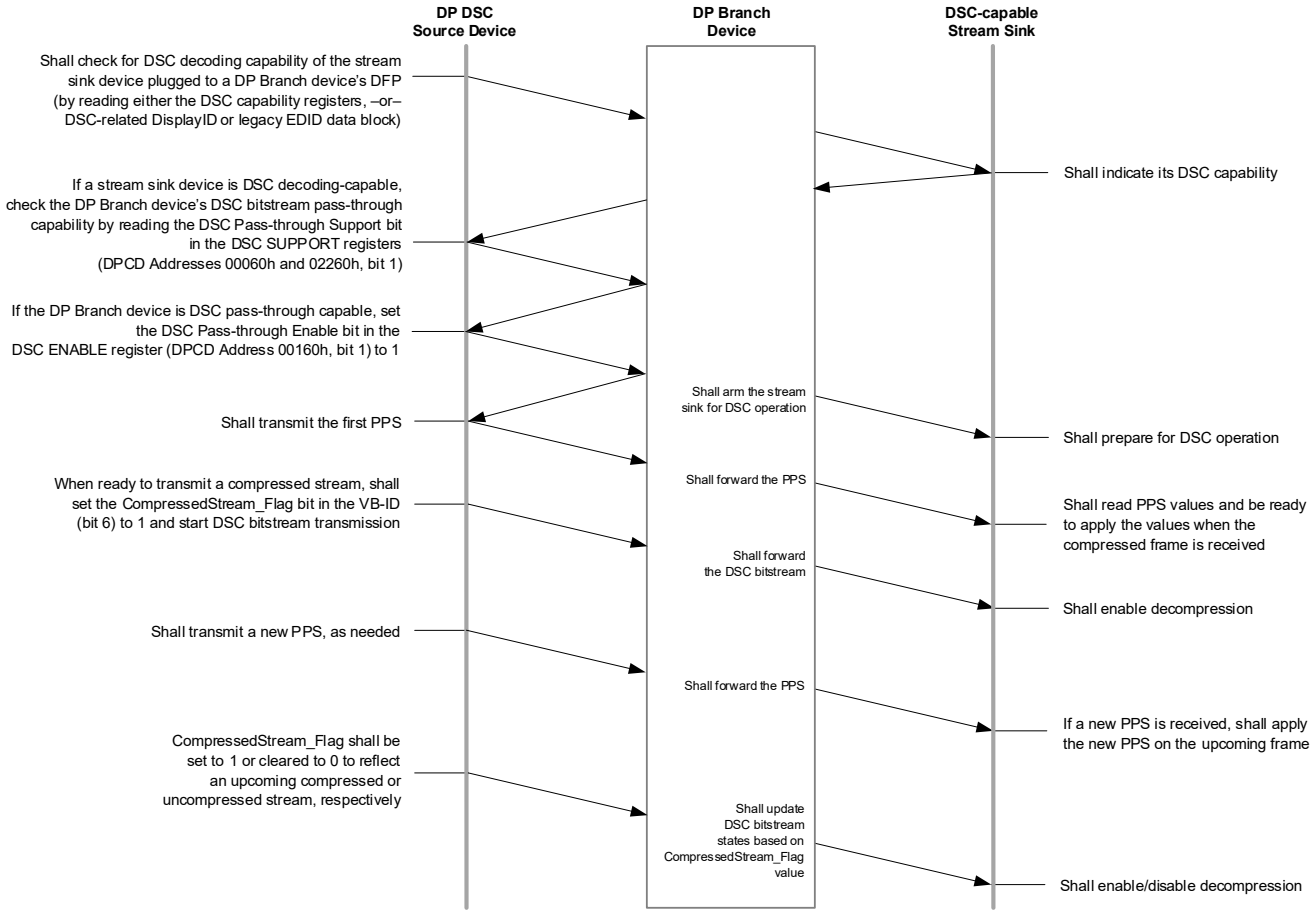


Figure 2-127: DSC Bitstream Pass-through Enable Sequence

2.9 DSC Support Mandate for 128b/132b Link Layer-capable DP Devices

New to *DP v2.0*.

All DP Source, Sink, and Branch devices that support 128b/132b Link Layer shall also support DSC bitstream transport, at all link rates both with 8b/10b Link Layer and 128b/132b Link Layer, with the exemptions listed in Table 2-160. The remainder of this section defines the mandates for 128b/132b Link Layer-capable DP Source, Sink, and Branch devices.

Table 2-160: DSC Support Mandate for 128b/132b Link Layer-capable DP Device Exemptions

DP Device Type	Exemption
All DP devices with 128b/132b Link Layer capability	DSC shall be disabled if the target usage has a safety regulation that prohibits any form of display stream compression. ***Note:*** *Whether DSC is disabled as a run-time option by way of software, –or– at a hardware level (e.g., by blowing a fuse), is usage- and/or implementation-specific and beyond the scope of this Standard.*
Single-stream-only DP Source device **(for which DSC is optional)**	DSC encoder is **not** needed if the single-stream-only DP Source device is limited to the following display stream data bandwidths: • **4- and 2-lane 128b/132b-capable DFP** – 19.29Gbps (i.e., 803.9MP/s at 24-bpp pixel stream) • **1-lane 128b/132b-capable DFP** – 9.65Gbps (i.e., 402.0MP/s at 24-bpp pixel stream)
Single-stream-only DP Sink device **(for which DSC is optional)**	DSC decoder is **not** needed if the single-stream-only DP Sink device is limited to the following display stream data bandwidths: • **4- and 2-lane 128b/132b-capable UFP** – 19.29Gbps (i.e., 803.9MP/s at 24-bpp pixel stream) • **1-lane 128b/132b-capable UFP** – 9.65Gbps (i.e., 402.0MP/s at 24-bpp pixel stream)
DP Branch device **(for which DSC is optional)**	DSC decoder is **not** needed if the DP Branch device has only a single DFP, –or– two DFPs with one of the two being a VGA DFP.

2.9.1 DSC Support Mandates for a DP Source Device with a 128b/132b Link Layer-capable DFP

A DP Source device with a 128b/132b Link Layer-capable DFP shall support the mandates listed in Table 2-161.

Table 2-161: DSC Support Mandates for a DP Source Device with a 128b/132b Link Layer-capable DFP

Parameter	Value
Maximum Display Stream Pixel Rate and Horizontal Active Pixel Count	• DSC encoding, unless the exemption rules defined in Table 2-160 apply • Link configuration with sufficient link data bandwidth for supporting the DSC bitstream for each of these parameters, unless the exemption rules defined in Table 2-160 apply
DSC Encoding Resources	• DP Source device with a multi-stream-capable and 128b/132b Link Layer-capable DFP shall have sufficient DSC encoding resources so that each display stream is at least 3840x2160 progressive 60frames/sec (594MP/s)
Minimum Colorimetry Format	• RGB
Minimum Pixel Component Bit Depth	• 8bpc

2.9.2 DSC Support Mandates for a DP Sink Device with a 128b/132b Link Layer-capable UFP

A DP Sink device with a 128b/132b Link Layer-capable UFP shall support the mandates listed in Table 2-162.

Table 2-162: DSC Support Mandates for a DP Sink Device with a 128b/132b Link Layer-capable UFP

Parameter	Value
Maximum Display Stream Pixel Rate and Horizontal Active Pixel Count	• DSC decoding, unless the exemption rules defined in Table 2-160 apply • Link configuration with sufficient link data bandwidth for supporting the DSC bitstream for each of these parameters, unless the exemption rules defined in Table 2-160 apply
Minimum Colorimetry Format	• RGB
Minimum Pixel Component Bit Depth	• 8bpc
Minimum DSC Bitstream Bit Depth	• 8 to 18bpp, inclusive, in increments of 1bpp
Dynamic PPS update – Compressed-to-Compressed	• Compressed frame-to-compressed frame update of DSC bitstream target bits/pixel, as indicated by the PPS SDP, without a visual glitch • Shall set the Dynamic PPS Update Support – Compressed-to-Compressed bit in the DSC SUPPORT and DSC SUPPORT AND DSC DECODER COUNT register(s) (DPCD Address(es) 00060h and DPCD Address 02260h, respectively, bit 2) to 1
Dynamic PPS update – Uncompressed-to/from-Compressed	• Uncompressed frame-to/from-compressed frame update of DSC bitstream target bits/pixel, as indicated by the PPS SDP, without a visual glitch, is **optional** • DP Sink device that supports the Uncompressed frame-to/from-Compressed frame update of a DSC bitstream shall set the Dynamic PPS Update Support – Uncompressed-to/from-Compressed bit in the DSC SUPPORT and DSC SUPPORT AND DSC DECODER COUNT register(s) (DPCD Address(es) 00060h and DPCD Address 02260h, respectively, bit 3) to 1

2.9.3 DSC Support Mandates for a DP Branch Device with a 128b/132b Link Layer-capable UFP

A DP Branch device with a 128b/132b Link Layer-capable UFP shall support the mandates listed in Table 2-163. Additionally, DSC decoder aggregation (see Section 2.9.3.3) is an **optional** feature for DP Branch devices, regardless of whether the device has a 128b/132b Link Layer-capable UFP.

Table 2-163: DSC Support Mandates for a DP Branch Device with a 128b/132b Link Layer-capable UFP

Parameter	Value
Maximum Stream Branch Capability	• DSC decoding, unless the exemption rules defined in Table 2-160 apply
DSC Extended Capability Registers[a]	• Supports the DSC Extended Capability Branch Total DSC Resources registers (DPCD Addresses 02260h through 02273h; see Table 2-193)
DSC Decoder Minimum Colorimetry Format	• RGB
DSC Decoder Minimum Pixel Component Bit Depth	• 8bpc
DSC Decoder Minimum DSC Bitstream Bit Depth	• 8 to 18bpp, inclusive, in increments of 1bpp
DSC Decoding Resources	• Can be mapped to any DFP • Sufficient resources for enabling the required minimum uncompressed display stream output from each of its DFPs (see Table 2-164)
DSC Bitstream Pass-through	• See Section 2.8.8 for details • Shall set the DSC Pass-through Support bit in the DSC SUPPORT and DSC SUPPORT AND DSC DECODER COUNT register(s) (DPCD Address(es) 00060h and DPCD Address 02260h, respectively, bit 1) to 1
Dynamic PPS update – Compressed-to-Compressed	• Compressed frame-to-compressed frame update of DSC bitstream target bits/pixel, as indicated by the PPS SDP, without a visual glitch • Shall set the Dynamic PPS Update Support – Compressed-to-Compressed bit in the DSC SUPPORT and DSC SUPPORT AND DSC DECODER COUNT register(s) (DPCD Address(es) 00060h and DPCD Address 02260h, respectively, bit 2) to 1
Dynamic PPS update – Uncompressed-to/from-Compressed	• Uncompressed frame-to/from-compressed frame update of DSC bitstream target bits/pixel, as indicated by the PPS SDP, without a visual glitch, is **optional** • DP Branch device that supports the Uncompressed frame-to/from-Compressed frame update of a DSC bitstream shall set the Dynamic PPS Update Support – Uncompressed-to/from-Compressed bit in the DSC SUPPORT and DSC SUPPORT AND DSC DECODER COUNT register(s) (DPCD Address(es) 00060h and DPCD Address 02260h, respectively, bit 3) to 1

*a. DSC Extended Capability Branch Total DSC Resources register support is **optional** for a DSC decoding-capable DP Sink device that has an 8b/10b Link Layer-only UFP.*

Table 2-164: DP Branch Device DFP Minimum Uncompressed Display Stream Output Mandate

DFP Type	Minimum Uncompressed Display Stream
DP	3840x2160 progressive 60frames/sec, 24bpp (594MP/s)
HDMI	
VGA	1920x1080 progressive 60frames/sec, 24bpp (148.5MP/s)

2.9.3.1 DP Branch Device Minimum Total DSC Decoding Resources

Table 2-165 defines the total number of DSC decoding resources that a DP Branch device needs to be able to meet the DFP minimum display stream output mandates (defined in Table 2-164) with a 2-lane UHBR10 UFP.

Table 2-165: DP Branch Device DSC Decoding Resources Needed to Meet DFP Minimum Uncompressed Display Stream Output Mandate with 2-lane UHBR10 UFP

# of DFPs	DFP Type(s)	Minimum DSC Decoding Resource
1	1x VGA	None
	1x DP/HDMI	None
2	1x DP/HDMI + 1x VGA	None
	2x DP/HDMI	1x 2-slice decoder
3	2x DP/HDMI + 1x VGA	2x 2-slice decoders
	3x DP/HDMI	3x 2-slice decoders
4	3x DP/HDMI + 1x VGA	3x 2-slice decoders
	4x DP/HDMI	4x 2-slice decoders

2.9.3.2 DP Branch Device Maximum per-DFP DSC Decoding Resources

Each DFP should need no more than a 4-slice decoder, at most. When the downstream link is 8b/10b channel-coded, the maximum pixel rate is 1077MP/s (24bpp over four lanes of HBR3). From Table 2-155, this pixel rate is supported by 4 slices/line. When the pixel rate is higher than 1077MP/s at 24bpp (e.g., 7680x4320 progressive at 60frames/sec), the DFP needs to be placed in DSC bitstream pass-through.

When the downstream link is 128b/132b channel-coded, the DP Sink device shall support DSC decoding resources for all DP Sink device-supported video resolutions, as defined in Section 2.9.2. Therefore, the DFP can be placed in DSC bitstream pass-through, and does **not** need to perform DSC decoding.

2.9.3.3 Optional DSC Decoder Aggregation

As defined in Table 2-165, a DP Branch device's DSC decoder needs to have at least two slices. Per Section 2.9.3.2, the maximum number of per-DP DSC decoder slices that a DP Branch device needs is four.

A DP Branch device may **optionally** support aggregation of two 2-slice DSC decoders to comprise a single 4-slice DSC decoder.

2.9.3.4 Sequence of DSC Bitstream Bit Depth Change that Involves a Time Slot Allocation Change

A DP Source device may change a VC Payload's time slot allocation when the device changes the DSC bitstream bit depth. A bit-depth increase may also increase the allocated time slot count. A bit-depth reduction may allow for the allocated time slot count to also be decreased. A DP Source device that needs to change the time slot allocation of an active DSC bitstream shall follow the sequence outlined in Table 2-166 when the bit depth is increased or decreased.

Table 2-166: Sequence of DSC Bitstream Bit Depth Change that Involves a Time Slot Allocation Change

Bit Depth Change	Sequence
Increase	1 Increase the time slot allocation, with either a Time Slot Allocation AUX transaction –or– ALLOCATE_PAYLOAD message transaction. 2 Transmit updated PPS SDP content to indicate the increased bit depth, followed by the associated DSC bitstream.
Decrease	3 Transmit updated PPS SDP content to indicate the decreased bit depth, followed by the associated DSC bitstream. 4 Decrease the time slot allocation, with either a Time Slot Allocation AUX transaction –or– ALLOCATE_PAYLOAD message transaction.

The time slot allocation change event is completely asynchronous to the PPS SDP content update/DSC bitstream pixel depth change that may either ensue (for cases in which the time slot allocation is increased) or precede (for cases in which the time slot is decreased) the change. A DP Source device may increase or decrease the DSC bitstream pixel bit depth without changing the time slot allocation if the already-allocated time slot allows for the increase or reduction (which is always the case for DSC bitstream pixel bit depth reduction).

2.10 DSC Capability, DSC Extended Capability, DSC Configuration, and DFP Capability Extension DPCD Registers

New to *DP v2.0*.

This section defines use of the *DP v2.0* (and higher) DSC Capability, DSC Extended Capability, DSC CONFIGURATION, and DFP Capability Extension DPCD registers. The following support mandates apply:

- DP Branch device that supports DSC bitstream decoding and pass-through and has a 128b/132b Link Layer-capable UFP shall support the registers listed above to enable the most flexible use of DSC decoding resources that can be configured by a DP Source device
- DP Sink device that supports DSC bitstream decoding and has a 128b/132b Link Layer-capable UFP shall support the new *DP v2.0* (and higher) DSC Capability and DSC Extended Capability DPCD registers

As defined in Section 2.6.1.1, a DP multi-stream Branch device shall enumerate DFP capabilities of DSC bitstream decoding, DSC pass-through, and pixel processing by enumerating a virtual DP Peer Branch device with virtual DPCD registers when a single-stream DPRX is plugged to the DFP. (See Figure 2-128, top.) The DP multi-stream Branch device shall **not** enumerate a virtual DP Peer Branch device with virtual DPCD registers on those DFPs that do not have a downstream device plugged or multiple-stream DPRX plugged. (See Figure 2-128, bottom.)

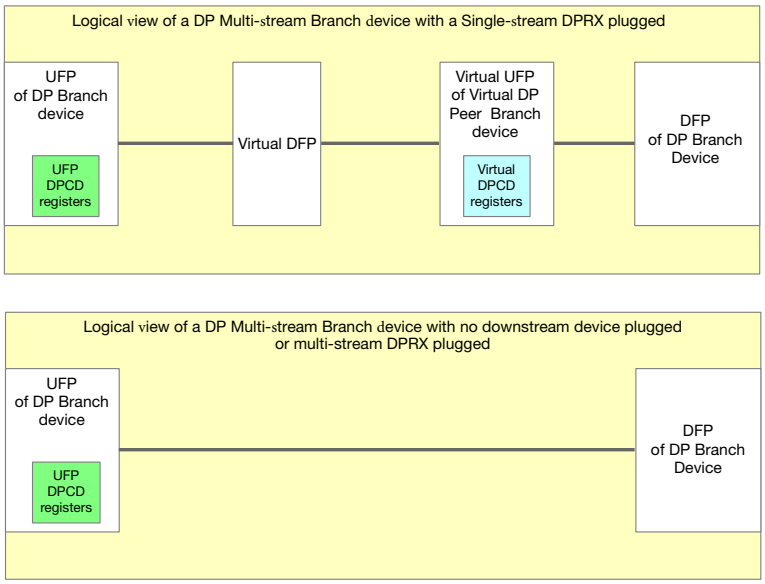


Figure 2-128: Logical Views of a DP Multi-stream Branch Device with (top) and without (bottom) a Single-stream DPRX Plugged to DFP

The *DP v2.0* (and higher) DSC Capability and DSC Extended Capability DPCD registers are available only in the UFP DPCD registers. The DSC CONFIGURATION register is available only in the virtual DPCD registers. (Both are described in further detail in the sections that follow.) A DP Branch device shall reply with an AUX_ACK and all 0s when a DP Source reads from the *DP v2.0* (and higher) DSC Capability and DSC Extended Capability DPCD registers of the virtual DPCD registers. The DP Branch device shall reply with an AUX_NAK when the DP Source device writes to the DSC CONFIGURATION register of the UFP DPCD registers.

A DP Branch device shall place the common GUID_2 register (DPCD Addresses 00040h through 0004Fh) values in the virtual DPCD registers to enumerate the physical enclosure boundary.

Note: *Typically, a DP multi-stream Branch device has multiple DFPs. However, it is also possible for a DP multi-stream Branch device to have only a single DFP that is configured for forwarding multiple streams –or– outputting a single stream.*

The method of using DSC Capability registers of virtual DPCD registers is sufficient for enumerating a DP Branch device whose DSC decoding resources are hard-wire-mapped to DFPs. However, the method is insufficient for enumerating the DSC decoding capability of a DP Branch device that has DSC decoding resources that can be mapped to DFPs (either with or without aggregation) as instructed by a DP Source device.

2.10.1 DSC Capability and DSC Extended Capability DPCD Registers

The *DP v2.0* (and higher) DSC Capability and DSC Extended Capability DPCD registers include the following two register sets:

- DSC Capability Branch Decoder Overall Throughput and Line Buffer Width DPCD Registers
- DSC Extended Capability Branch Total DSC Resources DPCD Registers

Both are defined in the sections that follow.

2.10.1.1 DSC Capability Branch Decoder Overall Throughput and Line Buffer Width DPCD Registers

The DSC Capability Branch Decoder Overall Throughput and Line Buffer Width DPCD registers are located at DPCD Addresses 000A0h through 000A2h (see Table 2-183). These registers are valid for a DP Branch device that has a DSC decoder with more than two slices. On a DP multi-stream Branch device, the register values are applicable both to a native 4-slice decoder and to that formed by aggregating two 2-slice decoders. A DP Branch device that has either one to two DSC slices, –or– does **not** have a DSC decoder, shall reply with all 0s when read.

The following mandates apply to two-slice decoders:

- **Overall peak throughput** – 340MP/s per slice
- **Line buffer width** – 2560 pixels per slice

2.10.1.2 DSC Extended Capability Branch Total DSC Resources DPCD Registers

The DSC Extended Capability Branch Total DSC Resources registers are located at DPCD Addresses 02260h through 02273h (see Table 2-193). These registers are available only in a Branch device's UFP. These registers are **not** available in the virtual DPCD registers of a virtual DP peer device that is enumerated within a DP Branch device. A DP Branch device that has virtual DPCD registers shall reply with 0s when a DP Source device issues a read request transaction to those registers by way of a REMOTE_DPCD_READ message transaction.

A DP Sink device shall reply with all 0s when a DP Source device issues an AUX read request transaction to those DPCD registers.

The following mandates apply to the base DSC Capabilities registers located at DPCD Addresses 00060h through 0006Fh:

- DP Sink and Branch device shall mirror the UFP DPCD Address 02260h through 0226Fh values to UFP DPCD Addresses 00060h through 0006Fh (except for DPCD Address 02260h, bits 7:5)
- DP Branch device shall place its pre-defined per-DFP DSC capabilities (i.e., capabilities that are **not** configurable by a DP Source device) in virtual DPCD Addresses 00060h through 0006Fh

2.10.2 DSC CONFIGURATION DPCD Register

The DSC CONFIGURATION register (DPCD Address 00161h) is available only in the virtual DPCD register of a virtual DP peer device. The register provides the ability to individually enable DSC Decoders 0 through 7. Access to the register is enabled only when the DSC Enable bit in the DSC ENABLE register (DPCD Address 00160h, bit 0) is set to 1.

A DP Branch device shall expose a default set of capabilities for each of its DFPs in the virtual DSC Capability DPCD register(s) (DPCD Address(es) 00060h through 0006Fh, and 02260h through 0226Fh). A DP Source device that needs to change the default per-DFP DSC configuration shall write to the DSC CONFIGURATION register prior to enabling DSC decompression on the DFP. This allows the DP Source device to indicate which decoder, or two aggregated decoders, to map to the DFP.

DP Sink and Branch devices shall reply with an AUX_NAK when a DP Source device issues an AUX write request transaction to the DSC CONFIGURATION register.

2.10.3 DFP Capability Extension DPCD Registers

A DP Branch device with a 128b/132b Link Layer-capable UFP shall indicate the detailed uncompressed display stream output capabilities of its DFP(s).

The DFP Capability Extension registers are located at DPCD Addresses 000A3h through 000AFh (see Table 2-183; *DP v2.0* (and higher)). These registers are valid when the DFP CAPABILITY EXTENSION SUPPORTED bit in the DFP CAPABILITY EXTENSION SUPPORT register (DPCD Address 000A3h, bit 0) is set to 1. These registers are applicable for 8b/10b channel-coded DP SST, HDMI, and VGA DFPs. A DP Branch device with a DP DFP that has DFP CAPABILITY EXTENSION SUPPORTED bit cleared to 0 shall support pixel rate, pixel bit depth, pixel encoding format, and horizontal and vertical video timing as long as the display stream bandwidth is within the DP DFP's link data bandwidth. If the DFP is operating in DP MST mode, –or– using 128b/132b channel-coding, the capability constraints within these registers do **not** apply.

When determining which pixel video stream format to transmit, a DP Source device shall take both of the following into account:

- DFP capabilities that a DP Branch device has enumerated in the DFP Capability Extension registers and Detailed Capabilities Info registers (DPCD Addresses 00080h through 0008Fh)
- Stream sink capabilities that are enumerated in DisplayID or legacy EDID

Although **optional**, support for DFP Capability Extension registers for a DP Branch device with an 8b/10b Link Layer-only UFP is recommended.

- DP single-stream-only Branch device shall map the DFP Capability Extension DPCD registers to UFP DPCD registers.
- DP multi-stream Branch device shall map the DFP Capability Extension DPCD registers to virtual DPCD registers for each DFP

2.10.4 DP Branch Device DSC Decoder Configuration Examples

Figure 2-129 illustrates an example topology in which a DP Branch device has three DFPs and three DSC decoders (see Table 2-167 for the associated DSC Extended Capability register configuration).

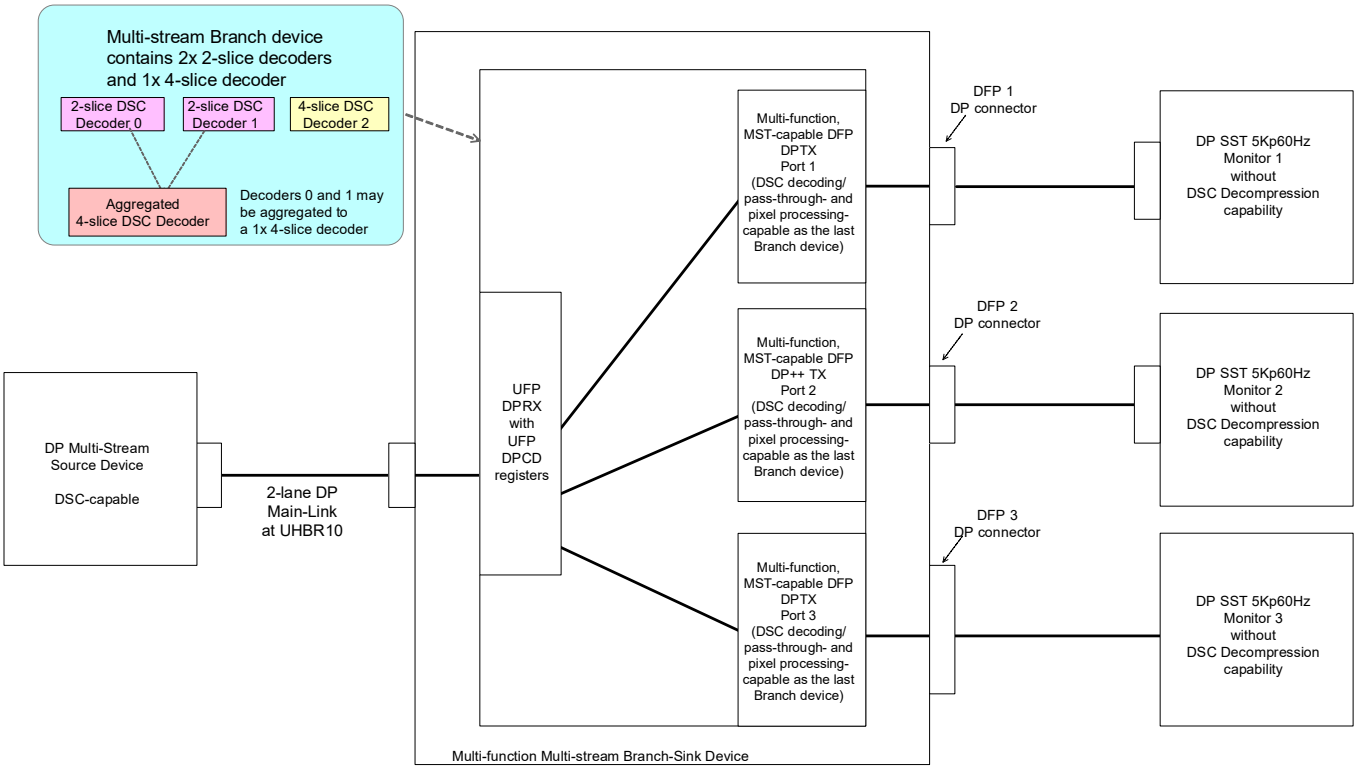


Figure 2-129: DP Multi-stream Branch Device with Three DSC Decoders Configuration Example

Table 2-167: DSC Extended Capability Branch Total DSC Resources DPCD Registers for Figure 2-129 Configuration Example

DPCD Address	Register Bit Values	Comment
02260h[a]	DSC Support = 1 DSC Decoder Count = 010b	DSC support is enabled, three DSC decoders (0, 1, and 2) are available for use.
02270h[b]	DSC Decoder 0 Aggregation Support = 001b DSC Decoder 0 Maximum Slice Count = 0	DSC Decoder 0 is a 2-slice decoder that may be aggregated with DSC Decoder 1.
02270h[c]	DSC Decoder 1 Aggregation Support = 000b DSC Decoder 1 Maximum Slice Count = 0	DSC Decoder 1 is a 2-slice decoder that may be aggregated with DSC Decoder 0.
02271h[d]	DSC Decoder 2 Aggregation Support = 010b DSC Decoder 2 Maximum Slice Count = 1	DSC Decoder 2 is a 4-slice decoder that does **not** support aggregation with the other DSC decoders.

a. *DSC_SUPPORT AND DSC DECODER COUNT register (bits 0 and 7:5, respectively).*
b. *DSC_MAX_SLICE_COUNT_AND_AGGREGATION_0 register (bits 3:1 and 0, respectively).*
c. *DSC_MAX_SLICE_COUNT_AND_AGGREGATION_0 register (DPCD Address 02270h, bits 7:5 and 4, respectively).*
d. *DSC_MAX_SLICE_COUNT_AND_AGGREGATION_1 register (DPCD Address 02271h, bits 3:1 and 0, respectively).*

The DP Branch device in Figure 2-129 enumerates its topology by using virtual DP peer devices, each with its own set of virtual DPCD registers as illustrated in Figure 2-130.

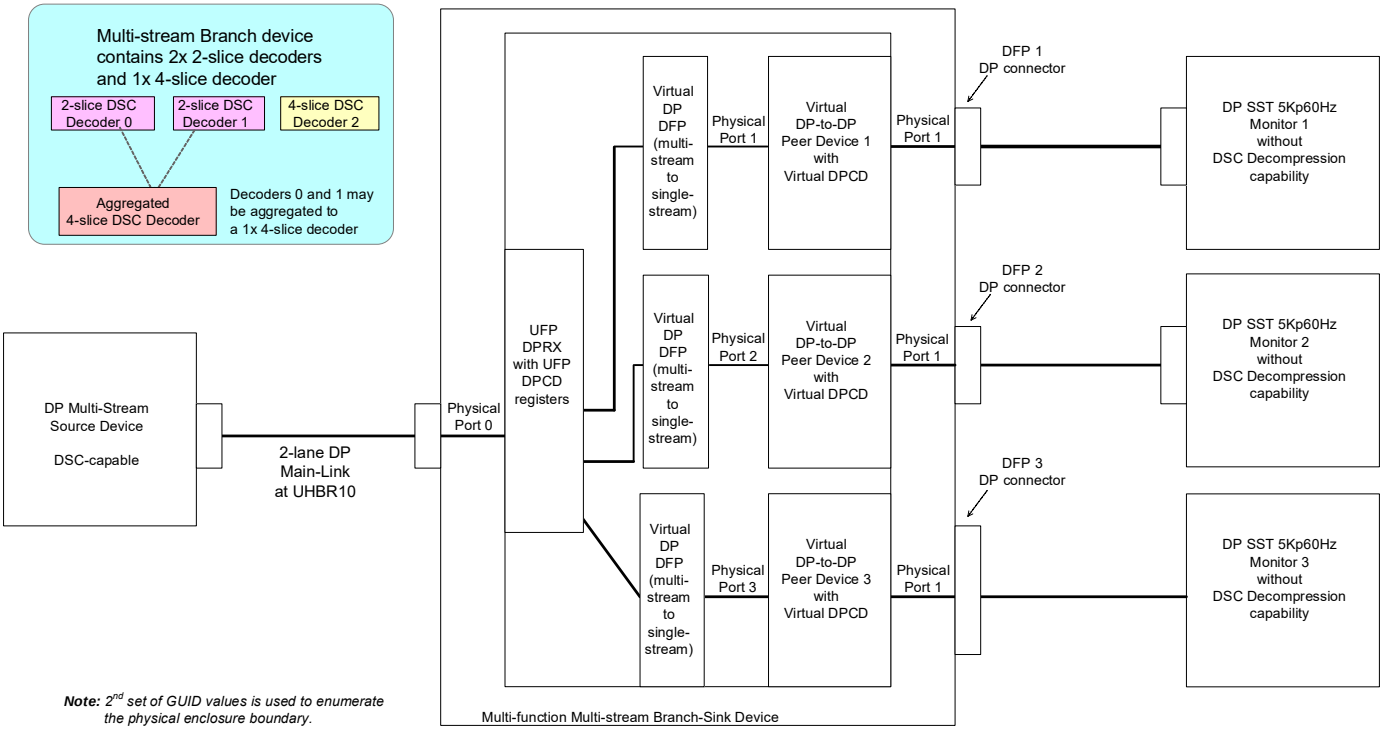


Figure 2-130: DP Multi-stream Branch Device Enumeration with Virtual DP Peer Devices Configuration Example

Figure 2-131 illustrates a topology configuration example in which:

- 4-slice decoder, DSC Decoder 2, is mapped to DFP 1
- 2-slice decoder, DSC Decoder 0, is mapped to DFP 2
- 2-slice decoder, DSC Decoder 1, is mapped to DFP 3

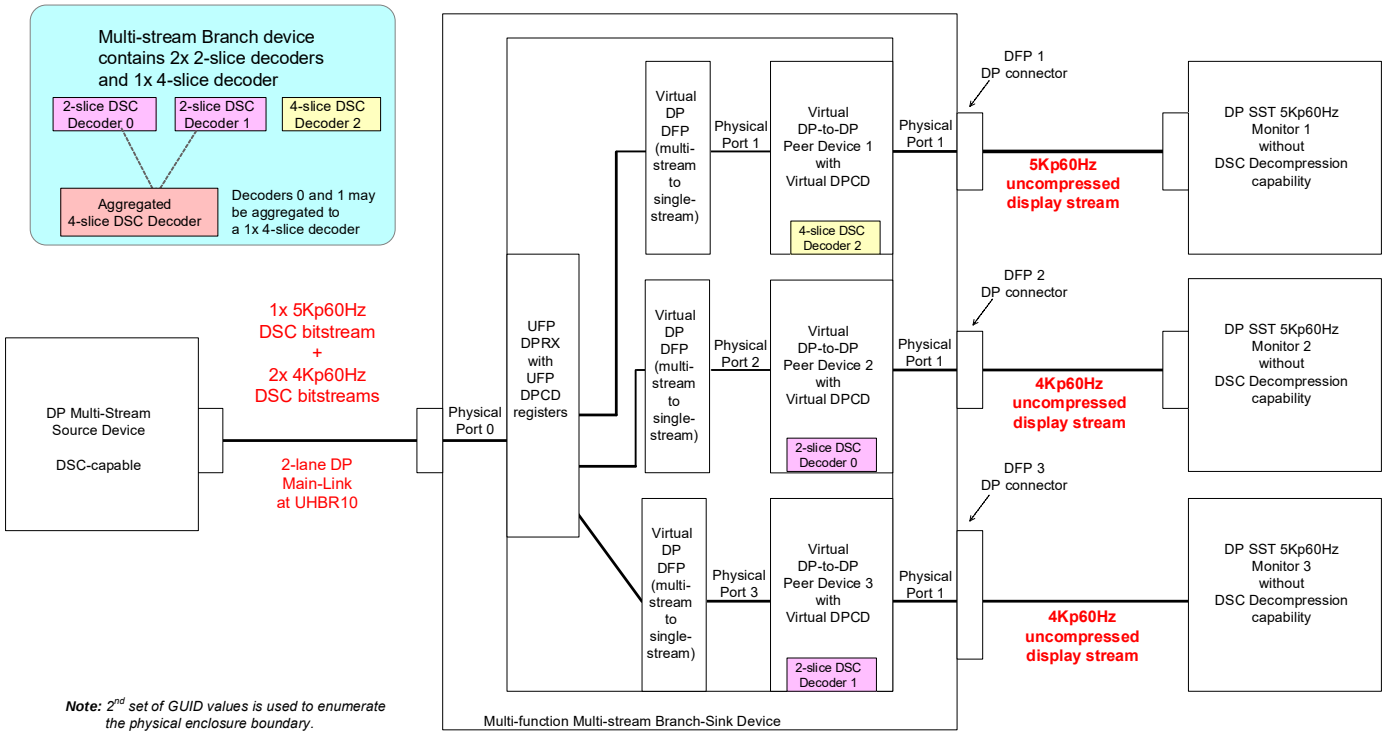


Figure 2-131: DP Multi-stream Branch Device Configuration Example #1

Before transmitting the PPS SDP and DSC bitstream to each DFP, the DP Source device writes to the DSC ENABLE and virtual DSC CONFIGURATION DPCD registers (DPCD Addresses 00160h and 00161h, respectively), as listed in Table 2-168.

Table 2-168: Virtual DSC Extended Capability DPCD Register Settings for Figure 2-131 Configuration Example #1

DFP #	Virtual DPCD Register	Value	Comment
1	DSC ENABLE	01h	Enable DSC decoder.
	DSC CONFIGURATION	04h	Map DSC Decoder 2 to DFP 1.
2	DSC ENABLE	01h	Enable DSC decoder.
	DSC CONFIGURATION	01h	Map DSC Decoder 0 to DFP 2.
3	DSC ENABLE	01h	Enable DSC decoder.
	DSC CONFIGURATION	02h	Map DSC Decoder 1 to DFP 3.

In the configuration example illustrated in Figure 2-132, the UFP link configuration is changed to 4-lane Main-Link at UHBR10, and the display plugged to virtual DP Peer Device 1 is switched to a DSC decoding-capable 8K4K progressive 60frames/sec monitor. The DP Source device performs the following tasks:

- Enables DSC bitstream pass-through on DFP 1
- Aggregates two 2-slice decoders, DSC Decoders 0 and 1
- Maps DSC Decoders 0 and 1 to DFP 2
- Maps one 4-slice decoder, DSC Decoder 2, to DFP 3

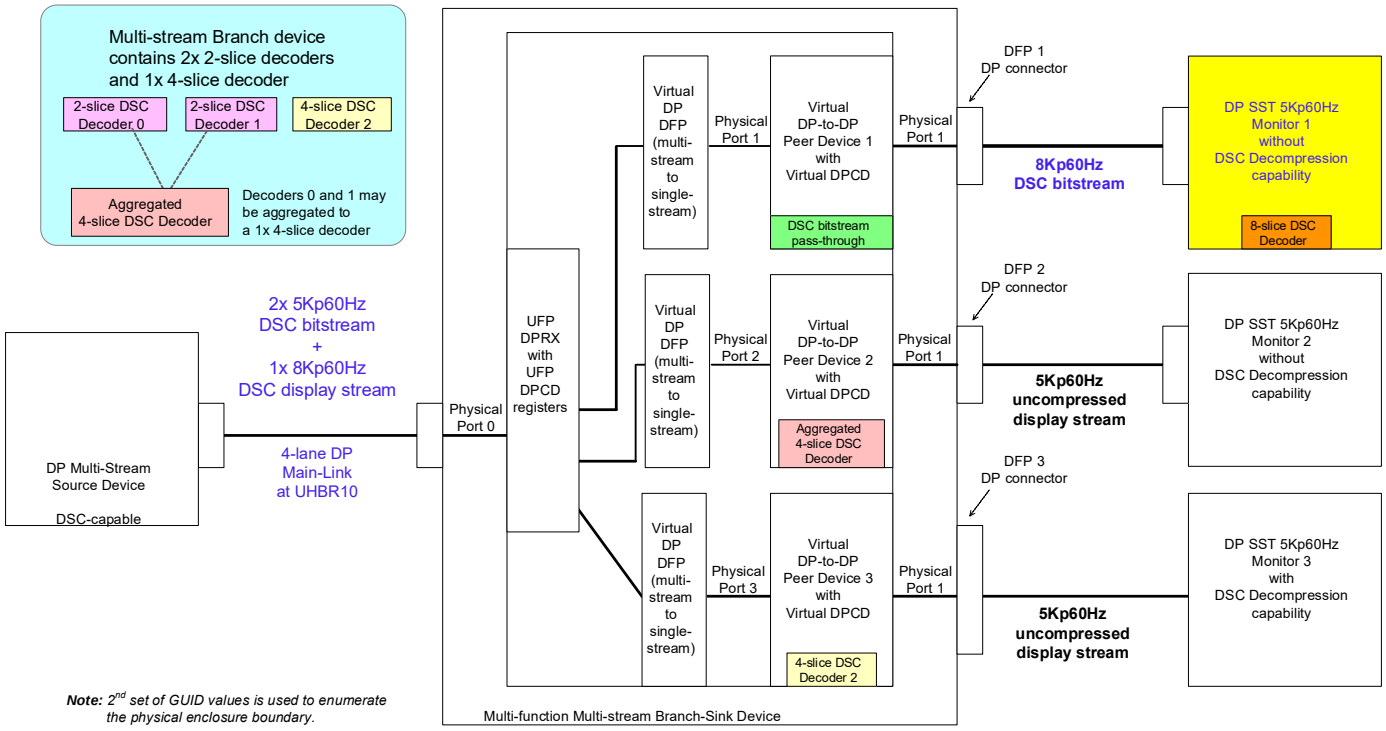


Figure 2-132: DP Multi-stream Branch Device Configuration Example #2

Before transmitting the PPS SDP and DSC bitstream to each DFP, the DP Source device writes to the virtual DSC ENABLE and DSC CONFIGURATION DPCD registers (DPCD Addresses 00160h and 00161h, respectively), as listed in Table 2-169.

Table 2-169: Virtual DSC Extended Capability DPCD Register Settings for Figure 2-132 Configuration Example #2

DFP #	Virtual DPCD Register	Value	Comment
1	DSC ENABLE	02h	Enable DSC bitstream pass-through.
	DSC CONFIGURATION	00h	No DSC decoders are mapped to this DFP.
2	DSC ENABLE	01h	Enable DSC decoder.
	DSC CONFIGURATION	03h	Aggregate DSC Decoders 0 and 1 and map them to DFP 2.
3	DSC ENABLE	01h	Enable DSC decoder.
	DSC CONFIGURATION	04h	Map DSC Decoder 2 to DFP 3.

2.11 AUX Transaction Syntax in Manchester Transaction Format

This section describes the syntaxes that are used for various AUX transactions within Manchester transaction format:

- Native AUX transaction syntax
- Syntax for mapping of an I^2C transaction onto an AUX transaction is referred to as an I^2C-over-AUX transaction

As described in Section 3.4, Manchester transaction format uses Manchester-II coding at the nominal bit rate of 1Mbps.

The AUX_CH PHY Layer consists of a single differential pair carrying self-clocking data. All transactions shall start with a preamble "SYNC" for synchronizing the Requester (DPTX) and the Replier (DPRX), and end with a "STOP" condition.

A 4-bit command, COMM3:0, shall be transmitted after the preamble, followed by a 20-bit address, ADDR19:0. DP capability, status and control functions are directly mapped to the 20-bit address space. In addition, DisplayPort uses these 20 bits to access I^2C devices.

After the transmission of command and address, the data bytes shall be transmitted except for Address-only transaction for I^2C-over-AUX transaction. Burst data transfer is supported. The burst data size shall be limited to a maximum of 16 bytes.

Bit 3 (msb) of the request command field indicates whether the transaction is a Native AUX transaction or an I^2C-over-AUX transaction.

Table 2-170: Bit/Byte Size of Various Data Types of AUX Transaction Syntax

Data Type	Bit Width
Command	4 bits
Address	Request transaction – 20 bits.
	Reply transaction – None (0000b shall be padded to Command, to form a byte).
Data	Request transaction: • For read – 1 byte (Length byte) • For write – 1 byte (Length byte) + *N* Data bytes • Length byte ("LEN") defines the number of bytes to be written to or to be read from the AUX Replier (DPRX) by the AUX Requester (DPTX) • *N* = Integer value from 1 to 16 (i.e., a DPTX shall limit the burst data size to 16 or fewer bytes)
	Reply transaction: • For read = *N* Data bytes • *N* = Integer value from 1 to 16, the number of bytes ready to be transmitted • For write = 0 or 1 Data byte • When AUX Replier NACKs the write request transaction, it shall indicate how many bytes have been written • For an I^2C write over the AUX_CH, the AUX Replier, following the ACK, shall indicate how many bytes have been written to the I^2C slave

Note: *In this Standard, "►" is attached to Requester-driven signals, and "◄" is attached to Replier-driven signals.*

2.11.1 Command Definition

Request and reply command definitions of AUX transactions are described in this section.

2.11.1.1 Request Command Definition

Table 2-171: Request Command Definition, Bit 3

Bit #	Value	Description
3	0	**I^2C-over-AUX Transaction** Functions as an I^2C-over-AUX transaction, and: • Bit 2 = MOT (Middle-of-Transaction) bit • Bits 1:0 = I^2C Command • 00b = Write • 01b = Read • 10b = Write_Status_Update_Request • 11b = RESERVED ***Note:*** *For further details regarding the MOT bit and I^2C Write Status Request, see Section 2.11.5, and Section 2.11.7. See also see Table 2-173, which provides further detail regarding bits 2:0 when bit 3 is cleared to 0.*
	1	**DisplayPort Transaction** Functions as a Native AUX transaction, and: • Bits 2:0 = Request type • 000b = Write • 001b = Read

2.11.1.2 Reply Command Definition

The 4-bit Reply Command field is divided into the Native AUX Reply field (bits 1:0) and I²C-over-AUX Reply field (bits 3:2). The I²C-over-AUX Reply field is valid only when Native AUX Reply field is AUX_ACK (i.e., cleared to 00b). When the Native AUX Reply field is not cleared to 00b, the I²C-over-AUX Reply field shall be cleared to 00b and ignored.

Table 2-172: Reply Command Definition, Bits 3:0

Bit #	Value	Description
1:0	**Native AUX Reply field**	
	00b	**AUX_ACK** For write transactions: • All the data bytes have been written. For read transactions: • Ready to reply to Read request with data following. • A DPRX (Replier) may assert a STOP condition before transmitting the total number of requested data bytes when all the bytes are **not** available.
	01b	**AUX_NACK** For write transactions: • AUX_NACK shall be followed by a data byte "M", where "M" indicates the number of data bytes successfully written. • When a DPTX is writing a DPCD address that is **not** supported by the DPRX, the DPRX shall reply with AUX_NACK and "M" equal to 0. For read transactions: • A DPRX receiving a Native AUX read request for an unsupported DPCD address shall reply with an AUX_ACK and read data equal to 0 instead of replying with AUX_NACK.
	10b	**AUX_DEFER** For write and read transactions: • Not ready for the write/read request. A DPTX may retry later.
	11b	**RESERVED**

Table 2-172: Reply Command Definition, Bits 3:0 (Continued)

Bit #	Value	Description
3:2	**I^2C-over-AUX Reply field** A DPRX shall not forward an I^2C transaction to an I^2C slave unless the AUX_CH has received all the data bytes. When the DPTX fails to receive all the data bytes, the DPTX either AUX NACKs (with "M" set equal to the number of received data bytes) or AUX DEFERs (not ready to receive the request transaction). The DPTX may either abort the I^2C-over-AUX transaction or retry at a later time. I^2C-over-AUX Reply field is only valid when paired with AUX ACK.	
	00b	**I^2C ACK** For I^2C write transactions: • I^2C ACK shall be followed by a data byte "M", where "M" is the number of bytes the DPRX has written to its I^2C slave without NACK. The data byte "M" shall be omitted when all the data bytes have been written. See Section 2.11.5.2 for examples. For I^2C read transactions: • I^2C slave has ACKed the I^2C address and the DPRX is ready to reply with data following. • DPRX may assert a STOP condition before transmitting the total number of requested data bytes when all the bytes are **not** available.
	01b	**I^2C NACK** For I^2C write transactions: • I^2C NACK shall be followed by a data byte "M", except when the I^2C slave has NACKed the I^2C address, in which case the reply transaction shall end with I^2C NACK without the data byte "M". Data byte "M" indicates the number of bytes that the DPRX has successfully written to its I^2C slave before receiving the NACK. The byte on which the NACK occurred is excluded from the number. For I^2C read transactions: • I^2C slave has NACKed the I^2C address.
	10b	**I^2C DEFER** For I^2C write and read transactions: • I^2C slave has yet to ACK or NACK the I^2C transaction.
	11b	**RESERVED**

2.11.2 AUX Transaction Response/Reply Timeouts

Updated in *DP v1.4a*.

The AUX Replier (DPRX) shall start replying to the AUX Requester (DPTX) within the 300us response period. The AUX Response Timeout timer starts ticking after the DPRX has finished receiving the AUX STOP condition, which ends the AUX Request transaction.

The timer is reset when the AUX Response Timeout timer period has elapsed, –or– the DPRX has started to transmit the AUX Sync pattern (which follows 10 to 16 active pre-charge pulses) for the Reply transaction.

If the DPTX does not receive a reply from the DPRX, the DPTX shall wait for an AUX Reply Timeout timer period before initiating the next AUX Request transaction.

When the DP Source device detects a hot plug event or wakes a DP Sink device from a low-power state, the DP Source device shall set its AUX Reply Timeout timer period to 3.2ms or longer. If the DP Source device determines that there are no LT-tunable PHY Repeaters (LTTPRs) present in the link, the DP Source device may reduce its AUX Reply Timeout timer period of 3.2ms minimum, to 400us minimum or longer (see Section 3.6.6.6.1 for LTTPR recognition details).

For all AUX transactions, the AUX Reply Timeout timer starts ticking after the DPTX finishes transmitting the AUX STOP condition.

The timer is reset when the AUX Reply Timeout timer period has elapsed, –or– the DPTX detects the first 0 in Manchester-II code, which is in active pre-charge pulses and AUX Sync pattern of the Reply transaction.

2.11.3 Native AUX Request Transaction Syntax

SYNC► COMM3:0|ADDR19:16► ADDR15:8► ADDR7:0► LEN7:0► (DATA0_7:0► …) STOP

2.11.3.1 Write Request Transactions

For write transactions (COMM3:0 = 1000), the Request transaction shall stop when the number of bytes (1 to 16 = LEN7:0 value + 1, all other values are invalid) has been transmitted from the Requester to the Replier.

2.11.3.2 Read Request Transactions

For read transactions (COMM3:0 = 1001b), the Request transaction shall stop after LEN7:0 (i.e., no data shall be transmitted). The Requester expects the Replier to reply with [LEN7:0 value + 1] bytes (= 1 to 16 bytes) of data.

2.11.4 Native AUX Reply Transaction Syntax

SYNC◄ COMM3:0|0000◄ (DATA0_7:0◄ …) STOP

2.11.4.1 Reply Transaction to Write Request

A reply transaction to a write request shall end in one of the following three conditions:

- The Replier has received a write request, and has completed the write. The Replier shall reply to the transaction by transmitting an AUX ACK.
  - SYNC◄ 00|AUX ACK|0000◄ STOP◄
- The Replier has received a write request, but has not completed the write. The Replier shall end the transaction by transmitting AUX NACK as the first COMM3:0, and then, the number of written bytes M as DATA0_7:0.
  - SYNC◄ 00|NACK|0000◄ DATA0_7:0◄ STOP◄

  Where DATA0_7:0 indicates the number of written bytes, M.
- Replier has received a write request, but is not ready to accept the write request. Replier shall reply with AUX_DEFER.
  - SYNC◄ 00|AUX_DEFER|0000◄ STOP◄

2.11.4.2 Reply Transaction to a Read Request

A reply transaction to a Read request shall end in one of the following four conditions:

- Replier has received a read request, but is not ready to reply with the read data. Shall end the transaction by transmitting AUX DEFER as the first COMM3:0.
  - SYNC◄ 00|AUX DEFER|0000◄ STOP◄
- Replier has received a read request and is ready. Shall reply by transmitting AUX ACK as the first command, transmit back the number of requested bytes, assert the STOP condition, and then release the AUX_CH.
  - SYNC◄ 00|AUX ACK|0000◄ STOP◄
- Replier has received a read request and is ready with some (M + 1 bytes) but not all, of requested data bytes. Shall reply by transmitting AUX ACK as the first command**,** transmit back the number of bytes that can be replied**,** assert the STOP condition, and then release the AUX_CH.
  - SYNC◄ 00|AUX ACK|0000◄ DATA0_7:0◄ …DATAM_7:0◄ STOP◄
- Replier has received a read request for *N* bytes and is ready. Shall reply with AUX ACK as the first command, transmit back the number of requested bytes, assert the STOP condition, and then release the AUX_CH.
  - SYNC◄ 00|AUX ACK|0000◄ DATA0_7:0◄ …DATAN-1_7:0◄ STOP◄

2.11.5 I^2C Bus Transaction Mapping onto AUX Syntax

The mapping of an I^2C transaction onto the I^2C-over-AUX transactions as defined in this Standard is agnostic to the application-specific usage of the I^2C data bytes. Neither the DPTX nor DPRX shall be aware of how each of the data bytes in the I^2C transaction is used for a specific I^2C application.

A single I^2C transaction may be mapped onto one or multiple I^2C-over-AUX transactions to accommodate the bit-rate difference between I^2C and the AUX_CH. How (or whether) to divide an I^2C transaction into multiple I^2C-over-AUX transactions is DPTX-implementation-specific. For an I^2C-over-AUX transaction, a DPTX may initiate an “Address-only” request transaction in which the DPTX STOPs the AUX transaction after transmitting the Request command field and 20-bit Address without transmitting LENGTH byte/data bytes.

2.11.5.1 I²C-over-AUX Request Transaction Command

When bit 3 (msb) of the Request command is cleared to 0 (see Table 2-171), the requested transaction shall be an I²C-over-AUX Transaction. A single I²C transaction may be divided into multiple I²C-over-AUX transactions, each with bit 3 of the Request command cleared to 0.

In an I²C bus transaction, the Request command's remaining three bits, 2:0, are defined as listed in Table 2-173.

Table 2-173: Request Command Definition, Bits 2:0, When Bit 3 = 0

Bit #	Value	Description
1:0	**I²C Command**	
	00b	**Write**
	01b	**Read**
	10b	**Write_Status_Update_Request** When the last I²C write transaction resulted in a reply of either I2C_DEFER or ACK followed by a data byte "M", where "M" is the number of bytes written to the I²C slave, AUX Requester (DPTX) may issue the following special request to inquire the status of the last I²C write: SYNC► COM3:0 (= 0110)|0000► 0000|0000► 0|7-bit I²C address (the same as the last) ► 0000|0000 (Length byte)► STOP► To this request, AUX Replier (DPRX) shall reply with the latest status.
	11b	**RESERVED**
2	1	**MOT (Middle-of-Transaction) bit** This bit shall be set when the I²C transaction does not end (or STOP) with the current AUX transaction. The I²C master in the DPRX shall transmit the 7-bit I²C address and read or write command only when: • This bit is set to 1 for the first time (i.e., in the first AUX transaction for the START of an I²C transaction), –or– • RepeatedStart is issued, which results in either a new I²C address or the same I²C address but with the read/write command opposite of the previous command.

2.11.5.2 I²C Write Transaction

In this section, mapping of an I²C Write transaction to the AUX transaction(s) is described using a method in which three data bytes are written. An I²C master in the Source device shall initiate an I²C Write transaction to an I²C slave in a Sink device by way of the AUX_CH between the DPTX (in the Source device) and DPRX (in the Sink device), as illustrated in Figure 2-133. Two variants of the operation are shown, demonstrating a variety of ways to accomplish the goal of performing an I²C Write transaction.

In the following descriptions, the I²C slave in the Sink device acknowledges the I²C Write. When the I²C slave non-acknowledges the I²C write (either I²C address is not supported or the write data byte is not accepted), what corrective action to take is up to the I²C master in the Source device and beyond the scope of this Standard.

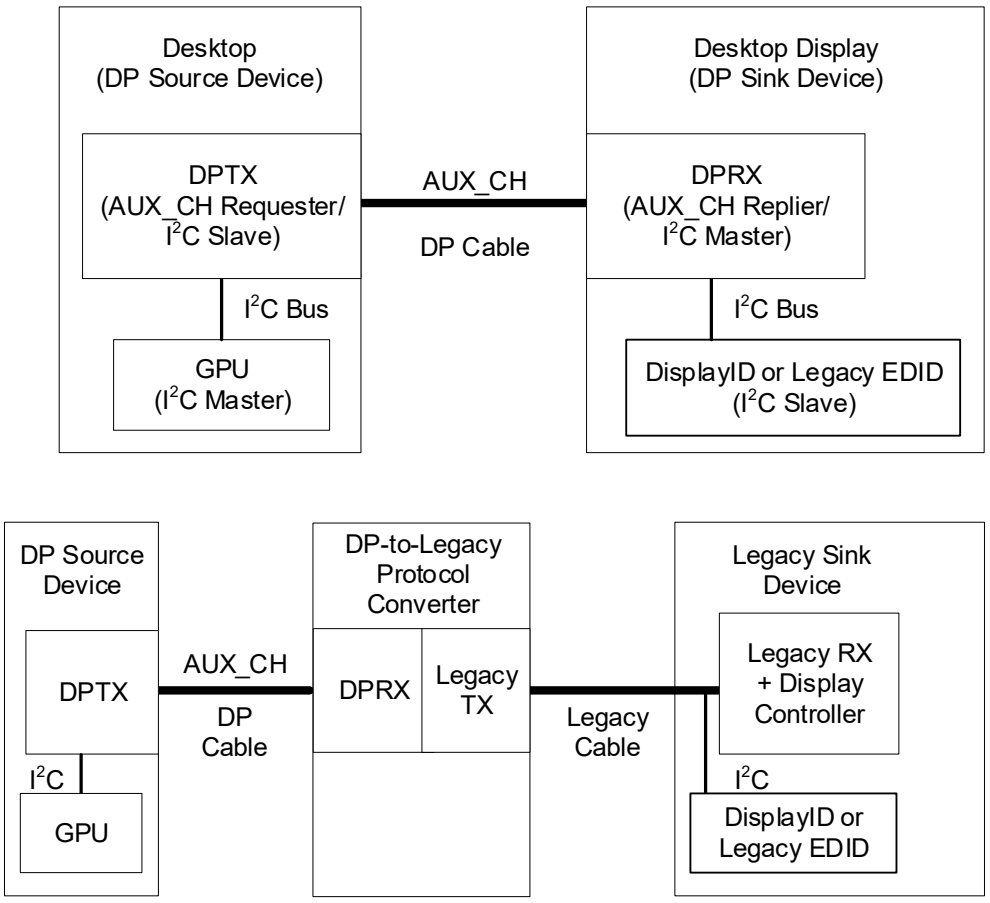


Figure 2-133: Examples of AUX_CH Bridging Two I²C Buses

I²C Write Method 1:

START► 1001000|0► ACK◄ Data0► ACK◄ Data1► ACK◄ Data2► ACK◄ STOP►

- I²C Write Mapping Method 1

  The I²C address byte transfer and each data byte write are mapped into separate AUX transactions. In the method illustrated in Table 2-174, the I²C bus' bit rate in the Sink device is set to 100kHz (= 10us per bit). At this bit rate, the I²C slave in the Sink device can acknowledge each byte within the AUX Response Timeout timer period. (See Section 2.11.2 for details regarding timeout timer period.)

Table 2-174: I²C Write Transaction Method 1

#	I²C Transaction in the Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I²C Transaction in the Sink Device
1	START► 1001000|0► (I²C Write with I²C address = 1001000; I²C clock stretched by DPTX before ACK)			
2		SYNC► 0100|0000► 00000000► 0|1001000► STOP► (Address-only transaction, with MOT = 1 and I²C address = 1001000)		
3			Wait up to 300us	START► 1001000|0► ACK◄
4			SYNC◄ 0000|0000◄ STOP◄ (I²C ACK|AUX ACK)	
5	ACK◄ Data0► (I²C clock stretched by DPTX before ACK to Data0)			
6		SYNC► 0100|0000► 00000000► 0|1001000► 0000|0000► Data0► STOP► (MOT = 1, the same I²C address, Length = 1 byte)		
7			Wait up to 300us	Data0► ACK◄

Table 2-174: I²C Write Transaction Method 1 (Continued)

#	I²C Transaction in the Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I²C Transaction in the Sink Device
8			SYNC◄ 0000|0000◄ STOP◄ (I²C ACK|AUX ACK)	
9	ACK◄ Data1► (I²C clock stretched by DPTX before ACK to Data1)			
10		SYNC► 0100|0000► 00000000► 0|1001000► 0000|0000► Data1► STOP► (MOT = 1, the same I²C address, Length = 1 byte)		
11			Wait up to 300us	Data1► ACK◄
12			SYNC◄ 0000|0000◄ STOP◄ (I²C ACK|AUX ACK)	
13	ACK◄ Data2► (I²C clock stretched by DPTX before ACK to Data2)			
14		SYNC► 0100|0000► 00000000► 0|1001000► 0000|0000► Data2► STOP► (MOT = 1, the same I²C address, Length = 1 byte)		
15			Wait up to 300us	Data2► ACK◄
16			SYNC◄ 0000|0000◄ STOP◄ (I²C ACK|AUX ACK)	
17	ACK◄ STOP►			

Table 2-174: I^2C Write Transaction Method 1 (Continued)

#	I^2C Transaction in the Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I^2C Transaction in the Sink Device
18		SYNC► 0000|0000► 00000000► 0|1001000► STOP► (Address-only transaction with MOT = 0 and the same I^2C address, indicating I^2C STOP to DPRX)		
19			Wait up to 300us	STOP►
20			SYNC◄ 0000|0000◄ STOP◄ (I^2C ACK|AUX ACK)	

- I^2C Write mapping Method 1 with a slower I^2C bus in the Sink device:

  In the version illustrated in Table 2-175, the bit rate of the I^2C bus in the Sink device is set to 25kHz (=40us per bit). At this bit rate, the I^2C slave in the Sink device cannot acknowledge any bytes within the AUX Response Timeout timer period. (See Section 2.11.2 for details regarding timeout timer period.) The DPTX shall issue an I^2C Status Update Request to work with such a slow I^2C bus in the Sink device.

Table 2-175: I^2C Write Transaction Method 1 with a Slow I^2C Bus in the Sink Device

#	I^2C Transaction in the Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I^2C Transaction in the Sink Device
1	START► 1001000|0► (I^2C Write with I^2C address = 1001000; I^2C clock stretched by DPTX before ACK)			
2		SYNC► 0100|0000► 00000000► 0|1001000► STOP► (Address-only transaction, with MOT = 1 and I^2C address = 1001000)		
3			Wait up to 300us	START► 1001000|0► (DPRX does not get ACK to I^2C address before AUX Reply Timeout timer times out)
4			SYNC◄ 1000|0000◄ STOP◄ (I^2C DEFER/AUX ACK)	
5		SYNC► 0110|0000► 00000000► 0|1001000► STOP► (Write_Status_Update_Request with MOT = 1 and the same I^2C address)		
6			Wait up to 300us	ACK◄ (DPRX gets ACK to I^2C address)
7			SYNC◄ 0000|0000◄ STOP◄ (I^2C ACK|AUX ACK)	

Table 2-175: I²C Write Transaction Method 1 with a Slow I²C Bus in the Sink Device (Continued)

#	I²C Transaction in the Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I²C Transaction in the Sink Device
8	ACK◄ Data0► (I²C clock stretched by DPTX before ACK to Data0)			
9		SYNC► 0100|0000► 00000000► 0|1001000► 0000|0000► Data0► STOP► (MOT = 1, the same I²C address, Length = 1 byte)		
10			Wait up to 300us	Data0► (DPRX does not get ACK for Data0 write before AUX Reply Timeout timer times out)
11			SYNC◄ 1000|0000◄ STOP◄ (I²C DEFER/AUX ACK)	
12		SYNC► 0110|0000► 00000000► 0|1001000► STOP► (Write_Status_Update_Request with MOT = 1 and the same I²C address)		
13			Wait up to 300us	ACK◄ (DPRX gets ACK to Data0 write)
14			SYNC◄ 0000|0000◄ STOP◄ (I²C ACK|AUX ACK)	
15	ACK◄ Data1► (I²C clock stretched by DPTX before ACK to Data1)			
16		SYNC► 0100|0000► 00000000► 0|1001000► 0000|0000► Data1► STOP► (MOT = 1, the same I²C address, Length = 1 byte)		

Table 2-175: I²C Write Transaction Method 1 with a Slow I²C Bus in the Sink Device (Continued)

#	I²C Transaction in the Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I²C Transaction in the Sink Device
17			Wait up to 300us	Data1► (DPRX does not get ACK for Data1 write before AUX Reply Timeout timer times out)
18			SYNC◄ 1000|0000◄ STOP◄ (I²C DEFER/AUX ACK)	
19		SYNC► 0110|0000► 00000000► 0|1001000► STOP► (Write_Status_Update_Request with MOT = 1 and the same I²C address)		
20			Wait up to 300us	ACK◄ (DPRX gets ACK to Data1 write)
21			SYNC◄ 0000|0000◄ STOP◄ (I²C ACK|AUX ACK)	
22	ACK◄ Data2► (I²C clock stretched by DPTX before ACK to Data2)			
23		SYNC► 0100|0000► 00000000► 0|1001000► 0000|0000► Data2► STOP► (MOT = 1, the same I²C address, Length = 1 byte)		
24			Wait up to 300us	Data2► (DPRX does not get ACK for Data2 write before AUX Reply Timeout timer times out)
25			SYNC◄ 1000|0000◄ STOP◄ (I²C DEFER/AUX ACK)	

Table 2-175: I^2C Write Transaction Method 1 with a Slow I^2C Bus in the Sink Device (Continued)

#	I^2C Transaction in the Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I^2C Transaction in the Sink Device
26		SYNC► 0110|0000► 00000000► 0|1001000► STOP► (Write_Status_Update_Request with MOT = 1 and the same I^2C address)		
27			Wait up to 300us	ACK◄ (DPRX gets ACK to Data2 write)
28			SYNC◄ 0000|0000◄ STOP◄ (I^2C ACK|AUX ACK)	
29	ACK◄ STOP►			
30		SYNC► 0000|0000► 00000000► 0|1001000► STOP► (Address-only transaction with MOT = 0 and the same I^2C address, indicating I^2C STOP to DPRX)		
31			Wait up to 300us	STOP►
32			SYNC◄ 0000|0000◄ STOP◄ (I^2C ACK|AUX ACK)	

- I^2C Write Mapping Method 2:

  I^2C address byte transfer is mapped into address-only AUX transaction, while the write of multiple data bytes is mapped into a single AUX transaction (as long as the number of bytes is less than or equal to 16 bytes, which is the maximum burst data byte size of AUX transaction).

  As a variation of Method 2, DPTX may combine the entire transaction (I^2C address transfer and data bytes write) into a single AUX transaction.

  Method 2 is faster than Method 1. However, if the I^2C slave in the Sink non-acknowledges the Write Data Byte, the I^2C Master in the Source device shall not know which byte was non-acknowledged.

  In the method illustrated in Table 2-176, four bytes of data (Data0 to Data3) are written. The bit rate of the I^2C bus in a Sink device is set to 100kHz (= 10us per bit). At this bit rate, the I^2C slave in the Sink device can acknowledge up to three bytes within the AUX Response Timeout timer period. (See Section 2.11.2 for details regarding timeout timer period.)

Table 2-176: I^2C Write Transaction Method 2

#	I^2C Transaction in Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I^2C Transaction in Sink Device
1	START► 1001000|0► (I^2C Write with I^2C address = 1001000; I^2C clock stretched by DPTX before ACK)			
2		SYNC► 0100|0000► 00000000► 0|1001000► STOP► (Address-only transaction, with MOT = 1 and I^2C address = 1001000)		
3			Wait up to 300us	START► 1001000|0► ACK◄
4			SYNC◄ 0000|0000◄ STOP◄ (I^2C ACK|AUX ACK)	
5	ACK◄ Data0► ACK◄ Data1► ACK◄ Data2► ACK◄ Data3► ACK◄ STOP►			

Table 2-176: I^2C Write Transaction Method 2 (Continued)

#	I^2C Transaction in Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I^2C Transaction in Sink Device
6		SYNC► 0000|0000► 00000000► 0|1001000► 0000|0011► Data0► Data1► Data2► Data3► STOP► (MOT = 0, the same I^2C address, Length = 4 bytes, indicating I^2C STOP to DPRX after 4 bytes of Write)		
7			Wait up to 300us	Data0► ACK◄ Data1► ACK◄ Data2► ACK◄
8			SYNC◄ 0000|0000◄ 0000|0011◄ STOP◄ (I^2C ACK|AUX ACK, three bytes written to I^2C slave)	Data3► ACK◄ STOP► (DPRX gets ACK to Data3 write while transmitting AUX Reply to DPTX)
9		SYNC► 0010|0000► 00000000► 0|1001000► STOP► (Write_Status_Update_Request with MOT = 0 and the same I^2C address)		
10			SYNC◄ 0000|0000◄ STOP◄ (I^2C ACK|AUX ACK, indicating the Requester (DPTX) of the completion of the 4-byte Write to I^2C Slave in the Sink device)	

2.11.5.3 I²C Read Transaction

In this section, the mapping of an I²C read transaction onto AUX transaction(s) is described using two methods, the first of which 2 bytes are read, and the second in which 10 bytes are read. An I²C master in the Source device shall initiate an I²C read transaction to an I²C slave in the Sink device by way of the AUX_CH between the DPTX (in the Source device) and DPRX (in the Sink device).

In the methods illustrated in this section, the I²C Slave in the Sink device acknowledges the I²C Read. When the I²C slave non-acknowledges the I²C Read (I²C address is **not** supported), what corrective action to take is up to the I²C Master in the Source device and beyond the scope of this Standard.

Method 1: I²C Read of Two Data Bytes

START► 1001000|1► ACK◄ Data0◄ ACK► Data1◄ NACK► STOP►

- I²C Read Mapping Method 1

  In Method 1, the I²C address byte transfer, and each data byte read are mapped into separate AUX transactions. In the method illustrated in Table 2-177, the bit rate of the I²C bus in the Sink device is set to 100kHz (= 10us per bit). At this bit rate, the I²C slave in the Sink device can transmit each byte within the AUX Response Timeout timer period. (See Section 2.11.2 for details regarding timeout timer period.)

Table 2-177: I²C Read Transaction Method 1

#	I²C Transaction in Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I²C Transaction in Sink Device
1	START► 1001000|1► (I²C read with I²C address = 1001000; I²C Clock stretched by DPTX before ACK)			
2		SYNC► 0101|0000► 00000000► 0|1001000► STOP► (Address-only I²C read with MOT = 1 and I²C address = 100100)		
3			Wait up to 300us	START► 1001000|1► ACK◄
4			SYNC◄ 0000|0000◄ STOP◄ (I²C ACK|AUX ACK, I²C address is acknowledged)	

Table 2-177: I^2C Read Transaction Method 1 (Continued)

#	I^2C Transaction in Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I^2C Transaction in Sink Device
5	ACK◄ (I^2C clock stretched by DPTX after ACK)			
6		SYNC► 0101|0000► 00000000► 0|1001000► 0000|0000► STOP► (I^2C read with MOT = 1, the same I^2C address, and Length = 1 byte)		
7			Wait up to 300us	Data0◄
8			SYNC◄ 0000|0000◄ Data0◄ STOP◄ (I^2C ACK|AUX ACK, transmits Data0)	
9	Data0◄ ACK► (I^2C clock stretched by DPTX after ACK)			
10		SYNC► 0101|0000► 00000000► 0|1001000► 0000|0000► STOP► (I^2C read with MOT = 1, the same I^2C address, and Length = 1 byte)		
11				ACK► Data1◄
12			SYNC◄ 0000|0000◄ Data1◄ STOP◄ (I^2C ACK|AUX ACK, transmits Data1)	

Table 2-177: I²C Read Transaction Method 1 (Continued)

#	I²C Transaction in Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I²C Transaction in Sink Device
13	Data1◄ NACK► STOP►			
14		SYNC► 0001|0000► 00000000► 0|1001000► STOP► (Address-only I²C read with MOT = 0 and the same I²C address, indicating the I²C STOP to DPRX)		
15			SYNC◄ 0000|0000◄ STOP◄ (I²C ACK|AUX ACK)	NACK► STOP►

I²C Read Method 2

START► 1001000|1► ACK◄ Data0◄ ACK► Data1◄ ACK► Data2◄ ACK► Data3◄ ACK► Data4◄ ACK► Data5◄ ACK► Data6◄ ACK► Data7◄ ACK► Data8◄ ACK► Data9◄ NACK► STOP►

- I²C Read Mapping Method 2

  In Method 2, DPTX pre-fetches read data from the I²C slave in the Sink device by way of the DPRX to speed up the read operation. As is the previous method, the bit rate of the I²C bus in the Sink device is set to 100kHz (= 10us per bit). At this bit rate, the I²C slave in the Sink device can transmit back up to 3 bytes within the AUX Response Timeout timer period. (See Section 2.11.2 for details regarding timeout timer period.)

Table 2-178: I²C Read Transaction Method 2

#	I²C Transaction in Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I²C Transaction in Sink Device
1	START► 1001000|1► (I²C read with I²C address = 1001000; I²C clock stretched by DPTX before ACK)			
2		SYNC► 0101|0000► 00000000► 0|1001000► 0000|1111► STOP► (I²C read with MOT = 1, I²C address = 100100, and Length = 16 bytes)		
3			Wait up to 300us	START► 1001000|1► ACK◄ (DPRX gets ACK to I²C address and Data0)
4			SYNC◄ 0000|0000◄ STOP◄ (I²C ACK|AUX ACK, I²C address is acknowledged, but no data available yet)	
5	ACK◄ (I²C clock stretched by DPTX after ACK)	SYNC► 0101|0000► 00000000► 0|1001000► 0000|1111► STOP► (I²C read with MOT = 1, the same I²C address, and Length = 16 bytes)		Data0◄ ACK►

Table 2-178: I²C Read Transaction Method 2 (Continued)

#	I²C Transaction in Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I²C Transaction in Sink Device
6			Wait up to 300us	Data1◄ ACK► Data2◄ ACK► Data3◄ ACK►
7			SYNC◄ 0000|0000◄ Data0◄ Data1◄ Data2◄ Data3◄ STOP◄ (I²C ACK|AUX ACK, transmits Data0 to Data3)	
8	Data0◄ ACK►	SYNC► 0101|0000► 00000000► 0|1001000► 0000|1111► STOP► (I²C Read with MOT = 1, the same I²C address, and Length = 16 bytes)		Data4◄ ACK►
9	Data1◄ ACK► Data2◄ ACK►		Wait up to 300us	Data5◄ ACK► Data6◄ ACK► Data7◄ ACK►
10	Data3◄ ACK► (I²C clock stretched by DPTX after the last ACK, as needed)		SYNC◄ 0000|0000◄ Data4◄ Data5◄ Data6◄ Data7◄ STOP◄ (I²C ACK|AUX ACK, transmits Data4 to Data7)	
11	Data4◄ ACK►	SYNC► 0101|0000► 00000000► 0|1001000► 0000|1111► STOP► (I²C Read with MOT = 1, the same I²C address, and Length = 16 bytes)		Data8◄ ACK►
12	Data5◄ ACK► Data6◄ ACK►		Wait up to 300us	Data9◄ ACK► Data10◄ ACK► Data11◄ ACK►
13	Data7◄ ACK► (I²C clock stretched by DPTX after the last ACK, as needed)		SYNC◄ 0000|0000◄ Data8◄ Data9◄ Data10◄ Data11◄ STOP◄ (I²C ACK|AUX ACK, transmits Data8 to Data11)	

Table 2-178: I²C Read Transaction Method 2 (Continued)

#	I²C Transaction in Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I²C Transaction in Sink Device
14	Data8◄ ACK►	SYNC► 0101|0000► 00000000► 0|1001000► 0000|1111► STOP► (I²C Read with MOT = 1, the same I²C address, and Length = 16 bytes)		Data12◄ ACK►
15	Data9◄ NACK► STOP►		Wait up to 300us	Data13◄ ACK► Data14◄ ACK► Data15◄ ACK►
16			SYNC◄ 0000|0000◄ Data12◄ Data13◄ Data14◄ Data15◄ STOP◄ (I²C ACK|AUX ACK, transmits Data12 to Data15)	
17		SYNC► 0001|0000► 00000000► 0|1001000► STOP► (Address-only I²C read with MOT = 0 and the same I²C address, indicating the I²C STOP to DPRX)		Data16◄ ACK►
18			SYNC◄ 0000|0000◄ STOP◄ (I²C ACK|AUX ACK)	Data17◄ NACK► STOP►

It should be noted that the I²C slave does not have a prior knowledge of how many bytes its I²C master wants to read. The I²C slave continues to transmit read data bytes until its master issues an I²C NACK. I²C-over-AUX syntax supports this paradigm. A DPTX which may be an I²C slave to its master (e.g., GPU software driver) shall issue an I²C-over-AUX read request transaction with LEN cleared to 0 (i.e., requesting one byte) and the MOT bit set to 1. When its master NACKs, a DPTX shall transmit an address-only read I²C-over-AUX read request with the MOT bit cleared to 0.

In some implementations, however, a DPTX may have prior knowledge of exactly how many bytes it wants to read by way of I^2C-over-AUX read transaction(s). This may be the case when a GPU with an integrated DPTX is transmitting MCCS commands by way of a DDC/CI transport mechanism; in this scenario, the GPU software driver may *synthesize* an I^2C-over-AUX transaction instead of a DPTX *translating* I^2C into an I^2C-over-AUX transaction.

If the number of bytes to be read is known and is less than or equal to 16, a DPTX may initiate an I^2C-over-AUX read request transaction with LEN set to the number of bytes minus 1 and MOT bit cleared to 0. A DPRX shall issue an I^2C stop condition to its I^2C slave after it has read number of bytes equal to LEN + 1. When the DPRX can read only a number of bytes that is fewer than [LEN + 1], the DPTX may repeat the same request transaction. Even in this condition, the DPRX shall issue an I^2C stop condition to its I^2C slave after it has read the number of bytes equal to LEN + 1.

If the number of bytes to be read is greater than 16, a DPTX may initiate an I^2C-over-AUX read request transaction with LEN set to 15 (= 16 bytes) and MOT bit set to 1. From the next transaction on, the DPTX shall reduce the LEN value to the number of read data bytes a DPRX can transmit out in a single I^2C-over-AUX read reply transaction so that the number of bytes a DPRX reads from its I^2C slave matches that which a DPTX receives from a DPRX. When the remaining number of bytes becomes less than or equal to 16, a DPTX may request the exact number of remaining bytes with the MOT bit cleared to 0.

2.11.5.4 I^2C Write followed by I^2C Read

When the I^2C write is followed by an I^2C Read by way of a Repeated Start condition, as defined in *I^2C Standard*, the MOT bit of the Request Command field shall remain equal to 1 while the transaction switches from I^2C write to I^2C read. Upon detecting this condition, the DPRX shall generate an I^2C Repeated Start condition and switch from I^2C write to I^2C read.

In this section, the mapping of an I^2C write transaction followed by an I^2C Read transaction onto AUX transactions is described using a method in which one data byte is written to set an address offset within a 256-byte I^2C data block and two data bytes are read.

The I^2C Write Mapping Method 1 and the I^2C Read Mapping Method 1 are used in this example. The DPTX may use other methods as described in the previous sections.

In the following description, the I^2C slave in the Sink device acknowledges the I^2C transaction. When the I^2C slave non-acknowledges it, what corrective action to take is up to the I^2C master in the Source device and beyond the scope of this Standard.

Example of an I^2C write followed by an I^2C read:

START► 1001000|0► ACK◄ Data0► ACK◄ REPEATED_START►
1001000|1► ACK◄ Data0'◄ ACK► Data1'◄ NACK► STOP►

Table 2-179: I^2C Write followed by an I^2C Read

#	I^2C Transaction in Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I^2C Transaction in Sink Device
1	START► 1001000|0► (I^2C write with I^2C address = 1001000; I^2C clock stretched by DPTX before ACK)			
2		SYNC► 0100|0000► 00000000► 0|1001000► STOP► (Address-only transaction, with MOT = 1 and I^2C address = 1001000)		
3			Wait up to 300us	START► 1001000|0► ACK◄
4			SYNC◄ 0000|0000◄ STOP◄ (I^2C ACK|AUX ACK)	
5	ACK◄ Data0► (I^2C clock stretched by DPTX before ACK to Data0)			
6		SYNC► 0100|0000► 00000000► 0|1001000► 0000|0000► Data0► STOP► (MOT = 1, the same I^2C address, Length = 1 byte)		
7			Wait up to 300us	Data0► ACK◄
8			SYNC◄ 0000|0000◄ STOP◄ (I^2C ACK|AUX ACK)	
9	ACK◄ REPEATED_START► 1001000|1► (Switches to I^2C read after issuing REPEATED_START condition with the same I^2C address; I^2C clock stretched by DPTX before ACK to I^2C read address)			

Table 2-179: I²C Write followed by an I²C Read (Continued)

#	I²C Transaction in Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I²C Transaction in Sink Device
10		SYNC► 0101|0000► 00000000► 0|1001000► STOP► (Address-only I²C read with MOT = 1 and the same I²C address, indicated I²C REPEATED_START condition to DPRX)		
11			Wait up to 300us	REPEATED_START► 1001000|1► ACK◄
12			SYNC◄ 0000|0000◄ STOP◄ (I²C ACK|AUX ACK, I²C address is acknowledged)	
13	ACK◄ (I²C clock stretched by DPTX after ACK)			
14		SYNC► 0101|0000► 00000000► 0|1001000► 0000|0000► STOP► (I²C read with MOT = 1, the same I²C address, and Length = 1 byte)		
15			Wait up to 300us	Data0'◄
16			SYNC◄ 0000|0000◄ Data0'◄ STOP◄ (I²C ACK|AUX ACK, transmits Data0')	
17	Data0'◄ ACK► (I²C clock stretched by DPTX after ACK)			
18		SYNC► 0101|0000► 00000000► 0|1001000► 0000|0000► STOP► (I²C read with MOT = 1, the same I²C address, and Length = 1 byte)		

Table 2-179: I²C Write followed by an I²C Read (Continued)

#	I²C Transaction in Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I²C Transaction in Sink Device
19				ACK► Data1'◄
20			SYNC◄ 0000|0000◄ Data1'◄ STOP◄ (I²C ACK|AUX ACK, transmits Data1')	
21	Data1'◄ NACK► STOP►			
22		SYNC► 0001|0000► 00000000► 0|1001000► STOP► (Address-only I²C read with MOT = 0 and the same I²C address, indicating the I²C STOP to DPRX)		
23			SYNC◄ 0000|0000◄ STOP◄ (I²C ACK|AUX ACK)	NACK► STOP►

2.11.6 Conversion of I²C Transaction to Native AUX Transaction (Informative)

Conversion of an I²C transaction into a Native AUX transaction by the DPTX is implementation-specific and beyond the scope of this Standard.

When mapping an I²C transaction over the AUX_CH, translation of an I²C-to-AUX transaction by the DPTX and an AUX-to-I²C transaction by the DPRX shall agree with one another. Therefore, the translation mechanism is defined in this Standard.

The conversion of an I²C transaction to a Native AUX transaction by the DPTX is transparent to the DPRX. Regardless of whether it is converted from an I²C transaction, the DPRX shall receive the same Native AUX transaction. It is for this reason that the conversion of an I²C transaction into a Native AUX transaction by the DPTX is beyond the scope of this Standard.

It should be noted that a Sink device is to reply to an I²C-over-AUX request transaction with AUX DEFER when it is not ready to receive an AUX transaction (as is the case with a Native request transaction). When a Source device receives an AUX DEFER reply, the device shall repeat the same request transaction if it wants to retry it.

2.11.7 I²C-over-AUX Transaction Clarifications and Implementation Rules

This section provides clarifications to I²C-over-AUX implementations. The objective is to eliminate interoperability issues that may be caused by varying interpretations of the specification.

A single I²C transaction may be (or is likely to be) divided into multiple I²C-over-AUX transactions. This is because the maximum number of data bytes per I²C-over-AUX transaction is limited to 16 bytes while *I²C Standard* does not prohibit even the infinite number of burst write/read operations.

A Source device may initiate Native AUX transactions in between I²C-over-AUX transactions for a given I²C transaction. However, a Source device shall not interleave I²C-over-AUX transactions for multiple I²C transactions – the Source device shall complete or terminate one I²C transaction before starting I²C-over-AUX transactions for another I²C transaction. It should be noted that each AUX transaction, regardless of whether it is a Native or I²C-over-AUX transaction, consists of a request transaction initiated by a Source device and a reply transaction initiated by a Sink device. Until it has received a reply transaction for the current request transaction, the Source device shall not initiate another request transaction.

I²C transaction syntax is implementation-specific. The syntax specification does not assume any fixed I²C transaction syntax in an attempt to make it applicable to any I²C implementation. The I²C master of a DPRX in a Sink device shall "imitate" the I2C_SCL/I2C_SDA waveforms of those received by the I²C slave of a DPTX in a Source device (with the exception of the timing of I²C clock stretching, as described in Section 2.11.7.1.6.8 and Section 2.11.7.2.6).

A DPTX in a Source device functioning as an I²C slave and AUX Requester may not know how many data bytes its I²C master is intending to write or read in an I²C transaction. Unless it knows the number of data bytes at the beginning of an I²C transaction, the DPTX should generate I²C-over-AUX transactions with the LEN value equal to 0 corresponding to one data byte. This ensures that the DPTX shall not write or read more bytes than intended by its I²C master.

As far as the bit rate is concerned, *I²C Standard* lists certain bit rates (100kbps, 400kbps, and 3.4Mbps) and *E-DDC Standard* (based on I²C as the PHY Layer) notes the bit rate of 100kbps. However, the I²C bit rate is dependent on implementations and "channel" qualities. Over a long-reach VGA cable, for example, it is common for a DDC master to need to reduce the bit rate down to 1kbps to approximately 10kbps. The AUX_CH bit rate, in comparison, shall be within the range of 1Mbps ±20% per Manchester format AUX transaction specification. The I²C-over-AUX specification comprehends this inherent difference (and the variation of the difference) of the bit rates between I²C and the AUX_CH. The extension of DPCD field for Sink device to declare its I²C bit rate capability and for Source device to set the I²C bit rate among those rates supported by the Sink device further adds to the robustness of the I²C-over-AUX specification for bridging the bit rate gap.

2.11.7.1 Clarifications for a Source Device

This section describes the clarifications for a Source device.

2.11.7.1.1 Downstream I^2C Bit Rate Detection/Configuration

The extension to the DPCD field for a DPRX to declare its I^2C bit rate capability and for a DPTX to program the I^2C bit rate among those rates supported by the DPRX should be referenced. Alternatively, a DPTX and DPRX may program the I^2C bit rate in a vendor-specific manner.

At a low bit rate, the I^2C slave interfacing with the I^2C master within the DPRX takes a long time to accept/transmit bytes. At 1kbps, for example, the transport of 1 byte including ACK/NACK takes about 10ms. Therefore, the DPTX shall extend the interval of successive I^2C-over-AUX transactions in case the downstream I^2C bit rate is low.

When an MST Source device is accessing the I^2C slave of a DP device that is connected by way of multiple MST Branch devices, the MST Source device shall determine the I^2C bit rate of the DP device with the I^2C slave and program the desired bit rate by originating REMOTE_I2C_READ and REMOTE_I2C_WRITE message transactions to the last MST Branch device that is driving the DP device. After programming the I^2C bit rate, the MST Source device originates a REMOTE_I2C message transaction to the last MST Branch device that generates the corresponding I^2C-over-AUX transactions.

2.11.7.1.2 Prompting the Termination of I^2C Transaction

An address-only I^2C-over-AUX (either write or read) with the MOT bit cleared to 0 prompts the Sink device to issue an I^2C STOP condition to its I^2C slave at any time, even before the current I^2C transaction is complete.

An address-only I^2C-over-AUX with the MOT bit cleared to 0 shall not be issued when there is no ongoing I^2C-over-AUX transaction. If a Source device needs to initiate an I^2C transaction to a certain I^2C Device Address and then terminate the transaction, the following I^2C-over-AUX transactions shall be used:

- Address-only transaction with the MOT bit set to 1
- Address-only transaction with the MOT bit cleared to 0

2.11.7.1.3 MOT Bit

The MOT bit cleared to 0 prompts the Sink device to issue an I^2C STOP condition to its I^2C slave after completing the current I^2C-over-AUX transaction. As noted above, a Source device may issue an address-only I^2C-over-AUX (either write or read) with the MOT bit cleared to 0 at any time to terminate the current I^2C transaction, even before the current I^2C transaction is complete.

2.11.7.1.4 Prompting Repeated I²C Start Condition

A Source device may issue I²C-over-AUX with the MOT bit set to 1, and then issue another I²C-over-AUX to the same I²C Device Address, but a different command (i.e., write followed by read or read followed by write). This action by the Source device prompts the Sink device to initiate the second I²C transaction following Repeated I²C Start, instead of I²C STOP.

A Source device may also issue I²C-over-AUX with the MOT bit set to 1, then issue another I²C-over-AUX to a different I²C Device Address either with the same command or a different command. This action also prompts the Sink device to initiate the second I²C transaction following Repeated Start condition, instead of I²C STOP condition.

2.11.7.1.5 I²C-write-over-AUX

A Source device may start I²C-write-over-AUX request transaction either with:

- An address-only I²C-write-over-AUX with the MOT bit set to 1, or
- Address + LEN + Data bytes I²C-write-over-AUX with the MOT bit cleared to 0 or set to 1

The remainder of this section describes the permissible I²C-over-AUX transactions following various replies from the Sink device. The Source device may issue a Native AUX transaction in between I²C-over-AUX transactions, even before a given I²C transaction is complete/terminated.

2.11.7.1.5.1 Upon Receiving the Reply of I2C_ACK|AUX_ACK followed by no “M” Value to a Request Transaction with MOT Bit Cleared to 0

The I²C transaction is completed. The Source device may initiate another AUX transaction, whether it is Native AUX transaction or I²C-over-AUX transaction to either the same or different I²C Device Address.

2.11.7.1.5.2 Upon Receiving the Reply of I2C_ACK|AUX_ACK followed by No “M” Value to a Request Transaction with MOT Bit Set to 1

The Source device shall issue one of the following two I²C-over-AUX transactions:

- Proceed with the next I²C-over-AUX transaction either with the same or different I²C Device Address. The transaction may be either an I²C-write-over-AUX or I²C-read-over-AUX.
  - If the ensuing I²C-over-AUX request transaction is either read or to a different I²C Device Address, the I²C master within the DPRX shall issue a REPEATED START condition to its I²C Device Address.
- Issue an address-only I²C-over-AUX with the MOT bit cleared to 0 to prompt an I²C STOP to terminate the current I²C-write-over-AUX transaction.

2.11.7.1.5.3 Upon I2C_DEFER|AUX_ACK Reply, with MOT Bit in Request Transaction Cleared to 0 or Set to 1

The Source device shall do one of the following:

- Issue an I2C_WRITE_STATUS_UPDATE command, –or–
- Issue an address-only I^2C-over-AUX with the MOT bit cleared to 0 to prompt an I2C STOP to terminate the current I^2C-write-over-AUX transaction. See Section 2.11.7.1.5.6 for an example of how to abort an I^2C-over-AUX transfer that has repeated AUX_DEFERs. This is similar to receiving an unexpectedly high number of repeated I2C_DEFER responses.

2.11.7.1.5.4 Upon the Reply of I2C_ACK|AUX_ACK followed by "M" Value to the I^2C-write-over-AUX, to a Request Transaction with MOT Bit Cleared to 0 or Set to 1

The Source device shall do one of the following:

- Issue an I2C_WRITE_STATUS_UPDATE command, –or–
- Issue an address-only I^2C-over-AUX with the MOT bit cleared to 0 to prompt an I^2C STOP to terminate the current I^2C-write-over-AUX transaction.

2.11.7.1.5.5 Upon Receiving I2C_NACK|AUX_ACK Reply followed by Either "M" Value or no "M" Value, to a Request Transaction with MOT Bit Cleared to 0 or Set to 1

After stopping the current I^2C transaction by issuing Address-only I^2C-over-AUX transaction with the MOT bit cleared to 0, the Source device may start another AUX transaction. As one of the possible transactions, it may attempt the I^2C-write-over-AUX transaction to the same I^2C Device Address to ensure that the Sink device consistently I2C_NACKs.

2.11.7.1.5.6 Upon Receiving AUX_DEFER Reply to a Request Transaction with MOT Bit Cleared to 0 or Set to 1

The Source device shall do one of the following:

- Repeat the identical I^2C-write-over-AUX transaction keeping the same LEN value and Data bytes, –or–
- Issue an address-only I^2C-over-AUX with the MOT bit cleared to 0 to prompt an I^2C STOP to terminate the current I^2C-write-over-AUX transaction. See Section 2.11.7.1.5.6.1 for more information. Prior to aborting the transfer, the Source device shall retry the transaction several times before assuming an error condition is present that justifies the abort.

2.11.7.1.5.6.1 Source Retry Attempts following AUX_DEFER Response prior to Aborting Transfer

A DP Source device shall retry at least seven times upon receiving AUX_DEFER before giving up the AUX transaction.

If the DP Source device has a way of knowing the I^2C bit rate capability options of the downstream device and of setting the rate, either through a vendor-specific method or through the I^2C Speed Control Capabilities Bit Map and I^2C Speed Control/Status Bit Map registers (DPCD Addresses 0000Ch and 00109h) for downstream devices with DPCD r1.2 or higher, the DP Source device should adjust the retry interval and/or number of request data bytes based on the I^2C bit rate.

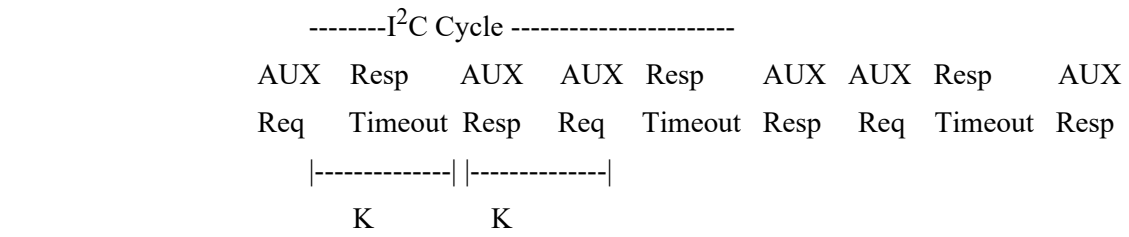
A Source device should take into account the various possible implementations from Sink devices of the I^2C-over-AUX burst write transaction. For example, a Sink device may issue AUX_DEFERs until all data in a write burst has been written to the I^2C Slave. Then it may respond with a single I^2C ACK. At various I^2C Bus Speeds and burst sizes, this results in a wide array of retry limits. For example, Table 2-180 lists the retry limits associated with various I^2C bus speeds and various burst sizes. Assuming a Sink device implementation that issues AUX_DEFERs until all data is written, we come up with a worst case retry limit. **This example is for reference purposes only**; it does **not** take into account many factors that affect overall response time. It does not take into account I^2C Slave clock stretching, DP Source retry interval (assumes that the Source device repeats the request immediately following a DP Sink AUX_DEFER response), or varying DP Sink device response times (assumes that the AUX Response Timeout timer timed out, and is immediately followed by a Sink device's AUX_DEFER response; see Section 2.11.2 for details regarding timeout timer period).

Table 2-180: Burst Write Sizes/Bus Speed Retry Limits

I^2C Bus Speed (kbps)	Burst Write Sizes / Maximum Number of Retries						
	1	2	4	6	8	12	16
1	43	63	102	138	171	232	285
5	8	13	20	27	34	46	57
10	4	6	10	14	17	23	28
100	0	0	1	1	2	2	3
400	0	0	0	0	0	0	1
1000	0	0	0	0	0	0	0

The calculations are based on the following assumptions:

- AUX request cycle consists of an I²C-over-AUX Request + 300us AUX Response Timeout + AUX Response. The AUX Request is 66 AUX_CH Bit times (pre-charge + Sync + Stop + CMD + Add + LEN) + 8 × BurstSize AUX_CH Bit times.
- An example timeline for the transfers is as follows:



- # of retries × K + 300us = I²C Cycle length,
  where K = Response Timeout + AUX Response + AUX Request
- # of retries = (I²C Cycle length – 300us) /
  (Response Timeout + AUX Response + AUX Request)

Note: *See Section 2.11.2 for details regarding Response Timeout.*

If the Source device has no way of knowing the downstream I²C bit rate, the Source device may either retry for the period specified for the worst-case bit rate (in the order of 1kbps) or request one byte to "gauge" the effective downstream I²C bit rate. Such precaution should be used when the downstream device is a DP-to-Legacy protocol converter Branch device, where a long "legacy" cable may force a low I²C bit rate.

The Source device shall properly terminate the pending I²C-over-AUX transaction before starting I²C-over-AUX for another I²C transaction. To abort the transfer (after the recommended number of retries has been attempted), an address-only I²C-over-AUX with the MOT bit cleared to 0 should be issued to prompt an I²C STOP to terminate the current transaction. If the response to this is an AUX_DEFER, the Source device may abort the transaction.

2.11.7.1.5.7 Upon Receiving AUX_NACK Reply followed by Either "M" Value or no "M" Value

The Source device may initiate another AUX transaction. (A Sink device shall not reply with AUX_NACK to I²C-write-over-AUX transaction unless there is a mismatch between the LEN + 1 value and the number of received data bytes.)

2.11.7.1.5.8 No Reply

The Source device may initiate another AUX transaction. (A Sink device shall reply unless the device has detected an illegal command, –or– is in a power-saving state resulting from the Source device writing 02h to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h) by way of a Native AUX transaction.)

2.11.7.1.6 I²C-read-over-AUX

A Source device may start I²C-read-over-AUX request transaction either with:

- An address-only I²C-read-over-AUX with the MOT bit set to 1, or
- An "Address + LEN" I²C-read-over-AUX with the MOT bit cleared to 0 or set to 1

The remainder of this section describes the permissible I²C-over-AUX transactions following various replies from the Sink device. The Source device may issue a Native AUX transaction in between I²C-over-AUX transactions, even before a given I²C transaction is complete/terminated.

2.11.7.1.6.1 Upon Receiving the Reply of I2C_ACK|AUX_ACK followed by the "Total" Number of Data Bytes Equal to LEN + 1, to a Request Transaction with MOT Bit Cleared to 0

The I²C transaction is completed. The Source device may initiate another AUX transaction, whether it is a Native AUX transaction, I²C-over-AUX transaction to either the same or different I²C Device Address.

2.11.7.1.6.2 Upon Receiving the Reply of I2C_ACK|AUX_ACK followed by the "Total" Number of Data Bytes Equal to LEN + 1 to a Request Transaction with MOT Bit Set to 1

The Source device shall issue one of the following two I²C-over-AUX transactions:

- Proceed with the next I²C-over-AUX transaction either with the same or different I²C Device Address. The transaction may be either I²C-write-over-AUX or I²C-read-over-AUX.
  - If the ensuing I²C-over-AUX request transaction is either a write to any address or a read to a different I²C Device Address, the I²C master within the DPRX shall issue a REPEATED START condition to its I²C Device Address.
- Issue an address-only I²C-over-AUX with the MOT bit cleared to 0 to prompt an I²C STOP to terminate the current I²C-read-over-AUX transaction.

2.11.7.1.6.3 Upon I2C_DEFER|AUX_ACK Reply, to a Request Transaction with MOT Bit Cleared to 0 or Set to 1

The Source device shall do one of the following:

- Repeat the identical I²C-read-over-AUX transaction with the same LEN value, –or–
- Issue an address-only I²C-over-AUX with the MOT bit cleared to 0 to prompt an I²C STOP to terminate the current I²C-read-over-AUX transaction. See Section 2.11.7.1.6.6 for an example of how to abort an I²C-over-AUX transfer that has repeated AUX_DEFERs. This is similar to receiving an unexpectedly high number of repeated I2C_DEFER responses.

2.11.7.1.6.4 Upon the Reply of I2C_ACK|AUX_ACK followed by the Total Number of Data Bytes Fewer than LEN + 1, to a Request Transaction with MOT Bit Cleared to 0 or Set to 1

The Source device shall:

- Repeat the identical I^2C-read-over-AUX transaction with the updated LEN value equal to the original LEN value minus the total number of data bytes received so far,
- Repeat the identical I^2C-read-over-AUX transaction with the same LEN value as the original value, –or–
- Issue an address-only I^2C-over-AUX with the MOT bit cleared to 0 to prompt an I^2C STOP to terminate the current I^2C-read-over-AUX transaction.

It should be noted that when the Source device repeats the same I^2C-read-over-AUX transaction with the same LEN value as the original value, the Sink device is likely to read more data bytes than the Source device needs.

2.11.7.1.6.5 Upon Receiving I2C_NACK|AUX_ACK Reply to a Request Transaction with MOT Bit Cleared to 0 or Set to 1

For I^2C read operation, I^2C slave only asserts either ACK or NACK to the Device Address. For read data byte transfer from the slave to the master, it is the I^2C master that asserts either ACK or NACK. Because of this fact, an I2C_NACK|AUX_ACK reply to the I^2C-read-over-AUX request transaction means that the I^2C slave in the Sink device has asserted NACK to the specified I^2C Device Address.

The Source device has the following options:

- Attempt an I^2C-write-over-AUX to the same I^2C Device Address to check whether the Sink device consistently I2C_NACKs to that I^2C Device Address
- Address-only I^2C-over-AUX with the MOT bit cleared to 0, to prompt the Sink device to terminate the current I^2C transaction
- Initiates an I^2C-over-AUX to a different I^2C Device Address, prompting the Sink device to issue a Repeated I^2C Start

2.11.7.1.6.6 Upon Receiving AUX_DEFER Reply to a Request Transaction with MOT Bit Cleared to 0 or Set to 1

The Source device shall do one of the following:

- Repeat the identical I^2C-read-over-AUX transaction keeping the same LEN value, –or–
- Issue Address-only I^2C-over-AUX with the MOT bit cleared to 0 to prompt an I^2C STOP to terminate the current I^2C-read-over-AUX transaction. See Section 2.11.7.1.6.6.1 for more information. Prior to aborting the transfer, the Source device shall retry the transaction several times before assuming an error condition is present that justifies the abort.

2.11.7.1.6.6.1 Source Retry Attempts following AUX_DEFER Response prior to Aborting Transfer

A DP Source device shall retry at least seven times upon receiving AUX_DEFER before giving up the AUX transaction.

If the DP Source device has a way of knowing the I^2C bit rate capability options of the downstream device and of setting the rate, either through vendor-specific method or through the I^2C Speed Control Capabilities Bit Map and I^2C Speed Control/Status Bit Map registers (DPCD Addresses 0000Ch and 00109h) for downstream devices with DPCD r1.2 or higher, the DP Source device should adjust the retry interval and/or number of request data bytes based on the I^2C bit rate.

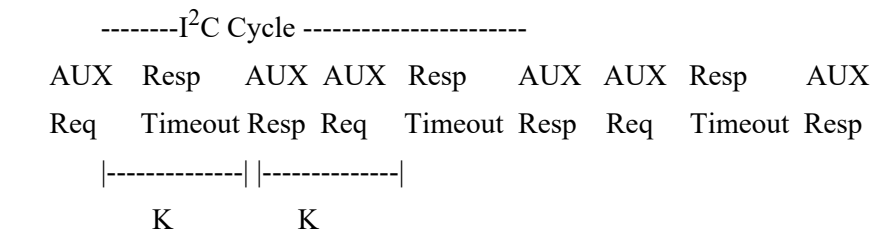
A Source device should take into account the various possible implementations from Sink devices of the I^2C-over-AUX burst read transaction. For example, a Sink device may issue AUX_DEFERs until all data in a read burst is ready. Then it may respond with all data words. At various I^2C Bus Speeds and burst sizes, this results in a wide array of retry limits. For example, Table 2-181 lists the retry limits associated with various I^2C bus speeds and various burst read sizes. Assuming a Sink device implementation which issues AUX_DEFERs until all read data is available, we come up with a worst case retry limit. **This example is for reference purposes only**; it does **not** take into account many factors which affect overall response time. It does not take into account I^2C Slave clock stretching, DP Source retry interval (it assumes Source repeats request immediately following DP Sink AUX_DEFER response), or varying DP Sink response times (assumes that the AUX Response Timeout timer timed out, and is immediately followed by a Sink device's AUX_DEFER response; see Section 2.11.2 for details regarding timeout timer period).

Table 2-181: Burst Read Sizes/Bus Speed Retry Limits

I^2C Bus Speed (kbps)	Burst Read Sizes / Maximum Number of Retries						
	1	2	4	6	8	12	16
1	44	66	110	154	198	287	375
5	9	13	22	31	39	57	75
10	4	6	11	15	20	28	37
100	0	0	1	1	2	3	4
400	0	0	0	0	0	0	1
1000	0	0	0	0	0	0	0

The calculations are based on the following assumptions:

- AUX request cycle consists of an I^2C-over-AUX Request (66 AUX_CH Bit times = pre-charge + Sync + Stop + CMD + Add + LEN) + 300us AUX Response Timeout + AUX Response
- An example timeline for the transfers is as follows:



- # of retries × K + 300us = I^2C Cycle length,
  where K = Response Timeout + AUX Response + AUX Request
- # of retries = (I^2C Cycle length – 300us) /
  (Response Timeout + AUX Response + AUX Request)

Note: *See Section 2.11.2 for details regarding Response Timeout.*

If the Source device has no way of knowing the downstream I^2C bit rate, the Source device may either retry for the period specified for the worst-case bit rate (in the order of 1kbps) or request one byte to "gauge" the effective downstream I^2C bit rate. Such precaution should be taken when the downstream device is a DP-to-Legacy protocol converter Branch device, where a long "legacy" cable may force a low I^2C bit rate.

The Source device shall properly terminate the pending I^2C-over-AUX transaction before starting I^2C-over-AUX for another I^2C transaction. To abort the transfer (after the recommended number of retries has been attempted), an address-only I^2C-over-AUX with the MOT bit cleared to 0 should be issued to prompt an I^2C STOP to terminate the current transaction. If the response to this is an AUX_DEFER, the Source device may abort the transaction.

2.11.7.1.6.7 No Reply

The Source device may initiate another AUX transaction. (A Sink device shall reply unless it either has detected an illegal command or is in a power-saving state due to the write of 02h to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h) by the Source device, by way of a Native AUX transaction.)

2.11.7.1.6.8 Clock Stretching

For an address-only I^2C-over-AUX with the MOT bit set to 1 and data byte transfer portion of I^2C-write-over-AUX transaction, the I^2C slave within a DPTX does not know in advance whether the DPRX shall reply with an I2C_ACK or I2C_NACK. Therefore, the I^2C slave shall stretch the I^2C clock after the eighth pulse (i.e., the last data bit), instead of after the ninth pulse (i.e., I^2C ACK/NACK).

For data byte transfer portion of an I^2C-read-over-AUX transaction, the I^2C slave within a DPTX shall stretch the I^2C clock after the ninth pulse (i.e., I^2C ACK/NACK) to monitor whether its I^2C master shall assert an I^2C ACK or NACK to the data byte.

2.11.7.2 Clarifications for a Sink Device

This section describes the clarifications for a Sink device.

2.11.7.2.1 I^2C Bit Rate Capability Declaration and Setting

A device with DPRX such as a Sink device declares its I^2C bit rate capability in the I^2C Speed Control Capabilities Bit Map register (DPCD Address 0000Ch). A device with a DPTX such as a Source device sets the I^2C bit rate by writing to the I^2C Speed Control/Status Bit Map register (DPCD Address 00109h). Alternatively, DPTX and DPRX may set the I^2C bit rate in a vendor-specific manner.

2.11.7.2.2 Termination/Completion of I^2C Transaction

Upon receiving an address-only I^2C-over-AUX request transaction with the MOT bit cleared to 0 from a Source device, the Sink device shall promptly issue an I^2C STOP condition to its I^2C slave, even before the current I^2C transaction is complete.

Upon receiving an address + LEN + Data bytes (for write, no Data bytes for read) I^2C-over-AUX request transaction with the MOT bit cleared to 0 from a Source device, the Sink device shall issue I^2C STOP condition upon completion of the current I^2C-over-AUX transaction (i.e., when all the address and/or data bytes have been ACKed by its I^2C slave).

When a Source device initiates a new I^2C transaction without properly completing/terminating the current I^2C transaction (which a Source device shall **not** do), a Sink device should reply with an I2C_NACK|AUX_ACK and issue an I^2C STOP condition to its I^2C slave.

When a Source device neither completes/terminates nor initiates a new I^2C transaction, a Sink device shall timeout after a certain period (e.g., 1 second) and issue I^2C STOP condition to its I^2C slave to avoid indefinitely locking up the I^2C bus within a Sink device. This scenario is possible when a Source device is powered down, disconnected, or somehow locked up in the middle of an I^2C transaction.

A Sink device supporting detection of Source and/or Powered-Source should issue an I^2C STOP condition to its I^2C slave when a disconnect event is detected in the middle of an I^2C transaction.

2.11.7.2.3 REPEATED I2C START Condition

A Source device may issue I^2C-over-AUX with the MOT bit set to 1, and then issue another I^2C-over-AUX to the same I^2C Device Address, but a different command (i.e., a write followed by a read or a read followed by a write).

A Source device may also issue I^2C-over-AUX with the MOT bit set to 1, and then issue another I^2C-over-AUX to a different I^2C Device Address with the same command (i.e., a write followed by a write or a read followed by a read).

The Sink device shall initiate the second I^2C transaction following Repeated I^2C Start, instead of an I^2C STOP.

2.11.7.2.4 I^2C-write-over-AUX

This section describes the permissible replies that can be issued by a Sink device after receiving an I^2C-write-over-AUX request transaction from a Source device. A Sink device shall reply with one of the ways described in this section.

2.11.7.2.4.1 I2C_ACK|AUX_ACK followed by No “M” Value

All the data bytes have been written to and ACKed by the I^2C slave.

- When the MOT bit was cleared to 0, the I^2C transaction is complete. The Sink device shall issue an I^2C STOP condition to its I^2C slave.
- When the MOT bit was set to 1, the I^2C transaction is still ongoing. The Sink device shall not issue an I^2C STOP condition.
    - If the ensuing I^2C-over-AUX transaction is either I^2C-read-over-AUX or to a different I^2C Device Address, the Sink device shall issue an I^2C REPEATED START condition to its I^2C slave.

2.11.7.2.4.2 I2C_ACK|AUX_ACK followed by "M" Value

Of the data bytes transmitted by the Source device, the number of bytes equal to "M" (that is smaller than LEN + 1 value) have been written to and ACKed by the I^2C slave.

The Sink device shall continue writing to its I^2C slave until the number of bytes equal to LEN + 1 has been ACKed by the slave.

- Upon receiving an ensuing I2C_WRITE_STATUS_UPDATE request transaction, the Sink device shall reply with I2C_ACK|AUX_ACK with the updated "M" value.
- Upon receiving an ensuing address-only I^2C-over-AUX with the MOT bit cleared to 0 transaction, the Sink device shall promptly issue an I^2C STOP condition to its slave, even before the current I^2C transaction is complete.
- Upon receiving an ensuing I^2C-over-AUX transaction that is neither I2C_WRITE_STATUS_UPDATE nor an address-only I^2C-over-AUX with the MOT bit cleared to 0, the Sink device should reply with an I2C_NACK|AUX_ACK to the Source device and promptly issue an I^2C STOP condition to its slave, even before the current I^2C transaction is complete. (A Source device shall issue either an I2C_WRITE_STATUS_UPDATE or an address-only I^2C-over-AUX with the MOT bit cleared to 0.)

2.11.7.2.4.3 I2C_DEFER|AUX_ACK

None of the data bytes has been ACKed/NACKed by the I^2C slave.

- A Sink device shall continue writing to its I^2C slave until the number of bytes equal to LEN + 1 has been ACKed by the slave.
  - After receiving an ensuing I2C_WRITE_STATUS_UPDATE request transaction, the Sink device shall reply with an I2C_ACK|AUX_ACK with the updated "M" value. However, if the Sink device has yet to receive an ACK from the I^2C slave, the device shall reissue an I2C_DEFER|AUX_ACK.
  - After receiving an ensuing address-only I^2C-over-AUX with the MOT bit cleared to 0 transaction, the Sink device shall reply with an I2C_ACK|AUX_ACK to the Source device and promptly issue an I^2C STOP condition to its slave, even before the current I^2C transaction is complete.
  - After receiving an ensuing I^2C-over-AUX transaction that is neither I2C_WRITE_STATUS_UPDATE nor an address-only I^2C-over-AUX with the MOT bit cleared to 0, the Sink device should reply with an I2C_NACK|AUX_ACK to Source device and promptly issue an I^2C STOP condition to its slave, even before the current I^2C transaction is complete. (A Source device shall issue either an I2C_WRITE_STATUS_UPDATE or an address-only I^2C-over-AUX with the MOT bit cleared to 0.)

2.11.7.2.4.4 I2C_NACK|AUX_ACK followed by Either "M" Value or No "M" Value

Either I^2C Device Address or Data byte are NACKed by the I^2C slave.

2.11.7.2.4.5 AUX_DEFER

A Sink device is handling the request, but is not ready to reply with either I2C_ACK or I2C_NACK. Until NACKed by the I^2C slave, the Sink device shall continue handling the request.

- Upon receiving an ensuing I^2C-write-over-AUX transaction identical to the previous transaction (the same I^2C Device Address, LEN value, and Data bytes), the Sink device shall reply to the Source device as described in this section while continuing handling the request.
- Upon receiving an ensuing address-only I^2C-write-AUX with the MOT bit cleared to 0 transaction, the Sink device shall reply with an I2C_ACK|AUX_ACK to the Source device and promptly issue an I^2C STOP condition to its slave, even before the current I^2C transaction is complete.
- Upon receiving an ensuing I^2C-over-AUX transaction that is neither identical to the previous transaction nor an address-only I^2C-write-over-AUX transaction, the Sink device should reply with an I2C_NACK|AUX_ACK to the Source device and promptly issue an I^2C STOP condition to its slave, even before the current I^2C transaction is complete. (A Source device shall issue either an I^2C-write-over-AUX transaction identical to the previous transaction or an address-only- I^2C-over-AUX with the MOT bit cleared to 0.)

2.11.7.2.4.6 AUX_NACK followed by Either “M” Value or No “M” Value

A Sink device shall not reply with AUX_NACK to I^2C-write-over-AUX transaction, unless there is a mismatch between the LEN + 1 value and the number of received data bytes.

2.11.7.2.4.7 No Reply

A Sink device shall reply unless it either has detected an illegal command or is in a power-saving state due to the write of 02h to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h) by the Source device, by way of a Native AUX transaction.

2.11.7.2.5 I^2C-read-over-AUX

This section describes the permissible replies by a Sink device after receiving an I^2C-read-over-AUX request transaction from a Source device. A Sink device shall reply with one of the ways illustrated in this section.

2.11.7.2.5.1 I2C_ACK|AUX_ACK followed by the Total Number of Data Bytes Equal to LEN + 1

All the data bytes have been read from the I^2C slave.

- When the MOT bit was cleared to 0, the I^2C transaction is complete. The Sink device shall issue NACK to the final Data byte and issue I^2C STOP condition to its I^2C slave.
- When the MOT bit was set to 1, the I^2C transaction is still on-going. The Sink device shall not issue I^2C STOP condition.
  - If the ensuing I^2C-over-AUX transaction is I^2C-write-over-AUX or I^2C-read-over-AUX to a different I^2C Device Address, the Sink device shall issue REPEATED I^2C START condition to its I^2C slave.

2.11.7.2.5.2 I2C_ACK|AUX_ACK followed by the Total Number of Bytes Fewer than LEN + 1

The Sink device shall continue reading from its I^2C slave until the number of bytes equal to LEN + 1 has been read.

- Upon receiving an ensuing I^2C-read-over-AUX transaction to the same I^2C device with the LEN value updated to be equal to the original value minus the total number of bytes replied by the Sink device so far, the Sink device shall reply with I2C_ACK|AUX_ACK with the Data bytes that have been read from the Slave but were not replied back to the Source device in the previous reply transaction(s).
- Upon receiving an ensuing I^2C-read-over-AUX transaction to the same I^2C device with the same LEN value as the original value, the Sink device shall reply with number of Data bytes equal to LEN + 1 (or fewer if it cannot), regardless of how many bytes it had already replied.
- Upon receiving an ensuing Address-only I^2C-over-AUX transaction with the MOT bit cleared to 0, the Sink device shall terminate the I^2C transaction by issuing an I^2C STOP.
- Upon receiving an ensuing I^2C-over-AUX transaction that is none of the above, the Sink device should reply with I2C_NACK|AUX_ACK to the Source device and promptly issue an I^2C STOP condition to its slave, even before the current I^2C transaction is complete.

2.11.7.2.5.3 I2C_DEFER|AUX_ACK

A Sink device shall continue reading from its I^2C slave until the number of bytes equal to LEN + 1 has been read.

- Upon receiving an ensuing I^2C-read-over-AUX transaction identical to the previous transaction (the same I^2C Device Address and LEN value), the Sink device shall reply with an I2C_ACK|AUX_ACK with the Data bytes that have been read from the Slave but were not replied back to the Source device in the previous reply transaction.
- Upon receiving an ensuing address-only I^2C-over-AUX with the MOT bit cleared to 0 transaction, the Sink device shall reply with an I2C_ACK|AUX_ACK to the Source device and promptly issue an I^2C STOP condition to its slave, even before the current I^2C transaction is complete.
- Upon receiving an ensuing I^2C-over-AUX transaction that is neither identical to the previous transaction nor an address-only I^2C-over-AUX with the MOT bit cleared to 0, the Sink device should reply with an I2C_NACK|AUX_ACK to the Source device and promptly issue an I^2C STOP condition to its slave, even before the current I^2C transaction is complete.

2.11.7.2.5.4 I2C_NACK|AUX_ACK

I^2C Device Address is NACKed by the I^2C slave.

It should be noted that the Sink device should **not** terminate the I^2C transaction following an I2C_NACK to the I^2C Device Address. Therefore, the Source device shall prompt the termination by issuing an address-only I^2C-over-AUX transaction with the MOT bit cleared to 0.

2.11.7.2.5.5 AUX_DEFER

The Sink device is handling the request, but is not ready to reply with either I2C_ACK or I2C_NACK. Until NACKed by the I^2C slave (to the I^2C Device Address). The Sink device shall continue handling the request.

- Upon receiving an ensuing I^2C-read-over-AUX transaction identical to the previous transaction (the same I^2C Device Address and LEN value), the Sink device shall reply to the Source device as described in this section while continuing handling the request.
- Upon receiving an ensuing address-only I^2C-over-AUX transaction with the MOT bit cleared to 0, the Sink device shall reply with an I2C_ACK|AUX_ACK to the Source device and promptly issue an I^2C STOP condition to its slave, even before the current I^2C transaction is complete.
- Upon receiving an ensuing I^2C-over-AUX transaction that is neither identical to the previous transaction nor an address-only I^2C-read-over-AUX transaction, the Sink device should reply with an I2C_NACK|AUX_ACK to the Source device and promptly issue an I^2C STOP condition to its slave, even before the current I^2C transaction is complete.

2.11.7.2.5.6 AUX_NACK

A Sink device shall **not** reply with an AUX_NACK to an I^2C-read-over-AUX transaction.

2.11.7.2.5.7 No Reply

A Sink device shall reply unless it either has detected an illegal command or is in a power-saving state due to the write of 02h to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h) by the Source device, by way of a Native AUX transaction.

2.11.7.2.6 Clock Stretching

When reading the last Data byte of an I^2C-read-over-AUX with the MOT bit set to 1, the I^2C master within a DPRX shall stretch the I^2C clock after the eighth pulse (i.e., the last data bit), instead of after the ninth pulse (I^2C ACK/NACK). When the ensuing I^2C-over-AUX transaction is the address-only with the MOT bit cleared to 0, the I^2C master within the DPRX shall assert I^2C NACK to its I^2C slave. Otherwise, I^2C master shall assert I^2C ACK.

For I^2C Device Address and Data write, I^2C master within a DPRX shall stretch the I^2C clock after the ninth pulse (i.e., ACK/NACK bit).

2.11.7.3 Accessing DisplayID or Legacy EDID of More than Two Blocks

A DisplayID or legacy EDID of more than two blocks may be used by a DP Sink device for stream sink capability exposure. A DP Source device and DP Sink device shall use E-DDC segment protocol to retrieve extra blocks. The DP Sink device shall automatically reset the segment offset to 0 whenever a DP Source device transmits an I^2C-over-AUX transaction with the MOT bit cleared to 0 (indicating an I^2C STOP condition).

2.12 AUX Services

This section describes two types of AUX services – AUX Link Services and AUX Device Services. These are the Link Layer services used by "Policy Makers" for link and device management in the Source and Sink devices.

Whenever the Hot Plug Detect signal is active (connectors are plugged in and the Sink device has at least trickle AC power), AUX services shall be available.

There are two Policy Makers:

- Stream Policy Maker
  - Manages stream
    - Stream transport initialization, and maintenance (more on this subject is covered in the following sections)
    - Uses AUX Device Services
    - Gets link information from Link Policy Maker
- Link Policy Maker
  - Manages link
    - Link discovery, initialization, and maintenance
    - Uses AUX Link Services

Both Source and Sink devices shall have these two policy makers. Policy Makers may be implemented as operating system, software driver, firmware, or hardware state machine. The choice is implementation-specific.

In this Standard, only the semantics of the interface between the Link Layer and Stream Policy Makers is defined. Syntax (i.e., API) is implementation-specific and is beyond the scope of this Standard.

2.12.1 Stream Transport Initiation Sequence

The Source Stream Policy Maker, before transport initiation, shall take the following actions:

- LTTPR recognition (see Section 3.6.6.6.1 details)
- Read DisplayID or legacy EDID from the Sink device
- Set stream attributes for MSA data and *CTA-861-G* INFOFRAME generation
- Should acquire the following information from the Link Policy Maker
  - Link Configuration field (DPCD Addresses 00100h through 001FFh; see Table 2-184) – Total link bandwidth
    - To avoid oversubscription of the link bandwidth
  - Receiver Capability field (DPCD Addresses 00000h through 000FFh; see Table 2-183) – Number and types of ports available in the RX
    - To determine the number and types of streams that may be transported
  - Link/Sink Device Status field (DPCD Addresses 00200h through 002FFh; see Table 2-185) – Synchronized? Excessive error symbols?
    - To ensure that the link is ready for transport

When a stream is ready for transport, the Source Stream Policy Maker shall start the transport of isochronous stream along with stream attributes data.

The Stream sink, upon receiving a stable stream, shall decode the stream attributes data and start reconstructing the incoming isochronous stream.

The Source Stream Policy Maker may incorporate the receiver capability information for the stream source management: A DP-aware Source Stream Policy Maker, for example, may try to limit the stream bandwidth to prevent link bandwidth oversubscription. If a stream is going to oversubscribe the link bandwidth, the Source Stream Policy Maker may inform the stream source. The stream source, upon receiving this notice, may take a corrective action, such as the reduction of image resolution and/or color depth (in bpp).

Although it is desirable, such an interaction between two policy makers is optional. In other words, DisplayPort Link shall be implemented to function with a legacy Source Stream Policy Maker that is unaware of DisplayPort.

Figure 2-134 illustrates diagrams of a typical Source and Sink device action flow when a Hot Plug Detect event occurs.

Notes: *The diagrams provided are for example purposes only. For example, although Figure 2-134 illustrates a DisplayID or legacy EDID Read preceding a DPCD read, it is not necessary to occur in that sequence.*

Figure 2-134 illustrates a typical action flow for a consumer detachable, box-to-box DP connection. When DisplayPort is used for an embedded connection, such as from a GPU to a laptop panel TCON within a laptop, a DPCD read may not be needed. In this embedded configuration, the Source device (GPU) may, instead, use the DPRX's pre-set receiver capability information.

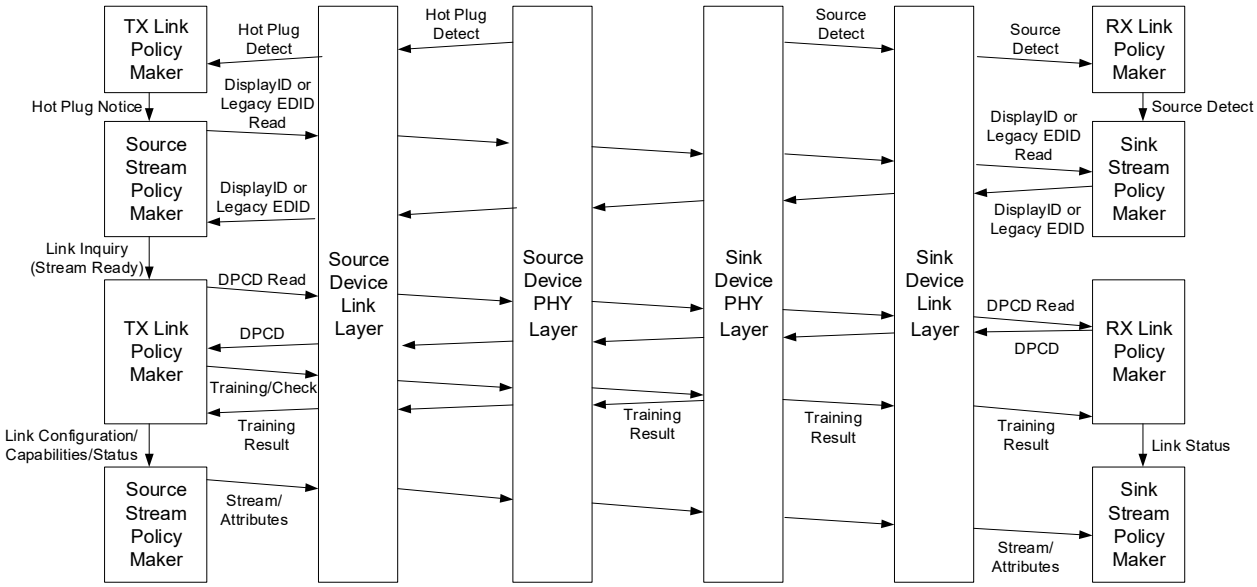


Figure 2-134: DP Source and Sink Device Action Flow Sequences when a Hot Plug Detect Event Occurs (Informative)

2.12.2 Stream Transport Termination Sequence

Examples of events that cause stream termination are as follows:

- Link error event notice by a Link Policy Maker
- Stream timing change
- Stream format change, unstable stream timing, or loss of stream

The stream source shall terminate the transport of the Main Stream and Secondary-data. It may re-initiate the transport following the initiation sequence after the link is re-established. The corrective action for the stream sink should be to either display a blank screen, possibly with an alert message, –or– to turn off the display until stable stream reception is resumed.

2.12.3 DPCD Field Address Mapping

Table 2-182 lists the DisplayPort address mapping and the tables in which they are listed (Table 2-183 through Table 2-199) for the byte-addressed DPCD.

Notes: *The address mapping tables included a* ***Byte #*** *column if the field includes multiple-byte registers. Byte numbers are listed in the tables only when the register is composed of two or more bytes.*

Unless indicated otherwise, all DPCD registers are applicable to both 8b/10b and 128b/132b channel coding.

Table 2-182: DPCD Field Address Mapping

DPCD Address	DPCD Field	See
00000h through 000FFh	Receiver Capability	Table 2-183
00100h through 001FFh	Link Configuration	Table 2-184
00200h through 002FFh	Link/Sink Device Status	Table 2-185
00300h through 003FFh	Source Device-specific	Table 2-186
00400h through 004FFh	Sink Device-specific	Table 2-187
00500h through 005FFh	Branch Device-specific	Table 2-188
00600h through 006FFh	Link/Sink Device Power Control	Table 2-189
00700h through 007FFh	eDP-specific	Table 2-190
00800h through 00FFFh	RESERVED (use to be defined)	–
01000h through 017FFh	Sideband MSG Buffers	Table 2-191
01800h through 01FFFh	RESERVED (use to be defined)	–
02000h through 021FFh	DPRX Event Status Indicator	Table 2-192
02200h through 022FFh	Extended Receiver Capability	Table 2-193
02300h through 02FFFh	RESERVED (use to be defined)	–
03000h through 030FFh	Protocol Converter Extension	Table 2-194
03100h through 5FFFFh	RESERVED (use to be defined)	–
60000h through 61CFFh	Multi-touch (for eDP)	Table 2-195
61D00h through 67FFFh	RESERVED (use to be defined)	–
68000h through 69FFFh	HDCP 1.3 and HDCP 2.2	Table 2-196
6A000h through DFFFFh	RESERVED (use to be defined)	–
E0000h through E00FFh	Tunneling Device-specific	Table 2-197
E0100h through EFFFFh	RESERVED (use to be defined)	–
F0000h through F02FFh	LTTPR	Table 2-198
F0300h through FFEFFh	RESERVED (use to be defined)	–
FFF00h through FFFFFh	*MyDP Standard*-specific	Table 2-199

2.12.3.1 DPCD Data Structure Revision Declaration

In this Standard, the Extended Receiver Capability field is added. The Extended Receiver Capability field at DPCD Addresses 02200h through 022FFh is valid with DPCD r1.4 (and higher). DPCD Addresses 02200h through 0220Fh (Extended Base Receiver Capability registers) match DPCD Addresses 00000h through 0000Fh (original Base Receiver Capability registers) except for the following three registers (the values might differ):

- DPCD_REV register (DPCD Address 00000h)
- 8b/10b_MAX_LINK_RATE register (DPCD Address 00001h)
- DOWN_STREAM_PORT_PRESENT register (DPCD Address 00005h)

The Extended Receiver Capability registers at DPCD Addresses 02200h through 0220Fh shall contain the DPRX's true capability, while the original Base Receiver Capability registers at DPCD Addresses 00000h through 0000Fh might indicate DPCD r1.1, a MAX_LINK_RATE of 2.7Gbps/lane, and no DFP to avoid interoperability issues with some of the existing DP Source devices that malfunction when they discover the higher capabilities within those three registers. A DPRX that supports the Extended Receiver Capability field shall set the EXTENDED_RECEIVER_CAPABILITY_FIELD_PRESENT bit in the 8b/10b_TRAINING_AUX_RD_INTERVAL register (DPCD Address 0000Eh, bit 7) to 1. The Extended Receiver Capability field has a data structure that helps a device that has a DPTX better comprehend the receiver's capability (e.g., the DPRX_FEATURE_ENUMERATION_LIST register (DPCD Address 02210h)). The DPCD Revision number at DPCD Address 00000h shall not be higher than that at DPCD Address 02200h.

A downstream device shall reset all DPCD Control and Configuration registers that are to be set by an upstream device, under the following conditions:

- After power-on reset, before asserting the HPD signal
- After detecting the disconnect of the upstream device

2.12.3.2 DPCD Field Address Mapping Tables

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00000h	**DPCD_REV** ***Note:*** *The DPCD revision number does not necessarily match the DP version number.* DPCD data structure revision number.			Read Only
		3:0	**Minor Revision Number**	
		7:4	**Major Revision Number** 10h = DPCD r1.0. 11h = DPCD r1.1. 12h = DPCD r1.2. 13h = DPCD r1.3 (for *eDP v1.4* DPRX only). 14h = DPCD r1.4. All other values are RESERVED. A DP device with a DPCD r1.2 (or higher) DPRX shall support the GUID register (DPCD Addresses 00030h through 0003Fh). Furthermore, a DPCD r1.2 (or higher) DP Sink device with stereo display capability support (as declared in DisplayID and legacy EDID) shall support handling of 3D Stereo in-band signaling by using the Video_Stream_Configuration (VSC) SDP.	
00001h	**8b/10b_MAX_LINK_RATE** Updated in *DP v2.0*. Valid only for 8b/10b Link Layer. A DP device that supports 128b/132b Link Layer link rates shall support all 8b/10b Link Layer link rates. ***Note:*** *For 128b/132b Link Layer, see the 128b/132b_SUPPORTED_LINK_RATES register (DPCD Address 02215h).* Main-Link Bandwidth Setting = Value × 0.27Gbps/lane. Four values are supported. All other values are RESERVED with the exception of *eDP v1.4* and *MyDP Standard* DPTXs. 06h = 1.62Gbps/lane (RBR). 14h = 5.4Gbps/lane (HBR2). 0Ah = 2.7Gbps/lane (HBR). 1Eh = 8.1Gbps/lane (HBR3). An eDP DPRX may program this register to 00h to indicate that the DPRX supports the Main-Link rates by way of the Link Rate Table method. (See *eDP v1.4*.) A *MyDP Standard* DPRX of an active *MyDP Standard* protocol converter (either MyDP-to-Legacy or MyDP-to-DP Lane-Count protocol converter) can support a value of 19h (6.75Gbps/lane). **SST-only Branch device in the presence of a downstream device** – For the mandated value of this register, see Section 2.1.4.1.			Read Only

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00002h	**MAX_LANE_COUNT**			Read Only
		4:0	**MAX_LANE_COUNT** Maximum number of lanes = Value. 01h = One lane (Lane 0 only). 02h = Two lanes (Lanes 0 and 1 only). 04h = Four lanes (Lanes 0, 1, 2, and 3). All other values are RESERVED. **SST-only Branch device in the presence of a downstream device** – For this field's mandated value, see Section 2.1.4.1.	
		5	**POST_LT_ADJ_REQ_SUPPORTED** 0 = POST_LT_ADJ_REQ sequence is not supported. 1 = POST_LT_ADJ_REQ sequence is supported. (See Section 3.5.1.2.5.) POST_LT_ADJ_REQ is the third link training sequence, and is used only when training to a link rate that is lower than UHBR10 and TPS4 cannot be used in the second (i.e., LANE*x*_CHANNEL_EQ_DONE) link training sequence. (TPS4 can be used only when the DPTX and DPRX both support TPS4.) An upstream device with a DPTX (Source or Branch device) aware of the POST_LT_ADJ_REQ sequence indicates granting of the POST_LT_ADJ_REQ sequence by setting the POST_LT_ADJ_REQ_GRANTED bit in the LANE_COUNT_SET register (DPCD Address 00101h, bit 5). The downstream device indicates that the POST_LT_ADJ_REQ sequence is in-progress by setting the POST_LT_ADJ_REQ_IN_PROGRESS bits in the LANE_ALIGN_STATUS_UPDATED and LANE_ALIGN_STATUS_UPDATED_ESI registers (DPCD Addresses 00204h and 0200Eh, respectively, bit 1). This is done at the end of the LANE*x*_CHANNEL_EQ_DONE sequence when the downstream device programs the Link/Sink Device Status field (DPCD Addresses 00200h through 002FFh; see Table 2-185) register bits to indicate LANE*x*_SYMBOL_LOCKED and INTERLANE_ALIGN_DONE completion.	

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00002h		6	**TPS3_SUPPORTED** Indicates Link Training Pattern Sequence 3 (TPS3) support. 0 = TPS3 is not supported. 1 = TPS3 is supported (shall be supported for Downstream devices that support HBR2; may be supported for others). A DPRX that is capable of supporting up to HBR2 (but **not** HBR3) shall support TPS3. Although it is not a normative mandate for a DPRX that is incapable of supporting HBR3, the DPRX should support TPS4. If TPS4 is not supported, the DPRX should support the POST_LT_ADJ_REQ sequence. (See Section 3.5.1.2.5.)	Read Only
		7	**ENHANCED_FRAME_CAP** ***Note:*** *Non-enhanced Framing (referred to as "Default Framing mode") was deprecated in DPCD r1.4.* Applies only to Single-Stream Transport (SST) mode. 0 = Enhanced Framing symbol sequence for BS and SR is not supported. 1 = Enhanced Framing symbol sequence for BS and SR is supported as described in Section 2.2.1.2. A DPRX with DPCD Data Structure r1.1 and higher (as expressed in the DPCD_REV register (DPCD Address 00000h)) shall set this bit to 1.	

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00003h	**MAX_DOWNSPREAD**			Read Only
		0	**MAX_DOWNSPREAD** Indicates whether the Spread-Spectrum Clock (SSC) is supported. SSC is enabled when this bit is set to 1 and the SPREAD_AMP bit in the DOWNSPREAD_CTRL register (DPCD Address 00107h, bit 4) is set to 1. 0 = No down spread (SSC is not supported). 1 = Up to 0.5% down spread (SSC is supported). Shall support up to 0.5% down spread for DPCD r1.1 (and higher) Sink and Branch devices. Therefore, this bit shall be set to 1.	
		1	**STREAM_REGENERATION_STATUS_CAPABILITY** New to *DP v2.0*. 0 = Not supported. 1 = Supported. STREAM_REGENERATION_STATUS bit in the SINK_STATUS SINK_STATUS_ESI registers (DPCD Addresses 00205h and 0200Fh, respectively, bit 2) is supported by the DPRX, and can be relied on by the DPTX.	
		5:2	**RESERVED**	Read all 0s
		6	**NO_AUX_TRANSACTION_LINK_TRAINING** 0 = DPTX shall issue AUX transactions to conduct link training. 1 = AUX transactions are not needed when the link configuration is already known. A DPTX, when it activates its Main-Link, can transmit TPS1 and TPS2 (or TPS3 or TPS4) for the minimum of 500us each. The known-good drive current and pre-emphasis level (or those used in the last "full" link training with AUX transactions) shall be used when link training is performed without AUX transactions. Regardless of this bit's value, a DP Sink device shall transmit an IRQ_HPD pulse when it cannot synchronize to the incoming stream. For embedded implementations in which there is no HPD line, either the proper operation should be guaranteed by design or the Source device can periodically poll the link status.	Read Only
		7	**TPS4_SUPPORTED** Indicates Link Training Pattern Sequence 4 (TPS4) support. 0 = TPS4 is not supported. 1 = TPS4 is supported (shall be supported for Downstream devices with DPCD r1.4, except for eDP DPRXs). TPS4 support declaration (by setting this bit) is required for all HBR3-capable DPRXs. DPRXs should support TPS4 and set this bit, regardless of whether the DPRX supports HBR3 because TPS4 is more conducive to robust link establishment than TPS2 and TPS3.	

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00004h	**NORP & DP_PWR_VOLTAGE_CAP** ***Note:*** *When bits 7:5 of this register are cleared to 000b, the downstream device is capable of producing the default 3.3V DP_PWR setting DP_PWR only. A downstream DP device capable of generating DP_PWR voltage higher than the default 3.3V DP_PWR setting shall complete the voltage level transition within 1ms. During the transition, the DP device shall not generate a voltage exceeding the voltage range of the higher of the two voltage levels between which the switching is taking place.*			Read Only
		0	**NORP** Number of Receiver Ports = Value + 1. 0 = One receiver port. 1 = Two or more receiver ports (see Note below). For SST mode, the maximum number is two (for which this bit is set to 1), one for an uncompressed video stream and the other for its associated audio stream. The receiver can simultaneously receive up to "NORP" isochronous streams. The smallest available Receiver Port number is assigned. For example, when there is only one receiver port, the receiver port is assigned to Receiver Port 0. Receiver Port 1 shall be assigned only after Receiver Port 0 has already been assigned. ***Note:*** *An MST Sink device might have more than two receiver ports because it can have three or more stream sinks. However, an MST Sink device shall program this bit according to the number of receiver ports when it is operating in SST mode. The MST Sink device shall operate in SST mode to interoperate with an SST upstream device.* *A Topology Manager in an MST Source device shall use the LINK_ADDRESS and REMOTE_DPCD message transactions to discover the number of receiver ports, rather than relying on this bit.*	
		1	**CRC_3D_OPTIONS_SUPPORTED** New to *DP v1.4a*. Enables the CRC_3D_OPTION1_SELECT bit in the TEST_SINK register (DPCD Address 00270h, bit 1). 0 = CRC 3D options are not supported. 1 = CRC 3D options are supported.	
		4:2	**RESERVED**	Read all 0s

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00004h		5	**5V_DP_PWR_CAP** 0 = Downstream device is not capable of producing +4.9 to +5.5V on the DP_PWR pin of its DP connector. 1 = Downstream device is capable of producing +4.9 to +5.5V on the DP_PWR pin of its DP connector.	Read Only
		6	**12V_DP_PWR_CAP** 0 = Downstream device is not capable of producing +12V ±10%. 1 = Downstream device is capable of producing +12V ±10% on the DP_PWR pin of its DP connector.	
		7	**18V_DP_PWR_CAP** 0 = Downstream device is not capable of producing +18V ±10%. 1 = Downstream device is capable of producing +18V ±10% on the DP_PWR pin of its DP connector.	

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00005h	**DOWN_STREAM_PORT_PRESENT**			Read Only
		0	**DFP_PRESENT** 1 = Device is a Branch device and has downstream-facing port(s) (DFP(s)).	
		2:1	**DFP_TYPE** Indicates DFP 0's DFP type. 00b = DisplayPort. 01b = Analog VGA or analog video over DVI-I. 10b = DVI, HDMI, or DP++. 11b = Others (this DFP type might not have a DisplayID or legacy EDID in the Sink device. For example, Sink devices on composite video and S-Video ports do not have a DisplayID or legacy EDID, but Sink devices on a wireless or USB interface might. A Branch device shall provide more-detailed Downstream enumeration data on all of its DFPs, including DFP 0 at DPCD Address 00080h and above. ***Note:*** *Further mandates for Branch devices are provided in Section 5.3.3. Mandates for Source devices when transmitting through a Branch device are provided in Section 5.1.6.*	
		3	**FORMAT_CONVERSION** 0 = This Branch device does not have a format conversion block. 1 = This Branch device has a format conversion block. ***Notes:*** *1 Applicable only to a Branch device.* *2 Topology Manager in an MST Source device shall use the LINK_ADDRESS message transaction to discover the DFP capability, rather than relying on this bit.*	
		4	**DETAILED_CAP_INFO_AVAILABLE** 0 = DFP capability field is 1 byte/port, starting from DPCD Address 00080h. 1 = DFP capability field is 4 bytes/port for the detailed capability description, starting from DPCD Address 00080h. For DPRX and DPCD r1.4, detailed capability information shall be supported.	
		7:5	**RESERVED**	Read all 0s

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00006h	**MAIN_LINK_CHANNEL_CODING_CAP** Updated in *DP v2.0*. The DPRX shall revert to 8b/10b Link Layer when a power-on reset or upstream device disconnect occurs. 0 = Not supported. 1 = Supported.			Read Only
		0	**8b/10b_SUPPORTED** Mandated to be set to 1.	
		1	**128b/132b_SUPPORTED** Set to 1 for DPRX that supports 128b/132b Link Layer.	
		7:2	**RESERVED**	Read all 0s
00007h	**DOWN_STREAM_PORT_COUNT**			Read Only
		3:0	**DFP_COUNT** Indicates the number of DFPs. 0h = No DFPs. Type and capability of the DFP are enumerated at DPCD Addresses 00080h through 0008Fh.	
		5:4	**RESERVED**	Read all 0s
		6	**MSA_TIMING_PAR_IGNORED** Applies to eDP and box-to-box DP. 0 = Sink device needs MSA timing parameters HTotal[15:0], HStart[15:0], HSyncPolarity[0] (HSP), HSyncWidth[14:0] (HSW), VTotal[15:0], VStart[15:0], VSyncPolarity[0] (VSP), and VSyncWidth[14:0] (VSW) to be transmitted by the Source device for rendering the incoming video stream. 1 = Sink device is capable of rendering the incoming video stream without the above-mentioned MSA timing parameters.	Read Only
		7	**OUI Support** 0 = OUI is not supported. 1 = OUI is supported (OUI and Device Identification shall be supported for DPCD r1.2 and DPCD r1.4; for DPCD r1.3 (which is for *eDP v1.4* DPRX), support for OUI is an implementation-specific option). Sink device IEEE_OUI registers (DPCD Addresses 00400h through 00402h), plus DPCD Addresses 00403h through 0040Bh for device identification. Branch device IEEE_OUI registers (DPCD Addresses 00500h through 00502h), plus DPCD Addresses 00503h through 0050Bh for device identification.	

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00008h	**RECEIVE_PORT0_CAP_0** Note updated in *DP v1.4*. Support for bits 5:3 added in *DP v1.4*. Receiver Port 0 Capability 0. ***Note:*** *A Source device operating in MST mode shall read this register from an SST device connected to an MST Branch device by way of a REMOTE_DPCD_READ message transaction.*			Read Only
		0	**RESERVED**	Read all 0s
		1	**LOCAL_EDID_PRESENT** 0 = This receiver port does not have a local DisplayID or legacy EDID. 1 = This receiver port has a local DisplayID or legacy EDID. A local DisplayID or legacy EDID shall be supported for Sink devices and format converters.	Read Only
		2	**ASSOCIATED_TO_PRECEDING_PORT** 0 = This port is used for the main isochronous stream. This bit shall always be cleared to 0 for Receiver Port 0. 1 = This port is used for the secondary isochronous stream of the main video stream received in the preceding port.	
		3	**HBLANK_EXPANSION_CAPABLE** 0 = DPRX is not capable of HBlank Expansion. 1 = DPRX is capable of HBlank Expansion.	
		4	**BUFFER_SIZE_UNIT** Defines the units to be used for defining the buffer size declared in the RECEIVE_PORT0_CAP_1 register (DPCD Address 00009h). 0 = Units are in pixel counts. 1 = Units are in byte counts. The DPRX shall ensure that the byte count unit is converted to the pixel count unit, as follows: Buffer_Size_in_Pixels = Buffer_Size_in_Bytes / Pixel_Depth_in_Bytes	
		5	**BUFFER_SIZE_PER_PORT** Defines units used for defining the buffer size declared in the RECEIVE_PORT0_CAP_1 register (DPCD Address 00009h). 0 = Buffer size is per-lane. 1 = Buffer size is per-port and independent of the lane count.	
		7:6	**RESERVED**	Read all 0s

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00009h	**RECEIVE_PORT0_CAP_1** Updated in *DP v1.4*. Receiver Port 0 Capability 1. ***Note:*** *A Source device operating in MST mode shall read this register from an SST device connected to an MST Branch device by way of a REMOTE_DPCD_READ message transaction.*			Read Only
		7:0	**BUFFER_SIZE** Buffer size = (Value + 1) × 32. Used for Horizontal Blanking Expansion, as described in Section 2.2.4.1.2. The unit is defined by the following RECEIVE_PORT0_CAP_0 register (DPCD Address 00008h) bits: • BUFFER_SIZE_UNIT bit (bit 4) value, and • BUFFER_SIZE_PER_PORT bit (bit 5) value, per-lane or per-port	
0000Ah	**RECEIVE_PORT1_CAP_0** Receiver Port 1 Capability 0. Bit definition is identical to the RECEIVE_PORT0_CAP_0 register (DPCD Address 00008h), but for Port 1. ***Notes:*** *1 When Receiver Port 1 is not present, this register is read all 0s.* *2 A Source device that is operating in MST mode does **not** use this register.*			Read Only

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
0000Bh	**RECEIVE_PORT1_CAP_1** Receiver Port 1 Capability 1. Bit definition is identical to the RECEIVE_PORT0_CAP_1 register (DPCD Address 00009h), but for Port 1. ***Notes:*** *1 When Receiver Port 1 not present, this register is read all 0s.* *2 A Source device that is operating in MST mode does **not** use this field.*			Read Only
0000Ch	**I^2C Speed Control Capabilities Bit Map**			Read Only
		7:0	Bit or bits set to indicate I^2C speed control capabilities. Source control of the I^2C speed should be supported when the DPRX implements a physical I^2C bus. If the DPRX does not implement a physical I^2C bus, this register is cleared to 00h. Otherwise, if the DPRX does not provide source control of the I^2C speed, this register is also cleared to 00h. In this case the DPRX, upon receiving an I^2C-over-AUX transaction, generates an I^2C transaction at the I^2C bit rate of its choice. Otherwise, bit values in this register are assigned to I^2C speeds. 01h = 1Kbps. 10h = 400Kbps. 02h = 5Kbps. 20h = 1Mbps. 04h = 10Kbps. 40h = RESERVED. 08h = 100Kbps. 80h = RESERVED.	
0000Dh	**eDP_CONFIGURATION_CAP** RESERVED for eDP. Always reads 00h for external receivers. See *eDP Standard*.			

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register					Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field			
0000Eh	**8b/10b_TRAINING_AUX_RD_INTERVAL**					Read Only
		6:0	**TRAINING_AUX_RD_INTERVAL** Updated in *DP v1.4*. Link Status/Adjust Request read interval during Main-Link training sequences. All other values are RESERVED.			
			Value	**LANE*x*_CR_DONE (Minimum)**	**LANE*x*_CHANNEL_EQ_DONE**	
			00h	100us	400us	
			01h	100us	4ms	
			02h	100us	8ms	
			03h	100us	12ms	
			04h	100us	16ms	
		7	**EXTENDED_RECEIVER_CAPABILITY_FIELD_PRESENT** New to *DP v1.3*. 0 = Not present. 1 = Present at DPCD Addresses 02200h through 022FFh. A DPCD r1.4 (or higher) DPRX shall have an Extended Receiver Capability field.			
0000Fh	**ADAPTER_CAP** Capabilities of Branch devices that adapt to legacy video transports.					Read Only
		0	**FORCE_LOAD_SENSE_CAP** 0 = Does not support VGA force load adapter sense mechanism. 1 = Supports VGA force load adapter sense mechanism.			
		1	**ALTERNATE_I2C_PATTERN_CAP** 0 = Does not support alternate I^2C patterns. 1 = Supports alternate I^2C patterns.			
		7:2	**RESERVED**			Read all 0s

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00010h through 0001Fh	**For DPCD r1.3 (*eDP v1.4* DPRX) only.** **For other DPCD Revisions up to DPCD r1.4, RESERVED.**			
	SUPPORTED_LINK_RATES See *eDP v1.4*.			
00020h	**SINK_VIDEO_FALLBACK_FORMATS** New to *DP v2.0*. After a DisplayID or legacy EDID read failure, a DP Source device shall read from this register to discover the DP Sink device-supported video fallback formats. A DP Source device may assume that 640x480 at 60Hz, 18bpp, is supported. Which video format to transmit is DP Source device policy-specific. DP Sink devices designed prior to the addition of this register will report 00h at this address. A DP single-stream Branch device with a DP DFP shall copy the plugged DP Sink device's SINK_VIDEO_FALLBACK_FORMATS register. A protocol conversion DP Branch device shall leave this register cleared to 00h.			Read Only
		0	**1024x768 at 60Hz, 24bpp Support** 0 = 1024x768 at 60Hz, 24bpp is not supported as a fallback mode. 1 = 1024x768 at 60Hz (as per *DMT Standard*), 24bpp is supported as a fallback mode (**optional**).	
		1	**1280x720 at 60Hz, 24bpp Support** 0 = 1280x720 at 60Hz, 24bpp is not supported as a fallback mode. 1 = 1280x720 at 60Hz (as per *CTA-861-G*), 24bpp is supported as a fallback mode (**optional**).	
		2	**1920x1080 at 60Hz, 24bpp Support** 0 = 1920x1080 at 60Hz, 24bpp is not supported as a fallback mode. 1 = 1920x1080 at 60Hz (as per *CTA-861-G*), 24bpp is supported as a fallback mode (**mandatory**).	
		7:3	**RESERVED**	Read all 0s

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00021h	**MSTM_CAP** Multi-Stream Transport (MST) mode capability.			Read Only
		0	**MST_CAP** Updated in *DP v2.0*. **8b/10b channel coding:** 0 = Does not support MST mode and does not have a Branching Unit, and therefore does not support Sideband MSG handling. 1 = Supports MST mode and has a Branching Unit, and therefore supports Sideband MSG handling. **128b/132b channel coding:** 0 = Does not support either multi-stream transport or Sideband MSG. 1 = Supports both multi-stream transport or Sideband MSG.	
		1	**SINGLE_STREAM_SIDEBAND_MSG_SUPPORT** New to *DP v2.0*. Valid only when the MST_CAP bit is cleared to 0. Applicable to both 8b/10b and 128b/132b channel coding. 0 = Does not support Sideband MSG. 1 = Supports Sideband MSG while not supporting multi-stream transport.	
		7:2	**RESERVED**	Read all 0s
00022h	**NUMBER_OF_AUDIO_ENDPOINTS** Number of audio endpoints available at this port. Applies to both audio devices (i.e., devices with no video endpoints) and devices with video endpoints that have audio endpoints associated with them. This value shall be 0 for Branch devices. ***Notes:*** *Audio endpoints are always associated with video endpoints in devices with video endpoints.* *A DP Sink device declares its audio stream sinking capability by setting the NORP bit in the NORP & DP_PWR_VOLTAGE_CAP register (DPCD Address 00004h, bit 0) to 1 and by placing the audio capability descriptor in the CTA Extension Block of DisplayID or legacy EDID. When these fields indicate the presence of an audio stream sinking capability and the NUMBER_OF_AUDIO_ENDPOINTS register is cleared to 0, a DP Source device shall assume that the number of audio endpoints for this DP device is equal to 1.* *A DP Sink device that has more than one audio endpoint shall set this register equal to the number of endpoints.*			Read Only

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00023h	**AV_SYNC_DATA_BLOCK_AV_GRANULARITY** ***Note:*** ***DPRX's AV_SYNC capability discovery*** *– Not all DPRXs with DPCD r1.2 or higher support the AV_SYNC feature. Devices with a DPTX that needs to use this register value should verify that the AV_SYNC_CAP bit in the DPRX_FEATURE_ENUMERATION_LIST register (DPCD Address 02210h, bit 2) is set to 1.*			Read Only
		3:0	**AG_FACTOR** Audio Granularity factor values used for the AUD_DEC_LAT7:0, AUD_DEC_LAT15:8, AUD_PP_LAT7:0, and AUD_PP_LAT15:8 fields in the AV_SYNC_DATA_BLOCK register (DPCD Addresses 00024h through 00027h, respectively). 0h = 3ms. 4h = 200us. 1h = 2ms (default). 5h = 100us. 2h = 1ms. 6h = 10us. 3h = 500us. 7h = 1us. All other values are RESERVED.	
		7:4	**VG_FACTOR** Video Granularity factor values used for the VID_INTER_LAT7:0 and VID_PROG_LAT7:0 fields in the AV_SYNC_DATA_BLOCK register (DPCD Addresses 00028h and 00029h, respectively). 0h = 3ms. 3h = 500us. 1h = 2ms (default). 4h = 200us. 2h = 1ms. 5h = 100us. All other values are RESERVED.	

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00024h	**AV_SYNC_DATA_BLOCK**			Read Only
	0	7:0	**AUD_DEC_LAT7:0** Worst-case Audio decode post processing latency, reported in the AUD_PP_LAT7:0 and AUD_PP_LAT15:8 fields (DPCD Addresses 00026h and 00027h, respectively). (Reported in terms of AG factor.)	
00025h	1	7:0	**AUD_DEC_LAT15:8**	
00026h	2	7:0	**AUD_PP_LAT7:0** Worst case Audio post processing latency. (Reported in terms of AG factor.)	
00027h	3	7:0	**AUD_PP_LAT15:8**	
00028h	4	7:0	**VID_INTER_LAT7:0** Worst-case Video interlaced latency for Video/Film mode. (Reported in terms of VG factor.)	
00029h	5	7:0	**VID_PROG_LAT7:0** Worst-case Video progressive latency for Video/Film mode. (Reported in terms of VG factor.)	
0002Ah	6	7:0	**REP_LAT7:0** Delay incurred in the repeater/Branch device while receiving and forwarding DP streams to the downstream device, in 10-us granularity.	
0002Bh	7	7:0	**AUD_DEL_INS7:0** Maximum additional delay that the Sink device is capable of inserting in addition to the inherent delays reported by the Sink device (AUD_DEC_LAT7:0, AUD_DEC_LAT15:8, AUD_PP_LAT7:0, and AUD_PP_LAT15:8 fields (DPCD Addresses 00024h through 00027h, respectively)), in 1-us granularity. Sink devices shall support a minimum of 5-ms delay insertion in the Audio path.	
0002Ch	8	7:0	**AUD_DEL_INS15:8**	
0002Dh	9	7:0	**AUD_DEL_INS23:16**	
0002Eh	**For DPCD r1.3 (*eDP v1.4* DPRX) only; otherwise, RESERVED**			
	RECEIVER_ADVANCED_LINK_POWER_MANAGEMENT_CAPABILITES See *eDP v1.4*.			
0002Fh	**For DPCD r1.3 (*eDP v1.4* DPRX) only; otherwise, RESERVED**			
	AUX FRAME SYNC See *eDP v1.4*.			

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00030h through 0003Fh	**GUID** Shall be supported in all DPCD r1.2 (or higher) DPRXs. Each set of DPCD registers, regardless of whether the register type is UFP DPCD or virtual DPCD, shall have a unique GUID value. Shall be generated according to *RFC 4122* and stored in Network Byte Order, i.e.: • DPCD Address 00030h contains the first octet (time_low, MSB) • DPCD Address 0003Fh contains the last octet (node(5)) When a Sink device has an integrated USB or hub device, the Container ID of the Sink device shall match the GUID in the Container Descriptor of that USB device or hub. All functions that are not removable from (i.e., are integrated into) the one physical device shall advertise the same Container ID GUID, regardless of the interface (DP or non-DP) through which it is reported. In a Sink device that has multiple audio and video endpoints, all the endpoints shall return the same GUID.			Read Only (Write/ Read Only when DPCD r1.2 or higher, but 00030h through 0003Fh are all 0s as power-on reset values)
00040h through 0004Fh	**GUID_2** ***Note:*** *DPCD Addresses 00040h through 00042h are assigned for DockPort capability enumeration in DP v1.4a. Because DockPort Standard has been deprecated, the DPCD Address range is being used for GUID_2.* New to *DP v2.0*. Second set of DPCD registers. Shall be all 0s in UFP DPCD registers. Virtual DPCD registers of a DP multi-stream Branch device with DPCD r1.4 or higher shall have the common non-zero value to enumerate the physical enclosure boundary of the Branch device. Shall be generated according to *RFC 4122* and stored in Network Byte Order, i.e.: • DPCD Address 00040h contains the first octet (time_low, MSB) • DPCD Address 0004Fh contains the last octet (node(5))			Read Only
00050h through 00053h	**RESERVED**			Read all 0s

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00054h through 00057h	**RX_GTC_VALUE** ***Note:*** ***DPRX's GTC capability discovery*** *– Not all DPRXs with DPCD r1.2 or higher support the GTC. Devices with a DPTX that needs to use this register value should verify one of the following:* • *GTC_CAP bit in the DPRX_FEATURE_ENUMERATION_LIST register (DPCD Address 02210h, bit 0) is set to 1* • *Downstream DPRX supports PSR2, which is defined in eDP Standard* *When a device with a DPTX attempts GTC lock acquisition with a DPRX that does not support GTC, the lock acquisition fails with the DPRX not updating the RX_GTC_VALUE register.*			Read Only
	0	7:0	**RX_GTC_VALUE7:0**	
	1	7:0	**RX_GTC_VALUE15:8**	
	2	7:0	**RX_GTC_VALUE23:16**	
	3	7:0	**RX_GTC_VALUE31:24**	
00058h	**RX_GTC_MSTR_REQ**			Read Only
		0	**RX_GTC_MSTR_REQ** 0 = RX does not request to be a GTC Master. 1 = RX requests to be a GTC Master.	
		1	**TX_GTC_VALUE_PHASE_SKEW_EN** 0 = DPTX resets its GTC value to the received RX_GTC_VALUE register (DPCD Addresses 00054h through 00057h) value, and uses the delta between its GTC value and the received RX_GTC_VALUE register value to frequency adjust its GTC value. 1 = DPTX resets its GTC value to the received RX_GTC_VALUE register value, but does **not** use the delta between its GTC value and the received RX_GTC_VALUE register value to frequency adjust its GTC value (i.e., the RX_GTC_VALUE register value is used only for phase adjust). Used only when the DPRX is the GTC Master.	
		7:2	**RESERVED**	Read all 0s
00059h	**RX_GTC_FREQ_LOCK_DONE**			Read Only
		0	**RX_GTC_FREQ_LOCK_DONE** 0 = DPRX has not achieved GTC_FREQ_LOCK_DONE. 1 = DPRX has achieved GTC_FREQ_LOCK_DONE. Used only when the DPTX is the GTC Master.	
		7:1	**RESERVED**	Read all 0s

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
0005Ah and 0005Bh	**RX_GTC_PHASE_SKEW_OFFSET**			Read Only
	0	7:0	**RX_GTC_PHASE_SKEW_OFFSET7:0**	
	1	7:0	**RX_GTC_PHASE_SKEW_OFFSET15:8**	
0005Ch through 0005Fh	**RESERVED**			Read all 0s

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
DSC Capability Register Set				
00060h through 0006Fh	The usages included here are specifically for *DP v1.4* (or higher), and are a superset of prior DSC DPCD register usage found in *eDP Standard*. (See *eDP Standard* for specifics.) Unused bits/addresses in the subset versions are marked as RESERVED.			
00060h	**DSC SUPPORT**			Read Only
		0	**DSC Support** ***Note:*** *Support is mandated for DP Sink and Branch devices that have a 128b/132b channel coding-capable UFP.* 0 = Decompression using DSC is not supported. 1 = Decompression using DSC is supported.	
		1	**DSC Pass-through Support** New to *DP v2.0*. ***Note:*** *Support is mandated for DP Branch devices that have a 128b/132b channel coding-capable UFP.* 0 = DSC bitstream pass-through is not supported. 1 = DSC bitstream pass-through is supported. See Section 2.8.8 for details.	
		2	**Dynamic PPS Update Support – Compressed-to-Compressed** New to *DP v2.0*. ***Note:*** *Support is mandated for DP Sink and Branch devices that have a 128b/132b channel coding-capable UFP.* 0 = Dynamic PPS update is not supported. 1 = Dynamic PPS update is supported. The device supports compressed frame-to-compressed frame update of the DSC bitstream target bits/pixel, as indicated by the PPS SDP, without a visual glitch.	
		3	**Dynamic PPS Update Support – Uncompressed-to/from-Compressed** New to *DP v2.0*. ***Note:*** *Support is mandated for DP Sink and Branch devices that have a 128b/132b channel coding-capable UFP.* 0 = Dynamic PPS update is not supported. 1 = Dynamic PPS update is supported. The device supports uncompressed frame-to/from-compressed frame update of the DSC bitstream target bits/pixel, as indicated by the PPS SDP, without a visual glitch.	
		7:4	**RESERVED**	Read all 0s

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00061h	**DSC ALGORITHM REVISION** ***Note:*** *DSC Version Major and DSC Version Minor field values are 1h and 2h, respectively, for both DSC v1.2 and DSC v1.2a.*			Read Only
		3:0	**DSC Version Major** Indicates the major version of DSC.	
		7:4	**DSC Version Minor** Indicates the minor version of DSC.	
00062h	**DSC RC BUFFER BLOCK SIZE**			Read Only
		1:0	**RC Buffer Block Size** Rate control buffer block size. 00b = 1KB. 10b = 16KB. 01b = 4KB. 11b = 64KB.	
		7:2	**RESERVED**	Read all 0s
00063h	**DSC RC BUFFER SIZE**			Read Only
		7:0	**Each Rate Buffer Size, in Units of Blocks** Buffer size (in blocks) = value + 1. Actual buffer size is calculated by multiplying the RC buffer size (in blocks) and the block size indicated by the RC Buffer Block Size field in the DSC RC BUFFER BLOCK SIZE register (DPCD Address 00062h, bits 1:0). **Example** – If RC Buffer Block Size is programmed to 11b (64KB) and the rate buffer size (in blocks) is 7Fh (128), each rate buffer size = 64KB × 128 = 8MB. ***Note:*** *Value is as specified in DSC Standard, Table E-1. It is the maximum algorithmic rate buffer size (`minRateBufferSize`) that the Sink device may support and is used by the Source device to ensure that the hrdDelay mandate is met.*	

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00064h	**DSC SLICE CAPABILITIES 1** Used in combination with the DSC SLICE CAPABILITIES 2 register (DPCD Address 0006Dh) to indicate the number of slices across a horizontal line that the DP DSC Sink device can support. 0 = Number of slices across a horizontal line per DP DSC Sink device is not supported. 1 = Number of slices across a horizontal line per DP DSC Sink device is supported.			Read Only
		0	**1_Slice_per_DP_DSC_Sink_Device**	
		1	**2_Slices_per_DP_DSC_Sink_Device**	
		2	**RESERVED**	Read 0
		3	**4_Slices_per_DP_DSC_Sink_Device**	Read Only
		4	**6_Slices_per_DP_DSC_Sink_Device** ***Note:*** *This value is not included as part of the standard slice value number set. A DP DSC Sink device may declare support of this number of slices across a horizontal line as an additional available configuration.*	
		5	**8_Slices_per_DP_DSC_Sink_Device**	
		6	**10_Slices_per_DP_DSC_Sink_Device** ***Note:*** *This value is not included as part of the standard slice value number set. A DP DSC Sink device may declare support of this number of slices across a horizontal line as an additional available configuration.*	
		7	**12_Slices_per_DP_DSC_Sink_Device**	
00065h	**DSC LINE BUFFER BIT DEPTH**			Read Only
		3:0	**Line Buffer Bit Depth** Contains the bit depth used by the Sink device to store the reconstructed pixels within the line buffer. 0000b = 9 bits. 0101b = 14 bits. 0001b = 10 bits. 0110b = 15 bits. 0010b = 11 bits. 0111b = 16 bits. 0011b = 12 bits. 1000b = 8 bits. 0100b = 13 bits. All other values are RESERVED.	
		7:4	**RESERVED**	Read all 0s

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00066h	**DSC FEATURE SUPPORT** 0 = Not supported. 1 = Supported.			Read Only
		0	**DSC Block Prediction Support**	
		1	**RGB Color Conversion Bypass Support** New to *DP v2.0*.	
		7:2	**RESERVED**	Read all 0s
00067h and 00068h	**MAXIMUM *bits_per_pixel* SUPPORTED BY THE DECOMPRESSOR** ***Notes:*** ***For DP v1.4a (and lower) and eDP v1.4 (and lower), this register is not used and shall be cleared to all 0s because the maximum bits_per_pixel is programmed to the bits/pixel of the input to the DSC encoder.*** Used by embedded displays with *DP v2.0* (and higher) and *eDP v1.4a* (and higher). Indicates the maximum ***bits_per_pixel*** that the DP DSC Sink device supports. Format is U6.4 (unsigned, four fractional bits).			
	For *DP v1.4a* (and lower) and *eDP v1.4* (and lower)			Read all 0s
	Note: *If cleared to all 0s, use the Maximum Allowed Bit Rate values in Table 2-154.*			
	0	7:0	**RESERVED**	
	1	7:0	**RESERVED**	
	For *DP v2.0* (and higher) and *eDP v1.4a* (and higher)			Read Only
	Note: *If cleared to all 0s, use the Maximum Allowed Bit Rate values in Table 2-153.*			
	0	7:0	***bits_per_pixel*7:0** Contains the least significant eight bits of the maximum ***bits_per_pixel*** that the DP DSC Sink device supports.	
	1	1:0	***bits_per_pixel*9:8** Contains the most significant two bits of the maximum ***bits_per_pixel*** that the DP DSC Sink device supports.	
		4:2	**RESERVED**	Read all 0s
		6:5	**MAX_BPP_DELTA_VERSION** 00b = Version 1. All other values are RESERVED.	Read Only
		7	**MAX_BPP_DELTA_AVAILABILITY** 0 = Not available. 1 = Available at DPCD Addresses 0006Eh (bits 7:0) and 0006Fh (bits 6:3).	

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00069h	**DSC DECODER PIXEL ENCODING FORMAT CAPABILITY** 0 = Not supported. 1 = Supported.			Read Only
		0	**RGB Support** DP DSC Sink devices shall support RGB color format.	
		1	**YCbCr 4:4:4 Support**	
		2	**YCbCr Simple 4:2:2 Support**	
		3	**YCbCr Native 4:2:2 Support** Native 4:2:2 mode is supported by *DSC v1.2* or higher.	
		4	**YCbCr Native 4:2:0 Support** Updated in *DP v1.4a*. Native 4:2:0 mode is supported by *DSC v1.2a* or higher.	
		7:5	**RESERVED**	Read all 0s
0006Ah	**DSC DECODER COLOR DEPTH CAPABILITY** Indicates whether the specified number of bits/(color) component is supported. 0 = Not supported. 1 = Supported.			Read Only
		0	**RESERVED**	Read 0
		1	**8 Bits/component Support** A DP DSC Sink device shall support 8bpc.	Read Only
		2	**10 Bits/component Support**	
		3	**12 Bits/component Support**	
		7:4	**RESERVED**	Read all 0s

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
0006Bh	**DSC Peak Throughput (DSC Sink)** ***Note:*** *For DP certification where DSC is supported, a value of 1 up to 14 for bits 3:0 and/or 7:4 is normative. If the value is programmed to 15, the device will* ***not*** *be eligible for DP certification. Devices with a value programmed to 15* ***cannot*** *be assumed to be interoperable with DP DSC-compliant devices. A value of 15 is to be used only for custom test devices or designs in which all devices within the stream are capable of supporting this special lower throughput rate.*			Read Only
		3:0	**Throughput Mode 0** Decoding of 3 pixels/clock (in MP/s) for 4:4:4 and Simple 4:2:2 modes. Values are indicated in decimal. 0 = Not supported. 8 = 700MP/s. 1 = 340MP/s. 9 = 750MP/s. 2 = 400MP/s. 10 = 800MP/s. 3 = 450MP/s. 11 = 850MP/s. 4 = 500MP/s. 12 = 900MP/s. 5 = 550MP/s. 13 = 950MP/s. 6 = 600MP/s. 14 = 1000MP/s. 7 = 650MP/s. 15 = 170MP/s (test or custom use only).	
		7:4	**Throughput Mode 1** Decoding of 6 pixels/clock (in MP/s) for Native 4:2:2 (*DSC v1.2* and higher) and Native 4:2:0 modes (*DSC v1.2a* and higher). Values are indicated in decimal. 0 = Not supported. 8 = 700MP/s. 1 = 340MP/s. 9 = 750MP/s. 2 = 400MP/s. 10 = 800MP/s. 3 = 450MP/s. 11 = 850MP/s. 4 = 500MP/s. 12 = 900MP/s. 5 = 550MP/s. 13 = 950MP/s. 6 = 600MP/s. 14 = 1000MP/s. 7 = 650MP/s. 15 = 170MP/s (test or custom use only).	Read Only
0006Ch	**DSC Maximum Slice Width** MaxSliceWidth = Number of pixels × 320. The minimum number allowed is 8 (2560 pixels).			Read Only

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
0006Dh	**DSC SLICE CAPABILITIES 2** Used in combination with the DSC SLICE CAPABILITIES 1 register (DPCD Address 00064h) to indicate the number of slices across a horizontal line that the DP DSC Sink device can support. 0 = Number of slices across a horizontal line per DP DSC Sink device is not supported. 1 = Number of slices across a horizontal line per DP DSC Sink device is supported.			Read Only
		0	**16_Slices_per_DP_DSC_Sink_Device**	
		1	**20_Slices_per_DP_DSC_Sink_Device**	
		2	**24_Slices_per_DP_DSC_Sink_Device**	
		7:3	**RESERVED**	Read all 0s
0006Eh and 0006Fh	**DSC_MAX_BPP_DELTA_AND_BPP_INCREMENT** ***Notes:*** ***For eDP v1.4b (and lower), this register is not used and shall be cleared to all 0s.*** ***For DP v1.4a (and lower), bits 2:0 of DPCD Address 0006Fh are used as the INCREMENT of bits_per_pixel SUPPORTED BY THE DECOMPRESSOR field of the BITS_PER_PIXEL_INCREMENT register. The remaining bits of the register are not used and shall be cleared to all 0s.*** ***For DP v2.0 (and higher), this register indicates not only the bpp increment but also the delta of the maximum-supported bpp by DP DSC Sink from the lowest maximum support requirement.***			
	For *eDP v1.4b* (and lower)			
	0	7:0	**RESERVED**	
	1	7:0	**RESERVED**	
	For *DP v1.4a* (and lower)			Read Only
	0	7:0	**RESERVED**	Read all 0s
		2:0	**INCREMENT OF *bits_per_pixel* SUPPORTED BY THE DECOMPRESSOR** Indicates the ***bits_per_pixel*** precision that the DP DSC Sink device supports. 000b = 1/16bpp. 011b = 1/2bpp. 001b = 1/8bpp. 100b = 1bpp. 010b = 1/4bpp. All other values are RESERVED.	Read Only
		7:3	**RESERVED**	Read all 0s

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
0006Eh and 0006Fh	***For DP v2.0 (and higher)***			Read Only
	0	4:0	**For MAX_BPP_DELTA Version 1:** **RGB_YCbCr444_SimpleYCbCr422_MAX_BPP_DELTA** 0 = Maximum allowed range (= the maximum bpc × 3). 1 = 16bpp. 2 = 17bpp. … 21 = 36bpp. 22 through 31 = RESERVED. All other version numbers are RESERVED.	
		7:5	**For MAX_BPP_DELTA Version 1:** **NativeYCbCr420_MAX_BPP_DELTA** 0 = Maximum allowed range (= the maximum bpc × 1.5). 1 = 12bpp. 2 = 13bpp. … 7 = 18bpp. All other version numbers are RESERVED.	
	1	2:0	**INCREMENT OF *bits_per_pixel* SUPPORTED BY THE DECOMPRESSOR** Indicates the ***bits_per_pixel*** precision that the DP DSC Sink device supports. 000b = 1/16bpp. 011b = 1/2bpp. 001b = 1/8bpp. 100b = 1bpp. 010b = 1/4bpp. All other values are RESERVED.	
		6:3	**For MAX_BPP_DELTA Version 1:** **NativeYCbCr422_MAX_BPP_DELTA** 0 = Maximum allowed range (= the maximum bpc × 2). 1 = 16bpp. 2 = 17bpp. … 9 = 24bpp. 10 through 15 = RESERVED. All other version numbers are RESERVED.	
		7	**RESERVED**	Read 0
End of DSC Capability Register Set				
00070h through 0007Fh	**For DPCD r1.3 (*eDP v1.4* DPRX) only; otherwise, RESERVED**			
	Used for Panel Self Refresh. See *eDP v1.4*.			

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00080h through 0008Fh	**Detailed Capabilities Info** 4-byte field, 1 byte/port type. DETAILED_CAP_INFO_AVAILABLE bit in the DOWN_STREAM_PORT_PRESENT register (DPCD Address 00005h, bit 4) = 0.			Read Only
	0		**DFPX_CAP** 1 byte/DFP. X = DFP number. Port_*x* capability is stored at the DFP number's address plus 80h.	
		2:0	**DFPX_TYPE** 000b = DisplayPort. 001b = Analog VGA. 010b = DVI. 011b = HDMI. 100b = Others without DisplayID or legacy EDID support. 101b = DP++. 110b = Wireless. 111b = RESERVED.	
		3	**DFPX_HPD** 0 = DFP is not HPD-aware. 1 = DFP is HPD-aware.	
00080h through 0008Fh	0	7:4	**NON_EDID_DFPX_ATTRIBUTE** Bits 2:0 = 100b. 1h = 720x480 interlaced, 60Hz. 2h = 720x480 interlaced, 50Hz. 3h = 1920x1080 interlaced, 60Hz. 4h = 1920x1080 interlaced, 50Hz. 5h = 1280x720 progressive, 60Hz. 7h = 1280x720 progressive, 50Hz. All other values are RESERVED. ***Notes:*** *1 A Source device may detect the interface type of the Sink device by reading the Video Input Definition byte of legacy EDID (or equivalent byte of DisplayID).* *2 Some interfaces may not have a built-in HPD support, but a Branch device may have its own HPD method. In that case, bit 3 shall be set to 1. For example, a Branch device with analog VGA DFP may periodically read legacy EDID (or equivalent byte of DisplayID) for the purpose of detecting an analog VGA Sink. HPD should be supported on the DFPs. For example, Windows Logo Program Device Requirements require HPD support on all digital display interfaces and strongly recommend HPD support for analog display interfaces.*	Read Only

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00080h through 0008Fh	**DETAILED_CAP_INFO_AVAILABLE bit in the DOWN_STREAM_PORT_PRESENT register (DPCD Address 00005h, bit 4) = 1** • DPCD Address 00080h (Byte 0) through 00083h (Byte 3) for DFP 0 • DPCD Address 00084h (Byte 0) through 00087h (Byte 3) for DFP 1 • DPCD Address 00088h (Byte 0) through 0008Bh (Byte 3) for DFP 2 • DPCD Address 0008Ch (Byte 0) through 0008Fh (Byte 3) for DFP 3 ***Note:*** *A DP upstream device shall read the capability from DPCD Addresses 00080h through 00083h. A DP Branch device with multiple DFPs shall report the detailed capability information of the lowest DFP number to which a downstream device is connected, consistent with the DisplayID or legacy EDID access routing policy of an SST-only DP Branch device as described in Section 2.1.4.1.*			Read Only
	0		**DFPX_CAP** X = DFP number. Port_*x* capability is stored at the DFP number's address plus 80h.	
		2:0	**DFPX_TYPE** 000b = DisplayPort. 001b = Analog VGA. 010b = DVI. 011b = HDMI. 100b = Others without DisplayID or legacy EDID support. 101b = DP++. 110b = Wireless. 111b = RESERVED.	
		3	**DFPX_HPD** 0 = DFP is not HPD-aware. 1 = DFP is HPD-aware.	
		7:4	**NON_EDID_DFPX_ATTR** Bits 2:0 = 100b. 1h = 720x480 interlaced, 60Hz. 2h = 720x480 interlaced, 50Hz. 3h = 1920x1080 interlaced, 60Hz. 4h = 1920x1080 interlaced, 50Hz. 5h = 1280x720 progressive, 60Hz. 7h = 1280x720 progressive, 50Hz. All other values are RESERVED.	

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00080h through 0008Fh	**For DP DFP**			Read all 0s
	3:1	**RESERVED**		
	For Analog VGA DFP			Read Only
	1	7:0	**Maximum Pixel Rate** Maximum pixel rate in MP/s, divided by 8.	
	2	1:0	**Maximum Bits/component** 00b = 8bpc is supported. 10b = 12bpc is supported. 01b = 10bpc is supported. 11b = 16bpc is supported. ***Note:*** *The DP input bits/component equal to or less than the maximum bits/component shall be supported by the analog VGA DAC.*	Read Only
		7:2	**RESERVED**	Read all 0s
	3	7:0	**RESERVED**	Read all 0s
	For DVI DFP			Read Only
	1	7:0	**Maximum TMDS Character Clock Rate** Maximum TMDS character clock rate supported in Mbps divided by 2.5 (e.g., 66 (42h) for 165MHz, 90 (5Ah) for 225MHz). ***Note:*** *A TMDS clock rate in excess of 165MHz on a DVI link is only supported for a Dual-Link DVI port.*	
	2	1:0	**Maximum Bits/component** 00b = 8bpc is supported. 10b = 12bpc is supported. 01b = 10bpc is supported. 11b = 16bpc is supported.	
		7:2	**RESERVED**	Read all 0s
	3	0	**RESERVED**	Read all 0s
		1	**DUAL_LINK** 0 = Single Link DVI output. 1 = Dual Link DVI output high pixel clock (assumed transition point of 165MHz).	Read Only
		2	**HIGH_COLOR_DEPTH** 0 = DVI High Color Depth is not supported. 1 = DVI High Color Depth is supported (meaningful only when Byte 2 is non-zero).	
		7:3	**RESERVED**	Read all 0s

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00080h through 0008Fh	**For HDMI DFP**			Read Only
	1	7:0	**Maximum TMDS Character Clock Rate** Maximum TMDS character clock rate supported in Mbps divided by 2.5. For example, a value of F0h (= 240 decimal) is placed in this register for a TMDS character clock rate of 600MHz.	
	2	1:0	**Maximum Bits/component** 00b = 8bpc is supported. 10b = 12bpc is supported. 01b = 10bpc is supported. 11b = 16bpc is supported.	
		7:2	**RESERVED**	Read all 0s
	3	0	**FRAME_SEQ_TO_FRAME_PACK** 0 = Conversion from Frame/Field Sequential 3D stereo video to Frame Pack is not supported. 1 = Conversion from Frame/Field Sequential 3D stereo video to Frame Pack is supported.	Read Only
		1	**YCBCR422_PASS_THROUGH_SUPPORT** 0 = Not supported. 1 = Supported.	
		2	**YCBCR420_PASS_THROUGH_SUPPORT** 0 = Not supported. 1 = Supported.	
		3	**CONVERSION_FROM_YCBCR444_TO_YCBCR422_SUPPORT** 0 = Not supported. 1 = Supported.	
		4	**CONVERSION_FROM_YCBCR444_TO_YCBCR420_SUPPORT** 0 = Not supported. 1 = Supported.	
		7:5	**RESERVED**	Read all 0s

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00080h through 0008Fh	**For DP++ DFP**			Read Only
	1	7:0	**Maximum TMDS Character Clock Rate** Maximum TMDS character clock rate supported in Mbps divided by 2.5.	
	2	1:0	**Maximum Bits/component** 00b = 8bpc is supported. 10b = 12bpc is supported. 01b = 10bpc is supported. 11b = 16bpc is supported.	
		7:2	**RESERVED**	Read all 0s
	3	0	**FRAME_SEQ_TO_FRAME_PACK** 0 = Conversion from Frame/Field Sequential 3D stereo video to Frame Pack is not supported. 1 = Conversion from Frame/Field Sequential 3D stereo video to Frame Pack is supported.	Read Only
		7:2	**RESERVED**	Read all 0s
	For Wireless DFP			Read Only
	1	**WIRELESS_CAP_BYTE**		
		3:0	**WIRELESS_TECHNOLOGY** 0h = WiGig Display Extension. All other values are RESERVED.	
		7:4	**RESERVED**	Read all 0s
	2	**WDE_TOPOLOGY** Only when WiGig Display Extension; otherwise, RESERVED.		Read Only
		1:0	**NUMBER_OF_WDE_TX_ON_DEVICE**	
		3:2	**WDE_TX_CONCURRENCY_CAP** Programmed to the number of WDE TXs that can be concurrently active.	
		7:4	**RESERVED**	Read all 0s
	3	7:0	**RESERVED**	Read all 0s

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00090h	**FEC_CAPABILITY_0** New to *DP v1.4*. Updated in *DP v2.0*. ***Note:*** *For bits 5:4, symbol size of Reed Solomon (RS) FEC is a variable.* ***8b/10b DisplayPort*** *– For RS(254, 250) FEC, the symbol size is set to 10 bits. Four 10-bit parity symbols are mapped to five 8b/10b codes plus four bits of CD_ADJ 8b/10b code.* ***128b/132b DisplayPort*** *– For RS(198, 194) FEC, the symbol size is 8 bits. Four 8-bit parity symbols (referred to as "four Parity bytes") are mapped to one 32-bit parity symbol, as defined in Section 3.5.2.4 and Section 3.5.2.11.*			Read Only
		0	**FEC_CAPABLE** 0 = Not capable. 1 = Capable.	
		1	**UNCORRECTED_BLOCK_ERROR_COUNT_CAPABLE** Indicates whether the DPRX is capable of counting the number of LL code uncorrected FEC blocks errors, as described in Section 3.5.3.3.1. Because this feature is mandatory, this bit shall be set to 1 for an FEC-capable DPRX. 0 = Not capable. 1 = Capable.	
		2	**CORRECTED_BLOCK_ERROR_COUNT_CAPABLE** Indicates whether the DPRX is capable of counting the number of LL code corrected FEC block errors, as described in Section 3.5.3.3.2. Because this feature is mandatory, this bit shall be set to 1 for an FEC-capable DPRX. 0 = Not capable. 1 = Capable.	
		3	**CORRECTED_BIT_ERROR_COUNT_CAPABLE** Indicates whether the DPRX is capable of counting the number of LL code corrected FEC bit errors, as described in Section 3.5.3.3.3. Because this feature is mandatory, this bit shall be set to 1 for an FEC-capable DPRX. 0 = Not capable. 1 = Capable.	

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00090h		4	**PARITY_BLOCK_ERROR_COUNT_CAPABLE** Indicates whether the DPRX is capable of counting the number of parity code corrected FEC block errors, as described in Section 3.5.3.3.2. Because this feature is mandatory, this bit shall be set to 1 for an FEC-capable DPRX. 0 = Not capable. 1 = Capable.	Read Only
		5	**PARITY_BIT_ERROR_COUNT_CAPABLE** Indicates whether the DPRX is capable of counting the number of parity code corrected FEC bit errors, as described in Section 3.5.3.3.3. Because this feature is mandatory, this bit shall be set to 1 for an FEC-capable DPRX. 0 = Not capable. 1 = Capable.	
		6	**FEC_RUNNING_INDICATOR_SUPPORTED** New to *DP v2.0*. 0 = Not supported. 1 = Supported. Indicates whether the FEC Running Indication provided by the FEC_RUNNING_INDICATOR bit in the FEC_STATUS register (DPCD Address 00280h, bit 2) is supported. **8b/10b channel coding** See Section 3.5.1.5.5 for further details. **128b/132b channel coding** Because FEC is always enabled, a 128b/132b channel coding-capable DPRX shall set this bit and the FEC_RUNNING_INDICATOR bit to 1 in normal operation, immediately after link training completion.	
		7	**FEC_ERROR_REPORTING_POLICY_SUPPORTED** Support for all five error counters (enumerated in bits 5:1 of this register) is required. Therefore, this bit shall be set to 1 for an FEC-capable DPRX. 0 = Not supported. Error reporting policy is an implementation-specific choice. 1 = Supported. Error reporting policy conforms to the policy described in Section 3.5.3.3.	Read Only

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00091h	**FEC_CAPABILITY_1** New to *DP v2.0*.			Read Only
		0	**AGGREGATED_ERROR_COUNTERS_CAPABLE** To select this option, a DPTX needs to increase the AGGREGATED_ENABLED_LANES_ERRORS bit in the FEC_CONFIGURATION register (DPCD Address 00120h, bit 6). 0 = Not supported. 1 = Supported. Indicates whether the DPRX can report FEC error counters selected from the FEC_ERROR_COUNT_SEL field in the FEC_CONFIGURATION register (DPCD Address 00120h, bits 3:1) as being aggregated across all enabled lanes.	
		7:1	**RESERVED**	Read all 0s
00092h through 0009Fh	**RESERVED**			Read all 0s
DSC Register Set – DSC Capability Branch Decoder Overall Throughput and Line Buffer Width				
000A0h	**BRANCH DSC OVERALL THROUGHPUT MODE 0** ***Note:*** *Available only in the UFP DPCD registers.* New to *DP v2.0*. See Section 2.10.1.1 for additional details. Decoding of 3 pixels/clock (in MP/s) for 4:4:4 and Simple 4:2:2 modes. Values are indicated in decimal. 0 = DP Source device shall parse the DSC peak throughput from the Throughput Mode 0 field in the DSC Peak Throughput (DSC Sink) register (DPCD Address 0006Bh, bits 3:0). 1 = 680MP/s. 2 through 255 = (600 + 50 × *N*)MP/s.			Read Only
000A1h	**BRANCH DSC OVERALL THROUGHPUT MODE 1** ***Note:*** *Available only in the UFP DPCD registers.* New to *DP v2.0*. See Section 2.10.1.1 for additional details. Decoding of 6 pixels/clock (in MP/s) for Native 4:2:2 mode (*DSC v1.2* or higher) and Native 4:2:0 mode (*DSC v1.2a* or higher). Values are indicated in decimal. 0 = DP Source device shall parse the DSC peak throughput from the Throughput Mode 1 field in the DSC Peak Throughput (DSC Sink) register (DPCD Address 0006Bh, bits 7:4). 1 = 680MP/s. 2 through 255 = (600 + 50 × *N*)MP/s.			Read Only

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
000A2h	**BRANCH DSC MAXIMUM LINE BUFFER WIDTH** ***Note:*** *Available only in the UFP DPCD registers.* New to *DP v2.0*. See Section 2.10.1.1 for additional details. MaximumLineBufferWidth = 8-bit value × 320 (in pixels). 0 = DP Source device shall determine the DP DSC decoder's output line width from the slice/line count that is enumerated in the DSC SLICE CAPABILITIES 1 register (DPCD Address 00064h) and the minimum slice width mandate. Minimum non-zero value for DP DSC Branch Sink devices is 16 decimal (5120 pixels).			Read Only
End of DSC Register Set – DSC Capability Branch Decoder Overall Throughput and Line Buffer Width				
DFP Capability Extension Register Set				
000A3h	**DFP CAPABILITY EXTENSION SUPPORT** New to *DP v2.0*. See Section 2.10.3 for additional details.			Read Only
		0	**DFP CAPABILITY EXTENSION SUPPORTED** 0 = DFP Capability Extension registers are not supported. 1 = DFP Capability Extension registers are supported.	
		7:1	**RESERVED**	Read all 0s
000A4h and 000A5h	**DFP MAXIMUM PIXEL RATE** New to *DP v2.0*. See Section 2.10.3 for additional details. Maximum pixel rate (in MP/s). Populates with FFFFh when there is no limit.			Read Only
	0	7:0	**DFP MAXIMUM PIXEL RATE7:0**	
	1	7:0	**DFP MAXIMUM PIXEL RATE15:8**	
000A6h and 000A7h	**DFP MAXIMUM VIDEO HORIZONTAL ACTIVE WIDTH** New to *DP v2.0*. See Section 2.10.3 for additional details. Maximum video horizontal active width (in pixels). Populates with FFFFh when there is no limit.			Read Only
	0	7:0	**DFP MAXIMUM VIDEO HORIZONTAL ACTIVE WIDTH7:0**	
	1	7:0	**DFP MAXIMUM VIDEO HORIZONTAL ACTIVE WIDTH15:8**	
000A8h and 000A9h	**DFP MAXIMUM VIDEO VERTICAL ACTIVE HEIGHT** New to *DP v2.0*. See Section 2.10.3 for additional details. Maximum video vertical active height (in lines). Populates with FFFFh when there is no limit.			Read Only
	0	7:0	**DFP MAXIMUM VIDEO VERTICAL ACTIVE HEIGHT7:0**	
	1	7:0	**DFP MAXIMUM VIDEO VERTICAL ACTIVE HEIGHT15:8**	

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
000AAh	**DFP SUPPORTED PIXEL ENCODING FORMAT** New to *DP v2.0*. See Section 2.10.3 for additional details. 0 = Not supported. 1 = Supported.			Read Only
		0	**RGB Support** Support for RGB is mandatory.	
		1	**YCbCr444 Support**	
		2	**YCbCr422 Support**	
		3	**YCbCr420 Support**	
		7:4	**RESERVED**	Read all 0s
000ABh	**DFP SUPPORTED RGB PIXEL COMPONENT BIT DEPTH** New to *DP v2.0*. See Section 2.10.3 for additional details. 0 = Not supported. 1 = Supported.			Read Only
		0	**6bpc Support**	
		1	**8bpc Support** 8bpc support is mandatory.	
		2	**10bpc Support**	
		3	**12bpc Support**	
		4	**16bpc Support**	
		7:5	**RESERVED**	Read all 0s
000ACh	**DFP SUPPORTED YCbCr444 PIXEL COMPONENT BIT DEPTH** New to *DP v2.0*. See Section 2.10.3 for additional details. 0 = Not supported. 1 = Supported.			Read Only
		0	**RESERVED**	Read 0
		1	**8bpc Support**	Read Only
		2	**10bpc Support**	
		3	**12bpc Support**	
		4	**16bpc Support**	
		7:5	**RESERVED**	Read all 0s

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
000ADh	**DFP SUPPORTED YCbCr422 PIXEL COMPONENT BIT DEPTH** New to *DP v2.0*. See Section 2.10.3 for additional details. 0 = Not supported. 1 = Supported.			Read Only
		0	**RESERVED**	Read 0
		1	**8bpc Support**	Read Only
		2	**10bpc Support**	
		3	**12bpc Support**	
		4	**16bpc Support**	
		7:5	**RESERVED**	Read all 0s
000AEh	**DFP SUPPORTED YCbCr420 PIXEL COMPONENT BIT DEPTH** New to *DP v2.0*. See Section 2.10.3 for additional details. 0 = Not supported. 1 = Supported.			Read Only
		0	**RESERVED**	Read 0
		1	**8bpc Support**	Read Only
		2	**10bpc Support**	
		3	**12bpc Support**	
		4	**16bpc Support**	
		7:5	**RESERVED**	Read all 0s
000AFh	**RESERVED for DFP Capability Extension Use**			Read all 0s
End of DFP Capability Extension Register Set				
PR Capability Register Set				
000B0h	**PANEL REPLAY CAPABILITY SUPPORTED** New to *DP v2.0*.			Read Only
		0	**Panel Replay Support** 0 = Panel Replay capability is not supported (default). 1 = Panel Replay capability is supported.	
		1	**Selective Update Support** 0 = Selective Update (SU) capability is not supported (default). 1 = SU capability is supported. The Panel Replay Support bit (bit 0) should also be set to 1.	
		7:2	**RESERVED**	Read all 0s

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
000B1h	**PANEL REPLAY CAPABILITY** New to *DP v2.0*.			Read Only
		4:0	**RESERVED**	Read all 0s
		5	**Panel Replay Selective Update Granularity Needed** 0 = SU coordinates do not need to adhere to any granularity. 1 = SU coordinates need to adhere to the granularity specified in the PANEL REPLAY SELECTIVE UPDATE X GRANULARITY CAPABILITY and PANEL REPLAY SELECTIVE UPDATE Y GRANULARITY CAPABILITY registers (DPCD Addresses 000B2h and 000B3h, and 000B4h, respectively).	Read Only
		7:6	**RESERVED**	Read all 0s
000B2h and 000B3h	**PANEL REPLAY SELECTIVE UPDATE X GRANULARITY CAPABILITY** New to *DP v2.0*. Sets the grid pattern granularity in the X direction. 0000h = No X-coordinate granularity requirement exists other than the standard restrictions, wherein the: • Starting X-coordinate shall be evenly divisible by 16 • Rectangle width shall be evenly divisible by 4 Non-zero = X-coordinate shall be evenly divisible by SU_X_GRANULARITY (i.e., mod (x_coordinate, SU_X_GRANULARITY) shall be 0). The SU region width (VSC SDP for Panel Replay DB10 through DB11) shall be evenly divisible by SU_X_GRANULARITY. The active video width shall also be evenly divisible by SU_X_GRANULARITY.			Read Only
	0	7:0	**SU_X_GRANULARITY7:0**	
	1	7:0	**SU_X_GRANULARITY15:8**	

Table 2-183: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Receiver Capability Field	
000B4h	**PANEL REPLAY SELECTIVE UPDATE Y GRANULARITY CAPABILITY** New to *DP v2.0*. Sets the grid pattern granularity in the Y direction. 00h or 01h = No restrictions to the SU region Y-coordinate (VSC SDP for Panel Replay DB12 through DB13). 02h or higher = Y-coordinate shall be evenly divisible by SU_Y_GRANULARITY (i.e., mod (y_coordinate, SU_Y_GRANULARITY) shall be 0). A DP Sink device should support values of 00h, 01h, 02h, or 04h to ensure interoperability with various DP Source devices. Values of 08h or 10h may be considered for system-specific implementations. SU region height shall be evenly divisible by SU_Y_GRANULARITY. Active video height shall also be evenly divisible by SU_Y_GRANULARITY.			Read Only
		7:0	**SU_Y_GRANULARITY** 00h or 01h = One-line address and height granularity. 02h = Two-line address and height granularity. 04h = Four-line address and height granularity. 08h = Eight-line address and height granularity. 10h = 16-line address and height granularity. All other values are RESERVED.	
End of PR Capability Register Set				
000B5h through 000FFh	**RESERVED**			Read all 0s

Table 2-184: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link Configuration Field	
00100h	**LINK_BW_SET**			Write/Read
	8b/10b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 01h)			
	Main-Link Bandwidth Setting = Value × 0.27Gbps/lane. ***Note:*** *Because the upstream device shall program this value within the 8b/10b_MAX_LINK_RATE register (DPCD Address 00001h), this register does not have a power-on reset default value. This field should be programmed to 06h because a certain PC graphics controller under basic software control (e.g., VBIOS) may choose to output 640x480 at 60Hz RGB video over a 1-lane Main-Link at RBR (1.62Gbps/lane) without programming this register and the LANE_COUNT_SET register (DPCD Address 00101h) in the event that the HPD input is not asserted when the basic software is loaded.* Four values are supported. All other values are RESERVED with the exception of *eDP v1.4* and *MyDP Standard* DPTXs. 06h = 1.62Gbps/lane (RBR). 14h = 5.4Gbps/lane (HBR2). 0Ah = 2.7Gbps/lane (HBR). 1Eh = 8.1Gbps/lane (HBR3). An *eDP v1.4* DPTX, after reading DPCD r1.3 (which is applicable only for *eDP v1.4* DPRX) and a 8b/10b_MAX_LINK_RATE register value of 00h uses the LINK_RATE_SET field in the LINK_RATE_SET and TX_GTC_CAPABILITY register (DPCD Address 00115h, bits 2:0) instead of writing to this register. (See *eDP v1.4*.) A *MyDP Standard* Source device, after reading the 8b/10b_MAX_LINK_RATE register of the downstream DPRX programmed to 19h (which can be the case only for a MyDP-to-legacy or MyDP-to-DP lane count converter) can program the LINK_BW_SET register (DPCD Address 00100h) to 19h to enable 6.75Gbps/lane.		
	128b/132b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 02h) New to *DP v2.0*. The DPRX shall revert to 8b/10b Link Layer when a power-on reset or upstream device disconnect occurs.			
	Three values are supported. All other values are RESERVED. 01h = 10Gbps/lane (UHBR10). 02h = 20Gbps/lane (UHBR20). 04h = 13.5Gbps/lane (UHBR13.5).			

Table 2-184: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link Configuration Field	
00101h	**LANE_COUNT_SET** Main-Link Lane Count = Value.			Write/Read
	8b/10b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 01h)			
		4:0	**LANE_COUNT_SET** ***Note:*** *Because the upstream device shall program this value within the MAX_LANE_COUNT register (DPCD Address 00002h), this field does not have a power-on reset default value. This field should be programmed to 01h. (See the Note within the LINK_BW_SET register (DPCD Address 00100h) description.)* 01h = One lane (Lane 0 only). 02h = Two lanes (Lanes 0 and 1 only). 04h = Four lanes (Lanes 0, 1, 2, and 3). All other values are RESERVED. A Source device may choose any lane count as long as it does not exceed the DPRX's capability.	
		5	**POST_LT_ADJ_REQ_GRANTED** Shall be cleared to 0 when a power-on reset or upstream device disconnect occurs. An upstream device with a DPTX sets this bit to 1 to grant the POST_LT_ADJ_REQ sequence by the downstream DPRX if the downstream DPRX supports POST_LT_ADJ_REQ, but does not support TPS4. If the upstream DPTX and downstream DPRX both support TPS4, TPS4 shall be used instead of POST_LT_ADJ_REQ. See Section 3.5.1.2.5 for details regarding POST_LT_ADJ_REQ.	Write/Read
		6	**RESERVED**	Read 0
		7	**ENHANCED_FRAME_EN** Shall be cleared to 0 when a power-on reset or upstream device disconnect occurs. 0 = Enhanced Framing symbol sequence is not enabled. 1 = Enhanced Framing symbol sequence for BS and SR is enabled. Applicable to SST-only mode. A DPTX shall set this bit to 1 when the DPRX has the ENHANCED_FRAME_CAP bit in the MAX_LANE_COUNT register (DPCD Address 00002h, bit 7) set to 1.	Write/Read

Table 2-184: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link Configuration Field	
00101h	**128b/132b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 02h)** New to *DP v2.0*. The DPRX shall revert to 8b/10b Link Layer when a power-on reset or upstream device disconnect occurs.			Write/Read
		4:0	**LANE_COUNT_SET** 01h = One lane (Lane 0 only). 02h = Two lanes (Lanes 0 and 1 only). 04h = Four lanes (Lanes 0, 1, 2, and 3). All other values are RESERVED.	
		7:5	**"Don't Care"**	
00102h	**TRAINING_PATTERN_SET** Effect of the bits 3:0 value is DPCD revision-dependent. Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs. The DPTX ends link training by writing 00h to this register when link training is complete.			
	For DPCD r1.1 (Bits 3:0)			Write/Read
		1:0	**TRAINING_PATTERN_SELECT** Link Training Pattern Sequence selection. 00b = Training not in progress (or disabled). 01b = Link Training Pattern Sequence 1. 10b = Link Training Pattern Sequence 2. 11b = RESERVED.	
		3:2	**LINK_QUAL_PATTERN_SET** 00b = Link quality test pattern not transmitted. 01b = D10.2 test pattern (unscrambled) transmitted (same as Link Training Pattern Sequence 1). 10b = Symbol Error Rate measurement pattern transmitted. 11b = PRBS7 transmitted. The PRBS7 bit sequence shall be as follows: `----- direction ---->` `0010000011000010100` `0111100100010110011101010 01` `1111010000111000100100110 11` `0101101111011000110100101 11` `0111001100101010111111100 00` ***Note:*** *Upper left is transmitted first and lower right is transmitted last.*	

Table 2-184: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link Configuration Field	
00102h	**For DPCD r1.2 and DPCD r1.3 (Bits 3:0)**			Write/Read
		1:0	**TRAINING_PATTERN_SELECT** Link Training Pattern Sequence selection. 00b = Training not in progress (or disabled). 01b = Link Training Pattern Sequence 1. 10b = Link Training Pattern Sequence 2. 11b = Link Training Pattern Sequence 3.	
		3:2	**RESERVED** Replaced with per-lane control in each Lane's LINK_QUAL_PATTERN_SET fields in the LINK_QUAL_LANE*x*_SET register(s) (DPCD Address(es) 0010Bh through 0010Eh, bits 6:0).	Read all 0s
	For DPCD r1.4 (Bits 3:0) in 8b/10b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 01h)			Write/Read
		3:0	**8b/10b_TRAINING_PATTERN_SELECT** Link training pattern selection. 0h = Training not in progress (or disabled; default). 1h = Link Training Pattern Sequence 1 (TPS1). 2h = Link Training Pattern Sequence 2 (TPS2). 3h = Link Training Pattern Sequence 3 (TPS3). 7h = Link Training Pattern Sequence 4 (TPS4). All other values are RESERVED.	
	For DPCD r1.4 (Bits 3:0) in 128b/132b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 02h) New to *DP v2.0*.			
		3:0	**128b/132b_TRAINING_PATTERN_SELECT** Link training pattern selection. The DPRX shall revert to 8b/10b Link Layer when a power-on reset or upstream device disconnect occurs. 0h = Training not in progress (or disabled; default). 1h = 128b/132b_TPS1. 2h = 128b/132b_TPS2. All other values are RESERVED.	

Table 2-184: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link Configuration Field	
00102h	**Bits 7:4 in 8b/10b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 01h)** Default is 0h.			Write/Read
		4	**RECOVERED_CLOCK_OUT_EN** 0 = Recovered clock output from a test pad of DPRX is not enabled. 1 = Recovered clock output from a test pad of DPRX is enabled.	
		5	**SCRAMBLING_DISABLE** 0 = DPTX scrambles data symbols before transmission. 1 = DPTX disables scrambler and transmits all symbols without scrambling.	
		7:6	**SYMBOL_ERROR_COUNT_SEL** 00b = Count Disparity and Illegal Symbol errors. 01b = Count Disparity errors only. 10b = Count Illegal Symbol errors only. 11b = RESERVED.	
	Bits 7:4 in 128b/132b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 02h) New to *DP v2.0*. The DPRX shall revert to 8b/10b Link Layer when a power-on reset or upstream device disconnect occurs.			Write/Read
		4	**RESERVED**	Read 0
		5	**SCRAMBLING_DISABLE** 0 = DPTX scrambles data symbols before transmission (default). 1 = DPTX disables scrambler and transmits all symbols without scrambling. ***Note:*** *"Don't care" for 128b/132b_TPS1.* To enable scrambling, the DPTX shall clear this bit to 0 before the start of link training. To disable scrambling, the DPTX shall set this bit to 1 before the start of link training. When the DPTX needs to change this bit's state, the DPTX shall initiate a new link training sequence. When disabling scrambling, the DPTX shall program the Lane's LINK_QUAL_PATTERN_SET field in the LINK_QUAL_LANE*x*_SET register(s) (DPCD Address(es) 0010Bh through 0010Eh, bits 6:0) and enable DC-balanced test patterns.	Write/Read
		7:6	**RESERVED**	Read all 0s

Table 2-184: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link Configuration Field	
00103h	**TRAINING_LANE0_SET** Lane 0 link training control. Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs.			Write/Read
	8b/10b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 01h)			
		1:0	**VOLTAGE_SWING_SET** 00b = Voltage Swing Level 0. 10b = Voltage Swing Level 2. 01b = Voltage Swing Level 1. 11b = Voltage Swing Level 3.	
		2	**MAX_SWING_REACHED** Transmitter shall support at least three levels of voltage swing (Levels 0, 1, and 2). May also support Voltage Swing Level 3. • If only three voltage swing levels are supported (VOLTAGE_SWING_SET field (bits 1:0) is programmed to 10b (Level 2)), this bit shall be set to 1, and cleared in all other cases • If all four voltage swing levels are supported (VOLTAGE_SWING_SET field (bits 1:0) is programmed to 11b (Level 3)), this bit shall be set to 1, and cleared in all other cases	
		4:3	**PRE-EMPHASIS_SET** 00b = Pre-emphasis Level 0. 10b = Pre-emphasis Level 2. 01b = Pre-emphasis Level 1. 11b = Pre-emphasis Level 3.	
		5	**MAX_PRE-EMPHASIS_REACHED** Transmitter shall support at least three levels of pre-emphasis (Levels 0, 1, and 2). May also support Pre-emphasis Level 3. May support independent pre-emphasis level control for each lane. • If only three pre-emphasis levels are supported (transmitter programmed PRE-EMPHASIS_SET field (bits 4:3) to 10b (Level 2)), the transmitter shall set this bit to 1 to indicate to the receiver that the maximum pre-emphasis level has been reached, and clear this bit in all other cases • If all four pre-emphasis levels are supported (transmitter programmed PRE-EMPHASIS_SET field (bits 4:3) to 11b (Level 3)), the transmitter shall set this bit to 1 to indicate to the receiver that the maximum pre-emphasis level has been reached, and clear this bit in all other cases	
		7:6	**RESERVED**	Read all 0s

Table 2-184: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link Configuration Field	
00103h	**128b/132b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 02h)** New to *DP v2.0*. See Section 3.5.5.3 for details.			Write/Read
		3:0	**TX_FFE_PRESET_VALUE**	
		7:4	**RESERVED**	Read all 0s
00104h	**TRAINING_LANE1_SET** Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs. Bit definition is identical to the TRAINING_LANE0_SET register (DPCD Address 00103h), but for Lane 1.			Write/Read
00105h	**TRAINING_LANE2_SET** Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs. Bit definition is identical to the TRAINING_LANE0_SET register (DPCD Address 00103h), but for Lane 2.			Write/Read
00106h	**TRAINING_LANE3_SET** Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs. Bit definition is identical to the TRAINING_LANE0_SET register (DPCD Address 00103h), but for Lane 3.			Write/Read

Table 2-184: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link Configuration Field	
00107h	**DOWNSPREAD_CTRL** Down-spreading control. Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs.			Write/Read
		3:0	**RESERVED**	Read all 0s
		4	**SPREAD_AMP** Spreading amplitude. Enables the Spread-Spectrum Clock (SSC) when the MAX_DOWNSPREAD bit in the MAX_DOWNSPREAD register(s) (DPCD Address(es) 00003h and 02203h, bit 0) is set to 1. 0 = Main-Link signal is not down spread (SSC is disabled.). 1 = Main-Link signal is down spread by 0.5% or less with a modulation frequency within the range of 30 to 33kHz (SSC is enabled).	Write/Read
		6:5	**RESERVED**	Read all 0s
		7	**MSA_TIMING_PAR_IGNORE_EN** 0 = Source device transmits valid data for MSA timing parameters HTotal[15:0], HStart[15:0], HSyncPolarity[0] (HSP), HSyncWidth[14:0] (HSW), VTotal[15:0], VStart[15:0], VSyncPolarity[0] (VSP), and VSyncWidth[14:0] (VSW). 1 = Source device may transmit invalid data for the above-mentioned MSA timing parameters. The Sink device shall ignore these parameters and regenerate the incoming video stream without depending on these parameters. (This bit can be set to 1 only when the MSA_TIMING_PAR_IGNORED bit in the DOWN_STREAM_PORT_COUNT register (DPCD Address 00007h, bit 6) is set to 1.)	Write/Read
00108h	**MAIN_LINK_CHANNEL_CODING_SET** Updated in *DP v2.0*. The DPRX shall revert to 8b/10b Link Layer when a power-on reset or upstream device disconnect occurs. 01h = 8b/10b Link Layer (default value when a power-on reset or upstream device disconnect occurs). 02h = 128b/132b Link Layer. All other values are RESERVED.			Write/Read

Table 2-184: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link Configuration Field	
00109h	**I^2C Speed Control/Status Bit Map** Shall be programmed to the default I^2C bit rate of the downstream device which is an implementation-specific choice.			Write/Read
		7:0	If the I^2C Speed Control Capabilities Bit Map register (DPCD Address 0000Ch) is cleared to 00h (indicating that the DPRX does not implement a physical I^2C bus or does not support I^2C speed control), a write to this register is ignored and a read returns 00h. Otherwise, bit values in this register are assigned to I^2C speeds. 01h = 1Kbps. 10h = 400Kbps. 02h = 5Kbps. 20h = 1Mbps. 04h = 10Kbps. 40h = RESERVED. 08h = 100Kbps. 80h = RESERVED. On a read, the DPRX returns a value with exactly one bit set to indicate the speed currently in use. On a write, software provides a mask to limit the speeds to be enabled. The DPRX shall use the slowest enabled speed. ***Note:*** *Software can select slowest capable speed by writing FFh.* If the result of the mask with the speed capabilities is 00h, the DPRX selects the speed to be used according to an implementation-specific algorithm.	
0010Ah	**eDP_CONFIGURATION_SET** Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs.			Read all 0s
	For non-eDP Sinks			
		7:0	**RESERVED**	
	For eDP Sinks			Write/Read
		0	**ALTERNATE_SCRAMBLER_RESET_ENABLE** See *eDP Standard*.	
		1	**RESERVED** (Deprecated FRAMING_CHANGE option for eDP.)	Read all 0s
		6:2	**RESERVED**	
		7	**PANEL_SELF_TEST_ENABLE** Source device sets this bit to 1 to enable optional LCD Panel Self Test, as specified in *eDP Standard*. Power-on default value = 0. For test mode use only. Changing the value of this bit while the link is active may produce unpredictable results.	Write/Read

Table 2-184: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link Configuration Field	
0010Bh	**LINK_QUAL_LANE0_SET** For DPCD r1.2 and higher. Updated in *DP v2.0*. Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs. The controls in this register supersede the LINK_QUAL_PATTERN_SET controls in the TRAINING_PATTERN_SET register (DPCD Address 00102h).			Write/Read
		6:0	**LINK_QUAL_PATTERN_SET** Indicates which Link Quality test pattern is transmitted. Values not listed are RESERVED. 00h = None. 03h = PRBS7, as defined in Appendix N (UHBR*x* bit rates) and Table 1-2 (HBR*x* bit rates). **HBR3, HBR2, HBR, and RBR bit rates:** 01h = D10.2 (unscrambled; same as Link TPS1). 02h = Symbol Error Rate Measurement pattern. 04h = 80-bit custom pattern. 05h = CP2520 Pattern 1. 06h = CP2520 Pattern 2. 07h = CP2520 Pattern 3 (which is TPS4). **UHBR10, UHBR13.5, and UHBR20 bit rates:** 08h = 128b/132b_TPS1 test pattern (Nyquist), as defined by Table 3-26. 10h = 128b/132b_TPS2 test pattern, as defined by Table 3-26. 18h = PRBS9, as defined in Appendix N. 20h = PRBS11, as defined in Appendix N. 28h = PRBS15, as defined in Appendix N. 30h = PRBS23, as defined in Appendix N. 38h = PRBS31, as defined in Appendix N. 40h = 264-bit custom pattern (DPCD Addresses 02230h through 02250h). 48h = SQ*num* – Square pattern of *num* 1s, followed by *num* 0s, as prewritten by the LINK_SQUARE_PATTERN_num + 1 register (DPCD Address 0010Fh) (needs to be written in advance, –or– by a single burst).	
		7	**RESERVED**	Read 0

Table 2-184: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link Configuration Field	
0010Ch	**LINK_QUAL_LANE1_SET** For DPCD r1.2 and higher. Updated in *DP v2.0*. Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs. Bit definition is identical to the LINK_QUAL_LANE0_SET register (DPCD Address 0010Bh), but for Lane 1.			Write/Read
0010Dh	**LINK_QUAL_LANE2_SET** For DPCD r1.2 and higher. Updated in *DP v2.0*. Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs. Bit definition is identical to the LINK_QUAL_LANE0_SET register (DPCD Address 0010Bh), but for Lane 2.			Write/Read
0010Eh	**LINK_QUAL_LANE3_SET** For DPCD r1.2 and higher. Updated in *DP v2.0*. Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs. Bit definition is identical to the LINK_QUAL_LANE0_SET register (DPCD Address 0010Bh), but for Lane 3.			Write/Read
0010Fh	**LINK_SQUARE_PATTERN_*num* + 1** New to *DP v2.0*. Valid only for UHBR bit rates. Use for all lanes that are programmed for a Square pattern (value of 48h) by the Lane's LINK_QUAL_PATTERN_SET field in the LINK_QUAL_LANE*x*_SET register(s) (DPCD Address(es) 0010Bh through 0010Eh, bits 6:0). Needs to be written in advance, –or– by a single burst. Defines the number of consecutive 1s (which is the same as the number of consecutive 0s), up to 256 1s followed by 256 0s (by defining that the 00h value indicates a "1010…" pattern). For example: 00h = Pattern is 101010101010…. 01h = Pattern is 110011001100…. 02h = Pattern is 111000111000…. 03h = Pattern is 1111000011110000…. 04h = Pattern is 11111000001111100000…. … FFh = 256 1s followed by 256 0s.			Write/Read
00110h	**RESERVED** (Deprecated Post Cursor2-related register.)			Read all 0s

Table 2-184: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link Configuration Field	
00111h	**MSTM_CTRL** Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs. Takes effect only when the MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0) is set to 1.			Write/Read
		0	**MST_EN** 0 = UFP shall transmit audio/visual data in Single-Stream Transport (SST) mode. 1 = UFP shall transmit audio/visual data in Multi-Stream Transport (MST) mode. The upstream device shall not change the value of this bit while transmitting Audio/Video data and the behavior of the receiving port in these circumstances is implementation-specific. A Multi-Stream-capable Sink, when rendering a single stream, may be configured into either SST or MST mode. The decision of which mode to use is up to the Source Stream Policy Maker or upstream Branch device. MST mode is forwarded by the Branching Unit of a downstream device to further downstream only when the DPTX sets the UP_REQ_EN bit (bit 1) to 1 to enable Message Transactions. It is because the MST transmission shall always be preceded by Message Transactions for Topology Management and Virtual Channel establishment.	
		1	**UP_REQ_EN** 0 = Prohibits the Downstream DPRX from originating/forwarding an UP_REQ message transaction. 1 = Allows the Downstream DPRX to originating/forwarding an UP_REQ message transaction. The DPTX may set this bit to 1 without setting the MST_EN bit (bit 0), to transmit in SST mode while playing the role of Topology Manager and Source Payload Bandwidth Manager. The DPTX may set this bit only when the Downstream DPRX has its MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0) set to 1. Setting this bit has no effect when the MST_CAP bit is cleared to 0. The DPTX shall set this bit to 1 before initiating a down request message.	
		2	**UPSTREAM_IS_SRC** 0 = Upstream device is either a Source device that predates *DP v1.2* –or– a Branch device. 1 = Set to 1 by a DP Source device to indicate to the downstream device the presence of a Source device, not a Branch device.	
		7:3	**RESERVED**	Read all 0s

Table 2-184: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link Configuration Field	
00112h through 00114h	**AUDIO_DELAY** Additional delay in 1-us granularity that is to be inserted by a Sink device. The Source device shall **not** program values that exceed the Sink device delay insertion capability reported in the AUD_DEL_INS7:0, AUD_DEL_INS15:8, and AUD_DEL_INS23:16 fields in the AV_SYNC_DATA_BLOCK register (DPCD Addresses 0002Bh through 0002Dh, respectively). Power reset default 0. Writing the audio delay value to the AUDIO_DELAY register may not have an effect when the Sink device's AV_SYNC_CAP bit in the DPRX_FEATURE_ENUMERATION_LIST register (DPCD Address 02210h, bit 2) is cleared to 0.			Write/Read
	0	7:0	**AUDIO_DELAY7:0** Shall be cleared to 00h upon power-on reset or an upstream device disconnect.	
	1	7:0	**AUDIO_DELAY15:8** Shall be cleared to 00h upon power-on reset or an upstream device disconnect.	
	2	7:0	**AUDIO_DELAY23:16** Shall be cleared to 00h upon power-on reset or an upstream device disconnect.	
00115h	**LINK_RATE_SET and TX_GTC_CAPABILITY** Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs.			Write/Read
		2:0	**LINK_RATE_SET** See *eDP Standard*.	
		3	**TX_GTC_CAP** 0 = DPTX does not have the GTC capability. 1 = DPTX has the GTC capability.	
		4	**TX_GTC_SLAVE_CAP** 0 = DPTX cannot operate as a GTC Slave. 1 = DPTX can operate as a GTC Slave.	
		7:5	**RESERVED**	Read all 0s
00116h	**For DPCD r1.3 (*eDP v1.4* DPRX) only; otherwise, RESERVED**			
	RECEIVER ADVANCED LINK POWER MANAGEMENT CONFIGURATION See *eDP v1.4*.			
00117h	**For DPCD r1.3 (*eDP v1.4* DPRX) only; otherwise, RESERVED**			
	SINK DEVICE AUX_FRAME_SYNC CONFIGURATION See *eDP v1.4*.			

Table 2-184: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link Configuration Field	
00118h	**UPSTREAM_DEVICE_DP_PWR_NEED** Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs.			Write/Read
		0	**DP_PWR_NOT_NEEDED_BY_UPSTREAM_DEVICE** 0 = Upstream device needs DP_PWR provided by a DPRX through DP_PWR connector pin for operation. 1 = Upstream device does not need DP_PWR provided by a DPRX through DP_PWR connector pin for operation. The DPRX with Source Detect capability may disable DP_PWR. The DPRX shall re-enable DP_PWR upon Source Detect event.	
		7:1	**RESERVED**	Read all 0s
00119h	**EXTENDED_DPRX_SLEEP_WAKE_TIMEOUT_GRANT** Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs.			Write/Read
		0	**DPRX_SLEEP_WAKE_TIMEOUT_PERIOD_GRANTED** 0 = Upstream DP device has not granted the extended wake timeout period. 1 = Upstream DP device has granted the wake timeout period requested by a downstream DP device at the EXTENDED_DPRX_SLEEP_WAKE_TIMEOUT_REQUEST register (DPCD Address 02211h).	
		7:1	**RESERVED**	Read all 0s
0011Ah through 0011Fh	**RESERVED**			Read all 0s

Table 2-184: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link Configuration Field	
00120h	**FEC_CONFIGURATION** New to *DP v1.4*. Updated in *DP v2.0*.			Read/Write (Cleared to 00h when a power-on reset or upstream device disconnect occurs)
		0	**FEC_READY** Valid only for 8b/10b channel coding. Don't care for 128b/132b channel coding. 0 = Not ready. A DP Source device shall set this bit to 1 and initiate and complete link training before starting FEC encoding. 1 = Ready. A DP Source may start FEC encoding without having to re-initiate link training. To enable FEC, the DPTX shall set this bit to 1 before the start of link training. To disable FEC, the DPTX shall clear this bit to 0 before the start of link training. When the DPTX wants to change the state of this bit, the DPTX shall initiate a new link training sequence.	
		3:1	**FEC_ERROR_COUNT_SEL** Set by the DPTX to select which error counter type is to be accessible through the FEC_ERROR_COUNT register (DPCD Addresses 00281h and 00282h). See Section 3.5.3.3 for further details. 000b = FEC_ERROR_COUNT_DIS. 001b = UNCORRECTED_BLOCK_ERROR_COUNT. 010b = CORRECTED_BLOCK_ERROR_COUNT. 011b = CORRECTED_BIT_ERROR_COUNT. 100b = PARITY_BLOCK_ERROR_COUNT. 101b = PARITY_BIT_ERROR_COUNT. All other values are RESERVED.	

Table 2-184: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link Configuration Field	
00120h		5:4	**LANE_DEC_SELECT** Set by the DPTX to select which lane or decoder's counter is to be accessible through the FEC_ERROR_COUNT register (DPCD Addresses 00281h and 00282h). Lane indication is ignored when the AGGREGATED_ENABLED_LANES_ERRORS bit (bit 6) is set to 1. See Section 3.5.3.3 for further details. 00b = Lane/Decoder 0. 10b = Lane/Decoder 2. 01b = Lane/Decoder 1. 11b = Lane/Decoder 3.	Read/Write (Cleared to 00h when a power-on reset or upstream device disconnect occurs)
		6	**AGGREGATED_ENABLED_LANES_ERRORS** New to *DP v2.0*. See Section 3.5.3.3 for further details. Valid when the AGGREGATED_ERROR_COUNTERS_CAPABLE bit in the FEC_CAPABILITY_1 register (DPCD Address 00091h, bit 0) is set to 1. 0 = Not enabled. LANE_DEC_SELECT field (bits 5:4) indicates the reported lane. 1 = Enabled. Errors reported in the FEC_ERROR_COUNT register (DPCD Addresses 00281h and 00282h) are of the type selected by the FEC_ERROR_COUNT_SEL field (bits 3:1). The reported value is aggregated across all enabled lanes. The LANE_DEC_SELECT field is ignored.	
		7	**PRECODING_DISABLE** New to *DP v2.0*. Valid only for 128b/132b channel coding. RESERVED for 8b/10b channel coding. 0 = Pre-coding is enabled (default). 1 = Pre-coding is disabled. Pre-coding is disabled during link training, regardless of this bit's state. To disable pre-coding, the DPTX shall set this bit to 1 before the start of link training. When the DPTX wants to change the state of this bit, the DPTX shall initiate a new link training sequence. Pre-coding is enabled for normal operation after link training.	
00121h through 00125h	**RESERVED** (Deprecated FAUX-related registers.)			Read all 0s
00126h through 00153h	**RESERVED**			Read all 0s

Table 2-184: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link Configuration Field	
00154h through 00157h	**TX_GTC_VALUE** Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs.			Write/Read
	0	7:0	**TX_GTC_VALUE7:0**	
	1	7:0	**TX_GTC_VALUE15:8**	
	2	7:0	**TX_GTC_VALUE23:16**	
	3	7:0	**TX_GTC_VALUE31:24**	
00158h	**RX_GTC_VALUE_PHASE_SKEW_EN** Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs.			Write/Read
		0	**RX_GTC_VALUE_PHASE_SKEW_EN** 0 = DPRX resets its GTC value to the received TX_GTC_VALUE register (DPCD Addresses 00154h through 00157h) value and uses the delta between its GTC value and the received TX_GTC_VALUE register value to frequency adjust its GTC value. 1 = DPRX resets its GTC value to the received TX_GTC_VALUE register value, but does **not** use the delta between its GTC value and the received TX_GTC_VALUE register value to frequency adjust its GTC value. In other words, the TX_GTC_VALUE register value is used only for GTC value phase adjust. Used only when the DPTX is the GTC Master.	
		7:1	**RESERVED**	Read all 0s
00159h	**TX_GTC_FREQ_LOCK_DONE** Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs.			Write/Read
		0	**TX_GTC_FREQ_LOCK_DONE** 0 = **DPTX** has not achieved GTC_FREQ_LOCK_DONE. 1 = **DPTX** has achieved GTC_FREQ_LOCK_DONE. Used only when the DPRX is the GTC Master.	
		7:1	**RESERVED**	Read all 0s
0015Ah and 0015Bh	**TX_GTC_PHASE_SKEW_OFFSET** Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs.			Write/Read
	0		**TX_GTC_PHASE_SKEW_OFFSET7:0**	
	1		**TX_GTC_PHASE_SKEW_OFFSET15:8**	
0015Ch through 0015Fh	**For DPCD r1.3 (*eDP v1.4* DPRX) only; otherwise, RESERVED**			
	AUX_FRAME_SYNC VALUE See *eDP v1.4*.			

Table 2-184: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link Configuration Field	
00160h	**For eDP Compression-related Function for DPCD r1.3 (*eDP v1.4* DPRX); RESERVED for DPCD r1.2 (and lower); RESERVED for DPCD r1.4 when used with *DP v1.3***			
00160h	**For DPCD r1.4 when used with *DP v1.4* (and higher)**			Read/Write
	DSC ENABLE New to *DP v1.4*. Available in UFP and virtual DPCD registers. 0 = Not enabled. 1 = Enabled.			
		0	**DSC Enable**	
		1	**DSC Pass-through Enable** New to *DP v2.0*.	
		7:2	**RESERVED**	Read all 0s
00161h	**For eDP Compression-related Function for DPCD r1.3 (*eDP v1.4* DPRX); RESERVED for DPCD r1.3 (and lower); RESERVED for DPCD r1.4 when used with *DP v1.4a* (and lower)**			
00161h	**For DPCD r1.4, *DP v2.0* (and higher)**			Read/Write
	DSC CONFIGURATION New to *DP v2.0*. Available only in the virtual DPCD register of a virtual DP peer device. 0 = Not enabled. 1 = Enabled.			
		0	**DSC Decoder 0 Enable**	
		1	**DSC Decoder 1 Enable**	
		2	**DSC Decoder 2 Enable**	
		3	**DSC Decoder 3 Enable**	
		4	**DSC Decoder 4 Enable**	
		5	**DSC Decoder 5 Enable**	
		6	**DSC Decoder 6 Enable**	
		7	**DSC Decoder 7 Enable**	
00162h through 0016Fh	**For DPCD r1.3 (*eDP v1.4* DPRX) only; otherwise, RESERVED**			
	RESERVED for future eDP Compression-related functions			
00170h	**For DPCD r1.3 (*eDP v1.4* DPRX) only; otherwise, RESERVED**			
	PANEL SELF REFRESH ENABLE AND CONFIGURATION See *eDP v1.4*			

Table 2-184: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link Configuration Field	
00171h through 0019Fh	**RESERVED**			Read all 0s
001A0h	**ADAPTER_CTRL** Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs. Control of Branch devices that adapt to legacy video transports. Takes effect only when the ADAPTER_CAP register (DPCD Address 0000Fh) is programmed to 3h.			Write/Read
		0	**FORCE_LOAD_SENSE** Prompts the DP-to-Legacy Converter device to sense the presence of a legacy Sink device.	
		7:1	**RESERVED**	Read all 0s
001A1h	**BRANCH_DEVICE_CTRL** Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs.			Write/Read
		0	**Hot Plug/Hot Unplug Event Notification Type** 0 = HPD long pulse is used for upstream notification (default). 1 = IRQ_HPD is used for upstream notification. The Source device shall set this bit to 1 to enable the Branch device to use IRQ_HPD for upstream notification of a downstream plug/unplug event if the UP_REQ_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 1) is cleared to 0. If the Branch device's UP_REQ_EN bit is set to 1, the Plug/Unplug Event Notification Type control bit is "don't care" (CONNECTION_STATUS_NOTIFY messages are used). HDCP-enabled devices, see *HDCP Specification* for additional information related to plug/unplug event handling.	
		7:1	**RESERVED**	Read all 0s
001A2h through 001AFh	**RESERVED**			Read all 0s

Table 2-184: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link Configuration Field	
001B0h	**PANEL REPLAY ENABLE AND CONFIGURATION** New to *DP v2.0*.			Read/Write
		0	**Source Device Enables Panel Replay Mode in Sink Device** 0 = Disable (default). 1 = Enable. A DP Sink device shall honor the VSC SDP's PR fields. Setting this bit does not automatically force the DP Sink device into a PR active state.	
		2:1	**RESERVED**	Read all 0s
		3	**IRQ_HPD with VSC SDP for PR Unrecoverable Error** 0 = Do not generate an IRQ_HPD when there is a VSC SDP for PR unrecoverable error (default). 1 = Generate an IRQ_HPD after finding a VSC SDP for PR unrecoverable error.	Read/Write
		4	**IRQ_HPD with RFB Storage Errors** 0 = Do not generate an IRQ_HPD when there is an RFB Storage error (default). 1 = Generate an IRQ_HPD after finding an RFB Storage error.	
		5	**IRQ_HPD with Active Frame CRC Errors** 0 = Do not generate an IRQ_HPD when there is an active frame CRC mismatch (default). 1 = Generate an IRQ_HPD after finding an active frame CRC mismatch.	
		6	**Selective Update Enable** 0 = Disable Selective Update (default). 1 = Enable Selective Update.	
		7	**RESERVED**	Read 0
001B1h through 001BFh	**RESERVED**			Read all 0s

Table 2-184: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link Configuration Field	
001C0h	**PAYLOAD_ALLOCATE_SET** Updated in *DP v2.0*. Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs. Writing 00h, 00h, and 3Fh to DPCD Addresses 001C0h, 001C1h, and 001C2h, respectively, clears the entire VC Payload ID table. When this occurs, the DPRX immediately ignores the incoming VC Payloads (if any) without waiting or ACT on the Main-Link. Takes effect only when the MST_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 0) is set to 1, –or– the MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 02h for 128b/132b channel coding.			Write/Read
		6:0	**VC Payload ID to Be Allocated** ID of 0 indicates that the time slots are unallocated.	
		7	**RESERVED**	Read 0
001C1h	**PAYLOAD_ALLOCATE_START_TIME_SLOT** Updated in *DP v2.0*. Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs. Takes effect only when the MST_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 0) is set to 1, –or– the MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 02h for 128b/132b channel coding.			Write/Read
		5:0	**Starting Time Slot of VC Payload ID in DPCD Address 002C0h**	
		7:6	**RESERVED**	Read all 0s
001C2h	**PAYLOAD_ALLOCATE_TIME_SLOT_COUNT** Updated in *DP v2.0*. Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs. Takes effect only when the MST_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 0) is set to 1, –or– the MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 02h for 128b/132b channel coding.			Write/Read
		6:0	**Time Slot Count of VC Payload ID in DPCD Address 002C0h**	
		7	**RESERVED**	Read all 0s
001C3h through 001FFh	**RESERVED**			Read all 0s

For details regarding how to clear the error counters, and how to read the error counters through the FEC_ERROR_COUNT register (DPCD Addresses 00281h and 00282h), see Section 3.5.3.3.

Table 2-185: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link/Sink Device Status Field	
Note: *A DPCD r1.2 (or higher) DPRX shall have the same Link/Sink Device Status field registers at DPCD Addresses 00200h through 00205h to the corresponding DPRX Event Status Indicator registers at DPCD Addresses 02002h through 0200Fh, as listed below. The Clearable/Read Only bit is cleared in both address ranges when an upstream device clears the bit within one of the ranges.* • *DPCD Addresses 00200h and 02002h* • *DPCD Addresses 00201h and 02003h* • *DPCD Addresses 00202h and 0200Ch* • *DPCD Addresses 00203h and 0200Dh* • *DPCD Addresses 00204h and 0200Eh* • *DPCD Addresses 00205h and 0200Fh*				
00200h (and 02002h)	**SINK_COUNT** Sink device count.			Read Only
		7, 5:0	**SINK_COUNT** Total number of stream sinks within this Sink device and those connected to the DFPs of this device. ***Note:*** *A Branch device shall add up the Rendering function counts read from all its DFPs. The Sink device shall increase the count by one if it also has a local Rendering function.*	
		6	**CP_READY** Set to 1 when all the Sink devices (local Sink device and those connected to its DFPs) are CP-capable. Set at the conclusion of Content Protection Authentication, as needed, by the appropriate Content Protection specification. ***Notes:*** *The Source device shall transmit content that needs content protection only when all the Branch and Sink devices in the link are CP-ready except for Repeater devices. (A Repeater device shall not be required to perform a decryption/encryption operation, and therefore shall not be required to be CP-ready.)* *HDCP does* ***not*** *use this bit.*	

Table 2-185: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link/Sink Device Status Field	
00201h (and 02003h)	**DEVICE_SERVICE_IRQ_VECTOR**			Write 1 to Clear/Read The Sink clears each bit when the Source writes 1 to the specific bit position by way of an AUX_CH write transaction. The Source may write 1 in multiple bit positions in a single transaction.
		0	**RESERVED (FOR FUTURE)** **REMOTE_CONTROL_COMMAND_PENDING** For DP devices that support Sideband MSG handling (MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0) is set to 1), a Sink device event (e.g., a remote control command pending) shall be handled as a message transaction.	
	Bit 1 definition is DPCD revision-dependent. **For DPCD r1.0 through DPCD r1.2 and DPCD r1.4 (Bit 1)**			
		1	**AUTOMATED_TEST_REQUEST** 1 = Source device shall read DPCD Addresses 00218h through 002BFh for the requested link test.	
	Definitions of Bits 7:2 are not DPCD revision-dependent			Write 1 to Clear/Read The Sink clears each bit when the Source writes 1 to the specific bit position by way of an AUX_CH write transaction. The Source may write 1 in multiple bit positions in a single transaction.
		2	**CP_IRQ** Used by an optional content protection system.	
		3	**MCCS_IRQ** Used by an optional MCCS system within the Sink device.	
		4	**DOWN_REP_MSG_RDY** 1 = Source device shall read the DOWN_REP_MSG from the DOWN_REP_MSG DPCD locations and process the Sideband MSG.	
		5	**UP_REQ_MSG_RDY** 1 = Source device shall read the UP_REQ_MSG from the UP_REQ_MSG DPCD locations and process the Sideband MSG.	
		6	**SINK_SPECIFIC_IRQ** Usage is vendor-specific.	
		7	**RESERVED**	Read 0

Table 2-185: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link/Sink Device Status Field	
00202h (and 0200Ch)	**LANE0_1_STATUS** Lane 0 and Lane 1 Status.			Read Only
		0	**LANE0_CR_DONE**	
		1	**LANE0_CHANNEL_EQ_DONE**	
		2	**LANE0_SYMBOL_LOCKED**	
		3	**RESERVED**	Read 0
		4	**LANE1_CR_DONE**	Read Only
		5	**LANE1_CHANNEL_EQ_DONE**	
		6	**LANE1_SYMBOL_LOCKED**	
		7	**RESERVED**	Read 0
00203h (and 0200Dh)	**LANE2_3_STATUS** Bit definition is identical to the LANE0_1_STATUS register (DPCD Address 00202h), but for Lanes 2 and 3.			Read Only
00204h (and 0200Eh)	**LANE_ALIGN_STATUS_UPDATED**			Read Only
		0	**INTERLANE_ALIGN_DONE**	
		1	**POST_LT_ADJ_REQ_IN_PROGRESS** Valid only for 8b/10b Link Layer. "Don't care" for 128b/132b Link Layer. Valid only for a DPRX that sets the POST_LT_ADJ_REQ_SUPPORTED bit in the MAX_LANE_COUNT register (DPCD Address 00002h, bit 5) and after a DPTX grants the procedure by setting the POST_LT_ADJ_REQ_GRANTED bit in the LANE_COUNT_SET register (DPCD Address 00101h, bit 5) to 1. 1 = DPRX is conducting the POST_LT_ADJ_REQ sequence.	
		5:2	**RESERVED**	Read all 0s
		6	**DOWNSTREAM_PORT_STATUS_CHANGED** Set in a Branch device when it detects a change in the connection status of any of its DFPs.	Read Only
		7	**LINK_STATUS_UPDATED** Link Status and Adjust Request updated since the last read. Set when updated and cleared after read.	

Table 2-185: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link/Sink Device Status Field	
00205h (and 0200Fh)	**SINK_STATUS** The Sink device shall set bits 1:0 as soon as it determines that the corresponding received stream is properly regenerated and within the supported stream format range. The Sink device shall clear bits 1:0 as soon as it determines that the corresponding received stream is no longer being properly regenerated or within the supported stream format range.			Read Only
		0	**RECEIVE_PORT_0_STATUS** 0 = Sink device is out of synchronization. 1 = Sink device is in synchronization.	
		1	**RECEIVE_PORT_1_STATUS** 0 = Sink device is out of synchronization. 1 = Sink device is in synchronization.	
		2	**STREAM_REGENERATION_STATUS** New to *DP v2.0*. Valid when the STREAM_REGENERATION_STATUS_CAPABILITY bit in the MAX_DOWNSPREAD registers (DPCD Addresses 00003h and 02203h, bit 1) is set to 1. 0 = Stream is not being regenerated. 1 = Stream is being regenerated and is ready to be displayed on a screen. The DPRX should update this bit within 10ms to reflect the current state of stream regeneration. ***Note:*** *For a Sink device, this means that the frame appears on a screen. For a Branch device, this means that transmission on the downstream DPTX has started. For an MST Branch device, this means that a first transmission to a DFP has started. If the Sink and MST Branch devices are located within the same enclosure, this can mean that the frame appears on a screen event.*	
		7:3	**RESERVED**	Read all 0s

Table 2-185: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link/Sink Device Status Field	
00206h	**ADJUST_REQUEST_LANE0_1**			Read Only
	8b/10b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 01h)			
	Voltage Swing and Equalization Setting Adjust Request (ADJ_REQ) for Lanes 0 and 1. When this register is read and found to have changed from a previous read, both during link training (including the POST_LT_ADJ_REQ sequence) and automated PHY Layer testing, the DPTX shall write the voltage swing and pre-emphasis level requested by this register to the TRAINING_LANE*x*_SET register(s) (DPCD Address(es) 00103h through 00106h).			
		1:0	**VOLTAGE_SWING_LANE0** 00b = Level 0. 10b = Level 2. 01b = Level 1. 11b = Level 3.	
		3:2	**PRE_EMPHASIS_LANE0** 00b = Level 0. 10b = Level 2. 01b = Level 1. 11b = Level 3.	
		5:4	**VOLTAGE_SWING_LANE1** 00b = Level 0. 10b = Level 2. 01b = Level 1. 11b = Level 3.	
		7:6	**PRE_EMPHASIS_LANE1** 00b = Level 0. 10b = Level 2. 01b = Level 1. 11b = Level 3.	
	128b/132b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 02h) New to *DP v2.0*. See Section 3.5.5.3 for details.			
		3:0	**TX_FFE_PRESET_VALUE_LANE0**	
		7:4	**TX_FFE_PRESET_VALUE_LANE1**	
00207h	**ADJUST_REQUEST_LANE2_3** Bit definition is identical to the ADJUST_REQUEST_LANE0_1 register (DPCD Address 00206h), but for Lanes 2 and 3.			Read Only
00208h	**TRAINING_SCORE_LANE0** Usage is Sink device implementation-specific.			Read Only
00209h	**TRAINING_SCORE_LANE1** Usage is Sink device implementation-specific.			Read Only
0020Ah	**TRAINING_SCORE_LANE2** Usage is Sink device implementation-specific.			Read Only
0020Bh	**TRAINING_SCORE_LANE3** Usage is Sink device implementation-specific.			Read Only

Table 2-185: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link/Sink Device Status Field	
0020Ch	**RESERVED** (Deprecated Post Cursor2-related register.)			Read all 0s
0020Dh and 0020Eh	**RESERVED** (Deprecated FAUX-related register.)			Read all 0s
0020Fh (and 02011h)	**For DPCD r1.4 when used with *DP v1.4* (and higher)**			Read/Write
	DSC STATUS New to *DP v1.4*.			
		0	**RC Buffer Under-run** 0 = No error. 1 = Buffer under-run. Sticky until cleared by a write of 1.	
		1	**RC Buffer Overflow** 0 = No error. 1 = Buffer overflow. Sticky until cleared by a write of 1.	
		2	**Chunk Length Error** 0 = No error. 1 = Chunk Length error. Sticky until cleared by a write of 1.	
		7:3	**RESERVED**	Read all 0s

Table 2-185: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link/Sink Device Status Field	
00210h and 00211h	**SYMBOL_ERROR_COUNT_LANE0** Updated in *DP v2.0*. **HBR*x* and RBR bit rates** • **Symbol Error Rate Measurement (repetition of scrambled 00h before 8b/10b encoding)** – Measures the number of mismatched symbols • **PRBS7 pattern** – Measures the number of mismatched bits • **CP2520 (HBR2 Compliance EYE pattern; repetition of scrambled 00h before 8b/10b encoding)** – Measures the number of mismatched symbols • **No test pattern is being transmitted (normal operation)** – Measures the number of illegal symbols or disparity errors as controlled by the SYMBOL_ERROR_COUNT_SEL field in the TRAINING_PATTERN_SET register (DPCD Address 00102h, bits 7:6) • **Symbol error count exceeds $2^{15} - 1$ (= 32767)** – Register value shall be held at $2^{15} - 1$ instead of wrapping around **UHBR*x* bit rates** • **128b/132b_TPS2 pattern** – Measures the mismatched symbols • **PRBS7, PRBS9, PRBS11, PRBS15, PRBS23, or PRBS31 patterns** – Measures the mismatched bits • **SQ*num* pattern**– Measures the mismatched symbols (specific SQ is a symbol) • **No test pattern for 128b/132 (assume there is nothing else to measure on 128b/132b normal operation)** – Counts the number of PHY_SYNC_ONLY or POST_LT_SCRAMBLER_RESET that are not sensed on expected timing			Read Only
	0	7:0	**SYMBOL_ERROR_COUNT_LANE0_7:0** Least significant eight bits of Lane 0's 15-bit symbol error count. Shall be cleared on an AUX_CH read by the transmitter.	
	1	6:0	**SYMBOL_ERROR_COUNT_LANE0_14:8** Most significant seven bits of Lane 0's 15-bit symbol error count. Shall be cleared on an AUX_CH read by the transmitter.	
		7	**SYMBOL_ERROR_COUNT_LANE0_VALID** 0 = Not valid. 1 = Valid.	
00212h and 00213h	**SYMBOL_ERROR_COUNT_LANE1** Updated in *DP v2.0*. Byte and bit definitions are identical to the SYMBOL_ERROR_COUNT_LANE0 register (DPCD Addresses 00210h and 00211h), but for Lane 1.			Read Only

Table 2-185: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link/Sink Device Status Field	
00214h and 00215h	**SYMBOL_ERROR_COUNT_LANE2** Updated in *DP v2.0*. Byte and bit definitions are identical to the SYMBOL_ERROR_COUNT_LANE0 register (DPCD Addresses 00210h and 00211h), but for Lane 2.			Read Only
00216h and 00217h	**SYMBOL_ERROR_COUNT_LANE3** Updated in *DP v2.0*. Byte and bit definitions are identical to the SYMBOL_ERROR_COUNT_LANE0 register (DPCD Addresses 00210h and 00211h), but for Lane 3.			Read Only

Table 2-185: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link/Sink Device Status Field	
Automated Testing Register Set ***Note:*** *DPCD Addresses 00218h through 002BFh comprise the Automated Testing register set. Although use of this register set is* ***optional****, this register set should be supported because the automation facilitates a test process.*				
00218h	**TEST_REQUEST** Updated in *DP v2.0*. Test requested by the Sink device.			Read Only
		0	**TEST_LINK_TRAINING** 0 = No link training test is requested. 1 = Link training test is requested. See the TEST_LINK_RATE register (DPCD Address 00219h) and the TEST_LANE_COUNT field in the TEST_LANE_COUNT register (DPCD Address 00220h, bits 4:0) for the requested link rate and lane count, respectively.	
		1	**TEST_VIDEO_PATTERN_REQUESTED** 0 = No video test pattern is requested. 1 = Video test pattern is requested.	
		2	**TEST_EDID_READ** 0 = No DisplayID or legacy EDID read test is requested. 1 = DisplayID or legacy EDID read test is requested. Checksum of the last DisplayID or legacy EDID block read is written to the TEST_EDID_CHECKSUM register (DPCD Address 00261h). The Source device shall also transmit a color square test pattern.	
		3	**LINK_TEST_PATTERN** 1 = Requests the Link Layer test pattern as specified in the LINK_QUAL_PATTERN_SEL field in the LINK_QUAL_PATTERN_SELECT register (DPCD Address 00248h, bits 6:0).	

Table 2-185: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

<table>
<tr><th>DPCD Address</th><th colspan="4">Register</th><th>Read/ Write over AUX_CH</th></tr>
<tr><th></th><th>Byte #</th><th>Bit #</th><th colspan="3">Definition within Link/Sink Device Status Field</th><th></th></tr>
<tr><td rowspan="11">00218h</td><td></td><td>5:4</td><td colspan="3">PHY_TEST_CHANNEL_CODING_TYPE
00b = 8b/10b.
01b = 128b/132b.</td><td rowspan="11">Read Only</td></tr>
<tr><td></td><td>6</td><td colspan="3">TEST_AUDIO_PATTERN_REQUESTED
New to DP v2.0.
0 = No audio test pattern is requested.
1 = Audio test pattern is requested.
Note: The audio test pattern type, operator-defined or sawtooth pattern, is selected by the TEST_AUDIO_PATTERN_TYPE register (DPCD Address 00272h).</td></tr>
<tr><td></td><td>7</td><td colspan="3">TEST_AUDIO_DISABLED_VIDEO
New to DP v2.0.
0 = Video stream output is requested when the TEST_AUDIO_PATTERN_REQUESTED bit (bit 6) is set to 1.
1 = Video stream output is requested to be disabled during an audio test.
Note: The TEST_VIDEO_PATTERN_REQUESTED bit (bit 1) might be set to 1 along with the TEST_AUDIO_PATTERN_REQUESTED bit (bit 6) and/or this bit. In that case, the device under test shall simultaneously comply with all test automation requests.</td></tr>
<tr><td colspan="3"></td><td>Bit 7</td><td>Bit 6</td><td>Bit 1</td><td>Comments</td></tr>
<tr><td colspan="3"></td><td>0</td><td>0</td><td>0</td><td>No audio or video test is requested.</td></tr>
<tr><td colspan="3"></td><td>0</td><td>0</td><td>1</td><td>Automated video with no audio is requested.</td></tr>
<tr><td colspan="3"></td><td>0</td><td>1</td><td>0</td><td>Automated audio and video test is requested, as defined by the Sink device’s legacy EDID Detailed Timing Descriptor (DTD).</td></tr>
<tr><td colspan="3"></td><td>0</td><td>1</td><td>1</td><td>Automated audio and video test is requested.</td></tr>
<tr><td colspan="3"></td><td>1</td><td>0</td><td>0</td><td>RESERVED</td></tr>
<tr><td colspan="3"></td><td>1</td><td>0</td><td>1</td><td>RESERVED</td></tr>
<tr><td colspan="3"></td><td>1</td><td>1</td><td>0</td><td>Automated audio with no video is requested.</td></tr>
<tr><td colspan="3"></td><td>1</td><td>1</td><td>1</td><td>RESERVED</td></tr>
</table>

Table 2-185: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link/Sink Device Status Field	
00219h	**TEST_LINK_RATE**			Read Only
	For PHY Test 8b/10b channel coding (PHY_TEST_CHANNEL_CODING_TYPE field in the TEST_REQUEST register (DPCD Address 00218h, bits 5:4) is cleared to 00b)			
	06h = 1.62Gbps/lane (RBR). 14h = 5.4Gbps/lane (HBR2). 0Ah = 2.7Gbps/lane (HBR). 1Eh = 8.1Gbps/lane (HBR3). Use of other link rate values for testing are implementation-specific.			
	For PHY Test 128b/132b channel coding (PHY_TEST_CHANNEL_CODING_TYPE field in the TEST_REQUEST register (DPCD Address 00218h, bits 5:4) is programmed to 01b)			
	01h = 10Gbps/lane (UHBR10). 03h = 13.5Gbps/lane (UHBR13.5). 02h = 20Gbps/lane (UHBR20). Use of other link rate values for testing are implementation-specific.			
0021Ah through 0021Fh	**RESERVED**			Read all 0s
00220h	**TEST_LANE_COUNT**			Read Only
		4:0	**TEST_LANE_COUNT** 01h = One lane (Lane 0 only). 02h = Two lanes (Lanes 0 and 1 only). 04h = Four lanes (Lanes 0, 1, 2, and 3). All other values are RESERVED.	
		7:5	**RESERVED**	Read all 0s
00221h	**TEST_VIDEO_PATTERN_TYPE** Updated in *DP v2.0*. Video test pattern requested by the Sink device. 00h = No video test pattern is transmitted. 02h = Black and white vertical lines. 01h = Color ramps. 03h = Color square. All other values are RESERVED.			Read Only
00222h and 00223h	**TEST_H_TOTAL** Horizontal total of transmitted video stream, in pixel count.			Read Only
	0	7:0	**TEST_H_TOTAL15:8**	
	1	7:0	**TEST_H_TOTAL7:0**	
00224h and 00225h	**TEST_V_TOTAL** Vertical total of transmitted video stream, in line count.			Read Only
	0	7:0	**TEST_V_TOTAL15:8**	
	1	7:0	**TEST_V_TOTAL7:0**	

Table 2-185: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link/Sink Device Status Field	
00226h and 00227h	**TEST_H_START** Horizontal active start from HSync start, in pixel count.			Read Only
	0	7:0	**TEST_H_START15:8**	
	1	7:0	**TEST_H_START7:0**	
00228h and 00229h	**TEST_V_START** Vertical active start from VSync start, in line count.			Read Only
	0	7:0	**TEST_V_START15:8**	
	1	7:0	**TEST_V_START7:0**	
0022Ah and 0022Bh	**TEST_HSYNC** HSync polarity and width, in pixel count.			Read Only
	0	6:0	**TEST_HSYNC_WIDTH14:8**	
		7	**TEST_HSYNC_POLARITY**	
	1	7:0	**TEST_HSYNC_WIDTH7:0**	
0022Ch and 0022Dh	**TEST_VSYNC** VSync polarity and width, in line count.			Read Only
	0	6:0	**TEST_VSYNC_WIDTH14:8**	
		7	**TEST_VSYNC_POLARITY**	
	1	7:0	**TEST_VSYNC_WIDTH7:0**	
0022Eh and 0022Fh	**TEST_H_WIDTH** Horizontal active video width, in pixel count (e.g., 400h = 1024 active).			Read Only
	0	7:0	**TEST_H_WIDTH15:8**	
	1	7:0	**TEST_H_WIDTH7:0**	
00230h and 00231h	**TEST_V_HEIGHT** Vertical active video height, in line count (e.g., 300h = 768 active).			Read Only
	0	7:0	**TEST_V_HEIGHT15:8**	
	1	7:0	**TEST_V_HEIGHT7:0**	

Table 2-185: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link/Sink Device Status Field	
00232h and 00233h	**TEST_MISC** ***Note:*** *DPCD Address 00232h, bits 7:0, are the same definition as the MISC0 field in the MSA data (see Table 2-94).*			Read Only
	0	0	**TEST_SYNCHRONOUS_CLOCK** 0 = Link clock and stream clock are asynchronous. 1 = Link clock and stream clock are synchronous.	
		2:1	**TEST_COLOR_FORMAT** 00b = RGB. 10b = YCbCr 4:4:4. 01b = YCbCr 4:2:2. 11b = RESERVED.	
		3	**TEST_DYNAMIC_RANGE** 0 = VESA range (from 0 to the maximum). 1 = CTA range (as defined in *CTA-861-G*, *Section 5*).	
		4	**TEST_YCBCR_COEFFICIENTS** 0 = *ITU-R BT.601*. 1 = *ITU-R BT.709*.	
		7:5	**TEST_BIT_DEPTH** 000b = 6bpc. 011b = 12bpc. 001b = 8bpc. 100b = 16bpc. 010b = 10bpc. All other values are RESERVED.	
	1	0	**TEST_REFRESH_RATE_DENOMINATOR** 0 = 1. 1 = 1.001.	
		1	**TEST_INTERLACED** 0 = Non-interlaced. 1 = Interlaced.	
		7:2	**RESERVED**	Read all 0s
00234h	**TEST_REFRESH_RATE_NUMERATOR** Indicates the refresh rate requested by the Sink device (e.g., 60 = 60-Hz numerator). Refresh rate = TEST_REFRESH_RATE_NUMERATOR / TEST_REFRESH_RATE_DENOMINATOR. (See TEST_REFRESH_RATE_DENOMINATOR bit in the TEST_MISC register (DPCD Address 00233h, bit 0).)			Read Only
00235h through 0023Fh	**RESERVED** For test automation extensions.			Read all 0s

Table 2-185: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link/Sink Device Status Field	
00240h and 00241h	**TEST_CRC_R_Cr** Stores the R or Cr component's 16-bit CRC value. ***Note:*** *This register is also used for CRC reporting as part of the Panel Self Refresh (PSR) specification defined in eDP v1.3 (or higher).*			Read Only
	0	7:0	**CRC_VALUE7:0**	
	1	7:0	**CRC_VALUE15:8**	
00242h and 00243h	**TEST_CRC_G_Y** Stores the G or Y component's 16-bit CRC value. ***Note:*** *This register is also used for CRC reporting as part of the PSR specification defined in eDP v1.3 (or higher).*			Read Only
	0	7:0	**CRC_VALUE7:0**	
	1	7:0	**CRC_VALUE15:8**	
00244h and 00245h	**TEST_CRC_B_Cb** Stores the B or Cb component's 16-bit CRC value. ***Note:*** *This register is also used for CRC reporting as part of the PSR specification defined in eDP v1.3 (or higher).*			Read Only
	0	7:0	**CRC_VALUE7:0**	
	1	7:0	**CRC_VALUE15:8**	
00246h	**TEST_SINK_MISC**			Read Only
		3:0	**TEST_CRC_COUNT** 4-bit wrap counter that increments each time the following TEST_CRC-related registers are updated: • TEST_CRC_R_Cr register (DPCD Addresses 00240h and 00241h) • TEST_CRC_G_Y register (DPCD Addresses 00242h and 00243h) • TEST_CRC_B_Cb register (DPCD Addresses 00244h and 00245h) Reset to 0 when the TEST_SINK_START bit in the TEST_SINK register (DPCD Address 00270h, bit 0) is cleared to 0. ***Note:*** *The TEST_CRC_x registers are updated each frame; however, the CRC result may be unchanged. The counter shall be incremented when a TEST_CRC_x register is updated, regardless of whether the CRC changed.*	
		4	**RESERVED**	Read 0
		5	**TEST_CRC_SUPPORTED** 0 = Sink device does not support CRC. 1 = Sink device supports CRC.	Read Only
		7:6	**RESERVED**	Read all 0s

Table 2-185: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link/Sink Device Status Field	
00247h	**RESERVED** For test automation extensions.			Read all 0s
00248h	**LINK_QUAL_PATTERN_SELECT** Updated in *DP v2.0*.			Read Only
		6:0	**LINK_QUAL_PATTERN_SEL** Indicates which Link Layer test pattern is selected. Values not listed are RESERVED. 00h = None. 03h = PRBS7, as defined in Appendix N (UHBR*x* bit rates) and Table 1-2 (HBR*x* bit rates). **HBR3, HBR2, HBR, and RBR bit rates:** 01h = D10.2 test pattern (unscrambled; same as PHY TPS1). 02h = Symbol Error Rate Measurement pattern. 04h = 80-bit custom pattern. 05h = CP2520 Pattern 1. 06h = CP2520 Pattern 2. 07h = CP2520 Pattern 3 (which is TPS4). **UHBR10, UHBR13.5, and UHBR20 bit rates:** 08h = 128b/132b_TPS1 test pattern (Nyquist), as defined by Table 3-26. 10h = 128b/132b_TPS2 test pattern, as defined by Table 3-26. 18h = PRBS9, as defined in Appendix N. 20h = PRBS11, as defined in Appendix N. 28h = PRBS15, as defined in Appendix N. 30h = PRBS23, as defined in Appendix N. 38h = PRBS31, as defined in Appendix N. 40h = 264-bit custom pattern (DPCD Addresses 02230h through 02250h). 48h = SQ*num* – Square pattern of *num* 1s, followed by *num* 0s, as: • Prewritten by the LINK_SQUARE_PATTERN_num + 1 register (DPCD Address 0010Fh) for the Lane's LINK_QUAL_PATTERN_SET field in the LINK_QUAL_LANE*x*_SET register(s) (DPCD Address(es) 0010Bh through 0010Eh, bits 6:0), –or– • Read by the PHY_SQUARE_PATTERN_num + 1 register (DPCD Address 00249h)	
		7	**RESERVED**	Read 0

Table 2-185: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link/Sink Device Status Field	
00249h	**PHY_SQUARE_PATTERN_*num* + 1** New to *DP v2.0*. Valid only for UHBR bit rates. Use for all Square pattern (value of 48h) requests by the LINK_QUAL_PATTERN_SEL field in the LINK_QUAL_PATTERN_SELECT register (DPCD Address 00248h, bits 6:0). Defines the number of consecutive 1s (which is the same as the number of consecutive 0s), all the way to 256 1s and 256 0s (by defining that the 00h value indicates a "1010…" pattern). For example: 00h = Pattern is 101010101010…. 04h = Pattern is 11111000001111100000…. 01h = Pattern is 110011001100…. … 02h = Pattern is 111000111000…. FFh = 256 1s followed by 256 0s. 03h = Pattern is 1111000011110000….			Write/Read
0024Ah and 0024Bh	**For DPCD r1.0 and r1.1**			Read all 0s
	RESERVED			
	For DPCD r1.2 (and higher)			Read Only
	HBR2_COMPLIANCE_SCRAMBLER_RESET Count of number of scrambled 0 symbols to be output for every Enhanced Framing Scrambler Reset sequence (SR BF BF SR). Count includes the reset sequence. Value less than four causes scrambled 0 symbols to be output with no scrambler reset sequence.			
	0	7:0	**HBR2_COMPLIANCE_SCRAMBLER_RESET_VALUE7:0**	
	1	7:0	**HBR2_COMPLIANCE_SCRAMBLER_RESET_VALUE15:8**	
0024Ch through 0024Fh	**RESERVED** For test automation extensions.			Read all 0s
00250h through 00259h	**TEST_80BIT_CUSTOM_PATTERN** Stores the 80-bit custom pattern for Source device compliance measurements (the LSB is transmitted first).			Read Only
	0	7:0	**TEST_80BIT_CUSTOM_PATTERN_VALUE7:0**	
	1	7:0	**TEST_80BIT_CUSTOM_PATTERN_VALUE15:8**	
	2	7:0	**TEST_80BIT_CUSTOM_PATTERN_VALUE23:16**	
	3	7:0	**TEST_80BIT_CUSTOM_PATTERN_VALUE31:24**	
	4	7:0	**TEST_80BIT_CUSTOM_PATTERN_VALUE39:32**	
	5	7:0	**TEST_80BIT_CUSTOM_PATTERN_VALUE47:40**	
	6	7:0	**TEST_80BIT_CUSTOM_PATTERN_VALUE55:48**	
	7	7:0	**TEST_80BIT_CUSTOM_PATTERN_VALUE63:56**	
	8	7:0	**TEST_80BIT_CUSTOM_PATTERN_VALUE71:64**	
	9	7:0	**TEST_80BIT_CUSTOM_PATTERN_VALUE79:72**	

Table 2-185: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link/Sink Device Status Field	
0025Ah	**CONTINUOUS_80BIT_PATTERN_FROM_DPRX_AUX_CH_CAPABILITY**			Read Only
		0	**CONTINUOUS_80BIT_PATTERN_FROM_DPRX_AUX_CH_CAP** 0 = Not supported. 1 = Supported.	
		7:1	**RESERVED**	Read all 0s
0025Bh	**CONTINUOUS_80BIT_PATTERN_FROM_DPRX_AUX_CH_CTRL**			Read/Write
		0	**CONTINUOUS_80BIT_PATTERN_FROM_DPRX_AUX_CH_EN** The DPRX shall clear this bit when either of the following occurs: • Duration expiration –or– • Detection of an upstream DP device disconnect 0 = Disable continuous transmission of the 80-bit pattern programmed by the TEST_80BIT_CUSTOM_PATTERN register (DPCD Addresses 00250h through 00259h). 1 = Enable continuous transmission of the 80-bit pattern programmed by the TEST_80BIT_CUSTOM_PATTERN register. While the transmission is enabled, AUX transactions over the AUX_CH are unavailable.	
		2:1	**DURATION_CTRL** 00b = 15sec. 10b = 60sec. 01b = 30sec. 11b = 120sec.	
		7:3	**RESERVED**	Read all 0s
0025Ch through 0025Fh	**RESERVED** For test automation extensions.			Read all 0s

Table 2-185: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link/Sink Device Status Field	
00260h	**TEST_RESPONSE**			Write/Read
		0	**TEST_ACK** 0 = Writing 0 has no effect on the TEST_REQ state. 1 = Positive acknowledgment of the TEST_REQ. Clears the TEST_REQ interrupt flag and indicates to the Sink device that the Source device has started the requested test mode.	
		1	**TEST_NAK** 0 = Writing 0 has no effect on the TEST_REQ state. 1 = Negative acknowledgment of the TEST_REQ. Clears the TEST_REQ interrupt flag and indicates to the Sink device that the Source device shall not start the requested test mode.	
		2	**TEST_EDID_CHECKSUM_WRITE** 0 = No DisplayID or legacy EDID checksum write to the TEST_EDID_CHECKSUM register (DPCD Address 00261h). 1 = DisplayID or legacy EDID checksum has been written to the TEST_EDID_CHECKSUM register.	
		7:3	**RESERVED**	Read all 0s
00261h	**TEST_EDID_CHECKSUM** In TEST_EDID mode, the checksum of the last DisplayID or legacy EDID block that was read is written here.			Write/Read
00262h and 00263h	**DSC_CRC_0** New to *DP v1.4a*. DSC CRC Engine 0.			Read Only
	0	7:0	**CRC_VALUE7:0**	
	1	7:0	**CRC_VALUE15:8**	
00264h and 00265h	**DSC_CRC_1** New to *DP v1.4a*. DSC CRC Engine 1.			Read Only
	0	7:0	**CRC_VALUE7:0**	
	1	7:0	**CRC_VALUE15:8**	
00266h and 00267h	**DSC_CRC_2** New to *DP v1.4a*. DSC CRC Engine 2.			Read Only
	0	7:0	**CRC_VALUE7:0**	
	1	7:0	**CRC_VALUE15:8**	

Table 2-185: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link/Sink Device Status Field	
00268h through 0026Fh	**RESERVED** For test automation extensions.			Read all 0s
00270h	**TEST_SINK**			Write/Read
		0	**TEST_SINK_START** 0 = Stop calculating CRC on the next frame. 1 = Start calculating CRC on the next frame. ***Note:*** *Calculation is performed on the entire frame. A 16-bit CRC is generated per component, based on the following polynomial:* $f(x) = x^{16} + x^{15} + x^2 + 1$ *The CRC calculation is only performed on active pixels. The msb is shifted in first. For any colorimetry format that is less than 16bpc, the lsb is zero-padded. See Appendix J for an example implementation.*	
		1	**CRC_3D_OPTION1_SELECT** New to *DP v1.4a*. Enabled when the CRC_3D_OPTIONS_SUPPORTED bit in the NORP & DP_PWR_VOLTAGE_CAP register (DPCD Address 00004h, bit 1) is set to 1. 0 = Option 0 is selected. 1 = Option 1 is selected. See Section H.1.2 for use details.	
		3:2	**RESERVED**	Read all 0s

Table 2-185: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link/Sink Device Status Field	
00270h		5:4	**PHY_SINK_TEST_LANE_SEL** Indicates which lane is enabled when the PHY_SINK_TEST_LANE_EN bit (bit 7) is set to 1 (i.e., only one lane is enabled for JTOL tests). 00b = Lane 0. 10b = Lane 2. 01b = Lane 1. 11b = Lane 3.	Write/Read
		6	**RESERVED**	Read 0
		7	**PHY_SINK_TEST_LANE_EN** 1 = Specific lane on the Sink device is tested for crosstalk, with other lanes receiving a “clock” pattern at approximately half the bit rate. In this mode, the receiver accumulates error counts for the enabled lane in: • SYMBOL_ERROR_COUNT_LANE0 register (DPCD Addresses 00210h and 00211h) for Lane 0 • SYMBOL_ERROR_COUNT_LANE1 register (DPCD Addresses 00212h and 00213h) for Lane 1 • SYMBOL_ERROR_COUNT_LANE2 register (DPCD Addresses 00214h and 00215h) for Lane 2 • SYMBOL_ERROR_COUNT_LANE3 register (DPCD Addresses 00216h and 00217h) for Lane 3 Sink device treatment of the other lanes is implementation-specific.	Write/Read
00271h	**TEST_AUDIO_MODE**			Read Only
		3:0	**TEST_AUDIO_SAMPLING_RATE** 0h = 32kHz. 3h = 88.2kHz. 5h = 176.4kHz. 1h = 44.1kHz. 4h = 96kHz. 6h = 192kHz. 2h = 48kHz. All other values are RESERVED.	
		7:4	**TEST_AUDIO_CHANNEL_COUNT** 0h = 1 Channel. 4h = 5 Channels. 1h = 2 Channels. 5h = 6 Channels. 2h = 3 Channels. 6h = 7 Channels. 3h = 4 Channels. 7h = 8 Channels. All other values are RESERVED.	

Table 2-185: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link/Sink Device Status Field	
00272h	**TEST_AUDIO_PATTERN_TYPE** Updated in *DP v2.0*. Audio test pattern requested by the Reference Sink device. 00h = Operator-defined. 01h = Sawtooth pattern. All other values are RESERVED.			Read Only
00273h	**TEST_AUDIO_PERIOD_CH1** Indicates period of test pattern for Channel 1 in audio samples.			Read Only
		3:0	**TEST_AUDIO_PERIOD_CH1** 0h = Unused. 4h = 24 samples. 8h = 384 samples. 1h = 3 samples. 5h = 48 samples. 9h = 768 samples. 2h = 6 samples. 6h = 96 samples. Ah = 1536 samples. 3h = 12 samples. 7h = 192 samples. All other values are RESERVED.	
		7:4	**RESERVED**	Read all 0s
00274h	**TEST_AUDIO_PERIOD_CH2** Indicates period of test pattern for Channel 2 in audio samples.			Read Only
		3:0	**TEST_AUDIO_PERIOD_CH2** Bit definition is identical to the TEST_AUDIO_PERIOD_CH1 field in the TEST_AUDIO_PERIOD_CH1 register (DPCD Address 00273h, bits 3:0), but for Channel 2.	
		7:4	**RESERVED**	Read all 0s
00275h	**TEST_AUDIO_PERIOD_CH3** Indicates period of test pattern for Channel 3 in audio samples.			Read Only
		3:0	**TEST_AUDIO_PERIOD_CH3** Bit definition is identical to the TEST_AUDIO_PERIOD_CH1 field in the TEST_AUDIO_PERIOD_CH1 register (DPCD Address 00273h, bits 3:0), but for Channel 3.	
		7:4	**RESERVED**	Read all 0s
00276h	**TEST_AUDIO_PERIOD_CH4** Indicates period of test pattern for Channel 4 in audio samples.			Read Only
		3:0	**TEST_AUDIO_PERIOD_CH4** Bit definition is identical to the TEST_AUDIO_PERIOD_CH1 field in the TEST_AUDIO_PERIOD_CH1 register (DPCD Address 00273h, bits 3:0), but for Channel 4.	
		7:4	**RESERVED**	Read all 0s

Table 2-185: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link/Sink Device Status Field	
00277h	**TEST_AUDIO_PERIOD_CH5** Indicates period of test pattern for Channel 5 in audio samples.			Read Only
		3:0	**TEST_AUDIO_PERIOD_CH5** Bit definition is identical to the TEST_AUDIO_PERIOD_CH1 field in the TEST_AUDIO_PERIOD_CH1 register (DPCD Address 00273h, bits 3:0), but for Channel 5.	
		7:4	**RESERVED**	Read all 0s
00278h	**TEST_AUDIO_PERIOD_CH6** Indicates period of test pattern for Channel 6 in audio samples.			Read Only
		3:0	**TEST_AUDIO_PERIOD_CH6** Bit definition is identical to the TEST_AUDIO_PERIOD_CH1 field in the TEST_AUDIO_PERIOD_CH1 register (DPCD Address 00273h, bits 3:0), but for Channel 6.	
		7:4	**RESERVED**	Read all 0s
00279h	**TEST_AUDIO_PERIOD_CH7** Indicates period of test pattern for Channel 7 in audio samples.			Read Only
		3:0	**TEST_AUDIO_PERIOD_CH7** Bit definition is identical to the TEST_AUDIO_PERIOD_CH1 field in the TEST_AUDIO_PERIOD_CH1 register (DPCD Address 00273h, bits 3:0), but for Channel 7.	
		7:4	**RESERVED**	Read all 0s
0027Ah	**TEST_AUDIO_PERIOD_CH8** Indicates period of test pattern for Channel 8 in audio samples.			Read Only
		3:0	**TEST_AUDIO_PERIOD_CH8** Bit definition is identical to the TEST_AUDIO_PERIOD_CH1 field in the TEST_AUDIO_PERIOD_CH1 register (DPCD Address 00273h, bits 3:0), but for Channel 8.	
		7:4	**RESERVED**	Read all 0s
0027Bh through 0027Fh	**RESERVED**			Read all 0s

Table 2-185: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link/Sink Device Status Field	
00280h	**FEC_STATUS** New to *DP v1.4*.			Clearable Read Only (Write 1 to clear the set bit)
		0	**FEC_DECODE_EN_DETECTED** Set by a DPRX when the DPRX detects the FEC_DECODE_EN control link symbol sequence over the Main-Link. 0 = Not detected. 1 = Detected.	
		1	**FEC_DECODE_DIS_DETECTED** Set by a DPRX when the DPRX detects the FEC_DECODE_DIS control link symbol sequence over the Main-Link. 0 = Not detected. 1 = Detected.	
		2	**FEC_RUNNING_INDICATOR** New to *DP v2.0*. When the FEC_RUNNING_INDICATOR_SUPPORTED bit in the FEC_CAPABILITY_0 register (DPCD Address 00090h, bit 6) is set to 1, indicates whether the FEC decoding logic is currently running on the DPRX. 0 = FEC is not running. 1 = FEC is running. **8b/10b channel coding** See Section 3.5.1.5.5 for further details. **128b/132b channel coding** Because FEC is always enabled, a 128b/132b channel coding-capable DPRX shall set this bit and the FEC_RUNNING_INDICATOR_SUPPORTED bit to 1 in normal operation, immediately after link training completion.	
		7:3	**RESERVED**	Read all 0s

Table 2-185: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link/Sink Device Status Field	
00281h and 00282h	**FEC_ERROR_COUNT** New to *DP v1.4*. The error counter is reset, and this register is cleared to all 0s when the FEC_ERROR_COUNT_SEL field in the FEC_CONFIGURATION register (DPCD Address 00120h, bits 3:1) is cleared to 000b. After the maximum error count is reached (= $2^{15} - 1$), the maximum error count is retained until the error counter is reset.			Read Only
	0	7:0	**FEC_ERROR_COUNT7:0** Least significant eight bits of the 15-bit error count.	
	1	6:0	**FEC_ERROR_COUNT14:8** Most significant seven bits of the 15-bit error count.	
		7	**FEC_ERROR_COUNT_VALID** 0 = Not valid. 1 = Valid.	
00283h through 002BFh	**RESERVED** For test automation extensions.			Read all 0s
End of Automated Testing Register Set				
002C0h	**PAYLOAD_TABLE_UPDATE_STATUS**			Clearable Read Only
		0	**VC Payload ID Table Updated** 0 = Not updated since the last time that this bit was cleared. 1 = Updated, cleared to 0 when the DP Source device writes 1.	
		1	**ACT Handled** 0 = ACT is not handled since the last time that this bit was read. 1 = ACT is handled, cleared to 0 when the VC Payload ID Table Updated bit (bit 0) is set to 1.	
		7:2	**8b/10b channel coding:** **RESERVED**	Read all 0s
			128b/132b channel coding: **VC_PAYLOAD_ID_SLOT0_5:0** New to *DP v2.0*. See Table 2-149 for time slot number to VC Payload ID mapping. Bits 5:0 of VC_PAYLOAD_ID_SLOT0.	Read Only

Table 2-185: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Link/Sink Device Status Field	
002C1h	**VC_PAYLOAD_ID_SLOT1** Updated in *DP v2.0*. • **8b/10b channel coding** – See Table 2-140 for time slot number to VC Payload ID mapping. • **128b/132b channel coding** – See Table 2-149 for time slot number to VC Payload ID mapping.			Read Only
		6:0	**VC_PAYLOAD_ID_SLOT1**	
		7	**8b/10b channel coding:** **RESERVED**	Read 0
		7	**128b/132b channel coding:** **VC_PAYLOAD_ID_SLOT0_6** New to *DP v2.0*. Bit 6 of VC_PAYLOAD_ID_SLOT0.	Read Only
002C2h	**VC_PAYLOAD_ID_SLOT2** Updated in *DP v2.0*. • **8b/10b channel coding** – See Table 2-140 for time slot number to VC Payload ID mapping. • **128b/132b channel coding** – See Table 2-149 for time slot number to VC Payload ID mapping.			Read Only
		6:0	**VC_PAYLOAD_ID_SLOT2**	
		7	**RESERVED**	Read 0
…	…			Read Only
002FFh	**VC_PAYLOAD_ID_SLOT63** Updated in *DP v2.0*. • **8b/10b channel coding** – See Table 2-140 for time slot number to VC Payload ID mapping. • **128b/132b channel coding** – See Table 2-149 for time slot number to VC Payload ID mapping.			Read Only
		6:0	**VC_PAYLOAD_ID_SLOT63**	
		7	**RESERVED**	Read 0

For details regarding how to select and clear the error counters through the FEC_CONFIGURATION register (DPCD Address 00120h), and how to read the error counters through the FEC_ERROR_COUNT register (DPCD Addresses 00281h and 00282h), see Section 3.5.3.3.

Table 2-186: Address Mapping within DPCD Source Device-specific Field (DPCD Addresses 00200h through 003FFh)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Source Device-specific Field	
00300h through 00302h	**IEEE_OUI** Shall be cleared to all 0s upon power-on reset or an upstream device disconnect. Defaults to all 0s before being written to by the Source device. Example: For IEEE OUI 00-1B-C5, Byte 0 is cleared to 00h, Byte 1 is programmed to 1Bh, and Byte 2 is programmed to C5h.			Write/Read (Burst write for 00300h through 0030Bh)
	0	7:0	First two hex digits.	
	1	7:0	Second two hex digits.	
	2	7:0	Third two hex digits.	
00303h through 00308h	**Device Identification String** Identifies the Source device. Up to six ASCII characters, starting at DPCD Address 00303h. Remaining bytes are 00h if fewer than six characters. Shall be cleared to all 0s upon power-on reset or an upstream device disconnect. All bytes default to 0s before being written to by the Source device. A Source device shall always update all six bytes (including any zero bytes) with a burst write.			Write/Read (Burst write for 00300h through 0030Bh)
00309h	**Hardware Revision** Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs.			Write/Read (Burst write for 00300h through 0030Bh)
		3:0	**Hardware Minor Revision** Integer, reset to 0 when the major revision increments. Typically incremented for a minor silicon (e.g., metal mask change) or board revision. Defaults to 0h before being written to by the Source device.	
		7:4	**Hardware Major Revision** Integer, typically incremented for a major silicon or board revision.	
0030Ah	**Firmware/Software Major Revision** Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs. Defaults to 00h before being written to by the Source device. Integer, typically incremented for new functionality.			Write/Read (Burst write for 00300h through 0030Bh)

Table 2-186: Address Mapping within DPCD Source Device-specific Field (DPCD Addresses 00200h through 003FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Source Device-specific Field	
0030Bh	**Firmware/Software Minor Revision** Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs. Defaults to 00h before being written to by the Source device. Integer, reset to 0 when the firmware/software major revision increments. Typically incremented for bug fixes.			Write/Read (Burst write for 00300h through 0030Bh)
0030Ch through 003FFh	**RESERVED** For Source device-specific usage, specified by the owner of the IEEE OUI that is written to in the Source device IEEE_OUI register (DPCD Addresses 00300h through 00302h), and identified by the Source Identification registers (DPCD Addresses 00300h through 0030Bh). A Sink device that does not support the Source-device specified behavior specified by the owner of the IEEE OUI written to in DPCD Addresses 00300h through 00302h as being associated with the Source Identification shall AUX_ACK all writes, but take no other action, and shall respond to reads with an AUX_ACK and the value 00h.			Vendor-specific

Table 2-187: Address Mapping within DPCD Sink Device-specific Field (DPCD Addresses 00400h through 004FFh)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Sink Device-specific Field	
00400h through 00402h	**IEEE_OUI** Shall be supported for Sink devices. Cleared to all 0s for Branch devices. Example: For IEEE OUI 00-1B-C5, Byte 0 is cleared to 00h, Byte 1 is programmed to 1Bh, and Byte 2 is programmed to C5h.			Read Only
	0	7:0	First two hex digits.	
	1	7:0	Second two hex digits.	
	2	7:0	Third two hex digits.	
00403h through 00408h	**Device Identification String** Identifies the Sink device. Up to six ASCII characters, starting at DPCD Address 00403h. Remaining bytes are 00h if fewer than six characters. Shall be supported for Sink devices. Cleared to 00h for Branch devices.			Read Only
00409h	**Hardware Revision**			Read Only
		3:0	**Hardware Minor Revision** Integer, reset to 0 when major revision increments. Typically incremented for a minor silicon (e.g., metal mask change) or board revision. Shall be supported for Sink devices. Cleared to 00h for Branch devices.	
		7:4	**Hardware Major Revision** Integer, typically incremented for a major silicon or board revision.	
0040Ah	**Firmware/Software Major Revision** Integer, typically incremented for new functionality. Shall be supported for Sink devices. Cleared to 00h for Branch devices.			Read Only
0040Bh	**Firmware/Software Minor Revision** Integer, reset to 0 when the firmware/software major revision increments. Typically incremented for bug fixes. Shall be supported for Sink devices. Cleared to 00h for Branch devices.			Read Only
0040Ch through 004FFh	**RESERVED** For Sink device-specific usage, specified by the owner of the IEEE OUI that is provided in the Sink device IEEE_OUI register (DPCD Addresses 00400h through 00402h). Branch devices shall AUX_ACK all writes, but take no other action and shall respond to reads with an AUX_ACK and the value 00h.			Vendor-specific

Table 2-188: Address Mapping within DPCD Branch Device-specific Field (DPCD Addresses 00500h through 005FFh)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Branch Device-specific Field	
00500h through 00502h	**IEEE_OUI** Shall be supported for Branch devices, cleared to all 0s for Sink devices. Example: For IEEE OUI 00-1B-C5, Byte 0 is cleared to 00h, Byte 1 is programmed to 1Bh, and Byte 2 is programmed to C5h.			Read Only
	0	7:0	First two hex digits.	
	1	7:0	Second two hex digits.	
	2	7:0	Third two hex digits.	
00503h through 00508h	**Device Identification String** Identifies the Branch device. Up to six ASCII characters, starting at DPCD Address 00503h. Remaining bytes are 00h if fewer than six characters. Shall be supported for Branch devices. Cleared to 00h for Sink devices.			Read Only
00509h	**Hardware Revision**			Read Only
		3:0	**Hardware Minor Revision** Integer, reset to 0 when major revision increments. Typically incremented for a minor silicon (e.g., metal mask change) or board revision. Shall be supported for Branch devices. Cleared to 00h for Sink devices.	
		7:4	**Hardware Major Revision** Integer, typically incremented for a major silicon or board revision.	
0050Ah	**Firmware/Software Major Revision** Integer, typically incremented for new functionality. Shall be supported for Branch devices. Cleared to 00h for Sink devices.			Read Only
0050Bh	**Firmware/Software Minor Revision** Integer, reset to 0 when the firmware/software major revision increments. Typically incremented for bug fixes. Shall be supported for Branch devices. Cleared to 00h for Sink devices.			Read Only
0050Ch through 005FFh	**RESERVED** For Branch device-specific usage, specified by the owner of the IEEE OUI that is written to in the Branch device IEEE_OUI register (DPCD Addresses 00500h through 00502h). Sink devices shall AUX_ACK all writes, but take no other action, and shall respond to reads with an AUX_ACK and the value 00h.			Vendor-specific

Table 2-189: Address Mapping within DPCD Link/Sink Device Power Control Field (DPCD Addresses 00600h through 006FFh)

DPCD Address	Register		Read/ Write over AUX_CH
	Bit #	Definition within Link/Sink Device Power Control Field	
00600h	**SET_POWER & SET_DP_PWR_VOLTAGE** ***Notes:*** *1 When bits 7:5 are cleared to 000b, the downstream device keeps the DP_PWR voltage to the default 3.3V DP_PWR setting. Only one bit may be set at a time. Setting a bit takes effect only when the downstream device is capable of generating the requested DP_PWR supply voltage as indicated in the xV_DP_PWR_CAP bits in the NORP & DP_PWR_VOLTAGE_CAP register (DPCD Address 00004h, bits 7:5). A downstream DP device capable of generating DP_PWR voltage higher than the default 3.3V DP_PWR setting shall complete the voltage level transition within 1ms. During the transition, the DP device shall not generate a voltage exceeding the voltage range of the higher of the two voltage levels between which the switching is taking place.* *2 An SST-in, SST-out Branch device shall forward this value to its downstream devices.* *When set to D3 state, a Sink device may place its AUX_CH circuit in a power-saving state. In this mode, the AUX_CH circuit may detect only the presence of a differential signal input without replying to an AUX request transaction. Upon detecting the presence of a differential signal input, the Sink device shall exit the power-saving state within 1ms.*		Write/Read
	2:0	**SET_POWER_STATE** Shall be programmed to 001b upon power-on reset or an upstream device disconnect. 001b = Set local Sink device and all downstream Sink devices to D0 (normal operation mode). 010b = Set local Sink device and all downstream Sink devices to D3 (power-down mode). 101b = Set Main-Link for local Sink device and all downstream Sink devices to D3 (power-down mode), keep AUX block fully powered, ready to reply within the AUX Response Timeout timer period defined in Section 2.11.2. All other values are RESERVED.	
	4:3	**RESERVED**	Read all 0s
	5	**SET_DN_DEVICE_DP_PWR_5V** Shall be cleared to 0 when a power-on reset or upstream device disconnect occurs. 1 = Set the downstream device's DP connector DP_PWR pin to 5V.	Write/Read
	6	**SET_DN_DEVICE_DP_PWR_12V** Shall be cleared to 0 when a power-on reset or upstream device disconnect occurs. 1 = Set the downstream device's DP connector DP_PWR pin to 12V.	
	7	**SET_DN_DEVICE_DP_PWR_18V** Shall be cleared to 0 when a power-on reset or upstream device disconnect occurs. 1 = Set the downstream device's DP connector DP_PWR pin to 18V.	

Table 2-189: Address Mapping within DPCD Link/Sink Device Power Control Field (DPCD Addresses 00600h through 006FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX_CH
	Bit #	Definition within Link/Sink Device Power Control Field	
00601h through 006FFh	**RESERVED for DPRX and Sink Device Power Control**		Read all 0s

Table 2-190: Address Mapping within DPCD eDP-specific Field (DPCD Addresses 00700h through 007FFh)

DPCD Address	Register		Read/ Write over AUX_CH
	Bit #	Definition within eDP-specific Field	
00700h through 007FFh	**RESERVED for eDP** See *eDP Standard*.		

Table 2-191: Address Mapping within DPCD Sideband MSG Buffers Field (DPCD Addresses 01000h through 017FFh)

DPCD Address	Register		Read/ Write over AUX_CH
	Bit #	Definition within Sideband MSG Buffers Field	
01000h through 011FFh	**DOWN_REQ** ***Note:*** *An MST-capable upstream device shall treat these registers as write-only because some MST-capable downstream devices may reply with all 0s when read.*		Write/Read
01200h through 013FFh	**UP_REP** ***Note:*** *An MST-capable upstream device shall treat these registers as write-only because some MST-capable downstream devices may reply with all 0s when read.*		Write/Read
01400h through 015FFh	**DOWN_REP**		Read Only
01600h through 017FFh	**UP_REQ**		Read Only

Table 2-192: Address Mapping within DPCD DPRX Event Status Indicator Field (DPCD Addresses 02000h through 021FFh)

DPCD Address	Register		Read/ Write over AUX_CH
	Bit #	Definition within DPRX Event Status Indicator Field	
Note: *This field shall be supported for DP devices with a DPRX that is DPCD r1.2 or higher. An MST upstream device shall use this field instead of the Link/Sink Device Status field registers, as follows:* • *DPCD Address 02002h (instead of 00200h)* • *DPCD Address 02003h (instead of 00201h)* • *DPCD Address 0200Ch (instead of 00202h)* • *DPCD Address 0200Dh (instead of 00203h)* • *DPCD Address 0200Eh (instead of 00204h)* • *DPCD Address 0200Fh (instead of 00205h)*			
02000h through 02001h	**RESERVED**		Read all 0s
02002h	**SINK_COUNT_ESI** Sink device count; same status available in the SINK_COUNT register (DPCD Address 00200h).		Read Only
	7, 5:0	**SINK_COUNT** Total number of Sink devices within this Branch device and those connected to the DFPs of this device. ***Note:*** *A Branch device shall add up the Rendering function counts read from all its DFPs. The Branch device shall increase the count by one if it also has Rendering function.*	
	6	**CP_READY** Set to 1 when all the Sink devices (local Sink device and those connected to its DFPs) are CP-capable. Set at the conclusion of Content Protection Authentication, as needed, by the appropriate Content Protection specification. ***Note:*** *The Source device shall transmit content that needs content protection only when all Branch and Sink devices within the link are CP-ready except for Repeater devices. (A Repeater device shall not be required to perform decryption/encryption operations, and therefore shall not be required to be CP-ready.)*	

Table 2-192: Address Mapping within DPCD DPRX Event Status Indicator Field (DPCD Addresses 02000h through 021FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX_CH
	Bit #	Definition within DPRX Event Status Indicator Field	
02003h	**DEVICE_SERVICE_IRQ_VECTOR_ESI0** Same flags available in the DEVICE_SERVICE_IRQ_VECTOR register (DPCD Address 00201h).		Clearable Read Only (Bit is cleared when 1 is written by way of an AUX_CH write transaction)
	0	**RESERVED (for FUTURE)** **REMOTE_CONTROL_COMMAND_PENDING** For DP devices that support Sideband MSG handling (MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0) is set to 1), a Sink Event (e.g., a remote control command pending) shall be handled as a message transaction.	
	Bit 1 definition is DPCD revision-dependent. **For DPCD r1.0 through DPCD r1.2 and DPCD r1.4 (Bit 1); otherwise, RESERVED**		
	1	**AUTOMATED_TEST_REQUEST** 1 = Source device shall read DPCD Addresses 00218h through 002BFh for the requested link test.	Clearable Read Only
	Definitions of Bits 7:2 are not DPCD revision-dependent		Clearable Read Only (Bit is cleared when 1 is written by way of an AUX_CH write transaction)
	2	**CP_IRQ** Used by an optional content protection system.	
	3	**MCCS_IRQ** Used by an optional MCCS system within the Sink device.	
	4	**DOWN_REP_MSG_RDY** 1 = Source device shall read the DOWN_REP_MSG from the DOWN_REP_MSG DPCD locations and process the Sideband MSG.	
	5	**UP_REQ_MSG_RDY** 1 = Source device shall read the UP_REQ_MSG from the UP_REQ_MSG DPCD locations and process the Sideband MSG.	
	6	**SINK_SPECIFIC_IRQ** Usage is vendor-specific.	
	7	**RESERVED**	Read 0

Table 2-192: Address Mapping within DPCD DPRX Event Status Indicator Field (DPCD Addresses 02000h through 021FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX_CH
	Bit #	Definition within DPRX Event Status Indicator Field	
02004h	**DEVICE_SERVICE_IRQ_VECTOR_ESI1**		Clearable Read Only (Bit is cleared when 1 is written by way of an AUX write transaction)
	0	**RX_GTC_MSTR_REQ_STATUS_CHANGE** The RX_GTC_MSTR_REQ status has changed (readable in the RX_GTC_MSTR_REQ bit in the RX_GTC_MSTR_REQ register (DPCD Address 00058h, bit 0)).	
	1	**LOCK_ACQUISITION_REQUEST** 0 = DPRX is not requesting a DPTX to initiate lock acquisition. 1 = DPRX is requesting a DPTX to initiate lock acquisition.	
	2	**CEC_IRQ** 1 = CEC-Tunneling-over-AUX status changed.	
	3	**PANEL_REPLAY_ERROR_STATUS** New to *DP v2.0*. A DPRX shall set this bit when one or more of the PANEL REPLAY ERROR STATUS bits (i.e., VSC SDP for PR UNCORRECTABLE ERROR, RFB STORAGE ERROR, and/or ACTIVE FRAME CRC ERROR; DPCD Address 02020h, bits 2:0, respectively) are set to 1. 1 = DP Source device shall read the PANEL REPLAY ERROR STATUS register (DPCD Address 02020h) to determine the Panel Replay errors.	
	4	**DSC_ERROR_STATUS** New to *DP v2.0*. 1 = DP Source device shall read the DSC STATUS register (DPCD Address 02011h).	
	7:5	**RESERVED**	Read all 0s

Table 2-192: Address Mapping within DPCD DPRX Event Status Indicator Field (DPCD Addresses 02000h through 021FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX_CH
	Bit #	Definition within DPRX Event Status Indicator Field	
02005h	**LINK_SERVICE_IRQ_VECTOR_ESI0**		Clearable Read Only (Bit is cleared when 1 is written by way of an AUX_CH write transaction)
	0	**RX_CAP_CHANGED** 1 = Upstream device shall read the Receiver Capability field (DPCD Addresses 00000h through 000FFh; see Table 2-183).	
	1	**LINK_STATUS_CHANGED** 1 = Upstream device shall read the Link/Sink Device Status field (DPCD Addresses 00200h through 002FFh; see Table 2-185).	
	2	**STREAM_STATUS_CHANGED** 1 = Upstream Source device shall re-check the Stream Status with the QUERY_STREAM_ENCRYPTION_STATUS message transaction. QUERY_STREAM_ENCRYPTION_STATUS is discussed in Appendix I.	
	3	**HDMI_LINK_STATUS_CHANGED** 1 = Upstream DP device shall read the DP-to-HDMI protocol converter's downstream HDMI link status registers. Downstream HDMI link quality is reported at the DOWNSTREAM_HDMI_ERROR_STATUS_CH*x* registers (DPCD Addresses 03031h through 03033h).	
	4	**CONNECTED_OFF_ENTRY_REQUESTED** 1 = A downstream DP device sets this bit to 1 and generates an IRQ_HPD pulse to request entry to the CONNECTED_OFF power state. The downstream DP device may enter the CONNECTED_OFF power state only after this bit is cleared by the upstream device writing 1 to this bit. If the upstream device does not clear this bit within 1 second after IRQ_HPD generation, the downstream device that requested entry into the CONNECTED_OFF power state shall clear this bit, enter the OFF power state, and then de-assert HPD output.	
	7:5	**RESERVED**	Read all 0s
02006h through 0200Ah	**RESERVED for eDP** Optional eDP PSR-related status registers. See *eDP v1.3* (or higher) for register definitions.		
0200Bh	**For DPCD r1.3 (*eDP v1.4* DPRX) only; otherwise, RESERVED**		
	eDP Advanced Link Power Management (ALPM)-related Functions See *eDP v1.4*.		

Table 2-192: Address Mapping within DPCD DPRX Event Status Indicator Field (DPCD Addresses 02000h through 021FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX_CH
	Bit #	Definition within DPRX Event Status Indicator Field	
0200Ch	**For DPCD r1.0 through DPCD r1.2 and DPCD r1.4**		Read Only
	LANE0_1_STATUS_ESI Same status available in the LANE0_1_STATUS register (DPCD Address 00202h).		
	0	**LANE0_CR_DONE**	
	1	**LANE0_CHANNEL_EQ_DONE**	
	2	**LANE0_SYMBOL_LOCKED**	
	3	**RESERVED**	Read 0
	4	**LANE1_CR_DONE**	Read Only
	5	**LANE1_CHANNEL_EQ_DONE**	
	6	**LANE1_SYMBOL_LOCKED**	
	7	**RESERVED**	Read 0
	For DPCD r1.3 (*eDP v1.4* DPRX) only; otherwise, RESERVED		
	SINK DEVICE AUX_FRAME_SYNC STATUS See *eDP v1.4*.		
0200Dh	**For DPCD r1.0 through DPCD r1.2 and DPCD r1.4**		Read Only
	LANE2_3_STATUS_ESI Same status available in the LANE2_3_STATUS register (DPCD Address 00203h). Bit definition is identical to the LANE0_1_STATUS_ESI register, but for Lanes 2 and 3.		

Table 2-192: Address Mapping within DPCD DPRX Event Status Indicator Field (DPCD Addresses 02000h through 021FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX_CH
	Bit #	Definition within DPRX Event Status Indicator Field	
0200Eh	**LANE_ALIGN_STATUS_UPDATED_ESI** Same status available in the LANE_ALIGN_STATUS_UPDATED register (DPCD Address 00204h).		Read Only
	0	**INTERLANE_ALIGN_DONE**	
	1	**POST_LT_ADJ_REQ_IN_PROGRESS** Valid only for 8b/10b Link Layer. "Don't care" for 128b/132b Link Layer. Valid only for a DPRX that sets the POST_LT_ADJ_REQ_SUPPORTED bit in the MAX_LANE_COUNT register (DPCD Address 00002h, bit 5) and after a DPTX grants the POST_LT_ADJ_REQ sequence by setting the POST_LT_ADJ_REQ_GRANTED bit in the LANE_COUNT_SET register (DPCD Address 00101h, bit 5). 1 = DPRX is conducting the POST_LT_ADJ_REQ sequence.	
	5:2	**RESERVED**	Read all 0s
	6	**DOWNSTREAM_PORT_STATUS_CHANGED** Set in a Branch device when it detects a change in the connection status of any of its DFPs.	Read Only
	7	**LINK_STATUS_UPDATED** Link Status and Adjust Request updated since the last read. Set when updated and cleared after read.	

Table 2-192: Address Mapping within DPCD DPRX Event Status Indicator Field (DPCD Addresses 02000h through 021FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX_CH
	Bit #	Definition within DPRX Event Status Indicator Field	
0200Fh	**SINK_STATUS_ESI** Same status available in the SINK_STATUS register (DPCD Address 00205h). The Sink device shall set bits 1:0 as soon as it determines that the corresponding received stream is properly regenerated and within the supported stream format range. The Sink device shall clear bits 1:0 as soon as it determines that the corresponding received stream is no longer being properly regenerated or within the supported stream format range.		Read Only
	0	**RECEIVE_PORT_0_STATUS** 0 = Sink device is out of synchronization. 1 = Sink device is in synchronization.	
	1	**RECEIVE_PORT_1_STATUS** 0 = Sink device is out of synchronization. 1 = Sink device is in synchronization.	
	2	**STREAM_REGENERATION_STATUS** New to *DP v2.0*. Valid when the STREAM_REGENERATION_STATUS_CAPABILITY bit in the MAX_DOWNSPREAD registers (DPCD Addresses 00003h and 02203h, bit 1) is set to 1. 0 = Stream is not being regenerated. 1 = Stream is being regenerated and is ready to be displayed on a screen. The DPRX should update this bit within 10ms to reflect the current state of stream regeneration. *For a Sink device, this means that the frame appears on a screen.* *For a Branch device, this means that transmission on the downstream DPTX has started.* *For an MST Branch device, this means that a first transmission to a DFP has started.* *If the Sink and MST Branch devices are located within the same enclosure, this can mean that the frame appears on a screen event.*	
	7:3	**RESERVED**	Read all 0s

Table 2-192: Address Mapping within DPCD DPRX Event Status Indicator Field (DPCD Addresses 02000h through 021FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX_CH
	Bit #	Definition within DPRX Event Status Indicator Field	
02010h	**RESERVED for eDP** See *eDP Standard*.		
02011h	**For DPCD r1.4 when used with *DP v1.4* (and higher)**		Read/Write
	DSC STATUS New to *DP v1.4*.		
	0	**RC Buffer Under-run** 0 = No error. 1 = Buffer under-run. Sticky until cleared by a write of 1.	
	1	**RC Buffer Overflow** 0 = No error. 1 = Buffer overflow. Sticky until cleared by a write of 1.	
	2	**Chunk Length Error** 0 = No error. 1 = Chunk Length error. Sticky until cleared by a write of 1.	
	7:3	**RESERVED**	Read all 0s
02012h	**RESERVED for eDP** See *eDP Standard*.		
02013h through 020AFh	**RESERVED**		Read all 0s

Table 2-192: Address Mapping within DPCD DPRX Event Status Indicator Field (DPCD Addresses 02000h through 021FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX_CH
	Bit #	Definition within DPRX Event Status Indicator Field	
PR Status Register Set			
02020h	**PANEL REPLAY ERROR STATUS** New to *DP v2.0*. When the DP Sink device sets any bit in this register to 1, the DP Sink device shall generate an IRQ_HPD if the associated interrupt has been enabled in the PANEL REPLAY ENABLE AND CONFIGURATION register (DPCD Address 001B0h).		Clearable Read Only
	0	**ACTIVE FRAME CRC ERROR** Sticky bit. Write 1 to clear. 0 = No Active Frame CRC error. 1 = Active Frame CRC mismatch.	
	1	**RFB STORAGE ERROR** Sticky bit. Write 1 to clear. 0 = No internal error. 1 = Internal error.	
	2	**VSC SDP for PR UNCORRECTABLE ERROR** Valid only with 8b/10b Link Layer encoding. Sticky bit. Write 1 to clear. 0 = No VSC SDP error. 1 = VSC SDP error that cannot be corrected with 4-bit RS (15, 13) FEC.	
	7:3	**RESERVED**	Read all 0s
02021h	**SU/PR EVENT STATUS INDICATOR** New to *DP v2.0*.		Clearable Read Only
	7:0	**RESERVED**	Read all 0s
02022h	**SINK DEVICE PANEL REPLAY STATUS** New to *DP v2.0*.		Read Only
	2:0	**Sink Device PANEL REPLAY Status** 000b = Sink device Panel Replay is inactive (default). 001b through 110b = RESERVED. 111b = DP Sink device internal error. The DP Sink device shall generate an IRQ_HPD and report a value of 111b until the DP Source device disables Panel Replay mode.	
	7:3	**RESERVED**	Read all 0s
02023h	**RESERVED**		Read all 0s

Table 2-192: Address Mapping within DPCD DPRX Event Status Indicator Field (DPCD Addresses 02000h through 021FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX_CH
	Bit #	Definition within DPRX Event Status Indicator Field	
02024h	**DEBUG 1_LAST RECEIVED VSC SDP CARRYING PANEL REPLAY INFORMATION** New to *DP v2.0*. Provides information regarding DP Sink device Panel Replay mode. A DP Source device is not mandated to use this register.		Read Only for Source device Read/Write for Sink device
	0	**PR State** Current PR_STATE bit (VSC SDP for Panel Replay DB1, bit 0) value within the DP Sink device.	
	1	**RESERVED**	Read 0
	2	**CRC Valid** Current CRC_VALID bit (VSC SDP for Panel Replay DB1, bit 2) value within the DP Sink device.	Read Only for Source device Read/Write for Sink device
	3	**SU Coordinates Valid** Current SU_COORDINATES_VALID bit (VSC SDP for Panel Replay DB1, bit 3) value within the DP Sink device.	
	7:4	**RESERVED**	Read all 0s
End of PR Status Register Set			
02025h through 021FFh	**RESERVED**		Read all 0s

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
Note: *Extended Receiver Capability registers are new to DP v1.3 and higher.*				
02200h	**DPCD_REV** ***Note:*** *The DPCD revision number does not necessarily match the DP version number.* DPCD data structure revision number.			Read Only
		3:0	**Minor Revision Number**	
		7:4	**Major Revision Number** 14h = DPCD r1.4. All other values are RESERVED; however, the DPTX shall ensure proper operation when it sees a DPCD revision value that is higher than DPCD r1.4.	
02201h	**8b/10b_MAX_LINK_RATE** ***Note:*** *For 128b/132b Link Layer, see the 128b/132b_SUPPORTED_LINK_RATES register (DPCD Address 02215h).* Updated in *DP v2.0*. Valid only for 8b/10b Link Layer. A DP device that supports 128b/132b Link Layer link rates shall support all 8b/10b Link Layer link rates. Main-Link Bandwidth Setting = Value × 0.27Gbps/lane. Four values are supported. All other values are RESERVED with the exception of *eDP v1.4* and *MyDP Standard* DPTXs. 06h = 1.62Gbps/lane (RBR). 14h = 5.4Gbps/lane (HBR2). 0Ah = 2.7Gbps/lane (HBR). 1Eh = 8.1Gbps/lane (HBR3). An eDP DPRX may program this register to 00h to indicate that the DPRX supports the Main-Link rates by way of the Link Rate Table method. (See *eDP v1.4*.) A *MyDP Standard* DPRX of an active *MyDP Standard* protocol converter (either MyDP-to-Legacy or MyDP-to-DP Lane-Count protocol converter) can support a value of 19h (6.75Gbps/lane). **SST-only Branch device in the presence of a downstream device** – For the mandated value of this register, see Section 2.1.4.1.			Read Only

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
02202h	**MAX_LANE_COUNT**			Read Only
		4:0	**MAX_LANE_COUNT** Maximum number of lanes = Value. 01h = One lane (Lane 0 only). 02h = Two lanes (Lanes 0 and 1 only). 04h = Four lanes (Lanes 0, 1, 2, and 3). All other values are RESERVED. **SST-only Branch device in the presence of a downstream device** – For the mandated value of this field, see Section 2.1.4.1.	
		5	**POST_LT_ADJ_REQ_SUPPORTED** 0 = POST_LT_ADJ_REQ sequence is not supported. 1 = POST_LT_ADJ_REQ sequence is supported. (See Section 3.5.1.2.5.) POST_LT_ADJ_REQ is the third link training sequence, and is used only when training to a link rate that is lower than UHBR10 and TPS4 cannot be used in the second (i.e., LANE*x*_CHANNEL_EQ_DONE) link training sequence. (TPS4 can be used only when the DPTX and DPRX both support TPS4.) An upstream device with a DPTX (Source or Branch device) aware of the POST_LT_ADJ_REQ sequence indicates granting of the POST_LT_ADJ_REQ sequence by setting the POST_LT_ADJ_REQ_GRANTED bit in the LANE_COUNT_SET register (DPCD Address 00101h, bit 5). The downstream device indicates that the POST_LT_ADJ_REQ sequence is in-progress by setting the POST_LT_ADJ_REQ_IN_PROGRESS bits in the LANE_ALIGN_STATUS_UPDATED and LANE_ALIGN_STATUS_UPDATED_ESI registers (DPCD Addresses 00204h and 0200Eh, respectively, bit 1). This is done at the end of the LANE*x*_CHANNEL_EQ_DONE sequence when the downstream device sets the Link/Sink Device Status field (DPCD Addresses 00200h through 002FFh; see Table 2-185) register bits to indicate LANE*x*_SYMBOL_LOCKED and INTERLANE_ALIGN_DONE completion.	
		6	**TPS3_SUPPORTED** Indicates Link Training Pattern Sequence 3 (TPS3) support. 0 = TPS3 is not supported. 1 = TPS3 is supported (shall be supported for Downstream devices that support HBR2; may be supported for others).	
		7	**ENHANCED_FRAME_CAP** Applies only to Single-Stream Transport (SST) mode. Shall be set to 1. 0 = Enhanced Framing symbol sequence for BS and SR is not supported. 1 = Enhanced Framing symbol sequence for BS and SR is supported as described in Section 2.2.1.2.	

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
02203h	**MAX_DOWNSPREAD**			Read Only
		0	**MAX_DOWNSPREAD** Indicates whether the Spread-Spectrum Clock (SSC) is supported. SSC is enabled when this bit is set to 1 and the SPREAD_AMP bit in the DOWNSPREAD_CTRL register (DPCD Address 00107h, bit 4) is set to 1. 0 = No down spread (SSC is not supported). 1 = Up to 0.5% down spread (SSC is supported). Shall support up to 0.5% down spread for DPCD r1.1 (and higher) Sink and Branch devices. Therefore, this bit shall be set to 1.	
		1	**STREAM_REGENERATION_STATUS_CAPABILITY** New to *DP v2.0*. 0 = Not supported. 1 = Supported. STREAM_REGENERATION_STATUS bit in the SINK_STATUS SINK_STATUS_ESI registers (DPCD Addresses 00205h and 0200Fh, respectively, bit 2) is supported by the DPRX, and can be relied on by the DPTX.	
		5:2	**RESERVED**	Read all 0s
		6	**NO_AUX_TRANSACTION_LINK_TRAINING** 0 = DPTX shall issue AUX transactions to conduct link training. 1 = AUX transactions are not needed when the link configuration is already known. A DPTX, when it activates its Main-Link, can transmit TPS1 and TPS2 (or TPS3 or TPS4) for the minimum of 500us each. The known-good drive current and pre-emphasis level (or those used in the last "full" link training with AUX transactions) shall be used when link training is performed without AUX transactions. Regardless of this bit's value, a DP Sink device shall transmit an IRQ_HPD pulse when it cannot synchronize to the incoming stream. For embedded implementations in which there is no HPD line, either the proper operation should be guaranteed by design or the Source device can periodically poll the link status.	Read Only
		7	**TPS4_SUPPORTED** Indicates Link Training Pattern Sequence 4 (TPS4) support. 0 = TPS4 is not supported. 1 = TPS4 is supported (shall be supported for downstream devices with DPCD r1.4, except for eDP DPRXs). TPS4 support declaration (by setting this bit) is required for all HBR3-capable DPRXs. DPRXs should support TPS4 and set this bit, regardless of whether the DPRX supports HBR3 because TPS4 is more conducive to robust link establishment than TPS2 and TPS3.	

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
02204h	**NORP & DP_PWR_VOLTAGE_CAP** ***Note:*** *When bits 7:5 are cleared to 000 (binary), the downstream device is capable of producing the default 3.3V DP_PWR setting DP_PWR only. A downstream DP device that is capable of generating DP_PWR voltage higher than the default 3.3V DP_PWR setting shall complete the voltage level transition within 1ms. During the transition, the DP device shall not generate a voltage exceeding the voltage range of the higher of the two voltage levels between which the switching is taking place.*			Read Only
		0	**NORP** Number of Receiver Ports = Value + 1. 0 = One receiver port. 1 = Two or more receiver ports (see Note below). For SST mode, the maximum number is two (for which this bit is set to 1), one for an uncompressed video stream and the other for its associated audio stream. The receiver can simultaneously receive up to "NORP" isochronous streams. The smallest available Receiver Port number is assigned. For example, when there is only one receiver port, the receiver port is assigned to Receiver Port 0. Receiver Port 1 shall be assigned only after Receiver Port 0 has already been assigned. ***Note:*** *An MST Sink device might have more than two receiver ports because it can have three or more stream sinks. However, an MST Sink device shall program this bit according to the number of receiver ports when it is operating in SST mode. The MST Sink device shall operate in SST mode to interoperate with an SST upstream device.* *A Topology Manager in an MST Source device shall use the LINK_ADDRESS and REMOTE_DPCD message transactions to discover the number of receiver ports, rather than relying on this bit.*	
		4:1	**RESERVED**	Read all 0s

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
02204h		5	**5V_DP_PWR_CAP** 0 = Downstream device is not capable of producing +4.9 to +5.5V on its DP connector's DP_PWR pin. 1 = Downstream device is capable of producing +4.9 to +5.5V on its DP connector's DP_PWR pin.	Read Only
		6	**12V_DP_PWR_CAP** 0 = Downstream device is not capable of producing +12V ±10% on its DP connector's DP_PWR pin. 1 = Downstream device is capable of producing +12V ±10% on its DP connector's DP_PWR pin.	
		7	**18V_DP_PWR_CAP** 0 = Downstream device is not capable of producing +18V ±10% on its DP connector's DP_PWR pin. 1 = Downstream device is capable of producing +18V ±10% on its DP connector's DP_PWR pin.	

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
02205h	**DOWN_STREAM_PORT_PRESENT**			Read Only
		0	**DFP_PRESENT** 1 = Device is a Branch device and has downstream-facing port(s) (DFP(s)).	
		2:1	**DFP_TYPE** Indicates the DFP type of DFP 0. 00b = DisplayPort. 01b = Analog VGA or analog video over DVI-I. 10b = DVI, HDMI, or DP++. 11b = Others (this DFP type might not have a DisplayID or legacy EDID in the Sink device (e.g., Sink devices on composite video and S-Video ports do not have a DisplayID or legacy EDID, but Sink devices on a wireless or USB interface might)). A Branch device shall provide more-detailed Downstream enumeration data on all its DFPs, including DFP 0 at DPCD Addresses 00080h through 0008Fh. ***Note:*** *Further mandates for Branch devices are provided in Section 5.3.3. Mandates for Source devices when transmitting through a Branch device are provided in Section 5.1.6.*	
		3	**FORMAT_CONVERSION** 0 = This Branch device does not have a format conversion block. 1 = This DFP has a format conversion block. ***Notes:*** *1 Applicable only to a Branch device.* *2 Topology Manager in an MST Source device shall use the LINK_ADDRESS message transaction to discover the DFP capability, rather than relying on this bit.*	
		4	**DETAILED_CAP_INFO_AVAILABLE** 0 = DFP capability field is 1 byte/port, starting from DPCD Address 00080h. 1 = DFP capability field is 4 bytes/port for the detailed capability description, starting from DPCD Address 00080h. Detailed capability information shall be supported.	
		7:5	**RESERVED**	Read all 0s

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
02206h	**MAIN_LINK_CHANNEL_CODING_CAP** Updated in *DP v2.0*. The DPRX shall revert to 8b/10b Link Layer when a power-on reset or upstream device disconnect occurs. 0 = Not supported. 1 = Supported.			Read Only
		0	**8b/10b_SUPPORTED** Mandated to be set to 1.	
		1	**128b/132b_SUPPORTED** Set to 1 for DPRX that supports 128b/132b Link Layer.	
		7:2	**RESERVED**	Read all 0s
02207h	**DOWN_STREAM_PORT_COUNT**			Read Only
		3:0	**DFP_COUNT** Value = Number of DFPs. 0h = No DFPs. DFP type and capability are enumerated at DPCD Addresses 00080h through 0008Fh.	
		5:4	**RESERVED**	Read all 0s
		6	**MSA_TIMING_PAR_IGNORED** Applies to eDP and box-to-box DP. 0 = Sink device needs MSA timing parameters HTotal[15:0], HStart[15:0], HSyncPolarity[0] (HSP), HSyncWidth[14:0] (HSW), VTotal[15:0], VStart[15:0], VSyncPolarity[0] (VSP), and VSyncWidth[14:0] (VSW) to be transmitted by the Source device for rendering the incoming video stream. 1 = Sink device is capable of rendering the incoming video stream without the above-mentioned MSA timing parameters.	Read Only
		7	**OUI Support** 0 = OUI is not supported. 1 = OUI is supported (for DPCD r1.2 and DPCD r1.4, OUI and Device Identification shall be supported). Sink device IEEE_OUI registers (DPCD Addresses 00400h through 00402h), plus DPCD Addresses 00403h through 0040Bh for device identification. Branch device IEEE_OUI registers (DPCD Addresses 00500h through 00502h), plus DPCD Addresses 00503h through 0050Bh for device identification.	

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
02208h	**RECEIVE_PORT0_CAP_0** Receiver Port 0 Capability 0. ***Note:*** *A Source device that is operating in MST mode does* ***not*** *use this register.*			Read Only
		0	**RESERVED**	Read all 0s
		1	**LOCAL_EDID_PRESENT** 0 = This receiver port does not have a local DisplayID or legacy EDID. 1 = This receiver port has a local DisplayID or legacy EDID. A local DisplayID or legacy EDID shall be supported for Sink devices and format converters.	Read Only
		2	**ASSOCIATED_TO_PRECEDING_PORT** 0 = This port is used for the main isochronous stream. This bit shall always be cleared to 0 for Receiver Port 0. 1 = This port is used for the secondary isochronous stream of the main video stream that is received in the preceding port.	
		7:3	**RESERVED**	Read all 0s
02209h	**RECEIVE_PORT0_CAP_1** Receiver Port 0 Capability 1. ***Note:*** *A Source device that is operating in MST mode does* ***not*** *use this register.*			Read Only
		7:0	**BUFFER_SIZE** Buffer size = (Value + 1) × 32 bytes/lane. The maximum is 8KB/lane.	
0220Ah	**RECEIVE_PORT1_CAP_0** Receiver Port 1 Capability 0. Bit definition is identical to the RECEIVE_PORT0_CAP_0 register (DPCD Address 02208h), but for Port 1. ***Notes:*** *1 When Receiver Port 1 is not present, this register is read all 0s.* *2 A Source device that is operating in MST mode does* ***not*** *use this register.*			Read Only

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
0220Bh	**RECEIVE_PORT1_CAP_1** Receiver Port 1 Capability 1. Bit definition is identical to the RECEIVE_PORT0_CAP_1 register (DPCD Address 02209h), but for Port 1. ***Notes:*** *1 When Receiver Port 1 not present, this register is read all 0s.* *2 A Source device that is operating in MST mode does **not** use this field.*			Read Only
0220Ch	**I^2C Speed Control Capabilities Bit Map**			Read Only
		7:0	Bit or bits set to indicate I^2C speed control capabilities. Source control of the I^2C speed should be supported when the DPRX implements a physical I^2C bus. If the DPRX does not implement a physical I^2C bus, this register is cleared to 00h. Otherwise, if the DPRX does not provide source control of the I^2C speed, this register is also cleared to 00h. In this case the DPRX, upon receiving an I^2C-over-AUX transaction, generates an I^2C transaction at the I^2C bit rate of its choice. Otherwise, bit values in this register are assigned to I^2C speeds. 01h = 1Kbps. 10h = 400Kbps. 02h = 5Kbps. 20h = 1Mbps. 04h = 10Kbps. 40h = RESERVED. 08h = 100Kbps. 80h = RESERVED.	

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
0220Dh	**eDP_CONFIGURATION_CAP** Always reads 00h for external receivers. Read only for eDP DPRXs.			Read Only
		0	**ALTERNATE_SCRAMBLER_RESET_CAPABLE** 1 = Indicates that this is an eDP device that can use the eDP alternate scrambler reset value of FFFEh.	
		1	**RESERVED** (Deprecated FRAMING_CHANGE option for eDP.)	Read all 0s
		7:2	**RESERVED for eDP**	
0220Eh	**8b/10b_TRAINING_AUX_RD_INTERVAL**			Read Only
		6:0	**TRAINING_AUX_RD_INTERVAL** Link Status/Adjust Request read interval during Main-Link training sequences. All other values are RESERVED.	
			Value / **LANE*x*_CR_DONE (Minimum)** / **LANE*x*_CHANNEL_EQ_DONE** 00h / 100us / 400us 01h / 100us / 4ms 02h / 100us / 8ms 03h / 100us / 12ms 04h / 100us / 16ms	
		7	**EXTENDED_RECEIVER_CAPABILITY_FIELD_PRESENT** 0 = Not present. 1 = Present at DPCD Addresses 02200h through 022FFh. A DPCD r1.4 (or higher) DPRX shall have an Extended Receiver Capability field.	

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
0220Fh	**ADAPTER_CAP** Capabilities of Branch devices that adapt to legacy video transports.			Read Only
		0	**FORCE_LOAD_SENSE_CAP** 0 = Does not support VGA force load adapter sense mechanism. 1 = Supports VGA force load adapter sense mechanism.	
		1	**ALTERNATE_I2C_PATTERN_CAP** 0 = Does not support alternate I^2C patterns. 1 = Supports alternate I^2C patterns.	
		7:2	**RESERVED**	Read all 0s
02210h	**DPRX_FEATURE_ENUMERATION_LIST** Support for bits 7:4 and 1 added in *DP v1.4*. 0 = Not supported. 1 = Supported.			Read Only
		0	**GTC_CAP** A DPRX indicates support for the GTC feature by setting this bit. The GTC feature is defined in Section 2.16.	
		1	**SST_SPLIT_SDP_CAP** A DPRX indicates support for SDP splitting in SST mode by setting this bit. The SST mode SDP Splitting feature is defined in Section 2.2.5.13. This bit shall always be set to 1 in all new designs.	
		2	**AV_SYNC_CAP** A DP device indicates support of the AV Sync capability through audio delay insertion by setting this bit. The AV Sync feature is defined in Section 2.15.	
		3	**VSC_SDP_EXTENSION_FOR_COLORIMETRY_SUPPORTED** A DP Source device, upon detecting this bit being set to 1 by a DP Sink device, can set the MSA MISC1 field, bit 6, to 1 to indicate that pixel encoding format and colorimetry format are indicated in the VSC SDP.	

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
02210h		4	**VSC_EXT_VESA_SDP_SUPPORTED**	Read Only
		5	**VSC_EXT_VESA_SDP_CHAINING_SUPPORTED** Shall support up to 64 VSC_EXT_VESA SDP chaining for DP Sink devices that support chaining. DP Sink devices that support more than 64 SDPs of chaining indicate the maximum chaining count beyond 64 in the VSC_EXT_VESA_SDP_MAX_CHAINING_COUNT field in the VSC_EXT_VESA_SDP_MAX_CHAINING register (DPCD Address 02212h, bits 7:0).	
		6	**VSC_EXT_CTA_SDP_SUPPORTED**	
		7	**VSC_EXT_CTA_SDP_CHAINING_SUPPORTED** Shall support up to 64 VSC_EXT_CTA SDP chaining for DP Sink devices that support chaining. DP Sink devices that support more than 64 SDPs of chaining indicate the maximum chaining count beyond 64 in the VSC_EXT_CTA_SDP_MAX_CHAINING_COUNT field in the VSC_EXT_CTA_SDP_MAX_CHAINING register (DPCD Address 02213h, bits 7:0).	
02211h	**EXTENDED_DPRX_SLEEP_WAKE_TIMEOUT_REQUEST**			Read Only
		7:0	**DPRX_SLEEP_WAKE_TIMEOUT_PERIOD** 00h = 1ms. 03h = 60ms. 01h = 20ms. 04h = 80ms. 02h = 40ms. 05h = 100ms. All other values are RESERVED. A downstream DP device (including a DP Sink device) shall request the minimum timeout duration that it is capable of supporting.	
02212h	**VSC_EXT_VESA_SDP_MAX_CHAINING** New to *DP v1.4*.			Read Only
		7:0	**VSC_EXT_VESA_SDP_MAX_CHAINING_COUNT** When the VSC_EXT_VESA_SDP_SUPPORTED bit in the DPRX_FEATURE_ENUMERATION_LIST register (DPCD Address 02210h, bit 5) is set to 1, a DP Sink device supports the maximum number of SDP chaining equal to 64 plus the value in this register.	
02213h	**VSC_EXT_CTA_SDP_MAX_CHAINING** New to *DP v1.4*.			Read Only
		7:0	**VSC_EXT_CTA_SDP_MAX_CHAINING_COUNT** When the VSC_EXT_CTA_SDP_SUPPORTED bit in the DPRX_FEATURE_ENUMERATION_LIST register (DPCD Address 02210h, bit 7) is set to 1, a DP Sink device supports the maximum number of SDP chaining equal to 64 plus the value in this register.	

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
02214h	**ADAPTIVE_SYNC_CAPABILITY** New to *DP v1.4a*.			Read Only
		0	**ADAPTIVE_SYNC_SDP_SUPPORTED** 0 = Not supported. 1 = Supported.	
		7:1	**RESERVED**	Read all 0s
02215h	**128b/132b_SUPPORTED_LINK_RATES** New to *DP v2.0*. Valid only when the 128b/132b_SUPPORTED field in the MAIN_LINK_CHANNEL_CODING_CAP register (DPCD Address 02206h, bit 1) is set to 1, for 128b/132b Link Layer. The DPRX shall revert to 8b/10b Link Layer when a power-on reset or upstream device disconnect occurs.			Read Only
		0	**10Gbps/lane Support** Link rate associated with UHBR10. 0 = Not supported. 1 = Supported. Support for this link rate is mandated for 128b/132b Link Layer-capable DP devices.	
		1	**20Gbps/lane Support** Link rate associated with UHBR20. 0 = Not supported. 1 = Supported. Highest link rate available. Support is **optional**.	
		2	**13.5Gbps/lane Support** Link rate associated with UHBR13.5. 0 = Not supported. 1 = Supported. Support is **optional**. ***Note:*** *Support for 13.5Gbps/lane is **optional**, even for a DPRX that supports 20Gbps/lane.*	
		7:3	**RESERVED**	Read all 0s

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register					Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field			
02216h	**128b/132b_TRAINING_AUX_RD_INTERVAL** New to *DP v2.0*. Valid only for 128b/132b Link Layer. Shall be cleared to 00h when operating in 8b/10b Link Layer.					Read Only
		6:0	**128b/132b_TRAINING_AUX_RD_INTERVAL** Link Status/Adjust Request read interval during Main-Link training sequences. All other values are RESERVED.			
			Value	**LANE*x*_CR_DONE (Minimum)**	**LANE*x*_CHANNEL_EQ_DONE**	
			00h	100us	400us	
			01h	100us	4ms	
			02h	100us	8ms	
			03h	100us	12ms	
			04h	100us	16ms	
			05h	100us	32ms	
			06h	100us	64ms	
		7	**RESERVED**			Read 0
02217h through 0222Fh	**RESERVED for Extended Receiver Capability**					Read all 0s
02230h through 02250h	**TEST_264BIT_CUSTOM_PATTERN** Stores the 264-bit custom pattern for Source device compliance measurements (the LSB is transmitted first).					Read Only
	0	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE7:0**			
	1	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE15:8**			
	2	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE23:16**			
	3	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE31;24**			
	4	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE39:32**			
	5	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE47:40**			
	6	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE55:48**			
	7	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE63:56**			

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
02230h through 02250h	8	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE71:64**	Read Only
	9	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE79:72**	
	10	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE87:80**	
	11	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE95:88**	
	12	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE103:96**	
	13	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE111:104**	
	14	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE119:112**	
	15	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE127:120**	
	16	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE135:128**	
	17	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE143:136**	
	18	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE151:144**	
	19	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE159:152**	
	20	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE167:160**	
	21	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE175:168**	
	22	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE183:176**	
	23	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE191:184**	
	24	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE199:192**	
	25	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE207:200**	
	26	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE215:208**	
	27	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE223:216**	
	28	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE231:224**	
	29	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE239:232**	
	30	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE247:240**	
	31	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE255:248**	
	32	7:0	**TEST_264BIT_CUSTOM_PATTERN_VALUE263:256**	

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
02251h	**CONTINUOUS_264BIT_PATTERN_FROM_DPRX_AUX_CH_CAPABILITY** New to *DP v2.0*.			Read Only
		0	**CONTINUOUS_264BIT_PATTERN_FROM_DPRX_AUX_CH_CAP** 0 = Not supported. 1 = Supported.	
		7:1	**RESERVED**	Read all 0s
02252h	**CONTINUOUS_264BIT_PATTERN_FROM_DPRX_AUX_CH_CTRL** New to *DP v2.0*.			Read/ Write
		0	**CONTINUOUS_264BIT_PATTERN_FROM_DPRX_AUX_CH_EN** The DPRX shall clear this bit when either of the following occurs: • Duration expiration –or– • Detection of an upstream DP device disconnect 0 = Disable continuous transmission of the 80-bit pattern programmed by the TEST_264BIT_CUSTOM_PATTERN register (DPCD Addresses 02230h through 02250h). 1 = Enable continuous transmission of the 80-bit pattern programmed by the TEST_264BIT_CUSTOM_PATTERN register. While the transmission is enabled, AUX transactions over the AUX_CH are unavailable.	
		2:1	**DURATION_CTRL** 00b = 15sec. 10b = 60sec. 01b = 30sec. 11b = 120sec.	
		7:3	**RESERVED**	Read all 0s
02253h through 022FFh	**RESERVED for Extended Receiver Capability**			Read all 0s

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
DSC Register Set – DSC Extended Capability Branch Total DSC Resources				
02260h	**DSC SUPPORT AND DSC DECODER COUNT** ***Note:*** *Available only in the UFP DPCD registers.* New to *DP v2.0*. See Section 2.10.1.2 for additional details.			Read Only
		0	**DSC Support** ***Note:*** *Support is mandated for DP Branch devices that have a 128b/132b channel coding-capable UFP.* *Value shall be mirrored to the UFP's DPCD Address 00060h, bit 0.* 0 = Decompression using DSC is not supported. 1 = Decompression using DSC is supported.	
		1	**DSC Pass-through Support** ***Notes:*** *Support is mandated for DP Branch devices that have a 128b/132b channel coding-capable UFP.* *Value shall be mirrored to the UFP's DPCD Address 00060h, bit 1.* 0 = DSC bitstream pass-through is not supported. 1 = DSC bitstream pass-through is supported. See Section 2.8.8 for details.	
		2	**Dynamic PPS Update Support – Compressed-to-Compressed** ***Notes:*** *Support is mandated for DP Branch devices that have a 128b/132b channel coding-capable UFP.* *Value shall be mirrored to the UFP's DPCD Address 00060h, bit 2.* 0 = Dynamic PPS update is not supported. 1 = Dynamic PPS update is supported. The device supports compressed frame-to-compressed frame update of the DSC bitstream target bits/pixel, as indicated by the PPS SDP, without a visual glitch.	
		3	**Dynamic PPS Update Support – Uncompressed-to/from-Compressed** New to *DP v2.0*. ***Note:*** *Support is mandated for DP Branch devices that have a 128b/132b channel coding-capable UFP.* 0 = Dynamic PPS update is not supported. 1 = Dynamic PPS update is supported. The device supports uncompressed frame-to/from-compressed frame update of the DSC bitstream target bits/pixel, as indicated by the PPS SDP, without a visual glitch.	
		4	**RESERVED**	Read all 0s
		7:5	**DSC Decoder Count** Valid only when bit 0 (DSC Support) is set to 1. The DSC decoder count is the value + 1, thus supporting the DSC decoder count ranging from 0 (bit 0 = 0) to 8 (bit 0 = 1, bits 7:5 = 111b).	Read Only

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
02261h	**DSC ALGORITHM REVISION** ***Notes:*** *Available only in the UFP DPCD registers.* *Common for all DSC decoders within a device.* *Value shall be mirrored to the UFP's DPCD Address 00061h.* *DSC Version Major and DSC Version Minor field values are 1h and 2h, respectively, for both DSC v1.2 and DSC v1.2a.* New to *DP v2.0*. See Section 2.10.1.2 for additional details.			Read Only
		3:0	**DSC Version Major** Indicates the major version of DSC.	
		7:4	**DSC Version Minor** Indicates the minor version of DSC.	
02262h	**DSC RC BUFFER BLOCK SIZE** ***Notes:*** *Available only in the UFP DPCD registers.* *Common for all DSC decoders within a device.* *Value shall be 00h because an RC Buffer Block size greater than 1KB is **not** needed.* *Value shall be mirrored to the UFP's DPCD Address 00062h.* New to *DP v2.0*. See Section 2.10.1.2 for additional details.			Read Only
		1:0	**RC Buffer Block Size** Rate control buffer block size. 00b = 1KB (see Notes). 10b = 16KB. 01b = 4KB. 11b = 64KB.	
		7:2	**RESERVED**	Read all 0s

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
02263h	**DSC RC BUFFER SIZE** ***Notes:*** *Available only in the UFP DPCD registers.* *Common for all DSC decoders within a device.* *Value shall be mirrored to the UFP's DPCD Address 00063h.* New to *DP v2.0*. See Section 2.10.1.2 for additional details.			Read Only
		7:0	**Each Rate Buffer Size, in Units of Blocks** Buffer size (in blocks) = value + 1. Actual buffer size is calculated by multiplying the RC buffer size (in blocks) and the block size indicated by the RC Buffer Block Size field in the DSC RC BUFFER BLOCK SIZE register (DPCD Address 02262h, bits 1:0). **Example** – If the RC Buffer Block Size is programmed to 11b (64KB) and the rate buffer size (in blocks) is 01111111b (128), each rate buffer size = 64KB × 128 = 8MB. ***Note:*** *Value is as specified in DSC Standard, Table E-1. It is the maximum algorithmic rate buffer size (`minRateBufferSize`) that the Sink device may support and is used by the Source device to ensure that the hrdDelay mandate is met.*	

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
02264h	**DSC SLICE CAPABILITIES 1** ***Notes:*** *Available only in the UFP DPCD registers.* *Value shall be mirrored to the UFP's DPCD Address 00064h.* New to *DP v2.0*. See Section 2.10.1.2 for additional details. Valid only when the DSC decoder count is 1 (i.e., DSC Support bit in the DSC SUPPORT AND DSC DECODER COUNT register (DPCD Address 02260h, bit 0) is set to 1, and the same register's DSC Decoder Count field (bits 7:5) is cleared to 000b). Used in combination with the DSC SLICE CAPABILITIES 2 register (DPCD Address 0226Dh) to indicate the number of slices across a horizontal line that the DP DSC Sink device can support. 0 = Number of slices across a horizontal line per DP DSC Sink device is not supported. 1 = Number of slices across a horizontal line per DP DSC Sink device is supported.			Read Only
		0	**1_Slice_per_DP_DSC_Sink_Device**	
		1	**2_Slices_per_DP_DSC_Sink_Device**	
		2	**RESERVED**	Read 0
		3	**4_Slices_per_DP_DSC_Sink_Device**	Read Only
		4	**6_Slices_per_DP_DSC_Sink_Device** ***Note:*** *This value is not included as part of the standard slice value number set. A DP DSC Sink device may declare support of this number of slices across a horizontal line as an additional available configuration.*	
		5	**8_Slices_per_DP_DSC_Sink_Device**	
		6	**10_Slices_per_DP_DSC_Sink_Device** ***Note:*** *This value is not included as part of the standard slice value number set. A DP DSC Sink device may declare support of this number of slices across a horizontal line as an additional available configuration.*	
		7	**12_Slices_per_DP_DSC_Sink_Device**	

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
02265h	**DSC LINE BUFFER BIT DEPTH** ***Notes:*** *Available only in the UFP DPCD registers.* *Common for all DSC decoders within a DP Branch device.* *Value shall be mirrored to the UFP's DPCD Address 00065h.* New to *DP v2.0*. See Section 2.10.1.2 for additional details.			Read Only
		3:0	**Line Buffer Bit Depth** Contains the bit depth used by the Sink device to store the reconstructed pixels within the line buffer. 0000b = 9 bits. 0101b = 14 bits. 0001b = 10 bits. 0110b = 15 bits. 0010b = 11 bits. 0111b = 16 bits. 0011b = 12 bits. 1000b = 8 bits. 0100b = 13 bits. All other values are RESERVED.	
		7:4	**RESERVED**	Read all 0s
02266h	**DSC FEATURE SUPPORT** ***Notes:*** *Available only in the UFP DPCD registers.* *Common for all DSC decoders within a DP Branch device.* *Value shall be mirrored to the UFP's DPCD Address 00066h.* New to *DP v2.0*. See Section 2.10.1.2 for additional details. 0 = Not supported. 1 = Supported.			Read Only
		0	**DSC Block Prediction Support**	
		1	**RGB Color Conversion Bypass Support** New to *DP v2.0*.	
		7:2	**RESERVED**	Read all 0s

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
02267h and 02268h	**MAXIMUM *bits_per_pixel* SUPPORTED BY THE DECOMPRESSOR** ***Note:*** ***For DP v1.4a (and lower) and eDP v1.4b (and lower), this register is not used and shall be cleared to all 0s.*** Used by embedded displays with *DP v2.0* (and higher). Indicates the maximum ***bits_per_pixel*** that the DP DSC Sink device supports. Format is U6.4 (unsigned, four fractional bits).			
	For *DP v1.4a* (and lower) and *eDP v1.4b* (and lower)			Read all 0
	0	7:0	**RESERVED**	
	1	7:0	**RESERVED**	
	For *DP v2.0* (and higher)			Read Only
	Notes: *Available only in the UFP DPCD registers.* *Common for all DSC decoders within a DP Branch device.* *Value shall be mirrored to the UFP's DPCD Addresses 00067h and 00068h.* *If cleared to all 0s, use the* ***Maximum Allowed Bit Rate*** *values in Table 2-153.* New to *DP v2.0*. See Section 2.10.1.2 for additional details.			
	0	7:0	***bits_per_pixel*7:0** Contains the least significant eight bits of the maximum ***bits_per_pixel*** that the DP DSC Sink device supports.	
	1	1:0	***bits_per_pixel*9:8** Contains the most significant two bits of the maximum ***bits_per_pixel*** that the DP DSC Sink device supports.	
		4:2	**RESERVED**	Read all 0s
		6:5	**MAX_BPP_DELTA_VERSION** 00b = Version 1. All other values are RESERVED.	Read Only
		7	**MAX_BPP_DELTA_AVAILABILITY** 0 = Not available. 1 = Available at DPCD Addresses 0006Eh (bits 7:0) and 0006Fh (bits 6:3).	

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
02269h	**DSC DECODER PIXEL ENCODING FORMAT CAPABILITY** ***Notes:*** *Available only in the UFP DPCD registers.* *Common for all DSC decoders within a DP Branch device.* *Value shall be mirrored to the UFP's DPCD Address 00069h.* New to *DP v2.0*. See Section 2.10.1.2 for additional details. 0 = Not supported. 1 = Supported.			Read Only
		0	**RGB Support** Support for RGB is mandatory.	
		1	**YCbCr 4:4:4 Support**	
		2	**YCbCr Simple 4:2:2 Support**	
		3	**YCbCr Native 4:2:2 Support** Native 4:2:2 mode is supported by *DSC v1.2* or higher.	
		4	**YCbCr Native 4:2:0 Support** Native 4:2:0 mode is supported by *DSC v1.2a* or higher.	
		7:5	**RESERVED**	Read all 0s
0226Ah	**DSC DECODER COLOR DEPTH CAPABILITY** ***Notes:*** *Available only in the UFP DPCD registers.* *Common for all DSC decoders within a DP Branch device.* *Value shall be mirrored to the UFP's DPCD Address 0006Ah.* New to *DP v2.0*. See Section 2.10.1.2 for additional details. 0 = Not supported. 1 = Supported.			Read Only
		0	**RESERVED**	Read 0
		1	**8 Bits/component Support** Support for 8bpc is mandatory.	Read Only
		2	**10 Bits/component Support**	
		3	**12 Bits/component Support**	
		7:4	**RESERVED**	Read all 0s

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
0226Bh	**DSC Peak Throughput** ***Notes:*** *Available only in the UFP DPCD registers.* *Common for all DSC decoders within a DP Branch device.* *Value shall be mirrored to the UFP's DPCD Address 0006Bh.* New to *DP v2.0*. See Section 2.10.1.2 for additional details.			Read Only
		3:0	**Throughput Mode 0** Decoding of 3 pixels/clock (in MP/s) for 4:4:4 and Simple 4:2:2 modes. Values are indicated in decimal. 0 = Not supported. 8 = 700MP/s. 1 = 340MP/s. 9 = 750MP/s. 2 = 400MP/s. 10 = 800MP/s. 3 = 450MP/s. 11 = 850MP/s. 4 = 500MP/s. 12 = 900MP/s. 5 = 550MP/s. 13 = 950MP/s. 6 = 600MP/s. 14 = 1000MP/s. 7 = 650MP/s. 15 = 170MP/s (test or custom use only).	
		7:4	**Throughput Mode 1** Decoding of 6 pixels/clock (in MP/s) for Native 4:2:2 (*DSC v1.2* and higher) and Native 4:2:0 modes (*DSC v1.2a* and higher). Values are indicated in decimal. 0 = Not supported. 8 = 700MP/s. 1 = 340MP/s. 9 = 750MP/s. 2 = 400MP/s. 10 = 800MP/s. 3 = 450MP/s. 11 = 850MP/s. 4 = 500MP/s. 12 = 900MP/s. 5 = 550MP/s. 13 = 950MP/s. 6 = 600MP/s. 14 = 1000MP/s. 7 = 650MP/s. 15 = 170MP/s (test or custom use only).	Read Only

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
0226Ch	**DSC Maximum Slice Width** ***Notes:*** *Available only in the UFP DPCD registers.* *Value shall be mirrored to the UFP's DPCD Address 0006Ch.* New to *DP v2.0*. See Section 2.10.1.2 for additional details. MaxSliceWidth = Number of pixels × 320. The minimum number allowed is 8 (2560 pixels).			Read Only
0226Dh	**DSC SLICE CAPABILITIES 2** ***Notes:*** *Available only in the UFP DPCD registers.* *Value shall be mirrored to the UFP's DPCD Address 0006Dh.* New to *DP v2.0*. See Section 2.10.1.2 for additional details. Valid only when the DSC decoder count is 1 (i.e., DSC Support bit in the DSC SUPPORT AND DSC DECODER COUNT register (DPCD Address 02260h, bit 0) is set to 1, and the same register's DSC Decoder Count field (bits 7:5) is greater than or equal to 000b). Used in combination with the DSC SLICE CAPABILITIES 1 register (DPCD Address 02264h) to indicate the number of slices across a horizontal line that the DP DSC Sink device can support. 0 = Number of slices across a horizontal line per DP DSC Sink device is not supported. 1 = Number of slices across a horizontal line per DP DSC Sink device is supported.			Read Only
		0	**16_Slices_per_DP_DSC_Sink_Device**	
		1	**20_Slices_per_DP_DSC_Sink_Device**	
		2	**24_Slices_per_DP_DSC_Sink_Device**	
		7:3	**RESERVED**	Read all 0s

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
0226Eh and 0226Fh	**DSC_MAX_BPP_DELTA_AND_BPP_INCREMENT** ***Notes:*** ***For DP v1.4a (and lower) and eDP v1.4b (and lower), this register is not used and shall be cleared to all 0s.***			
	For *DP v1.4a* (and lower) and *eDP v1.4b* (and lower)			Read all 0s
	0	7:0	**RESERVED**	
	1	7:0	**RESERVED**	
	For *DP v2.0* (and higher)			Read Only
	Notes: *Available only in the UFP DPCD registers.* *Common for all DSC decoders within a DP Branch device.* *Value shall be mirrored to the UFP's DPCD Addresses 0006Eh and 0006Fh.* New to *DP v2.0*. See Section 2.10.1.2 for additional details.			
	0	4:0	**For MAX_BPP_DELTA Version 1:** **RGB_YCbCr444_SimpleYCbCr422_MAX_BPP_DELTA** 0 = Maximum allowed range (= the maximum bpc × 3). 1 = 16bpp. 2 = 17bpp. … 21 = 36bpp. 22 through 31 = RESERVED. All other version numbers are RESERVED.	
		7:5	**For MAX_BPP_DELTA Version 1:** **NativeYCbCr420_MAX_BPP_DELTA** 0 = Maximum allowed range (= the maximum bpc × 1.5). 1 = 12bpp. 2 = 13bpp. … 7 = 18bpp. All other version numbers are RESERVED.	
	1	2:0	**INCREMENT OF *bits_per_pixel* SUPPORTED BY THE DECOMPRESSOR** Indicates the ***bits_per_pixel*** precision that the DP DSC Sink device supports. 000b = 1/16bpp. 011b = 1/2bpp. 001b = 1/8bpp. 100b = 1bpp. 010b = 1/4bpp. All other values are RESERVED.	
		6:3	**For MAX_BPP_DELTA Version 1:** **NativeYCbCr422_MAX_BPP_DELTA** 0 = Maximum allowed range (= the maximum bpc × 2). 1 = 16bpp. 2 = 17bpp. … 9 = 24bpp. 10 through 15 = RESERVED. All other version numbers are RESERVED.	
		7	**RESERVED**	Read 0

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
02270h	**DSC_MAX_SLICE_COUNT_AND_AGGREGATION_0** ***Note:*** *Available only in the UFP DPCD registers.* New to *DP v2.0*. See Section 2.10.1.2 for additional details. Valid only when the DSC decoder count is 2 or more (i.e., DSC Support bit in the DSC SUPPORT AND DSC DECODER COUNT register (DPCD Address 02260h, bit 0) is set to 1, and the same register's DSC Decoder Count field (bits 7:5) is greater than or equal to 001b).			Read Only
		0	**DSC Decoder 0 Maximum Slice Count** 0 = Two slices, supporting 2- and 1-slice configurations. 1 = Four slices, supporting 4, 2-, and 1-slice configurations.	
		3:1	**DSC Decoder 0 Aggregation Support** 000b = Aggregation with the other DSC decoder(s) is not supported. *N* (not equal to 000b) = Aggregation with DSC Decoder *N* is supported.	
		4	**DSC Decoder 1 Maximum Slice Count** 0 = Two slices, supporting 2- and 1-slice configurations. 1 = Four slices, supporting 4, 2-, and 1-slice configurations.	
		7:5	**DSC Decoder 1 Aggregation Support** 001b = Aggregation with the other DSC decoder(s) is not supported. *N* (not equal to 001b) = Aggregation with DSC Decoder *N* is supported.	

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
02271h	**DSC_MAX_SLICE_COUNT_AND_AGGREGATION_1** ***Note:*** *Available only in the UFP DPCD registers.* New to *DP v2.0*. See Section 2.10.1.2 for additional details. Bits 3:0 are valid only when the DSC decoder count is 3 or more (i.e., DSC Support bit in the DSC SUPPORT AND DSC DECODER COUNT register (DPCD Address 02260h, bit 0) is set to 1, and the same register's DSC Decoder Count field (bits 7:5) is greater than or equal to 010b). Bits 7:4 are valid only when the DSC decoder count is 4 or more (i.e., DSC Support bit in the DSC SUPPORT AND DSC DECODER COUNT register (DPCD Address 02260h, bit 0) is set to 1, and the same register's DSC Decoder Count field (bits 7:5) is greater than or equal to 011b).			Read Only
		0	**DSC Decoder 2 Maximum Slice Count** 0 = Two slices, supporting 2- and 1-slice configurations. 1 = Four slices, supporting 4, 2-, and 1-slice configurations.	
		3:1	**DSC Decoder 2 Aggregation Support** 010b = Aggregation with the other DSC decoders is not supported. *N* (not equal to 010b) = Aggregation with DSC Decoder *N* is supported.	
		4	**DSC Decoder 3 Maximum Slice Count** 0 = Two slices, supporting 2- and 1-slice configurations. 1 = Four slices, supporting 4, 2-, and 1-slice configurations.	
		7:5	**DSC Decoder 3 Aggregation Support** 011b = Aggregation with the other DSC decoders is not supported. *N* (not equal to 011b) = Aggregation with DSC Decoder *N* is supported.	

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
02272h	**DSC_MAX_SLICE_COUNT_AND_AGGREGATION_2** ***Note:*** *Available only in the UFP DPCD registers.* New to *DP v2.0*. See Section 2.10.1.2 for additional details. Bits 3:0 are valid only when the DSC decoder count is 5 or more (i.e., DSC Support bit in the DSC SUPPORT AND DSC DECODER COUNT register (DPCD Address 02260h, bit 0) is set to 1, and the same register's DSC Decoder Count field (bits 7:5) is greater than or equal to 100b). Bits 7:4 are valid only when the DSC decoder count is 6 or more (i.e., DSC Support bit in the DSC SUPPORT AND DSC DECODER COUNT register (DPCD Address 02260h, bit 0) is set to 1, and the same register's DSC Decoder Count field (bits 7:5) is greater than or equal to 101b).			Read Only
		0	**DSC Decoder 4 Maximum Slice Count** 0 = Two slices, supporting 2- and 1-slice configurations. 1 = Four slices, supporting 4, 2-, and 1-slice configurations.	
		3:1	**DSC Decoder 4 Aggregation Support** 100b = Aggregation with the other DSC decoders is not supported. *N* (not equal to 100b) = Aggregation with DSC Decoder *N* is supported.	
		4	**DSC Decoder 5 Maximum Slice Count** 0 = Two slices, supporting 2- and 1-slice configurations. 1 = Four slices, supporting 4, 2-, and 1-slice configurations.	
		7:5	**DSC Decoder 5 Aggregation Support** 100b = Aggregation with the other DSC decoders is not supported. *N* (not equal to 101b) = Aggregation with DSC Decoder *N* is supported.	

Table 2-193: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02000h through 022FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Extended Receiver Capability Field	
02273h	**DSC_MAX_SLICE_COUNT_AND_AGGREGATION_3** ***Note:*** *Available only in the UFP DPCD registers.* New to *DP v2.0*. See Section 2.10.1.2 for additional details. Bits 3:0 are valid only when the DSC decoder count is 7 or more (i.e., DSC Support bit in the DSC SUPPORT AND DSC DECODER COUNT register (DPCD Address 02260h, bit 0) is set to 1, and the same register's DSC Decoder Count field (bits 7:5) is greater than or equal to 110b). Bits 7:4 are valid only when the DSC decoder count is 8 (i.e., DSC Support bit in the DSC SUPPORT AND DSC DECODER COUNT register (DPCD Address 02260h, bit 0) is set to 1, and the same register's DSC Decoder Count field (bits 7:5) is equal to 111b).			Read Only
		0	**DSC Decoder 6 Maximum Slice Count** 0 = Two slices, supporting 2- and 1-slice configurations. 1 = Four slices, supporting 4, 2-, and 1-slice configurations.	
		3:1	**DSC Decoder 6 Aggregation Support** 110b = Aggregation with the other DSC decoders is not supported. *N* (not equal to 110b) = Aggregation with DSC Decoder *N* is supported.	
		4	**DSC Decoder 7 Maximum Slice Count** 0 = Two slices, supporting 2- and 1-slice configurations. 1 = Four slices, supporting 4, 2-, and 1-slice configurations.	
		7:5	**DSC Decoder 7 Aggregation Support** 111b = Aggregation with the other DSC decoder is not supported. *N* (not equal to 111b) = Aggregation with DSC Decoder *N* is supported.	
End of DSC Register Set – DSC Extended Capability Branch Total DSC Resources				
02274h through 0225Fh	**RESERVED for Extended Receiver Capability**			Read all 0s

Table 2-194: Address Mapping within DPCD Protocol Converter Extension Field (DPCD Addresses 03000h through 030FFh)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Protocol Converter Extension Field	
The Protocol Converter Extension field, containing CEC-tunneling registers, is valid only with DPCD r1.4 (or higher).				
03000h	**CEC_TUNNELING_CAPABILITY** Consumer Electronics Channel (CEC)-Tunneling-over-AUX capability.			Read Only
		0	**CEC_TUNNELING_CAPABLE** Set to 1 by a DP-to-HDMI protocol converter to indicate CEC-Tunneling-over-AUX capability to the DP Source device. Support of CEC-Tunneling-over-AUX by a DP-to-HDMI protocol converter paired with a DP Source device to constitute an HDMI Source device is an implementation-specific choice.	
		1	**CEC_SNOOPING_CAPABLE** Set to 1 by a DP-to-HDMI protocol converter that is capable of passively snooping CEC messages to indicate CEC-Tunneling-over-AUX capability to the DP Source device.	
		2	**CEC_MULTIPLE_LA_CAPABLE** Set to 1 by a DP-to-HDMI protocol converter that is capable of functioning as a Follower for multiple CEC Logical Addresses to indicate CEC-Tunneling-over-AUX capability to the DP Source device.	
		7:3	**RESERVED**	Read all 0s

Table 2-194: Address Mapping within DPCD Protocol Converter Extension Field (DPCD Addresses 03000h through 030FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Protocol Converter Extension Field	
03001h	**CEC_TUNNELING_CONTROL**			Read/Write
		0	**CEC_TUNNELING_ENABLE** Prompts a DP-to-HDMI protocol converter to enable CEC message reception from, and transmission to, the CEC bus. The DP-to-HDMI protocol converter does **not** receive CEC messages unless this bit is set to 1. Additionally, the DP-to-HDMI protocol converter does **not** acknowledge CEC messages unless this bit is set to 1 and at least one bit is set in the CEC_LOGICAL_ADDRESS_MASK register (DPCD Addresses 0300Eh and 0300Fh). When this bit is set to 1, temporary storage for received CEC messages is reset/cleared to 0 in the CEC_RX_MESSAGE_BUFFER register (DPCD Addresses 03010h through 0301Fh). Setting this bit to 1 shall bring the CEC-Tunneling-over-AUX function of the DP-to-HDMI protocol converter to a defined initial state. The DP-to-HDMI protocol converter, upon power-on reset and an upstream DP device disconnect/connect, shall clear this bit to 0. When the upstream DP device clears this bit, the DP-to-HDMI protocol converter shall flush the buffer and clear the status indication flags.	
		1	**CEC_SNOOPING_ENABLE** Prompts a DP-to-HDMI protocol converter to enable passive CEC message reception from the CEC bus when bit 0 (CEC_TUNNELING_ENABLE) is set to 1. Writes are ignored when the CEC_TUNNELING_ENABLE bit is cleared to 0. 0 = Receive all directly addressed CEC messages selected by the CEC_LOGICAL_ADDRESS_MASK register (DPCD Addresses 0300Eh and 0300Fh), and all CEC Broadcast messages. 1 = Receive all CEC messages, regardless of the Destination logical address. A DP-to-HDMI protocol converter, upon power-on reset or an upstream DP device disconnect/connect, shall clear this bit to 0. When the upstream DP device clears this bit, the DP-to-HDMI protocol converter shall flush the buffer and clear the status indication flags. Regardless of this bit's state, a DP-to-HDMI protocol converter shall function only as a Follower for CEC frames according to the CEC_LOGICAL_ADDRESS_MASK register. This means that the protocol converter shall not acknowledge or report CEC Line errors for CEC frames in which the bit corresponding to the Destination address is not set in the CEC_LOGICAL_ADDRESS_MASK register.	
		7:2	**RESERVED**	Read all 0s

Table 2-194: Address Mapping within DPCD Protocol Converter Extension Field (DPCD Addresses 03000h through 030FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Protocol Converter Extension Field	
03002h	**CEC_RX_MESSAGE_INFO** A DP-to-HDMI protocol converter shall clear this register to 00h upon power-on reset, an upstream DP device disconnect/connect, or when the CEC_TUNNELING_ENABLE bit in the CEC_TUNNELING_CONTROL register (DPCD Address 03001h, bit 0) is cleared to 0.			Read Only
		3:0	**CEC_RX_MESSAGE_LEN** CEC frame length received from the CEC bus by a DP-to-HDMI protocol converter and placed into the CEC_RX_MESSAGE_BUFFER register (DPCD Addresses 03010h through 0301Fh). The DP-to-HDMI protocol converter determines this by detecting the START bit and then waiting for the end-of-message (EOM) bit or the first not acknowledged block. The actual length (in number of blocks/bytes) is equal to CEC_RX_MESSAGE_LEN value + 1.	
		4	**CEC_RX_MESSAGE_HPD_STATE** Set to 1 by a DP-to-HDMI protocol converter if the logical HPD (see Table 5-9) was asserted at the start of this message.	
		5	**CEC_RX_MESSAGE_HPD_LOST** Set to 1 by a DP-to-HDMI protocol converter if the logical HPD (see Table 5-9) was de-asserted since the start of the previous message, since power-on reset, or an upstream device disconnect/connect.	
		6	**CEC_RX_MESSAGE_ACKED** Set to 1 by a DP-to-HDMI protocol converter if the received CEC frame was acknowledged. For broadcast messages, this is 1 if no device negatively acknowledged any block in the frame. For a directly addressed message, this is 1 if the Follower acknowledged all blocks within the frame.	
		7	**CEC_RX_MESSAGE_ENDED** Set to 1 by a DP-to-HDMI protocol converter if the last block in the received CEC frame was the final block in the CEC message.	

Table 2-194: Address Mapping within DPCD Protocol Converter Extension Field (DPCD Addresses 03000h through 030FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Protocol Converter Extension Field	
03003h	**CEC_TX_MESSAGE_INFO** A DP-to-HDMI protocol converter shall clear this register to 00h upon power-on reset, an upstream DP device disconnect/connect, or when the CEC_TUNNELING_ENABLE bit in the CEC_TUNNELING_CONTROL register (DPCD Address 03001h, bit 0) is cleared to 0.			Read/Write
		3:0	**CEC_TX_MESSAGE_LEN** CEC message length that is to be transmitted by a DP-to-HDMI protocol converter on the CEC bus. Actual number of bytes is equal to CEC_TX_MESSAGE_LEN value + 1.	
		6:4	**CEC_TX_RETRY_COUNT** Number of CEC frame re-transmissions that a DP-to-HDMI protocol converter shall attempt if a directly addressed message is not acknowledged, a broadcast message is negatively acknowledged, or a CEC Line Error is detected. Valid values are 0 through 5. All other values are RESERVED.	
		7	**CEC_TX_MESSAGE_SEND / CEC_TX MESSAGE_BUFFER_UNAVAILABLE** Set to 1 by a DP Source device after it has written a complete CEC message to the CEC TX_MESSAGE_BUFFER, to prompt a DP-to-HDMI protocol converter to transmit the message on the CEC bus after first ensuring that the bus has been inactive for the appropriate *signal free time*, as required by CEC specification. A DP-to-HDMI protocol converter shall clear this bit to 0 after the protocol converter has transmitted the CEC message on the CEC bus. The DP Source shall **not** write a new CEC TX message into the CEC_TX_MESSAGE_BUFFER until this bit is cleared to 0 by the DP-to-HDMI protocol converter.	

Table 2-194: Address Mapping within DPCD Protocol Converter Extension Field (DPCD Addresses 03000h through 030FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Protocol Converter Extension Field	
03004h	**CEC_TUNNELING_IRQ_FLAGS** A DP-to-HDMI protocol converter shall assert an IRQ_HPD pulse with the CEC_IRQ bit set whenever it sets a bit in this field to 1. The DP Source device shall write a 1 to a bit to acknowledge the interrupt and clear the bit. A DP-to-HDMI protocol converter shall clear this register to 00h upon power-on reset, an upstream DP device disconnect/connect, or when the CEC_TUNNELING_ENABLE bit in the CEC_TUNNELING_CONTROL register (DPCD Address 03001h, bit 0) is cleared to 0.			Write 1 to Clear/Read
		0	**CEC_RX_MESSAGE_INFO_VALID** Set to 1 by a DP-to-HDMI protocol converter after it has written a received CEC message into the CEC_RX_MESSAGE_BUFFER register (DPCD Addresses 03010h through 0301Fh) and updated CEC_RX_MESSAGE_INFO. The DP Source device shall read the CEC message from the CEC_RX_MESSAGE_BUFFER register before clearing this bit. The reason is as follows: A DP-to-HDMI protocol converter shall move the next CEC RX message. If the CEC RX message is present and if this bit is cleared, from its temporary buffer to the CEC_RX_MESSAGE_BUFFER register, do the following: 1 Set this bit. 2 Set the CEC_IRQ bit in the DEVICE_SERVICE_IRQ_VECTOR_ESI1 register (DPCD Address 02004h, bit 2). 3 Generate an IRQ_HPD, regardless of whether the DP Source device has read the previously placed CEC RX message. If the DP Source device clears this bit before reading the CEC RX message in the CEC_RX_MESSAGE_BUFFER register, the message may be overwritten with the next message.	
		1	**CEC_RX_MESSAGE_OVERFLOW** Set to 1 by a DP-to-HDMI protocol converter when a CEC frame is received and there is no temporary storage available to hold the message data. (See the CEC_RX_MESSAGE_BUFFER register (DPCD Addresses 03010h through 0301Fh).) The protocol converter shall not receive additional CEC messages (i.e., as a Follower it shall negatively acknowledge a CEC frame on the CEC bus and drop a frame while snooping) until the CEC_RX_MESSAGE_OVERFLOW bit is cleared by the DP Source device.	
		3:2	**RESERVED**	Read all 0s

Table 2-194: Address Mapping within DPCD Protocol Converter Extension Field (DPCD Addresses 03000h through 030FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Protocol Converter Extension Field	
03004h		4	**CEC_TX_MESSAGE_SENT** Set to 1 by a DP-to-HDMI protocol converter when the CEC message in the CEC_TX_MESSAGE_BUFFER was successfully transmitted within the permitted number of retries.	Write 1 to Clear/Read
		5	**CEC_TX_LINE_ERROR** Set to 1 by a DP-to-HDMI protocol converter when the CEC message in the CEC_TX_MESSAGE_BUFFER was not successfully transmitted after the specified number of retries, due to detection of a CEC Line Error on any block in the CEC frame during the last transmission attempt.	
		6	**CEC_TX_ADDRESS_NACK_ERROR** Set to 1 by a DP-to-HDMI protocol converter when the CEC message in the CEC_TX_MESSAGE_BUFFER was not successfully transmitted after the specified number of retries, due to a negative acknowledge of the Header Block of the CEC frame during the last transmission attempt.	
		7	**CEC_TX_DATA_NACK_ERROR** Set to 1 by a DP-to-HDMI protocol converter when the CEC message in the CEC_TX_MESSAGE_BUFFER was not successfully transmitted after the specified number of retries, due to a negative acknowledge of a Data Block in the CEC frame during the last transmission attempt.	
03005h through 0300Dh	**RESERVED for Protocol Converter Extension**			Read all 0s

Table 2-194: Address Mapping within DPCD Protocol Converter Extension Field (DPCD Addresses 03000h through 030FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Protocol Converter Extension Field	
0300Eh and 0300Fh	**CEC_LOGICAL_ADDRESS_MASK** A DP-to-HDMI protocol converter shall program these 16 bits to 8000h (to enable as a Follower for a Broadcast message) upon power-on reset, an upstream DP device disconnect/connect, or when the CEC_TUNNELING_ENABLE bit in the CEC_TUNNELING_CONTROL register (DPCD Address 03001h, bit 0) is cleared to 0.			Read/Write
		14:0	**CEC_LOGICAL_ADDRESS_MASK** Defines the set of logical addresses for which a DP-to-HDMI protocol converter shall function as a Follower, and controls message delivery for *directly addressed* messages when snooping is disabled. Broadcast messages are always delivered. A DP-to-HDMI protocol converter shall function as a Follower for a CEC message **only when** the CEC_LOGICAL_ADDRESS_MASK contains the Destination address of the CEC message; this includes: • Acknowledging a directly addressed message • Negatively acknowledging a broadcast message • Reporting a detected CEC Line Error Bit 0 = Logical Address 0 — Bit 8 = Logical Address 8 Bit 1 = Logical Address 1 — Bit 9 = Logical Address 9 Bit 2 = Logical Address 2 — Bit 10 = Logical Address 10 Bit 3 = Logical Address 3 — Bit 11 = Logical Address 11 Bit 4 = Logical Address 4 — Bit 12 = Logical Address 12 Bit 5 = Logical Address 5 — Bit 13 = Logical Address 13 Bit 6 = Logical Address 6 — Bit 14 = Logical Address 14 Bit 7 = Logical Address 7 0 = Do not function as a Follower for this address. Do not deliver messages with this Destination address to the CEC_RX_MESSAGE_BUFFER register (DPCD Addresses 03010h through 0301Fh) unless CEC_SNOOPING_ENABLE=1. 1 = Function as a Follower for this address. Deliver messages with this Destination address to the CEC_RX_MESSAGE_BUFFER even if CEC_SNOOPING_ENABLE=0. When CEC_MULTIPLE_LA_CAPABLE=1, a DP-to-HDMI protocol converter shall accept any 16-bit value in this field.	

Table 2-194: Address Mapping within DPCD Protocol Converter Extension Field (DPCD Addresses 03000h through 030FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Protocol Converter Extension Field	
0300Eh and 0300Fh		15	**CEC_LOGICAL_ADDRESS_MASK** Logical Address 15. 0 = Do not function as a Follower for Broadcast messages, and do not report CEC Line Errors detected while receiving the Header Block of a CEC frame. 1 = Function as a Follower for Broadcast messages, and report CEC Line Errors detected while receiving the Header Block of a CEC frame. When CEC_MULTIPLE_LA_CAPABLE=0, a DP-to-HDMI protocol converter shall reply with AUX_NACK if the DP Source device attempts to write a value where more than one of bits 14:0 is set to 1. It shall also reply with AUX_NACK if bit 15 is cleared to 0 (the protocol converter always functions as a Follower for broadcast messages in this case).	Read/Write
03010h through 0301Fh	**CEC_RX_MESSAGE_BUFFER** 16-byte buffer filled by a DP-to-HDMI protocol converter when a CEC message is received and this buffer is available (either no previous message or the previous message has been read by an upstream DP device). The first byte of the buffer (= DPCD 03010h) always contains the first byte of the received CEC message. A DP-to-HDMI protocol converter shall discard messages terminated due to CEC Line Errors. When a DP-to-HDMI protocol converter receives bytes of one or more additional CEC messages while the CEC_RX_MESSAGE_INFO_VALID bit remains set to 1, it shall store those bytes into a temporary storage not mapped to DPCD addresses. The temporary storage should be large enough to hold two seconds of CEC traffic and shall at least hold one second of CEC traffic.			Read/Write
03020h through 0302Fh	**CEC_TX_MESSAGE_BUFFER** 16-byte buffer filled by a DP Source device with a CEC message to be transmitted to the CEC bus by a DP-to-HDMI protocol converter. The first byte of the buffer (= DPCD 03020h) always contains the first byte of the CEC message, which determines the Initiator and Destination address. ***Note:*** *The Initiator logical address used for message transmission shall be determined solely by the first four bits of the first byte of this buffer.*			Read/Write
03030h	**DOWNSTREAM_LINK_ERROR_REPORTING_SUPPORTED**			Read Only
		0	**DOWNSTREAM_LINK_ERROR_REPORTING_SUPPORTED** 0 = Not supported. 1 = Supported.	
		7:1	**RESERVED**	Read all 0s

Table 2-194: Address Mapping within DPCD Protocol Converter Extension Field (DPCD Addresses 03000h through 030FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Protocol Converter Extension Field	
03031h	**DOWNSTREAM_HDMI_ERROR_STATUS_CH0** ***Note:*** *Status is asynchronously updated on a 100-ms cycle and cleared when read by an upstream DP device.*			Read Only
		0	1 = More than three errors have occurred since the last read.	
		1	1 = More than 10 errors have occurred since the last read.	
		2	1 = More than 100 errors have occurred since the last read.	
		7:3	**RESERVED**	Read all 0s
03032h	**DOWNSTREAM_HDMI_ERROR_STATUS_CH1** ***Note:*** *Status is asynchronously updated on a 100-ms cycle and cleared when read by an upstream DP device.*			Read Only
		0	1 = More than three errors have occurred since the last read.	
		1	1 = More than 10 errors have occurred since the last read.	
		2	1 = More than 100 errors have occurred since the last read.	
		7:3	**RESERVED**	Read all 0s
03033h	**DOWNSTREAM_HDMI_ERROR_STATUS_CH2** ***Note:*** *Status is asynchronously updated on a 100-ms cycle and cleared upon a read by an upstream DP device.*			Read Only
		0	1 = More than three errors have occurred since the last read.	
		1	1 = More than 10 errors have occurred since the last read.	
		2	1 = More than 100 errors have occurred since the last read.	
		7:3	**RESERVED**	Read all 0s
03034h	**HDMI_SINK_YCBCR420_COMPONENT_BIT_DEPTH_SUPPORT** ***Note:*** *Bits 2:0 are valid after an HDMI EDID read. Consequently, the Source device is unable to rely on those bits until after it has completed a full HDMI EDID read of all HDMI EDID blocks.*			Read Only
		0	**10bpc_Supported** 0 = 10bpc is not supported. 1 = 10bpc is supported.	
		1	**12bpc_Supported** 0 = 12bpc is not supported. 1 = 12bpc is supported.	
		2	**16bpc_Supported** 0 = 16bpc is not supported. 1 = 16bpc is supported.	
		7:3	**RESERVED**	Read all 0s

Table 2-194: Address Mapping within DPCD Protocol Converter Extension Field (DPCD Addresses 03000h through 030FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Protocol Converter Extension Field	
03035h through 0304Fh	**RESERVED for Protocol Converter Extension**			Read all 0s
03050h	**PROTOCOL_CONVERTER_CONTROL_0** Register name changed and bit 0 description expanded in *DP v1.4*.			Read/Write
		0	**HDMI_DVI_OUTPUT_CONFIG** Valid only when the DFPX_TYPE is set to HDMI, in which case this bit defaults to 1. Otherwise, this bit defaults to 0. The Source device shall clear this bit to 0 if DFPX_TYPE is set to HDMI but the Source device determines (through DisplayID or legacy EDID processing) that the connected display is DVI. 0 = DVI. Protocol converter shall not transmit HDMI INFOFRAMEs and shall **not** use video guard bands. Protocol converter may also suppress audio, although the Source device is **not** expected to transmit audio as a result of DisplayID or legacy EDID processing. 1 = HDMI. Protocol converter shall transmit HDMI INFOFRAMEs, use video guard bands, and pass-through audio.	
		7:1	**RESERVED**	Read all 0s

Table 2-194: Address Mapping within DPCD Protocol Converter Extension Field (DPCD Addresses 03000h through 030FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Protocol Converter Extension Field	
03051h	**PROTOCOL_CONVERTER_CONTROL_1** Register name changed and support for bits 3:1 added in *DP v1.4*.			Read/Write
		0	**CONVERSION_TO_YCBCR420_ENABLE** Shall be cleared to 0 at power-on reset or when an upstream device is disconnected. 0 = Disable. 1 = Enable.	
		1	**HDMI_EDID_PROCESSING_DISABLE** May be set by the Source device before it reads the Sink device's HDMI EDID to disable autonomous HDMI EDID processing by the protocol converter when the protocol converter snoops the HDMI EDID reads. ***Note:*** *The protocol converter may read and process the HDMI EDID before setting SINK_COUNT to 1; however, this behavior is* ***not*** *preferred.* 0 = HDMI autonomous HDMI EDID processing enabled (default). 1 = HDMI autonomous HDMI EDID processing disabled. Protocol converter shall ensure that the 16bpc_Supported, 12bpc_Supported, and 10bpc_Supported bits in the HDMI_SINK_YCBCR420_COMPONENT_BIT_DEPTH_SUPPORT register (DPCD Address 03034h, bits 2:0, respectively) always reads as 000b, and that scrambling is not autonomously enabled for TMDS Character Rates less than 340Mcsc.	
		2	**HDMI_AUTONOMOUS_SCRAMBLING_DISABLE** 0 = HDMI autonomous scrambling is enabled (default). 1 = HDMI autonomous scrambling disabled. Scrambling of HDMI output is controlled by bit 3 (HDMI_FORCE_SCRAMBLING).	
		3	**HDMI_FORCE_SCRAMBLING** No effect unless bit 2 (HDMI_AUTONOMOUS_SCRAMBLING_DISABLE) is set to 1. 0 = HDMI scrambling is disabled (default). 1 = HDMI scrambling is enabled.	
		7:4	**RESERVED**	Read all 0s

Table 2-194: Address Mapping within DPCD Protocol Converter Extension Field (DPCD Addresses 03000h through 030FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Protocol Converter Extension Field	
03052h	**PROTOCOL_CONVERTER_CONTROL_2** Register name changed in *DP v1.4*.			Read/Write
		0	**CONVERSION_TO_YCBCR422_ENABLE** Shall be cleared to 0 when a power-on reset or upstream device disconnect occurs. 0 = Disable. 1 = Enable.	
		7:1	**RESERVED**	Read all 0s
03053h	**RESERVED for Protocol Converter Extension**			Read all 0s
03054h and 03055h	**OUTPUT_HTOTAL** New to *DP v1.4*. Updated in *DP v1.4a*. Used when Horizontal Blanking Expansion is supported. A DP Source device shall program the OUTPUT_HTOTAL, OUTPUT_HSTART, and OUTPUT_HSP_HSW registers (DPCD Addresses 03054h through 03059h, respectively) in a single AUX burst write transaction prior to transmitting the video stream to be expanded by a DPRX. The DPRX shall clear this register to 0000h (default value) only in the event of a device reset –or– when a Powered-Source disconnect is detected by use of the Upstream Device Detection function. 0000h = Disable Horizontal Blanking Expansion. Non-zero = Enable Horizontal Blanking Expansion.			Read/Write
	0	7:0	**OUTPUT_HTOTAL7:0** Least significant eight bits of the 16-bit OUTPUT_HTOTAL.	
	1	7:0	**OUTPUT_HTOTAL15:8** Most significant eight bits of the 16-bit OUTPUT_HTOTAL.	
03056h and 03057h	**OUTPUT_HSTART** New to *DP v1.4*. Updated in *DP v1.4a*. Used when Horizontal Blanking Expansion is supported. A DP Source device shall program the OUTPUT_HTOTAL, OUTPUT_HSTART, and OUTPUT_HSP_HSW registers (DPCD Addresses 03054h through 03059h, respectively) in a single AUX burst write transaction prior to transmitting the video stream to be expanded by a DPRX. The DPRX shall clear this register to 0000h (default value) only in the event of a device reset –or– when a Powered-Source disconnect is detected by use of the Upstream Device Detection function.			Read/Write
	0	7:0	**OUTPUT_HSTART7:0** Least significant eight bits of the 16-bit OUTPUT_HSTART.	
	1	7:0	**OUTPUT_HSTART15:8** Most significant eight bits of the 16-bit OUTPUT_HSTART.	

Table 2-194: Address Mapping within DPCD Protocol Converter Extension Field (DPCD Addresses 03000h through 030FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Protocol Converter Extension Field	
03058h and 03059h	**OUTPUT_HSP_HSW** New to *DP v1.4*. Updated in *DP v1.4a*. Used when Horizontal Blanking Expansion is supported. A DP Source device shall program the OUTPUT_HTOTAL, OUTPUT_HSTART, and OUTPUT_HSP_HSW registers (DPCD Addresses 03054h through 03059h, respectively) in a single AUX burst write transaction prior to transmitting the video stream to be expanded by a DPRX. The DPRX shall clear this register to 0000h (default value) only in the event of a device reset –or– when a Powered-Source disconnect is detected by use of the Upstream Device Detection function.			Read/Write
	0	7:0	**OUTPUT_HSP_HSW7:0** Least significant eight bits of the 15-bit OUTPUT_HSP_HSW.	
	1	6:0	**OUTPUT_HSP_HSW14:8** Most significant seven bits of the 15-bit OUTPUT_HSP_HSW.	
		7	**OUTPUT_HSP** 0 = Positive pulse (default). 1 = Negative pulse.	
0305Ah through 030FFh	**RESERVED for Protocol Converter Extension**			Read all 0s

Table 2-195: Address Mapping within DPCD Multi-touch (for eDP) Field (DPCD Addresses 60000h through 61CFFh)

DPCD Address	Register		Read/ Write over AUX_CH
	Bit #	Definition within Multi-touch (for eDP) Field	
The Multi-touch field is valid only with *eDP v1.4* (or higher) (applicable to the eDP DPRX).			
60000h through 61CFFh	**RESERVED for Multi-touch (for *eDP v1.4* or higher)**		

Table 2-196: Address Mapping within DPCD HDCP 1.3 and HDCP 2.2 Field (DPCD Addresses 68000h through 69FFFh)

DPCD Address	Register		Read/ Write over AUX_CH
	Bit #	Definition within HDCP 1.3 and HDCP 2.2 Field	
68000h through 68FFFh	**RESERVED for HDCP 1.3** See *HDCP for DP r1.3*.		
69000h through 69FFFh	**RESERVED for HDCP 2.2** See *HDCP to DP r2.3*.		

Table 2-197: Address Mapping within DPCD Tunneling Device-specific Field (DPCD Addresses E0000h through E00FFh)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Tunneling Device-specific Field	
E0000h through E0002h	**IEEE_OUI** Example: For IEEE OUI 00-1B-C5, Byte 0 is cleared to 00h, Byte 1 is programmed to 1Bh, and Byte 2 is programmed to C5h.			Read Only
	0	7:0	First two hex digits.	
	1	7:0	Second two hex digits.	
	2	7:0	Third two hex digits.	
E0003h through E0008h	**Device Identification String** Identifies the Tunneling device. Up to six ASCII characters, starting at DPCD Address E0003h. Remaining bytes are 00h if fewer than six characters.			Read Only
E0009h	**Hardware Revision**			Read Only
		3:0	**Hardware Minor Revision** Integer, reset to 0 when the major revision increments. Typically incremented for a minor silicon (e.g., metal mask change) or board revision.	
		7:4	**Hardware Major Revision** Integer, typically incremented for a major silicon or board revision.	
E000Ah	**Firmware/Software Major Revision** Integer, typically incremented for new functionality.			Read Only
E000Bh	**Firmware/Software Minor Revision** Integer, reset to 0 when the firmware/software major revision increments. Typically incremented for bug fixes.			Read Only
E000Ch	**RESERVED** For tunneling-specific usage, specified by the owner of the IEEE OUI that is written to in the Tunneling device IEEE_OUI register (DPCD Addresses E0000h through E0002h).			Vendor-specific

Table 2-197: Address Mapping within DPCD Tunneling Device-specific Field (DPCD Addresses E0000h through E00FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within Tunneling Device-specific Field	
E000Dh	**DP TUNNELING and PANEL REPLAY OPTIMIZATION SUPPORT** New to *DP v2.0*. ***Note:*** *The definition of this register is valid only for DP tunneling bridges that have DPCD Addresses E0000h through E000Bh programmed to a set of specific values. These values will be added to DP v2.0 by way of the Specification Change Request (SCR) process.Crumb SCR indicated by Comment 2861 during d3.*			Read Only
		0	**DP Tunneling Support** 0 = LTTPR Re-timer (default). 1 = Tunnel.	
		5:1	**RESERVED**	Read all 0s
		6	**Panel Replay Tunneling Optimization Support** 0 = Not supported (default). 1 = Supported.	Read Only
		7	**RESERVED**	Read 0
E000Eh through E00FFh	**RESERVED** For tunneling-specific usage, specified by the owner of the IEEE OUI that is written to in the Tunneling device IEEE_OUI register (DPCD Addresses E0000h through E0002h).			Vendor-specific

Table 2-198: Address Mapping within DPCD LTTPR Field (DPCD Addresses F0000h through F02FFh)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within LTTPR Field	
LTTPR-related registers at DPCD Addresses F0000h through F02FFh are valid only for DPCD r1.4 (or higher). ***Note:*** *DPCD Addresses F0010h through F005Fh comprise the PHY_REPEATER1 CONFIGURATION AND STATUS FIELD.*				
F0000h	**LT_TUNABLE_PHY_REPEATER_FIELD_DATA_STRUCTURE_REV** Updated in *DP v2.0*. LTTPR shall return the lowest common denominator of its own value and the downstream LTTPR link value only when the response received on a DFP is non-zero. If response received on a DFP is 0, the value of this field is returned. An LTTPR that supports 8b/10b channel coding shall program this register to 14h. An LTTPR that supports 128b/132b channel coding shall program this register to 20h.			Read Only
		3:0	**Minor Revision Number**	
		7:4	**Major Revision Number**	

Table 2-198: Address Mapping within DPCD LTTPR Field (DPCD Addresses F0000h through F02FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within LTTPR Field	
F0001h	**8b/10b_MAX_LINK_RATE_PHY_REPEATER** Updated in *DP v2.0*. Valid only for 8b/10b Link Layer. A DP device that supports 128b/132b Link Layer link rates shall support all 8b/10b Link Layer link rates. ***Note:*** *For 128b/132b Link Layer, see the MAIN_LINK_CHANNEL_CODING_PHY_REPEATER and MAIN_LINK_CHANNEL_CODING_PHY_REPEATER registers (DPCD Addresses F0007h and F0006h, respectively).* Main-Link Bandwidth Setting = Value × 0.27Gbps/lane. Four values are supported. All other values are RESERVED with the exception of *eDP v1.4* and *MyDP Standard* DPTXs. 06h = 1.62Gbps/lane (RBR). 14h = 5.4Gbps/lane (HBR2). 0Ah = 2.7Gbps/lane (HBR). 1Eh = 8.1Gbps/lane (HBR3). An LTTPR shall return the lower of its own value and the downstream PHY Repeater link value only when the response received on a DFP is non-zero. If the response received on a DFP is 0, the value of this field is returned. An *eDP v1.4* DPRX may program the 8b/10b_MAX_LINK_RATE register value to 00h to indicate that the DPRX supports the Main-Link rates by way of the Link Rate Table method. (See *eDP v1.4*.) A *MyDP Standard* DPRX of an active *MyDP Standard* protocol converter (either MyDP-to-Legacy or MyDP-to-DP Lane-Count protocol converter) can support a value of 19h (6.75Gbps/lane).			Read Only
F0002h	**PHY_REPEATER_CNT** Indicates the number of LTTPRs that are present. Up to eight LTTPRs are supported. 80h = One LTTPR is present. 04h = Six LTTPRs are present. 40h = Two LTTPRs are present. 02h = Seven LTTPRs are present. 20h = Three LTTPRs are present. 01h = Eight LTTPRs are present. 10h = Four LTTPRs are present. FFh = Nine or more LTTPRs are present. 08h = Five LTTPRs are present. All other values are RESERVED. This field shall default to 80h when the data response received on a DFP is 0. For the case in which a value other than 01h or FFh is received on a DFP, the value of this field is data received on the DFP divided by 2. If the value received by the DFP is 01h or FFh, this field shall report FFh. This field is also used by the LTTPR to determine which PHY_REPEATER[8:1] CONFIGURATION AND STATUS register(s) to use during link training.			Read Only

Table 2-198: Address Mapping within DPCD LTTPR Field (DPCD Addresses F0000h through F02FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within LTTPR Field	
F0003h	**PHY_REPEATER_MODE** Indicates the mode in which an LTTPR is operating. An LTTPR shall return the lowest common denominator of its own value and the downstream PHY_REPEATER_MODE value only when the response received on a DFP is 55h or AAh. If the response received on a DFP is a value other than 55h or AAh, this field's value is returned. Shall be programmed to 55h when a power-on reset or an upstream device disconnect occurs. A DPTX can use this field to control the PHY_REPEATER_MODE of all PHY Repeaters between the DPTX and DPRX. For example, a write request of AAh causes all PHY Repeaters to operate in Non-transparent mode. A DPTX operating with 8b/10b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 01h) may configure LTTPRs to either Transparent (default) or Non-transparent mode. A DPTX that establishes the DP link with 128b/132b channel coding shall write 02h to the MAIN_LINK_CHANNEL_CODING_SET register and configure LTTPRs to Non-transparent mode. 55h = Transparent mode (default). AAh = Non-transparent mode.			Write/Read
F0004h	**MAX_LANE_COUNT_PHY_REPEATER** New to *DP v1.4a*.			Read Only
		4:0	**MAX_LANE_COUNT** An LTTPR shall return the lower of its own value and the downstream PHY Repeater link value only when the response received on a DFP is non-zero. If the response received on a DFP is 0, the value of this field is returned. The MAX_LANE_COUNT_PHY_REPEATER register may be updated prior to being read by the DPTX. The LTTPR shall **not** change its MAX_LANE_COUNT_PHY_REPEATER value after the DPTX has read the capability unless one of the following occurs: • HPD disconnect is signaled • DPTX has disabled the Main-Link • LTTPR is reset or powered off On device reset, the MAX_LANE_COUNT field in the MAX_LANE_COUNT register (DPCD Address 00002h, bits 4:0) shall be programmed to 04h. 01h = One lane (Lane 0 only). 02h = Two lanes (Lanes 0 and 1 only). 04h = Four lanes (Lanes 0, 1, 2, and 3). All other values are RESERVED.	
		7:5	**RESERVED**	Read all 0s

Table 2-198: Address Mapping within DPCD LTTPR Field (DPCD Addresses F0000h through F02FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within LTTPR Field	
F0005h	**PHY_REPEATER_EXTENDED_WAKE_TIMEOUT** New to *DP v1.4a*.			Write/Read
		6:0	**EXTENDED_WAKE_TIMEOUT_REQUEST** Represents the cumulative number of 10ms that is needed by the downstream LTTPRs to exit a power-saving state. If an LTTPR requires a non-zero time to exit a power-saving state, the LTTPR shall modify the AUX response and then increase this field by a maximum of five units.	Read Only
		7	**EXTENDED_WAKE_TIMEOUT_GRANT** Shall be cleared to 0 on power-on reset –or– an upstream device disconnect. 0 = DP Source device has not granted the extended wake timeout. 1 = DP Source device has granted the extended wake timeout requested in the EXTENDED_WAKE_TIMEOUT_REQUEST field (bits 6:0).	Write/Read
F0006h	**MAIN_LINK_CHANNEL_CODING_PHY_REPEATER** New to *DP v2.0*. Valid only for 128b/132b Link Layer, when the LT_TUNABLE_PHY_REPEATER_FIELD_DATA_STRUCTURE_REV register (DPCD Address F0000h) is programmed to 20h. Shall be cleared to 00h when operating in 8b/10b Link Layer.			Read Only
		0	**128b/132b SUPPORTED** Shall be set by the LTTPR that is nearest to the DPRX (i.e., LTTPR with a PHY_REPEATER_CNT register (DPCD Address F0002h) value of 80h). Each LTTPR on the way back to the DPTX shall clear this bit unless the LTTPR supports 128b/132b Link Layer. The DPTX may enable 128b/132b PHY Logical Sub-layer only when the following conditions exist: • This bit is set to 1, and • DPRX supports 128b/132b Link Layer 0 = Not supported. 1 = Supported.	Read Only
		7:1	**RESERVED**	Read All 0s

Table 2-198: Address Mapping within DPCD LTTPR Field (DPCD Addresses F0000h through F02FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within LTTPR Field	
F0007h	**PHY_REPEATER_128b/132b_RATES** New to *DP v2.0*. Valid only for 128b/132b Link Layer, when the LT_TUNABLE_PHY_REPEATER_FIELD_DATA_STRUCTURE_REV register (DPCD Address F0000h) is programmed to 20h. Shall be cleared to 00h when operating in 8b/10b Link Layer. Shall be set by the LTTPR that is nearest to the DPRX (i.e., LTTPR with a PHY_REPEATER_CNT register (DPCD Address F0002h) value of 80h). Each LTTPR on the way back to the DPTX shall clear the bits that do not correspond to the LTTPR's current bit rate. 0 = Not supported. 1 = Supported.			Read Only
		0	**10Gbps/lane Support**	
		1	**13.5Gbps/lane Support**	
		2	**20Gbps/lane Support**	
		7:3	**RESERVED**	Read All 0s
F0008h through F000Fh	**RESERVED for LTTPR Capability and ID-related registers**			Read all 0s
F0010h	**TRAINING_PATTERN_SET_PHY_REPEATER1** Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs. Bit definition is identical to the TRAINING_PATTERN_SET register (DPCD Address 00102h). This field is mirrored in all PHY Repeaters. The remaining PHY Repeaters between the DPTX and DPRX shall snoop writes to this field.			Write/Read

Table 2-198: Address Mapping within DPCD LTTPR Field (DPCD Addresses F0000h through F02FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within LTTPR Field	
F0011h	**TRAINING_LANE0_SET_PHY_REPEATER1** Updated in *DP v2.0*. Lane 0 link training control for LTTPR1. Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs. The LTTPR that is upstream of LTTPR1 shall snoop writes to this field and update its voltage swing and pre-emphasis levels based on the value written to this field.			Write/Read
	8b/10b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 01h)			
		1:0	**VOLTAGE_SWING_SET** 00b = Voltage Swing Level 0. 10b = Voltage Swing Level 2. 01b = Voltage Swing Level 1. 11b = Voltage Swing Level 3.	
		2	**MAX_SWING_REACHED** Transmitter shall support at least three levels of voltage swing (Levels 0, 1, and 2). May also support Voltage Swing Level 3. • If only three voltage swing levels are supported (VOLTAGE_SWING_SET field (bits 1:0) is programmed to 10b (Level 2)), this bit shall be set to 1, and cleared in all other cases • If all four voltage swing levels are supported (VOLTAGE_SWING_SET field (bits 1:0) is programmed to 11b (Level 3)), this bit shall be set to 1, and cleared in all other cases	
		4:3	**PRE-EMPHASIS_SET** 00b = Pre-emphasis Level 0. 10b = Pre-emphasis Level 2. 01b = Pre-emphasis Level 1. 11b = Pre-emphasis Level 3.	
		5	**MAX_PRE-EMPHASIS_REACHED** Transmitter shall support at least three levels of pre-emphasis (Levels 0, 1, and 2). May also support Pre-emphasis Level 3. May support independent pre-emphasis level control for each lane. • If only three pre-emphasis levels are supported (transmitter programmed PRE-EMPHASIS_SET field (bits 4:3) to 10b (Level 2)), the transmitter shall set this bit to 1 to indicate to the receiver that the maximum pre-emphasis level has been reached, and clear this bit in all other cases • If all four pre-emphasis levels are supported (transmitter programmed PRE-EMPHASIS_SET field (bits 4:3) to 11b (Level 3)), the transmitter shall set this bit to 1 to indicate to the receiver that the maximum pre-emphasis level has been reached, and clear this bit in all other cases	
		7:6	**RESERVED**	Read all 0s

Table 2-198: Address Mapping within DPCD LTTPR Field (DPCD Addresses F0000h through F02FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within LTTPR Field	
F0011h	**128b/132b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 02h)** New to *DP v2.0*.			Write/Read
		3:0	**TX_FFE_PRESET_VALUE** Indicates the preset transmitter Feed Forward Equalization (FFE) value. See Section 3.5.5.3 for details.	
		7:4	**RESERVED**	Read all 0s
F0012h	**TRAINING_LANE1_SET_PHY_REPEATER1** Updated in *DP v2.0*. Register definition is identical to the TRAINING_LANE0_SET_PHY_REPEATER1 register (DPCD Address F0011h), but for Lane 1.			Write/Read
F0013h	**TRAINING_LANE2_SET_PHY_REPEATER1** Updated in *DP v2.0*. Register definition is identical to the TRAINING_LANE0_SET_PHY_REPEATER1 register (DPCD Address F0011h), but for Lane 2.			Write/Read
F0014h	**TRAINING_LANE3_SET_PHY_REPEATER1** Updated in *DP v2.0*. Register definition is identical to the TRAINING_LANE0_SET_PHY_REPEATER1 register (DPCD Address F0011h), but for Lane 3.			Write/Read
F0015h through F001Fh	**RESERVED for LTTPR1**			Read all 0s
F0020h	**TRAINING_AUX_RD_INTERVAL_PHY_REPEATER1** New to *DP v1.4a*.			Read Only
		6:0	**TRAINING_AUX_RD_INTERVAL_PHY_REPEATER1** Bit definition is identical to the 8b/10b_TRAINING_AUX_RD_INTERVAL register (DPCD Address 0220Eh).	
		7	**RESERVED**	Read 0

Table 2-198: Address Mapping within DPCD LTTPR Field (DPCD Addresses F0000h through F02FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within LTTPR Field	
F0021h	**8b/10b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 01h)**			Read Only
	TRANSMITTER_CAPABILITY_PHY_REPEATER1 New to *DP v1.4a*.			
		0	**VOLTAGE_SWING_LEVEL_3_SUPPORTED** 0 = Not supported. 1 = Supported.	
		1	**PRE_EMPHASIS_LEVEL_3_SUPPORTED** 0 = Not supported. 1 = Supported.	
		7:2	**RESERVED**	Read all 0s
	128b/132b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 02h) New to *DP v2.0*.			Read all 0s
	RESERVED			
F0022h	**128b/132b_TRAINING_AUX_RD_INTERVAL_PHY_REPEATER1** New to *DP v2.0*. Valid only for 128b/132b Link Layer. Shall be cleared to 00h when operating in 8b/10b Link Layer, –or– when LTTPR1 does **not** support 128b/132b Link Layer.			Read Only
		6:0	**128b/132b_TRAINING_AUX_RD_INTERVAL_PHY_REPEATER1** 00h = 400us. 04h = 16ms. 01h = 4ms. 05h = 32ms. 02h = 8ms. 06h = 64ms. 03h = 12ms. All other values are RESERVED.	
		7	**RESERVED**	Read 0
F0023h through F002Fh	**RESERVED for LTTPR1**			Read all 0s
F0030h	**LANE0_1_STATUS_PHY_REPEATER1** Bit definition is identical to the LANE0_1_STATUS register (DPCD Address 00202h).			Read Only
F0031h	**LANE2_3_STATUS_PHY_REPEATER1** Bit definition is identical to the LANE2_3_STATUS register (DPCD Address 00203h).			Read Only
F0032h	**LANE_ALIGN_STATUS_UPDATED_PHY_REPEATER1** Bit definition is identical to the LANE_ALIGN_STATUS_UPDATED register (DPCD Address 00204h).			Read Only

Table 2-198: Address Mapping within DPCD LTTPR Field (DPCD Addresses F0000h through F02FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within LTTPR Field	
F0033h	**ADJUST_REQUEST_LANE0_1_PHY_REPEATER1** Voltage Swing and Equalization Setting Adjust Request (ADJ_REQ) for Lanes 0 and 1. When this register is read and found to have changed from a previous read, both during link training (including the POST_LT_ADJ_REQ sequence) and automated PHY Layer testing, the DPTX shall write the voltage swing and pre-emphasis level requested by this register to the TRAINING_LANE0_SET_PHY_REPEATER*y* (e.g., DPCD Address F0011h for LTTPR1, Lane 0) and TRAINING_LANE1_SET_PHY_REPEATER*y* registers.			Read Only
	8b/10b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 01h)			
		1:0	**VOLTAGE_SWING_LANE0** 00b = Level 0. 10b = Level 2. 01b = Level 1. 11b = Level 3.	
		3:2	**PRE_EMPHASIS_LANE0** 00b = Level 0. 10b = Level 2. 01b = Level 1. 11b = Level 3.	
		5:4	**VOLTAGE_SWING_LANE1** 00b = Level 0. 10b = Level 2. 01b = Level 1. 11b = Level 3.	
		7:6	**PRE_EMPHASIS_LANE1** 00b = Level 0. 10b = Level 2. 01b = Level 1. 11b = Level 3.	
	128b/132b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 02h) New to *DP v2.0*. See Section 3.5.5.3 for details.			
		3:0	**TX_FFE_PRESET_VALUE_LANE0**	
		7:4	**TX_FFE_PRESET_VALUE_LANE1**	
F0034h	**ADJUST_REQUEST_LANE2_3_PHY_REPEATER1** Updated in *DP v2.0*. Register definition is identical to the ADJUST_REQUEST_LANE0_1_PHY_REPEATER1 register (DPCD Address F0033h), but for Lanes 2 and 3.			Read Only

Table 2-198: Address Mapping within DPCD LTTPR Field (DPCD Addresses F0000h through F02FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within LTTPR Field	
F0035h and F0036h	**SYMBOL_ERROR_COUNT_LANE0_PHY_REPEATER1** Updated in *DP v2.0*. Valid only for 8b/10b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 01h). Shall be cleared to 00h for 128b/132b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 02h). Bit definition is identical to the SYMBOL_ERROR_COUNT_LANE0 register (DPCD Addresses 00210h and 00211h). If an LTTPR implements 8b/10b decode on its UFP and encode on its DFP, the LTTPR shall implement this counter; otherwise, support for this counter is **optional**. The SYMBOL_ERROR_COUNT_LANE0_VALID bit (DPCD Address F0036h, bit 7) shall be cleared to 0 in an LTTPR that does not support this counter.			Read Only
F0037h and F0038h	**SYMBOL_ERROR_COUNT_LANE1_PHY_REPEATER1** Updated in *DP v2.0*. Valid only for 8b/10b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 01h). Shall be cleared to 00h for 128b/132b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 02h). Bit definition is identical to the SYMBOL_ERROR_COUNT_LANE1 register (DPCD Addresses 00212h and 00213h). If an LTTPR implements 8b/10b decode on its UFP and encode on its DFP, the LTTPR shall implement this counter; otherwise, support for this counter is **optional**. The SYMBOL_ERROR_COUNT_LANE0_VALID bit (DPCD Address F0038h, bit 7) shall be cleared to 0 in an LTTPR that does not support this counter.			Read Only
F0039h and F003Ah	**SYMBOL_ERROR_COUNT_LANE2_PHY_REPEATER1** Updated in *DP v2.0*. Valid only for 8b/10b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 01h). Shall be cleared to 00h for 128b/132b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 02h). Bit definition is identical to the SYMBOL_ERROR_COUNT_LANE2 register (DPCD Addresses 00214h and 00215h). If an LTTPR implements 8b/10b decode on its UFP and encode on its DFP, the LTTPR shall implement this counter; otherwise, support for this counter is **optional**. The SYMBOL_ERROR_COUNT_LANE0_VALID bit (DPCD Address F003Ah, bit 7) shall be cleared to 0 in an LTTPR that does not support this counter.			Read Only

Table 2-198: Address Mapping within DPCD LTTPR Field (DPCD Addresses F0000h through F02FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within LTTPR Field	
F003Bh and F003Ch	**SYMBOL_ERROR_COUNT_LANE3_PHY_REPEATER1** Updated in *DP v2.0*. Valid only for 8b/10b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 01h). Shall be cleared to 00h for 128b/132b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 02h). Bit definition is identical to the SYMBOL_ERROR_COUNT_LANE3 register (DPCD Addresses 00216h and 00217h). If an LTTPR implements 8b/10b decode on its UFP and encode on its DFP, the LTTPR shall implement this counter; otherwise, support for this counter is **optional**. The SYMBOL_ERROR_COUNT_LANE0_VALID bit (DPCD Address F003Ch, bit 7) shall be cleared to 0 in an LTTPR that does not support this counter.			Read Only
F003Dh through F003Fh	**IEEE_OUI** Example: For IEEE OUI 00-1B-C5, Byte 0 is cleared to 00h, Byte 1 is programmed to 1Bh, and Byte 2 is programmed to C5h.			Read Only
	0	7:0	First two hex digits.	
	1	7:0	Second two hex digits.	
	2	7:0	Third two hex digits.	
F0040h through F0045h	**LT-tunable PHY Repeater Device Identification String** Identifies an LTTPR device. Up to six ASCII characters, starting at *XXX*h, where *XXX* is vendor-specific. Remaining bytes are 00h if fewer than six characters.			Read Only
F0046h	**Hardware Revision**			Read Only
		3:0	**Hardware Minor Revision** Integer, reset to 0 when major revision increments. Typically incremented for a minor silicon (e.g., metal mask change) or board revision.	
		7:4	**Hardware Major Revision** Integer, typically incremented for a major silicon or board revision.	
F0047h	**Firmware/Software Major Revision** Integer, typically incremented for new functionality.			Read Only
F0048h	**Firmware/Software Minor Revision** Integer, reset to 0 when the firmware/software major revision increments. Typically incremented for bug fixes.			Read Only
F0049h through F005Fh	**Vendor-specific Space for PHY_Repeater1** For LTTPR-specific usage, specified by the owner of the IEEE OUI that is written to in the LTTPR device IEEE_OUI register (DPCD Addresses F003Dh through F003Fh).			Vendor-specific

Table 2-198: Address Mapping within DPCD LTTPR Field (DPCD Addresses F0000h through F02FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within LTTPR Field	
F0060h through F00AFh	**PHY_REPEATER2 CONFIGURATION AND STATUS FIELD** Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs. Bit definitions are identical to the REPEATER1 CONFIGURATION AND STATUS FIELD (DPCD Addresses F0010h through F005Fh), but for LTTPR2.			Write/Read and Read Only
F00B0h through F00FFh	**PHY_REPEATER3 CONFIGURATION AND STATUS FIELD** Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs. Bit definitions are identical to the REPEATER1 CONFIGURATION AND STATUS FIELD (DPCD Addresses F0010h through F005Fh), but for LTTPR3.			Write/Read and Read Only
F0100h through F014Fh	**PHY_REPEATER4 CONFIGURATION AND STATUS FIELD** Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs. Bit definitions are identical to the REPEATER1 CONFIGURATION AND STATUS FIELD (DPCD Addresses F0010h through F005Fh), but for LTTPR4.			Write/Read and Read Only
F0150h through F019Fh	**PHY_REPEATER5 CONFIGURATION AND STATUS FIELD** Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs. Bit definitions are identical to the REPEATER1 CONFIGURATION AND STATUS FIELD (DPCD Addresses F0010h through F005Fh), but for LTTPR5.			Write/Read and Read Only
F01A0h through F01EFh	**PHY_REPEATER6 CONFIGURATION AND STATUS FIELD** Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs. Bit definitions are identical to the REPEATER1 CONFIGURATION AND STATUS FIELD (DPCD Addresses F0010h through F005Fh), but for LTTPR6.			Write/Read and Read Only
F01F0h through F023Fh	**PHY_REPEATER7 CONFIGURATION AND STATUS FIELD** Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs. Bit definitions are identical to the REPEATER1 CONFIGURATION AND STATUS FIELD (DPCD Addresses F0010h through F005Fh), but for LTTPR7.			Write/Read and Read Only
F0240h through F028Fh	**PHY_REPEATER8 CONFIGURATION AND STATUS FIELD** Shall be cleared to 00h when a power-on reset or upstream device disconnect occurs. Bit definitions are identical to the REPEATER1 CONFIGURATION AND STATUS FIELD (DPCD Addresses F0010h through F005Fh), but for LTTPR8.			Write/Read and Read Only

Table 2-198: Address Mapping within DPCD LTTPR Field (DPCD Addresses F0000h through F02FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within LTTPR Field	
F0290h	**FEC_STATUS_PHY_REPEATER1**			Write/Read and Read Only
		0	**FEC_DECODE_EN_DETECTED** 0 = FEC_DECODE_EN control link symbol sequence is not detected. 1 = FEC_DECODE_EN control link symbol sequence is detected.	
		1	**FEC_DECODE_DIS_DETECTED** 0 = FEC_DECODE_DIS control link symbol sequence is not detected. 1 = FEC_DECODE_DIS control link symbol sequence is detected.	
		7:2	**RESERVED**	Read all 0s
F0291h and F0292h	**FEC_ERROR_COUNT_PHY_REPEATER1** New to *DP v1.4*.			Write/Read and Read Only
	0	7:0	**FEC_ERROR_COUNT_PHY_REPEATER1_7:0** Least significant eight bits of the 15-bit error count.	
	1	6:0	**FEC_ERROR_COUNT_PHY_REPEATER1_14:8** Most significant seven bits of the 15-bit error count.	
		7	**FEC_ERROR_COUNT_VALID** 0 = Not valid. 1 = Valid.	
F0293h	**RESERVED for LTTPR1**			Read all 0s
F0294h	**FEC_CAPABILITY_0_PHY_REPEATER1** New to *DP v1.4a*. Updated in *DP v2.0*.			Read Only
		0	**FEC_CAPABLE** 0 = LTTPR is agnostic to FEC operation. 1 = LTTPR performs FEC decode at its UFP and FEC encode at its DFP.	
		7:1	Bit definitions are identical to the FEC_CAPABILITY_0 register (DPCD Address 00090h), but for LTTPR1.	
F0295h	**FEC_CAPABILITY_1_PHY_REPEATER1** New to *DP v2.0*. Bit definitions are identical to the FEC_CAPABILITY_1 register (DPCD Address 00091h), but for LTTPR1.			Read Only
F0296h and F0297h	**RESERVED for LTTPR1**			Read all 0s

Table 2-198: Address Mapping within DPCD LTTPR Field (DPCD Addresses F0000h through F02FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within LTTPR Field	
F0298h	**FEC_STATUS_PHY_REPEATER2** New to *DP v1.4a*. Bit definitions are identical to the FEC_STATUS_PHY_REPEATER1 register (DPCD Address F0290h), but for LTTPR2.			Write/Read and Read Only
F0299h and F029Ah	**FEC_ERROR_COUNT_PHY_REPEATER2** New to *DP v1.4a*. Bit definitions are identical to the FEC_ERROR_COUNT_PHY_REPEATER1 register (DPCD Addresses F0291h and F0292h), but for LTTPR2.			Write/Read and Read Only
F029Bh	**RESERVED for LTTPR2**			Read all 0s
F029Ch	**FEC_CAPABILITY_0_PHY_REPEATER2** New to *DP v1.4a*. Updated in *DP v2.0*. Bit definitions are identical to the FEC_CAPABILITY_0_PHY_REPEATER1 register (DPCD Address F0294h), but for LTTPR2.			Read Only
F029Dh	**FEC_CAPABILITY_1_PHY_REPEATER2** New to *DP v2.0*. Bit definitions are identical to the FEC_CAPABILITY_1_PHY_REPEATER1 register (DPCD Address F0295h), but for LTTPR2.			Read Only
F029Eh and F029Fh	**RESERVED for LTTPR2**			Read all 0s

Table 2-198: Address Mapping within DPCD LTTPR Field (DPCD Addresses F0000h through F02FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within LTTPR Field	
F02A0h	**FEC_STATUS_PHY_REPEATER3** New to *DP v1.4a*. Bit definitions are identical to the FEC_STATUS_PHY_REPEATER1 register (DPCD Address F0290h), but for LTTPR3.			Write/Read and Read Only
F02A1h and F02A2h	**FEC_ERROR_COUNT_PHY_REPEATER3** New to *DP v1.4a*. Bit definitions are identical to the FEC_ERROR_COUNT_PHY_REPEATER1 register (DPCD Addresses F0291h and F0292h), but for LTTPR3.			Write/Read and Read Only
F02A3h	**RESERVED for LTTPR3**			Read all 0s
F02A4h	**FEC_CAPABILITY_0_PHY_REPEATER3** New to *DP v1.4a*. Updated in *DP v2.0*. Bit definitions are identical to the FEC_CAPABILITY_0_PHY_REPEATER1 register (DPCD Address F0294h), but for LTTPR3.			Read Only
F02A5h	**FEC_CAPABILITY_1_PHY_REPEATER3** New to *DP v2.0*. Bit definitions are identical to the FEC_CAPABILITY_1_PHY_REPEATER1 register (DPCD Address F0295h), but for LTTPR3.			Read Only
F02A6h and F02A7h	**RESERVED for LTTPR3**			Read all 0s

Table 2-198: Address Mapping within DPCD LTTPR Field (DPCD Addresses F0000h through F02FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within LTTPR Field	
F02A8h	**FEC_STATUS_PHY_REPEATER4** New to *DP v1.4a*. Bit definitions are identical to the FEC_STATUS_PHY_REPEATER1 register (DPCD Address F0290h), but for LTTPR4.			Write/Read and Read Only
F02A9h and F02AAh	**FEC_ERROR_COUNT_PHY_REPEATER4** New to *DP v1.4a*. Bit definitions are identical to the FEC_ERROR_COUNT_PHY_REPEATER1 register (DPCD Addresses F0291h and F0292h), but for LTTPR4.			Write/Read and Read Only
F02ABh	**RESERVED for LTTPR4**			Read all 0s
F02ACh	**FEC_CAPABILITY_0_PHY_REPEATER4** New to *DP v1.4a*. Updated in *DP v2.0*. Bit definitions are identical to the FEC_CAPABILITY_0_PHY_REPEATER1 register (DPCD Address F0294h), but for LTTPR4.			Read Only
F02ADh	**FEC_CAPABILITY_1_PHY_REPEATER4** New to *DP v2.0*. Bit definitions are identical to the FEC_CAPABILITY_1_PHY_REPEATER1 register (DPCD Address F0295h), but for LTTPR4.			Read Only
F02AEh and F02AFh	**RESERVED for LTTPR4**			Read all 0s

Table 2-198: Address Mapping within DPCD LTTPR Field (DPCD Addresses F0000h through F02FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within LTTPR Field	
F02B0h	**FEC_STATUS_PHY_REPEATER5** New to *DP v1.4a*. Bit definitions are identical to the FEC_STATUS_PHY_REPEATER1 register (DPCD Address F0290h), but for LTTPR5.			Write/Read and Read Only
F02B1h and F02B2h	**FEC_ERROR_COUNT_PHY_REPEATER5** New to *DP v1.4a*. Bit definitions are identical to the FEC_ERROR_COUNT_PHY_REPEATER1 register (DPCD Addresses F0291h and F0292h), but for LTTPR5.			Write/Read and Read Only
F02B3h	**RESERVED for LTTPR5**			Read all 0s
F02B4h	**FEC_CAPABILITY_0_PHY_REPEATER5** New to *DP v1.4a*. Updated in *DP v2.0*. Bit definitions are identical to the FEC_CAPABILITY_0_PHY_REPEATER1 register (DPCD Address F0294h), but for LTTPR5.			Read Only
F02B5h	**FEC_CAPABILITY_1_PHY_REPEATER5** New to *DP v2.0*. Bit definitions are identical to the FEC_CAPABILITY_1_PHY_REPEATER1 register (DPCD Address F0295h), but for LTTPR5.			Read Only
F02B6h and F02B7h	**RESERVED for LTTPR5**			Read all 0s

Table 2-198: Address Mapping within DPCD LTTPR Field (DPCD Addresses F0000h through F02FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within LTTPR Field	
F02B8h	**FEC_STATUS_PHY_REPEATER6** New to *DP v1.4a*. Bit definitions are identical to the FEC_STATUS_PHY_REPEATER1 register (DPCD Address F0290h), but for LTTPR6.			Write/Read and Read Only
F02B9h and F02BAh	**FEC_ERROR_COUNT_PHY_REPEATER6** New to *DP v1.4a*. Bit definitions are identical to the FEC_ERROR_COUNT_PHY_REPEATER1 register (DPCD Addresses F0291h and F0292h), but for LTTPR6.			Write/Read and Read Only
F02BBh	**RESERVED for LTTPR6**			Read all 0s
F02BCh	**FEC_CAPABILITY_0_PHY_REPEATER6** New to *DP v1.4a*. Updated in *DP v2.0*. Bit definitions are identical to the FEC_CAPABILITY_0_PHY_REPEATER1 register (DPCD Address F0294h), but for LTTPR6.			Read Only
F02BDh	**FEC_CAPABILITY_1_PHY_REPEATER6** New to *DP v2.0*. Bit definitions are identical to the FEC_CAPABILITY_1_PHY_REPEATER1 register (DPCD Address F0295h), but for LTTPR6.			Read Only
F02BEh and F02BFh	**RESERVED for LTTPR6**			Read all 0s

Table 2-198: Address Mapping within DPCD LTTPR Field (DPCD Addresses F0000h through F02FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within LTTPR Field	
F02C0h	**FEC_STATUS_PHY_REPEATER7** New to *DP v1.4a*. Bit definitions are identical to the FEC_STATUS_PHY_REPEATER1 register (DPCD Address F0290h), but for LTTPR7.			Write/Read and Read Only
F02C1h and F02C2h	**FEC_ERROR_COUNT_PHY_REPEATER7** New to *DP v1.4a*. Bit definitions are identical to the FEC_ERROR_COUNT_PHY_REPEATER1 register (DPCD Addresses F0291h and F0292h), but for LTTPR7.			Write/Read and Read Only
F02C3h	**RESERVED for LTTPR7**			Read all 0s
F02C4h	**FEC_CAPABILITY_0_PHY_REPEATER7** New to *DP v1.4a*. Updated in *DP v2.0*. Bit definitions are identical to the FEC_CAPABILITY_0_PHY_REPEATER1 register (DPCD Address F0294h), but for LTTPR7.			Read Only
F02C5h	**FEC_CAPABILITY_1_PHY_REPEATER7** New to *DP v2.0*. Bit definitions are identical to the FEC_CAPABILITY_1_PHY_REPEATER1 register (DPCD Address F0295h), but for LTTPR7.			Read Only
F02C6h and F02C7h	**RESERVED for LTTPR7**			Read all 0s

Table 2-198: Address Mapping within DPCD LTTPR Field (DPCD Addresses F0000h through F02FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX_CH
	Byte #	Bit #	Definition within LTTPR Field	
F02C8h	**FEC_STATUS_PHY_REPEATER8** New to *DP v1.4a*. Bit definitions are identical to the FEC_STATUS_PHY_REPEATER1 register (DPCD Address F0290h), but for LTTPR8.			Write/Read and Read Only
F02C9h and F02CAh	**FEC_ERROR_COUNT_PHY_REPEATER8** New to *DP v1.4a*. Bit definitions are identical to the FEC_ERROR_COUNT_PHY_REPEATER1 register (DPCD Addresses F0291h and F0292h), but for LTTPR8.			Write/Read and Read Only
F02CBh	**RESERVED for LTTPR8**			Read all 0s
F02CCh	**FEC_CAPABILITY_0_PHY_REPEATER8** New to *DP v1.4a*. Updated in *DP v2.0*. Bit definitions are identical to the FEC_CAPABILITY_0_PHY_REPEATER1 register (DPCD Address F0294h), but for LTTPR8.			Read Only
F02CDh	**FEC_CAPABILITY_1_PHY_REPEATER8** New to *DP v2.0*. Bit definitions are identical to the FEC_CAPABILITY_1_PHY_REPEATER1 register (DPCD Address F0295h), but for LTTPR8.			Read Only
F02CEh and F02CFh	**RESERVED for LTTPR8**			Read all 0s
F02D0h through F02FFh	**RESERVED for LTTPR**			Read all 0s

Table 2-199: Address Mapping within DPCD *MyDP Standard*-specific Field (DPCD Addresses FFF00h through FFFFFh)

DPCD Address	Register		Read/ Write over AUX_CH
	Bit #	Definition within *MyDP Standard*-specific Field	
FFF00h	**RESERVED for MyDP**		
FFF01h	**MyDP_POWR_CAP** See *MyDP Standard*.		
FFF02h through FFFFFh	**RESERVED for MyDP**		

2.12.4 AUX Link Services

To transport an isochronous data stream from the Source device to the Sink device, Link Policy Maker shall first establish the Main-Link. The Main-Link shall be established in the following sequence of steps.

Note: *All the commands are memory-mapped, whether setting or acquiring link parameters.*

Step_1:

Unless it has prior knowledge to do otherwise, the DP Source device shall initiate Link Discovery by performing LTTPR recognition, as described in Section 3.6.6.6.1, followed by reading the Receiver Capability field (DPCD Addresses 00000h through 000FFh; see Table 2-183) and Extended Receiver Capability field (DPCD Addresses 02200h through 022FFh; see Table 2-193) through the AUX_CH. The Receiver Capability and Extended Receiver Capability fields shall describe the Sink device DPRX's Main-Link receiver capability, such as the maximum bit rate and maximum number of lanes. Details on reading the DPCD are explained later in this section.

Step_2:

Based on the DPCD information, the Source device shall start link initialization. The following sequences shall take place during link initialization:

1 Source device's Link Policy Maker shall start link training. This function call notifies the Sink device of the training pattern's ensuing transport through the Main-Link PHY Layer, with link configuration and training attributes defined in this function.

2 Source device's Link Policy Maker shall check the training status and report of final results to the Stream Policy Maker.

If the Link Policy Maker detects a failed link training attempt, it shall take corrective action. Possible corrective actions are:

- Reduction of the bit rate if the link was in the high bit rate mode
- Termination of link initialization

This loop of setting the Main-Link configuration and forwarding training pattern, while checking the status shall end with the final result of either pass or fail. "Pass" means that LANE*x*_CR_DONE, LANE*x*_SYMBOL_LOCKED, and INTERLANE_ALIGN_DONE have been achieved on each configured lane (with a skew of two LS_Clk period between adjacent lanes). Otherwise, it is "fail."

After the Main-Link is established, the Source device's Link Policy Maker shall check the link status whenever it detects the HPD (Hot Plug Detect) signal toggle after the rising edge of HPD. The Source device shall ignore low or high pulse period of less than 0.25ms. In other words, the Source device shall not check the link status until at least 0.25ms after the rising edge.

The Sink device shall clear the HPD signal to a low level for 0.5 to 1ms before setting it high again whenever there is a status change in the link or device. This shall notify the Source device of the status change.

The Source device shall check the Link/Sink Device Status field (DPCD Addresses 00200h through 002FFh; see Table 2-185) through an AUX read transaction to identify the cause within 100ms of the rising edge of the HPD. Upon identifying the cause, the Link Policy Maker shall take corrective action.

If the HPD is the result of a new device being connected, either directly to the Source device (signaled by a long HPD), or downstream of a Branch device (indicated by incrementing the DFP_COUNT field value in the DOWN_STREAM_PORT_COUNT register (DPCD Address 00007h, bits 3:0) and signaled by an IRQ_HPD pulse), the Source device shall read the new DisplayID or legacy EDID that has been made available to it to ensure that content being transmitted over the link is able to be properly received and rendered.

Note: ***(Informative)*** *If the HPD signal toggling (or bouncing) is the result of the Hot Unplug followed by Hot Plug of a cable-connector assembly, the HPD signal is likely to remain unstable during the de-bouncing period, which is in the order of tens of milliseconds. The Source device may either check the HPD signal's stability before initiating an AUX read transaction, –or– immediately initiate the AUX read transaction after each HPD rising edge.*

2.12.4.1 IEEE OUI and Device Identification

Device designs with different DP PHY Layer and/or Link Layer implementations shall be distinguished by unique combinations of IEEE OUI, Device Identification String, Hardware Version and firmware/software version (collectively referred to as the "Source Device Identification," "Sink Device Identification," –or– "Branch Device Identification," as appropriate). The specific values for the offsets 00*n*03h through 00*n*0Bh are determined by the owner of the OUI specified in 00*n*00h through 00*n*02h, where $n = 3$ for Source devices, $n = 4$ for Sink devices, and $n = 5$ for Branch devices. The Source device shall use a burst write when updating the Source Device Identification.

This Standard does not preclude the Source device from dynamically updating the Source Device Identification. For example, if the Source device supports multiple independent Source device-specific behaviors, and needs to dynamically switch between them, then the Source device shall use distinct Source Identifications for these. A Sink device shall maintain the current values of the Source device-specific registers and associated states for the functions associated with each Source Identification that it supports, preserving these when the Source device switches away from the corresponding Source Device Identification and reinstating them when Source device switches back to the corresponding Source Device Identification.

2.12.4.2 DPCD in Multi-Link Topology with SST-only Mode Source Device

A DisplayPort topology has multiple links when one or more Sink devices connect to a Source device by way of Branch device(s). A Branch device forwarding SST mode from an input port to an output port, functioning as an SST-mode Repeater device, shall comprehend the DPCD(s) of its downstream links as described in Section 2.1.4.1. An SST-only mode upstream DP device shall check only the DPCD of its immediate downstream device regardless of the link topology.

2.12.4.2.1 Receiver Capability of Downstream Legacy Link

Generally speaking, a legacy link does **not** have a Receiver Capability field equivalent to that defined for DPCD.

Capabilities vary. Some legacy links can support both audio and video, while others are limited to video only. Supported pixel data rate and colorimetry format are also dependent on the type of legacy link and its implementation.

A DP Source device, when connected to a legacy Sink device by way of a DP-to-Legacy protocol converter, shall determine the stream format based on the Sink device capability expressed in the DisplayID or legacy EDID of the legacy Sink device and whether the cable adapter is an HDMI cable adapter.

2.12.4.3 Link Initialization through Link Training

DP link initialization (before transporting a stream) shall be performed unless the Source Main-Link transmitter and the Sink Main-Link receiver are already in synchronization as indicated in the Link/Sink Device Status field (DPCD Addresses 00200h through 002FFh; see Table 2-185). During link initialization, AUX transactions shall be used to train the link with a desired set of link configuration parameters. For a detailed description of the link training sequence, see Section 3.5.1.2.

An exception for link training mandates exists for embedded DP connections. When a DP Source device reads 1 in the NO_AUX_TRANSACTION_LINK_TRAINING bit in the MAX_DOWNSPREAD register (DPCD Address 00003h, bit 6) of DP Sink device, it may transmit TPS1 (which is a repetition of D10.2 symbols without scrambling) and TPS2, TPS3, or TPS4, depending on the capabilities that are common between the DPTX and DPRX before switching to normal operation without AUX transactions (i.e., no AUX transactions are used to initiate link training, during training or on completion of successful link training).

There is another exception for a box-to-box connection. When the DP Source device is resuming the transmission (e.g., after waking from sleep), the DP Source device may skip the AUX transactions for the link training when both of the following conditions exist:

- Source device has determined that the HPD signal has remained continuously asserted (apart from IRQ_HPD notifications) since the link was last in full operation.
- Source device has read 1 in NO_AUX_TRANSACTION_LINK_TRAINING bit after the initial Sink device detection.

If the conditions listed above exist, and if the Source device determines that bandwidth to be used is the same as that used when the link was last in full operation, the Source device may transmit TPS1 and TPS2 (500-us minimum for each) using the last known good voltage swing and pre-emphasis settings before switching to the normal operation without AUX transactions. Regardless of whether full Link Training is skipped, the DP Sink device shall transmit an IRQ_HPD pulse over the HPD signal line when it fails to synchronize to the incoming Main-Link stream.

After Link Training is successfully completed (which means that the DPRX is synchronized to incoming Main-Link data) and before transport of a main video stream starts, the Source Main-Link transmitter shall be transmitting the "Idle Pattern" consisting of BS symbol sequence BS + BF + BF + BS followed by the NoVideoStream_Flag bit in the VB-ID (bit 3) set to 1 inserted every 2^{13} (or 8192) link symbols. Every 512^{th} occurrence of the BS symbol sequence set shall be replaced by the scrambler reset symbol sequence SR + BF + BF + SR.

The Source device shall start transmitting the Idle Pattern after it has cleared the Training_Pattern byte in the DPCD. The Sink device should be ready to receive the "Idle Pattern" as soon as it updates the Link/Sink Device Status field (DPCD Addresses 00200h through 002FFh; see Table 2-185), to indicate the successful completion of link training to the Source device.

Link training may result in the available bandwidth being lower than that originally attempted (e.g., an attempt to train at HBR fails, and training falls back to RBR). The Source device shall not attempt to transmit an AV stream that needs a bandwidth higher than the bandwidth currently in use.

A link may be retrained for some reason. A Source device shall be tolerant to the available bandwidth resulting from retraining being lower than the bandwidth resulting from prior training, and this may in turn require a video mode set change.

For a closed embedded connection, the DPTX and DPRX may be set to pre-calibrated parameters without going through the full link training sequence. In this mode, the DPTX may start a normal operation following transmission of the Clock Recovery Pattern with pre-calibrated drive current and pre-emphasis level.

When switching to an MST mode following the link training, the DPTX of an upstream device shall set the MST_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 0) prior to starting Link Training. The upstream device shall transmit a minimum of four MST Link Frames (four SR cycles) of empty MTPs prior to the startup of a stream.

Note: *FEC parity symbols are* ***not*** *transmitted during link training. For 8b/10b channel coding, this is true regardless of whether the DP Source device has set or cleared the DP Sink device's FEC_READY bit in the FEC_CONFIGURATION register (DPCD Address 00120h, bit 0).*

2.12.4.4 Link Maintenance

The downstream device with a DPRX shall maintain the Link Status flags in the following registers during normal operation:

- LANE*x_y*_STATUS register(s) (DPCD Address(es) 00202h and 00203h) and LANE*x_y*_STATUS_ESI register(s) (DPCD Address(es) 0200Ch and 0200Dh)
- LANE_ALIGN_STATUS_UPDATED and LANE_ALIGN_STATUS_UPDATED_ESI registers (DPCD Addresses 00204h and 0200Eh, respectively)

After losing synchronization with the Source device for any reason other than after receiving a request to program the SET_POWER_STATE field in the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h, bits 2:0) to 10b, –or– to request link retraining, the Sink device shall do the following:

1 Clear the INTERLANE_ALIGN_DONE bit in the LANE_ALIGN_STATUS_UPDATED and LANE_ALIGN_STATUS_UPDATED_ESI register(s).

2 Issue a distinct IRQ_HPD (i.e., distinct from an IRQ_HPD issued for any other reason).

The Link Policy Maker of the Source device shall check the link status whenever it detects the IRQ_HPD signal toggle within 100ms of the HPD signal's rising edge for possible Main-Link synchronization loss. This check is performed by reading status-related registers located at DPCD Addresses 00200h through 00205h –or– 02002h, 02003h, and 0200Ch through 0200Fh.

Note: *The format change in the transported stream does not necessarily result in a Link Status change, as long as the link remains stable. For example, some Source devices may choose to continue transmitting stuffing symbols when the stream has stopped. In this case, the Main-Link remains synchronized.*

2.12.4.5 HBR*x*/RBR Link Quality Test Support

DisplayPort supports a test procedure for measuring the link quality. The following features are supported:

- Transmission of a Nyquist pattern (repetition of D10.2 symbols without scrambling)
- Symbol Error measurement pattern
- PRBS7 bit pattern
- Custom 80-bit repeating pattern
- CP2520 (HBR2 Compliance EYE pattern)

The DP Source device may support test pattern selection independently for each Main-Link lane.

Table 2-200 summarizes which patterns for Link Training and Link Quality Measurement are scrambled.

Table 2-200: 8b/10b Encoding and Scrambling Rules for Link Management

Pattern Type	8b/10b Encoded?	Scrambled?
TPS1	Yes	No
TPS2	Yes	No
TPS3	Yes	No
TPS4	Yes	Yes
D10.2 Test Pattern (Same as TPS1)	Yes	No
Symbol Error Rate Measurement Pattern	Yes	Yes
PRBS7	No	No
Custom 80-bit pattern	No	No
CP2520 Patterns 1/2/3	Yes	Yes

When transmitting a pattern that is not scrambled, the Source device shall set the SCRAMBLING_DISABLE bit in the TRAINING_PATTERN_SET register (DPCD Address 00102h, bit 5). When a Link Quality test pattern is being transmitted by a DPTX, the bit is “don’t care.”

2.12.4.5.1 Transmission of Nyquist Pattern

This pattern consists of repetition of D10.2 symbols (without scrambling), identical to TPS1 for LANE*x*_CR_DONE. This pattern results in the Main-Link toggling at its highest frequency (e.g., 1.35GHz when the link rate is 2.7Gbps/lane). System integrators may use this pattern to measure, for example, the jitter performance of the transmitted signals.

The DP Source device signals transmission of this pattern by writing 01h to the Lane's LINK_QUAL_PATTERN_SET field in the LINK_QUAL_LANE*x*_SET register(s) (DPCD Address(es) 0010Bh through 0010Eh, bits 6:0).

Upon being notified of the transmission of this pattern, the DP Sink device shall blank its screen while keeping the DPRX running.

2.12.4.5.2 Symbol Error Rate Measurement Pattern

This pattern consists of repetition of data 00h (prior to 8b/10b encoding) that is scrambled by a transmitter. (See Appendix E for details regarding the scrambling polynomial.) The DP Source device shall periodically (every 2^{13} or 8192 symbols) transmit a Single Stream Transport BS symbol sequence. The PHY Layer shall replace every 512^{th} BS symbol sequence with an SR symbol sequence to reset the scrambler.

VB-ID/Mvid/Maud values, as well as the other data symbols, shall be cleared to 00h while the Symbol Error Rate Measurement Pattern is being transmitted.

Upon being notified of the transmission of this pattern, the DP Sink device shall start increasing the SYMBOL_ERROR_COUNT_LANE*x* register's (DPCD Addresses 00210h through 00217h; each register is composed of two bytes, within which the error count is stored in the 15 least significant bits) value each time it has an unscrambled data value other than 00h.

The DP Source device shall read the SYMBOL_ERROR_COUNT_LANE*x* values some time later. Using the read values and elapsed time, the device shall calculate the approximate symbol error rate.

Transmitting $1E^{+9}$ link symbols takes approximately 10 seconds. Therefore, the transmitter should wait for 10 to 100 seconds before reading the Symbol Error count from a receiver.

Symbol error rate is calculated as follows:

- At 8.1Gbps/lane (HBR3):

  $$\textit{Symbol Error Rate in units of } 10^{-9} = \textit{Error\_Count} / (0.81 \times \textit{Measurement Period in seconds})$$

- At 5.4Gbps/lane (HBR2):

  $$\textit{Symbol Error Rate in units of } 10^{-9} = \textit{Error\_Count} / (0.54 \times \textit{Measurement Period in seconds})$$

- At 2.7Gbps/lane (HBR):

  $$\textit{Symbol Error Rate in units of } 10^{-9} = \textit{Error\_Count} / (0.27 \times \textit{Measurement Period in seconds})$$

- At 1.62Gbps/lane (RBR):

  $$\textit{Symbol Error Rate in units of } 10^{-9} = \textit{Error\_Count} / (0.162 \times \textit{Measurement Period in seconds})$$

2.12.4.5.3 PRBS and Bit Pattern

See Table 1-2 for a detailed description of the PRBS7 bit pattern used by the LINK_QUAL_PATTERN_SET field in the LINK_QUAL_LANE*x*_SET register(s) (DPCD Address(es) 0010Bh through 0010Eh, bits 6:0).

2.12.4.5.4 80-Bit Custom Pattern

An upstream DP device that supports HBR2 shall be capable of transmitting a repeating 80-bit custom pattern. An upstream DP device that does not support HBR2 may be capable of transmitting a repeating 80-bit custom pattern. The custom pattern is **not** scrambled or encoded with 8b/10b. This custom pattern allows for more flexibility during Physical Compliance testing of upstream devices only (i.e., the custom pattern does **not** apply to downstream devices).

2.12.4.5.5 CP2520 (HBR2 Compliance EYE Pattern)

An upstream DP device that is capable of supporting HBR2 shall be capable of transmitting the repetition of scrambled data 00h with 8b/10b encoding. (See Appendix E for details regarding the scrambling polynomial.) This capability may be used by upstream devices that do not support HBR2. The upstream device shall output an Enhanced Framing Scrambler Reset sequence (SR BF BF SR) for every HBR2_COMPLIANCE_SCRAMBLER_RESET register (DPCD Addresses 0024Ah and 0024Bh) symbols transmitter (the count to include the four symbols comprising the scrambler reset sequence). If the HBR2_COMPLIANCE_SCRAMBLER_RESET count is fewer than four, a scrambler reset sequence is not transmitted.

An HBR2-capable downstream DP device shall be capable of receiving the CP2520 (HBR2 Compliance EYE pattern) from test equipment. During compliance testing, the downstream device scrambler shall be reset by an SR symbol after Link Training completes. The HBR2 downstream DP device shall start increasing the SYMBOL_ERROR_COUNT_LANE*x* register's (DPCD Addresses 00210h through 00217h; each register is composed of two bytes, within which the error count is stored in the 15 least significant bits) value each time it has an unscrambled data value other than 00h.

2.12.4.6 UHBR*x* Link Quality Test Support

DisplayPort supports a test procedure for measuring the link quality at UHBR bit rates. The following features are supported:

- Transmission of a Nyquist pattern (128b/132b_TPS1)
- Symbol Error measurement pattern (128b/132b_TPS2)
- PRBS7, PRBS9, PRBS11, PRBS15, PRBS23, and PRBS31 bit patterns
- Custom 264-bit repeating pattern
- Square sequence pattern

The DP Source device may support test pattern selection independently for each Main-Link lane.

Table 2-201 summarizes which patterns for Link Training and Link Quality Measurement are scrambled.

Table 2-201: 128b/132b Encoding and Scrambling Rules for Link Management

Pattern Type	128b/132b Encoded?	Scrambled?
128b/132b_TPS1 (Nyquist pattern)	No	No
128b/132b_TPS2 (Symbol Error measurement Pattern)	Yes	Yes
PRBS7, PRBS9, PRBS11, PRBS15, PRBS23, PRBS31	No	No
Custom 264-bit pattern	No	No
Square sequence pattern	No	No

When transmitting a pattern that is not scrambled, the Source device shall set the SCRAMBLING_DISABLE bit in the TRAINING_PATTERN_SET register (DPCD Address 00102h, bit 5). DP Sink devices shall **not** rely on this bit being set.

2.12.4.6.1 Transmission of Nyquist Pattern

This pattern consists of repetition of Nyquist symbols (without scrambling), identical to 128b/132b_TPS1 for LANE*x*_CR_DONE. This pattern results in the Main-Link toggling at its highest frequency (e.g., 10GHz when the link rate is 20Gbps/lane). System integrators may use this pattern to measure, for example, the jitter performance of the transmitted signals.

A DP Source device signals transmission of this pattern by writing 08h to the Lane's LINK_QUAL_PATTERN_SET field in the LINK_QUAL_LANE*x*_SET register(s) (DPCD Address(es) 0010Bh through 0010Eh, bits 6:0).

After being notified of the transmission of this pattern, a DP Sink device shall blank its screen while keeping the DPRX running.

2.12.4.6.2 Symbol Error Rate Measurement Pattern

See Section 3.5.2.13 for 128b/132b_TPS2 generation.

After being notified of the transmission of this pattern, the DP Sink device shall start increasing the SYMBOL_ERROR_COUNT_LANE*x* register's (DPCD Addresses 00210h through 00217h; each register is composed of two bytes, within which the error count is stored in the 15 least significant bits) value each time it has an unscrambled data value other than 00h.

The DP Source device shall read the SYMBOL_ERROR_COUNT_LANE*x* values some time later. Using the read values and elapsed time, the device shall calculate the approximate symbol error rate.

Transmitting $1E^{+9}$ link symbols takes approximately 10 seconds. Therefore, the transmitter should wait for 10 to 100 seconds before reading the Symbol Error count from a receiver.

Symbol error rate is calculated as follows:

- At 10Gbps/lane (UHBR10):

  Symbol Error Rate in units of 10^{-9} *= Error_Count / (0.3125 × Measurement Period in seconds)*

- At 13.5Gbps/lane (UHBR13.5):

  Symbol Error Rate in units of 10^{-9} *= Error_Count / (0.421875 × Measurement Period in seconds)*

- At 20Gbps/lane (UHBR20):

  Symbol Error Rate in units of 10^{-9} *= Error_Count / (0.625 × Measurement Period in seconds)*

2.12.4.6.3 PRBS and Bit Pattern

See Appendix N for a detailed description of the UHBR*x* PRBS bit patterns used by the LINK_QUAL_PATTERN_SET field in the LINK_QUAL_LANE*x*_SET register(s) (DPCD Address(es) 0010Bh through 0010Eh, bits 6:0).

2.12.4.6.4 128b/132b Channel Coding 264-Bit Custom Pattern

An upstream DP device that supports 128b/132b channel coding (UHBR10, UHBR13.5, or UHBR20) shall be capable of transmitting a repeating 264-bit custom pattern. This custom pattern is **not** scrambled, does **not** have FEC, and shall **not** be interrupted by any sync pattern (PHY_SYNC_ONLY, or LT_SCRAMBLER_RESET or POST_LT_SCRAMBLER_RESET). The custom pattern allows for more flexibility during PHY Layer Compliance testing of upstream devices only (i.e., the custom pattern does **not** apply to downstream devices).

2.12.4.6.5 Square Sequence Pattern

This pattern consists of the repetition of continuous 1s, followed by continuous 0s (without scrambling).

A DP Source device signals transmission of this pattern by writing 48h to the Lane's LINK_QUAL_PATTERN_SET field in the LINK_QUAL_LANE*x*_SET register(s) (DPCD Address(es) 0010Bh through 0010Eh, bits 6:0).

The number of continuous 1s followed by continuous 0s are written in the LINK_SQUARE_PATTERN_num + 1 register (DPCD Address 0010Fh), from a single 1, followed by a single 0, and then up to 256 1s followed by up to 256 0s.

After being notified of this pattern's transmission, a DP Sink device shall blank its screen while keeping the DPRX running.

2.12.5 AUX Device Services

AUX Device Services are used for the purpose of communication between the graphic host (a DP Source device) and display device (a DP Sink device). The following are examples of display device services that are supported by using AUX transactions:

- DisplayID or legacy EDID Support
- MCCS Support
- Sink Event Notification

DisplayID or legacy EDID and MCCS over DDC/CI are supported by mapping I^2C transactions onto DisplayPort to maintain maximum software transparency.

In addition, the AUX transactions are expected to be used for an optional content protection feature.

2.12.5.1 E-DDC Support through I^2C Mapping

E-DDC allows the display to inform the host about its identity and capability using an I^2C bus. E-DDC enables the communication channel to address a larger set of data than the 128 bytes of the base DisplayID or legacy EDID block. E-DDC allows access of up to 32KB of data based on a segment pointer which allows access to multiple blocks of 256 bytes.

Using the I^2C bus transaction mapping described in Section 2.11.5, E-DDC transactions may be supported with AUX transactions over the AUX_CH.

2.12.5.2 MCCS over DDC/CI Support through I^2C-over-AUX Transactions

MCCS provides a set of commands that may be used to control the functions and features of the display.

By using the I^2C-over-AUX transactions described in Section 2.11.5, MCCS transactions over DDC/CI may be supported over the AUX_CH.

DP v1.4a does **not** define a minimum set necessary of MCCS commands. However, some specifications, including the *MCCS Standard* and operating system logo programs, do define minimum sets that need to be supported.

2.12.5.3 Sink Event Notification

DP v1.4a supports a mechanism through which a Sink device can notify the Source device of a Sink event.

Appendix B describes an example of how the sink event notification may be supported.

2.13 Alternate Scrambler Reset for eDP

2.13.1 Protocol Differentiation Method

An alternate, optional scrambler reset method is defined to ensure non-interoperability between compliant eDP Sources and non-eDP Sinks in which such non-interoperability is defined as the inability to reliably convey audio or video data from a Source to a Sink device.

Consistent with other eDP practices, the system integrator is ultimately responsible for ensuring interoperability between the eDP Source and Sink device chosen for a particular application. Determination by a given device (Source, Sink, or Branch) used in an embedded system is implementation-specific and beyond the scope of this Standard.

With the alternate scrambler reset method, the SR symbol resets the LFSRs in the Source and Sink devices to FFFEh, rather than (the non-eDP connection) to FFFFh. This method shall be implemented only in devices that provide eDP connections over embedded (non-user-accessible) interconnects. Tamper-resistant methods[a] should be used in devices that allow operation in either eDP or box-to-box DisplayPort applications, to be determined at manufacturing/assembly time by the system integrator:

2.13.2 Symbol Error Rate Measurement Pattern Output (Informative)

Table 2-202 contains the first 50 symbols of the Symbol Error Rate Measurement Pattern following a Scrambler Reset. These are 8-bit values after scrambling and before 8b/10b encoding.

a. *For example: package bond options, fuses, or external strapping options, buried vias/trace connections.*

Table 2-202: Symbol Error Rate Measurement Pattern following Scrambler Reset

Symbol #	Normal Scrambling (hex)	Alternate Scrambling (hex)	Symbol #	Normal Scrambling (hex)	Alternate Scrambling (hex)
1	FF	FF	26	02	CF
2	17	97	27	77	F1
3	C0	C0	28	2A	64
4	14	88	29	CD	07
5	B2	12	30	34	C5
6	E7	65	31	BE	DF
7	02	C9	32	E0	3F
8	82	94	33	A7	27
9	72	BA	34	5D	92
10	6E	BB	35	24	D0
11	28	AB	36	B1	0D
12	A6	2A	37	9B	D9
13	BE	01	38	A1	74
14	6D	14	39	BD	A9
15	BF	61	40	22	86
16	8D	2F	41	D4	23
17	BE	00	42	45	D2
18	40	29	43	1D	D4
19	A7	F8	44	D3	A3
20	E6	6F	45	D7	8D
21	2C	87	46	EA	A0
22	D3	CF	47	76	90
23	E2	F3	48	EE	3B
24	B2	14	49	2C	87
25	07	85	50	DA	96

2.14 Messaging AUX Client

The Messaging AUX client described in this section achieves the following features:

- Mechanism for transmitting requests and receiving replies from remote DP nodes using Native AUX transactions to maintain a DP topology map, to add, update, and delete Virtual Channels, to read or write remote devices DPCD locations, and to transmit I^2C transactions to I^2C devices connected to remote DP nodes (e.g., DisplayID or legacy EDID read).
- Mechanism for reporting status changes to clients of the Messaging AUX client
- Mechanism for reporting errors in delivery of requests to the request originator.

The Messaging AUX client is a client of the AUX transaction arbiter that provides the means of communication between any two DP nodes of a topology. Figure 2-135 illustrates the position of the Messaging AUX client in DP nodes.

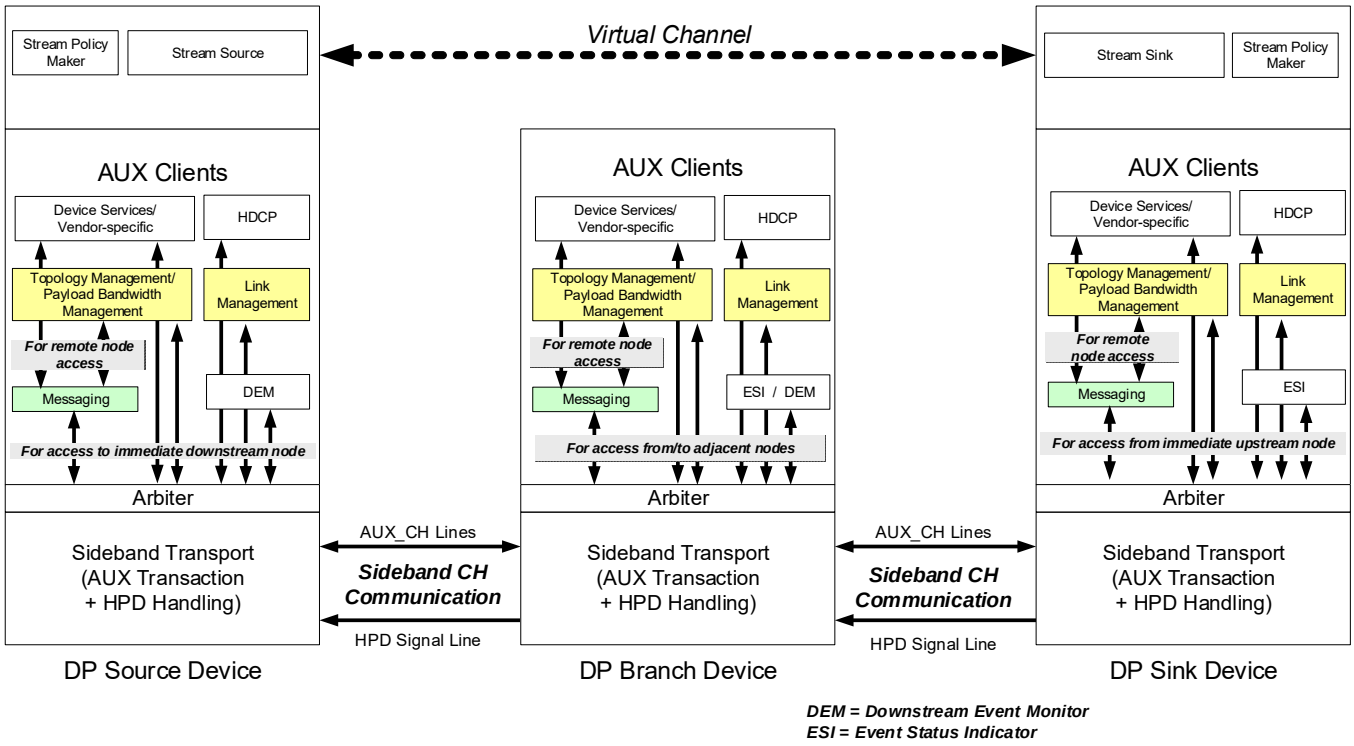


Figure 2-135: Messaging AUX Client in DP Nodes

Clients of the Messaging AUX Client are the Topology Management, Payload Bandwidth Management, and Device-/Vendor-specific Services for Stream/Link Policy Maker.

This section consists of the following sub-sections:

- Section 2.14.1 – Messaging AUX Client Layers

  Brief overview of the two functional layers constituting the Messaging AUX Client Layer; Message Transaction Layer on top of Sideband MSG Layer.

- Section 2.14.2 – Message Transaction Layer

  A Request and Reply Message Transaction pair constitutes a Message Transaction sequence. Request Message Transactions may be originated either by a DPTX of an upstream DP node (DOWN_REQ_MSG) or DPRX of a downstream DP node (UP_REQ_MSG). Syntax of Request and Reply Message Transactions and handling of multiple Message Transactions are covered in this sub-section.

- Section 2.14.3 – Sideband MSG Layer

  The Sideband MSG consists of Sideband MSG Header and Body. The Sideband MSG Header describes the target DP Node address (referred to as "Relative Address" (RAD)) and which nodes along the message path are to receive the message. The Sideband MSG Body carries the Body of the Message Transaction. If the Message Transaction Body does not fit in a single Sideband MSG Body, it is divided into multiple Sideband MSG Bodies. Each Sideband MSG Header for a given Message Transaction has the same Sideband MSG Header except a bit indicating End Of Transaction (EMT) or Start of Transaction (SMT).

- Section 2.14.4 – AUX Support for Messaging AUX Client

  Sideband MSG uses Native AUX write/read transactions to certain DPCD address range to move Sideband MSG Header and Body between adjacent DP nodes. The intermediate DP nodes update Relative Address and forward the Sideband MSG to the target DP node.

- Section 2.14.5 – RAD Updated by MST Devices in the Path

  The RAD is an array of nibbles of size Link_Count_Total – 1 contained in Sideband MSG Header.

- Section 2.14.6 – Broadcast Message Transactions

  Messaging AUX Client provides for Broadcast messages as well as targeted messages. Broadcast Message Transactions are identified with a unique Relative Address with which the recipients of the Broadcast Message can reply with an ACK/NACK Message.

- Section 2.14.7 – Message Delivery

  Procedures and mandates are defined for delivering Sideband MSGs between DP devices that are using Native AUX requests.

- Section 2.14.8 – Error Handling

  Errors are handled at the Message Transaction Layer. The Sideband MSG shall be dropped when an error is detected at the Sideband MSG Layer, thus causing a Message Transaction timeout error.

- Section 2.14.9 – Descriptions of Available Message Transaction Requests

  Describes the 14 available Request Message Transactions.

The message syntax used within this section assumes the following:

- First byte defined is transmitted first
- All fields are defined from most-significant bit and most significant byte first
- The byte-aligned () function returns true when the next input bit is the first bit of a new byte (the next bit is on a new byte boundary)

2.14.1 Messaging AUX Client Layers

The Messaging AUX Client consists of two functional layers – Message Transaction and Sideband MSG – as illustrated in Figure 2-136.

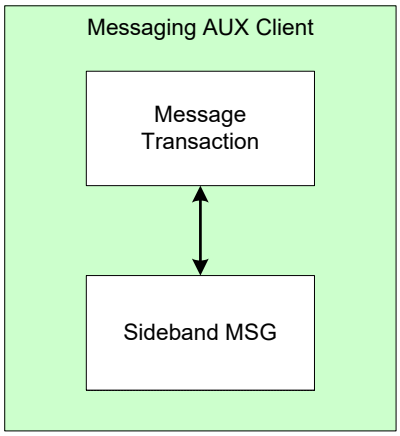


Figure 2-136: Messaging AUX Client Layers

The Message Transaction Layer implements the Message Transaction protocol that is built on top of the Sideband MSG protocol. The Message Transaction protocol is a request-reply protocol supporting the topology discovery and maintenance, establishment or removal of VC Payloads and transfer of data between DP nodes for Device-or Vendor-specific Services.

Message Transaction protocol has a version number associated with it, as defined in Table 2-203. A Source device obtains this version number on a path by transmitting the GET_MESSAGE_TRANSACTION_VERSION Message Transaction to the last MST device with a branching unit driving a stream sink. This last MST device responds with the Message Transaction protocol version number that it implements, –or– replies with a NAK if that device does not support the GET_MESSAGE_TRANSACTION_VERSION Message Transaction. Upstream devices treat a NAK as indicating a Protocol Version Number of 1.

All MST-capable Branch and Sink devices compliant to *DP v1.3* (or higher) shall support the GET_MESSAGE_TRANSACTION_VERSION Message Transaction. Such devices shall minimally return a value that corresponds to the Version and Revision number for the DisplayPort Standard, as indicated in Table 2-203. In particular, DP-compliant devices shall not return a Protocol Version Number of 01h because the GET_MESSAGE_TRANSACTION_VERSION Message Transaction is now supported.

Table 2-203: Transaction Message Version Numbers

DisplayPort Standard Version	DPCD Revision Number	Transaction Message Version Number
DP v1.2a	DPCD r1.2	01h
DP v1.3, *DP v1.4a*, and *DP v2.0*	DPCD r1.4	02h

Only DP MST devices that implement the Topology Maintenance function as a Topology Manager can originate request Message Transactions with a target DP device address. Any DP MST device can originate Broadcast Message Transactions as Broadcast Message Transactions do **not** contain a target DP device.

A Message Transaction request originated by a DPTX is referred to as a down (i.e., downward direction) request message, DOWN_REQ_MSG, and the associated reply is referred to as a down reply message, DOWN_REP_MSG. (See Figure 2-137.) A Message Transaction request originated by a DPRX is referred to as an up (i.e., upward-direction) request message, UP_REQ_MSG, and the associated reply is referred to as an up reply message, UP_REP_MSG. (See Figure 2-138.)

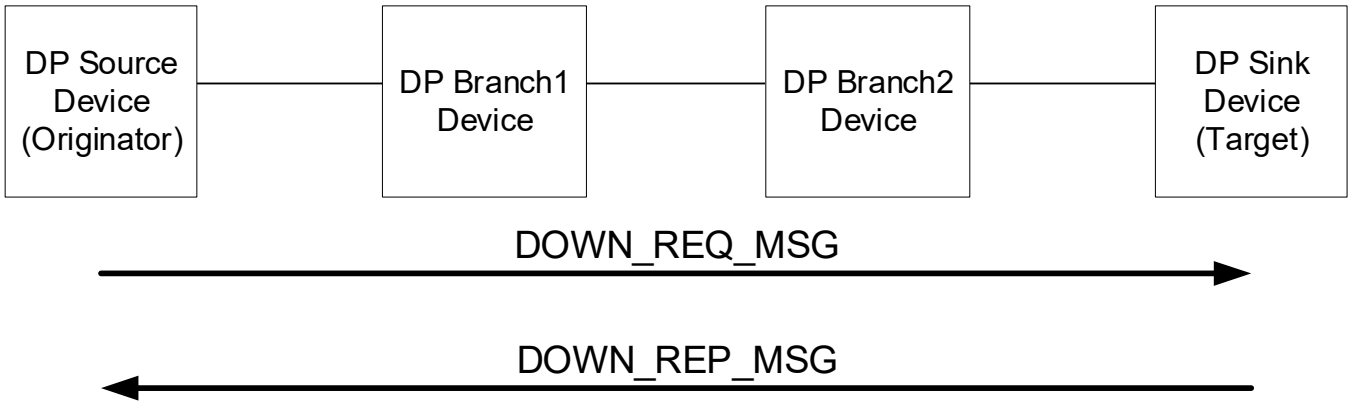


Figure 2-137: DOWN_REQ_MSG and DOWN_REP_MSG

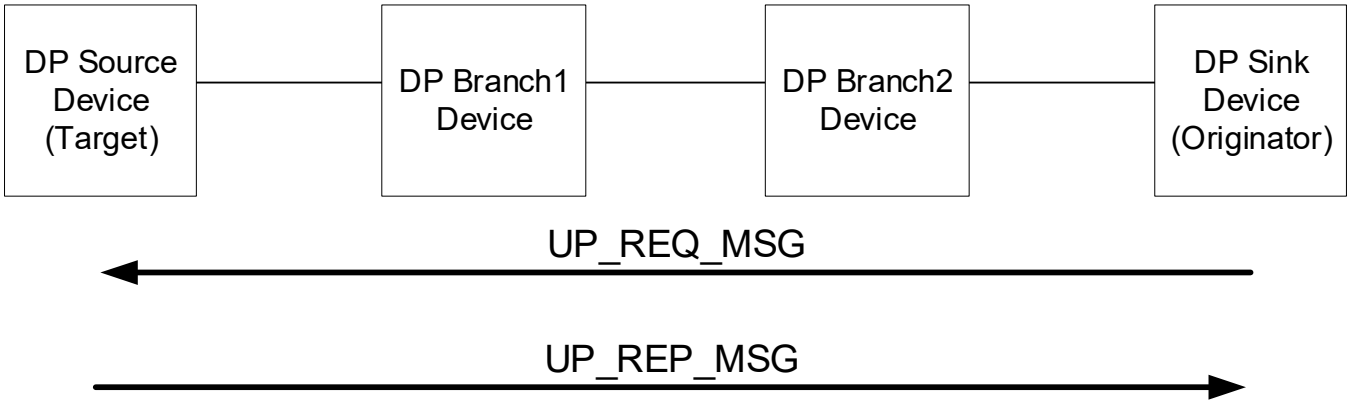


Figure 2-138: UP_REQ_MSG and UP_REP_MSG

The Sideband MSG Layer implements the Sideband MSG protocol using Native AUX transactions as the underlying layer. The Sideband MSG protocol consists of data packets transmitted between two DP nodes. A Sideband MSG data packet consists of a Sideband MSG header containing the DP node address (Relative Address, or RAD) followed by the Sideband packet body containing the Sideband MSG client data and Sideband MSG body CRC.

Native AUX transactions are used to transfer the data from a DP node to its immediate downstream or upstream DP node.

2.14.2 Message Transaction Layer

The Message Transaction Layer implements the Message Transaction protocol. The Message Transaction protocol is used by one DP node to obtain or update information in another DP node.

2.14.2.1 Message Transaction Protocol

The Message Transaction protocol is composed of Message Transaction sequences. There are two types of message transactions – Request and Reply Message transactions. A Request-and-Reply Message Transaction pair defines a Message Transaction sequence.

Table 2-204: Message_Transaction_Sequence Syntax

Syntax	# of Bits
Message_Transaction_Sequence() { Message_Transaction_Request() Message_Transaction_Reply() }	

2.14.2.2 Message_Transaction_Request()

Table 2-205: Message_Transaction_Request Syntax

Syntax	# of Bits
Message_Transaction_Request() { zero Request_Identifier Request_Data() }	 1 7

2.14.2.2.1 Request_Identifier

The Request_Identifier field specifies the information that is to be obtained or updated. Table 2-206 lists the valid Request_Identifiers, and whether the request includes request data.

Table 2-206: Request Names and their Corresponding Request_Identifier

Request_Identifier	Request Name	Request Data
00h	GET_MESSAGE_TRANSACTION_VERSION	✔
01h	LINK_ADDRESS	
02h	CONNECTION_STATUS_NOTIFY	✔
10h	ENUM_PATH_RESOURCES	✔
11h	ALLOCATE_PAYLOAD	✔
12h	QUERY_PAYLOAD	✔
13h	RESOURCE_STATUS_NOTIFY	✔
14h	CLEAR_PAYLOAD_ID_TABLE	
20h	REMOTE_DPCD_READ	✔
21h	REMOTE_DPCD_WRITE	✔
22h	REMOTE_I2C_READ	✔
23h	REMOTE_I2C_WRITE	✔
24h	POWER_UP_PHY	✔
25h	POWER_DOWN_PHY	✔
30h	SINK_EVENT_NOTIFY	✔
38h	QUERY_STREAM_ENCRYPTION_STATUS	✔

2.14.2.2.2 Request_Data()

Updated in *DP v2.0*.

Request_Data is dependent on the Request_Identifier of the request message transaction. Table 2-207 specifies the Request_Data for requests that have request data fields. Section 2.14.9 defines the fields that are included in Table 2-207. Requests that are not listed in Table 2-207 do **not** includes request data.

Table 2-207: Request_Data Syntax

Syntax	# of Bits
Request_Data()	
{	
if (Request_Identifier == 00h) **GET_MESSAGE_TRANSACTION_VERSION**	
{	
Port_Number	4
Zeros	4
}	
else (Request_Identifier == 02h **CONNECTION_STATUS_NOTIFY**	
{	
Port_Number	4
zeros	4
Global_Unique_Identifier	128
zero	1
Legacy_Device_Plug_Status	1
DisplayPort_Device_Plug_Status	1
Messaging_Capability_Status	1
Input_Port	1
Peer_Device_Type	3
}	
else if (Request_Identifier == 10h) **ENUM_PATH_RESOURCES**	
{	
Port_Number	4
zeros	4
}	
else if (Request_Identifier == 11h **ALLOCATE_PAYLOAD**	
{	
Port_Number	4
Number_SDP_Streams	4
zero	1
Virtual_Channel_Payload_Identifier	7
Payload_Bandwidth_Number	16
for (i = 0; i < Number_SDP_Streams; i++)	
{	
SDP_Stream_Sink[i]	4
}	
while (!bytealigned())	
{	
zeros	1
}	
}	

Table 2-207: Request_Data Syntax (Continued)

Syntax	# of Bits
else if (Request_Identifier == 12h) **QUERY_PAYLOAD**	
{	
Port_Number	4
zeros	4
zero	1
Virtual_Channel_Payload_Identifier	7
}	
else if (Request_Identifier == 13h) **RESOURCE_STATUS_NOTIFY**	
{	
Port_Number	4
zeros	4
Global_Unique_Identifier	128
Available_PBN	16
}	
else if (Request_Identifier == 20h) **REMOTE_DPCD_READ**	
{	
Port_Number	4
DPCD_Address	20
Number_Of_Bytes_To_Read	8
}	
else if (Request_Identifier == 21h) **REMOTE_DPCD_WRITE**	
{	
Port_Number	4
DPCD_Address	20
Number_Of_Bytes_To_Write	8
for (i = 0; i < Number_Of_Bytes_To_Write; i++)	
Write_Data[i]	8
}	
else if (Request_Identifier == 22h) **REMOTE_I2C_READ**	
{	
Port_Number	4
zeros	2
Number_Of_I2C_Transactions	2
for (i = 0; i < Number_Of_I2C_Transactions - 1; i++)	
{	
zero	1
Write_I2C_Device_Identifier[i]	7
Number_Of_Bytes_To_Write[i]	8
for (j = 0; j < Number_Of_Bytes_To_Write; j++)	
{	
I2C_Data_To_Write[i][j]	8
}	
zeros	3
No_Stop_Bit[i]	1
I2C_Transaction_Delay[i]	4
}	
zero	1
Read_I2C_Device_Identifier[i + 1]	7
Number_Of_Bytes_To_Read	8
}	

Table 2-207: Request_Data Syntax (Continued)

Syntax	# of Bits
else if (Request_Identifier == 23h) **REMOTE_I2C_WRITE**	
{	
Port_Number	4
zeros	5
Write_I2C_Device_Identifier	7
Number_Of_Bytes_To_Write	8
for (i = 0; i < Number_Of_Bytes_To_Write; i++)	8
I2C_Data_To_Write[i]	
}	
else if (Request_Identifier == 24h) **POWER_UP_PHY**	
{	
Port_Number	4
zeros	4
}	
else if (Request_Identifier == 25h) **POWER_DOWN_PHY**	
{	
Port_Number	4
zeros	4
}	
else if (Request_Identifier == 30h) **SINK_EVENT_NOTIFY**	
{	
Port_Number	4
zeros	4
Global_Unique_Identifier	128
Event_Identifier	16
}	
else if (Request_Identifier == 38h) **QUERY_STREAM_ENCRYPTION_STATUS**	
{	
Stream_ID	8
Client_ID	56
Stream_Event	2
Stream_Event_Mask	1
Stream_Behavior	2
Stream_Behavior_Mask	1
zeros	2
}	
}	

2.14.2.3 Message_Transaction_Reply()

Each Message Transaction request shall have a corresponding Message Transaction reply. Table 2-208 defines the Message_Transaction_Reply syntax.

Table 2-208: Message_Transaction_Reply Syntax

Syntax	# of Bits
Message_Transaction_Reply() { Reply_Type Request_Identifier Reply_Data() }	 1 7

2.14.2.3.1 Reply_Type

The Reply_Type field identifies whether the Message Transaction reply is an acknowledge (ACK), or negative acknowledge (NAK), message. Reply_Type set to 1 indicates the Message Transaction is a NAK. Reply_Type cleared to 0 indicates an ACK Message Transaction.

2.14.2.3.2 Request_Identifier

The Request_Identifier field is a copy of the Request Message Transaction field of the same name. This associates the reply with the corresponding request.

2.14.2.3.3 Reply_Data()

The contents of the Message Transaction Reply_Data field depend on the Reply_Type field and the Request_Identifier field value, as defined in Table 2-209.

Table 2-209: Reply_Data Syntax

Syntax	# of Bits
Reply_Data() { if (Reply_Type == ‘1’) { Global_Unique_Identifier Reason_For_Nak NAK_Data } else ACK_Data() }	 128 8 8

2.14.2.3.3.1 Global_Unique_Identifier

The global unique identifier of the DP device originating the NAK reply message transaction.

2.14.2.3.3.2 Reason_For_Nak

Indicates why a NAK reply was generated. Table 2-210 lists the defined NAK reasons.

Table 2-210: Reasons for NAK

Reason_For_Nak Value	Short Name	Description
01h	WRITE_FAILURE	Insufficient buffer space to store message transaction.
02h	INVALID_RAD	Invalid address including link count, transmitting a Sideband MSG to a logical port.
03h	CRC_FAILURE	Message Transaction CRC error.
04h	BAD_PARAM	Invalid request parameter.
05h	DEFER	Unable to process message within timeout period **(defer)**.
06h	LINK_FAILURE	Link failure.
07h	NO_RESOURCES	Insufficient resources.
08h	DPCD_FAIL	DPCD access failure.
09h	I2C_NAK	I^2C NAK received.
0Ah	ALLOCATE_FAIL	ALLOCATE_PAYLOAD request failure (not due to lack of resources).

2.14.2.3.3.3 WRITE_FAILURE

This reply is transmitted when a DP MST device is unable to transmit the Sideband MSG to the adjacent DP MST device as specified in Section 2.14.7.

2.14.2.3.3.4 INVALID_RAD

This reply is transmitted when the request message is received by an end device with an LCR that is **not** equal to 0.

2.14.2.3.3.5 CRC_FAILURE

This reply is transmitted when a DP MST device detects an invalid Sideband MSG Header CRC value or when the targeted device detects an invalid Sideband MSG Body CRC value.

2.14.2.3.3.6 BAD_PARAM

This reply is transmitted when a Message Transaction parameter is in error; for example, the next port number is invalid or no device is connected to the port associated with the port number.

2.14.2.3.3.7 DEFER

This reply is transmitted when a DP MST device cannot execute the message transaction within the time allocated, as specified in Section 2.14.7. For example, this reply shall be transmitted when an ALLOCATE_PAYLOAD message transaction is received while another ALLOCATE_PAYLOAD message transaction is being executed. When this condition occurs, the DP MST device that is receiving the second ALLOCATE_PAYLOAD shall transmit a NAK reply with DEFER as the Reason_For_Nak to the second ALLOCATE_PAYLOAD message transaction.

2.14.2.3.3.8 LINK_FAILURE

This reply is transmitted in response to the Message Transaction requests that require an active Main-Link. These requests are ENUM_PATH_RESOURCES and ALLOCATE_PAYLOAD. This reply is transmitted when the link cannot be established with the downstream DPRX.

2.14.2.3.3.9 NO_RESOURCES

This reply is transmitted in response to an ALLOCATE_PAYLOAD Message Transaction when the requested PBN bandwidth is unavailable. The reply is transmitted by the DP MST device that detects the lack of bandwidth. This reply is not transmitted when the ALLOCATE_PAYLOAD Message Transaction failed because the resource is in use by another source, –or– a new stream cannot be allocated because the stream count limit has been reached. The stream count limit is an implementation decision and may be less than 63.

2.14.2.3.3.10 DPCD_FAIL

This reply is associated with the REMOTE_DPCD requests. The reply is transmitted when an AUX NACK or DEFER is received to any Native AUX transaction resulting from the execution of the REMOTE_DPCD request. The DPCD_FAIL response is transmitted after all AUX retries.

2.14.2.3.3.11 I2C_NAK

This reply is associated with the REMOTE_I2C requests. The reply is transmitted when an AUX NACK or DEFER is received to any I^2C-over-AUX transaction resulting from the execution of the REMOTE_DPCD request. The I2C_NAK response is transmitted after all AUX retries.

2.14.2.3.3.12 ALLOCATE_FAIL

This reply is transmitted in response to an ALLOCATE_PAYLOAD Message Transaction when the ALLOCATE_PAYLOAD Message Transaction fails for any reason other than the available PBN for the link is less than the requested PBN.

2.14.2.3.3.13 NAK_Data

Any other information needed for the NAK reply. For example, the DPCD write failure Reason_For_Nak reply uses the NAK_Data field to indicate the number of bytes written before the failure occurred.

2.14.2.3.3.14 ACK_Data()

Table 2-211 defines the data that is supplied with the ACK reply for requests that reply with data. The data fields listed in the table are defined in Section 2.14.9, which describes each request.

Table 2-211: ACK_Data Syntax

Syntax	# of Bits
ACK_Data()	
{	
if (Request_Identifier == 00h) **GET_MESSAGE_TRANSACTION_VERSION**	
{	
Message_Transaction_Version_Number	8
}	
else (Request_Identifier == 01h) **LINK_ADDRESS**	
{	
Global_Unique_Identifier	128
zeros	4
Number_Of_Ports	4
for (i = 0; i < Number_Of_Ports; i++)	
{	
Input_Port[i]	1
Peer_Device_Type[i]	3
Port_Number[i]	4
Messaging_Capability_Status[i]	1
DisplayPort_Device_Plug_Status[i]	1
if (Peer_Device_Type[i] == 101b)	
{	
Current_Capabilities_Structure	128
}	
if (Input_Port[i] == 0)	
{	
Legacy_Device_Plug_Status[i]	1
zeros	5
DPCD_Revision	8
Peer_Global_Unique_Identifier	128
Number_SDP_Streams[i]	4
Number_SDP_Stream_Sinks[i]	4
}	
else	
{	
zeros	6
}	
}	
}	
else if (Request_Identifier == 10h) **ENUM_PATH_RESOURCES**	
{	
Port_Number	4
zeros	4
Full_Payload_Bandwidth_Number_Available	16
Payload_Bandwidth_Number	16
}	
else if (Request_Identifier == 11h) **ALLOCATE_PAYLOAD**	
{	
Port_Number	4
zeros	5
Virtual_Channel_Payload_Identifier	7
Allocated_Payload_Bandwidth_Number	16
}	

Table 2-211: ACK_Data Syntax (Continued)

Syntax	# of Bits
else if (Request_Identifier == 12h) **QUERY_PAYLOAD**	
{	
Port_Number	4
zeros	4
Allocated_PBN	16
}	
else if (Request_Identifier == 20h) **REMOTE_DPCD_READ**	4
{	4
zeros	8
Port_Number	
Number_Of_Bytes_Read	8
for (i = 0; i < Number_Of_Bytes_To_Read; i++)	
Data_Read[i]	
}	
else if (Request_Identifier == 21h) **REMOTE_DPCD_WRITE**	4
{	4
zeros	
Port_Number	
else if (Request_Identifier == 22h) **REMOTE_I2C_READ**	
{	
zeros	4
Port_Number	4
Number_Of_Bytes_Read	8
for (i = 0; i < Number_Of_Bytes_To_Read; i++)	
Data_Read[i]	8
}	
else if (Request_Identifier == 24h) **POWER_UP_PHY**	
{	
Port_Number	4
zeros	4
}	
else if (Request_Identifier == 25h) **POWER_DOWN_PHY**	
{	
Port_Number	4
zeros	4
}	
else if (Request_Identifier == 38h) **QUERY_STREAM_ENCRYPTION_STATUS**	
{	
Stream_State	2
Stream_Repeater_Function	1
Stream_Encryption	1
Stream_Authentication	1
Zeros	3
Stream_Output_Sink_Type	3
Stream_Output_CP_Type	2
Zeros	2
Signed	1
Stream_ID	8
if (Signed == 1)	
{	
L'	160 or 256
}	
}	
}	

2.14.2.4 Multiple Message Transaction Request Handling

A Message Transaction originator can issue up to two requests to a given Target DP MST node without waiting for a reply. The Target DP MST node may execute requests simultaneously. Message Transaction execution shall not inhibit forwarding node type Sideband MSGs to other DP MST nodes. Path messages shall not be forwarded until the DP MST node performs the action indicated by the message. If it is necessary for one message to complete before another message may be executed, it is the message originator's responsibility to wait for the first message to complete (by receiving an ACK) before issuing the second message.

2.14.3 Sideband MSG Layer

The Sideband MSG provides the mechanism for transferring data between DP MST nodes. The Sideband MSG protocol is used to transfer Message Transaction requests and replies between DP MST nodes. If the Message Transaction length is greater than what can fit into a Sideband MSG body, the Message Transaction is split across multiple Sideband MSGs. Figure 2-139 illustrates how a Message Transaction is split across multiple Sideband MSGs. In the example, the Sideband MSG header size is assumed to be five bytes in length. The first byte of a Sideband MSG is written to the beginning of the appropriate DPCD Sideband MSG buffer.

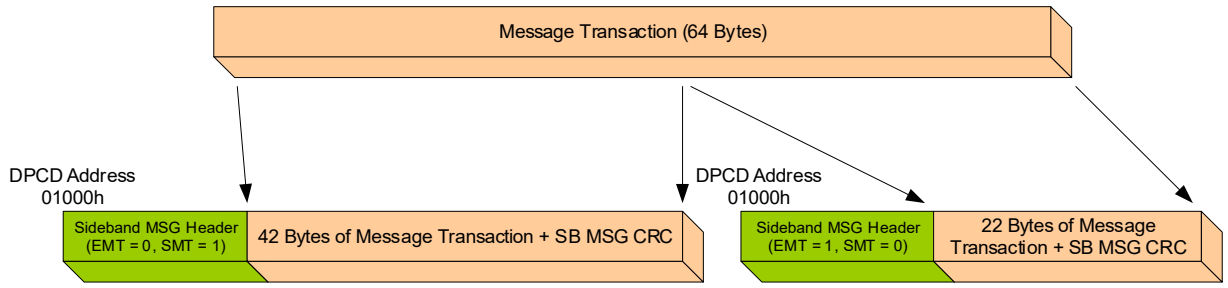


Figure 2-139: Mapping Message Transaction to Multiple Sideband MSGs (SB MSG CRC Is the Sideband_MSG_Data_CRC Field)

A Sideband MSG packet consists of a Sideband_MSG_Header and Sideband_MSG_Body. The Sideband MSG packet shall be less than or equal to 48 bytes. The Sideband_MSG_Header contains addressing information while the Sideband_MSG_Body contains the data to be transferred. Table 2-212 defines the Sideband MSG syntax.

Table 2-212: Sideband_MSG Syntax

Syntax	# of Bits
`Sideband_MSG` `{` `  Sideband_MSG_Header()` `  Sideband_MSG_Body()` `}`	

2.14.3.1 Sideband_MSG_Header()

The Sideband MSG header specifies which DP nodes are to process or receive Sideband MSG data. Table 2-213 defines the Sideband_MSG_Header syntax.

Table 2-213: Sideband_MSG_Header Syntax

Syntax	# of Bits
Sideband_MSG_Header()	
{	
Link_Count_Total	4
Link_Count_Remaining	4
for (i = 0; i < Link_Count_Total – 1; i++)	
{	
Relative_Address[i]	4
}	
while (!bytealigned())	
{	
zero_bit	1
}	
Broadcast_Message	1
Path_Message	1
Sideband_MSG_Body_Length	6
Start_Of_Message_Transaction	1
End_Of_Message_Transaction	1
zero	1
Message_Sequence_No	1
Sideband_MSG_Header_CRC	4
}	

2.14.3.1.1 Link_Count_Total

Link_Count_Total (LCT) is the total number of DP links a Sideband MSG traverses from message originator to message target. The maximum value for Link_Count_Total is 15. Therefore, the total number of physical DP links is 15.

2.14.3.1.2 Link_Count_Remaining

Link_Count_Remaining (LCR) is the remaining number of DP links a Sideband MSG shall traverse to reach the message target. The Link_Count_Remaining value is initialized to the Link_Count_Total value by the originator Sideband MSG Layer. Along the message path, the DPTX while forwarding the Sideband MSG decrements the Link_Count_Remaining value by one. The Link_Count_Remaining value is equal to Link_Count_Total – 1 when the message arrives at the first DP node from the message originator.

2.14.3.1.3 Relative_Address

The Relative_Address (RAD) is the address of a DP node relative to the originator of the Sideband MSG. How the RAD is updated by intermediate MST devices along the path of the Message Transaction to a target device is described in Section 2.14.5.

2.14.3.1.4 Sideband_MSG_Body_Length

The Sideband_MSG_Body_Length gives the number of bytes contained in the Sideband MSG body. The number of data bytes transferred in the Sideband MSG body is the Sideband_MSG_Body_Length field value minus 1. The Sideband_MSG_Body_Length field value includes the Sideband_MSG_Data_CRC. The Message Transaction's size can be calculated by adding all the Sideband_MSG_Body_Length field values needed to transfer the Message Transaction and then subtracting the count of Sideband MSGs that are needed to transfer the Message Transaction.

2.14.3.1.5 Start_Of_Message_Transaction

When set to 1, the Start_Of_Message_Transaction (SMT) bit indicates that the Sideband MSG body contains the start of a new Message Transaction.

2.14.3.1.6 End_Of_Message_Transaction

When set to 1, the End_Of_Message_Transaction (EMT) bit indicates that the current Sideband MSG is the last Sideband MSG for the current message transaction. This bit shall be set to 1, even if the current message transaction needs only one Sideband MSG.

2.14.3.1.7 Path_Message

When set to 1, the Path_Message bit indicates that all DP MST nodes between the originator and the target shall read and react to the data in the Sideband MSG data area. When cleared to 0, intermediate DP nodes along the message transaction path may still need to modify the data within the Sideband MSG data area, but the data is only targeted for the target DP MST node. All DP MST nodes along the Sideband MSG path shall modify the relative address and Link Count Remaining fields (LCR) as stated in Section 2.14.3.1.3 and Section 2.14.3.1.2, respectively, regardless of the state of the Path_Message bit. A DP device can only execute one path message at a time regardless of the source of the message.

2.14.3.1.8 Message_Sequence_No

The Message_Sequence_No (MSN), bit identifies individual Message Transactions to a given DP device. A DP Message Transaction originator cannot transmit two Message Transactions with the same MSN to the same DP device without a reply to the first Message Transaction being received first.

2.14.3.1.9 Sideband_MSG_Header_CRC

The result of a CRC-4 calculation over the Sideband_MSG_Header starts with the Link_Count_Total and ends with the Message_Sequence_No field. The polynomial for the CRC-4 is $x^4 + x + 1$. The CRC-4 calculation is defined below.

```
uint8_t crc4(const uint8_t * data, size_t NumberOfNibbles)
{
	uint8_t	BitMask		= 0x80;
	uint8_t	BitShift	= 7;
	uint8_t	ArrayIndex	= 0;
	int	NumberOfBits	= NumberOfNibbles * 4;
	uint8_t	Remainder	= 0;

	while (NumberOfBits != 0)
	{
		NumberOfBits--;

		Remainder <<= 1;
		Remainder |= (data[ArrayIndex] & BitMask) >> BitShift;

		BitMask >>= 1;
		BitShift--;

		if (BitMask == 0)
		{
			BitMask = 0x80;
			BitShift = 7;
			ArrayIndex++;
		}

		if ((Remainder & 0x10) == 0x10)
		{
		   Remainder ^= 0x13;
		}
	}

	NumberOfBits = 4;
	while (NumberOfBits != 0)
	{
		NumberOfBits--;

		Remainder <<= 1;

		if ((Remainder & 0x10) != 0)
		{
		   Remainder ^= 0x13;
		}
	}

	return Remainder;
}
```

2.14.3.2 Sideband_MSG_Body()

The Sideband MSG body contains the data to be transferred between DP MST nodes. The Sideband MSG protocol does not examine the contents of the Sideband MSG body. Table 2-214 defines the Sideband_MSG_Body syntax.

Table 2-214: Sideband_MSG_Body Syntax

Syntax	# of Bits
Sideband_MSG_Body() { for (i = 0; i < Sideband_MSG_Body_Length - 1; i++) { Sideband_MSG_Data	8
} Sideband_MSG_Data_CRC	8
}	

2.14.3.2.1 Sideband_MSG_Data

The Sideband MSG data contains the information to be transferred from one DP node to another. The Sideband_MSG_Body_Length field specifies the number of data bytes in the Sideband MSG body. The number of data bytes is the Sideband_MSG_Body_Length field value minus one.

2.14.3.2.2 Sideband_MSG_Data_CRC

The result of a CRC-8 calculation over the Sideband_MSG_Data field of the Sideband_MSG_Body. The polynomial for the CRC-8 is $x^8 + x^7 + x^6 + x^4 + x^2 + 1$. The CRC-8 calculation is defined below.

```
uint8_t crc4(const uint8_t * data, uint8_t NumberOfBytes)
{
	uint8_t	BitMask		= 0x80;
	uint8_t	BitShift	= 7;
	uint8_t	ArrayIndex	= 0;
	uint16_t	NumberOfBits	= NumberOfBytes * 8;
	uint16_t	Remainder	= 0;

	while (NumberOfBits != 0)
	{
		NumberOfBits--;

		Remainder <<= 1;
		Remainder |= (data[ArrayIndex] & BitMask) >> BitShift;

		BitMask >>= 1;
		BitShift--;

		if (BitMask == 0)
		{
			BitMask = 0x80;
			BitShift = 7;
			ArrayIndex++;
		}

		if ((Remainder & 0x100) == 0x100)
		{
			Remainder ^= 0xD5;
		}
	}

	NumberOfBits = 8;
	while (NumberOfBits != 0)
	{
		NumberOfBits--;

		Remainder <<= 1;

		if ((Remainder & 0x100) != 0)
		{
			Remainder ^= 0xD5;
		}
	}

	return Remainder & 0xFF;
}
```

2.14.4 AUX Support for Messaging AUX Client

Sideband MSG packets move from DP MST node to node, using Native AUX read and write transactions. In the following sub-sections, AUX is used to indicate AUX transactions.

2.14.4.1 Messaging AUX Client DPCD Locations

See Section 2.12 for the following DPCD locations associated with the Messaging AUX client.

2.14.4.1.1 MST_CAP Bit of the MSTM_CAP DPCD Location

The MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0) specifies whether the MST DPRX supports the Messaging framework. If the DPRX indicates that it supports the Messaging framework, the DPRX shall be ready to accept Message Transactions from an MST DPTX.

2.14.4.1.2 UP_REQ_EN Bit of the MSTM_CTRL DPCD Location

The UP_REQ_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 1) specifies whether the MST DPTX accepts and responds to UP Sideband MSGs. After the MST DPTX sets the UP_REQ_EN bit to 1, the DPTX shall be ready to accept and reply to Message Transactions from an MST DPRX.

2.14.4.1.3 DOWN_REP_MSG_RDY Bit of the DEVICE_SERVICE_IRQ_VECTOR DPCD Location

The MST DPRX sets the DOWN_REP_MSG_RDY bit in the DEVICE_SERVICE_IRQ_VECTOR and DEVICE_SERVICE_IRQ_VECTOR_ESI0 registers (DPCD Addresses 00201h and 02003h, respectively, bit 4) to 1 after a valid DOWN_REP Sideband MSG is written to the DOWN_REP DPCD locations. After the DOWN_REP_MSG_RDY bit is set, the MST DPRX issues an IRQ_HPD to the connected MST DPTX.

When the MST DPTX detects the IRQ_HPD, the MST DPTX reads the DEVICE_SERVICE_IRQ_VECTOR and DEVICE_SERVICE_IRQ_VECTOR_ESI0 registers checking whether the DOWN_REP_MSG_RDY bit is set to 1. If the DOWN_REP_MSG_RDY bit is set to 1, the DOWN_REP Sideband MSG is read from the MST DPRX DOWN_REP DPCD locations. The DPTX shall clear the DOWN_REP_MSG_RDY bit to 0 when reading of the message is complete.

The MST DPTX shall not be required to wait for the IRQ_HPD signal. The MST DPTX can poll the appropriate MST DPRX DPCD locations to determine whether any action is needed. The MST DPRX shall generate the IRQ_HPD signal regardless of whether the MST DPTX supports IRQ_HPD signal detection.

2.14.4.1.4 UP_REQ_MSG_RDY bit of the DEVICE_SERVICE_IRQ_VECTOR DPCD Location

The MST DPRX sets the UP_REQ_MSG_RDY bit in the DEVICE_SERVICE_IRQ_VECTOR and DEVICE_SERVICE_IRQ_VECTOR_ESI0 registers (DPCD Addresses 00201h and 02003h, respectively, bit 5) to 1 after a valid UP_REQ Sideband MSG is written to the MST UP_REQ DPCD locations. After the UP_REQ_MSG_RDY bit is set, the MST DPRX issues an IRQ_HPD to the connected MST DPTX.

When the MST DPTX detects the IRQ_HPD, the MST DPTX reads the DEVICE_SERVICE_IRQ_VECTOR and DEVICE_SERVICE_IRQ_VECTOR_ESI0 registers, checking whether the UP_REQ_MSG_RDY bit is set to 1. If the UP_REQ_MSG_RDY bit is set to 1, the UP_REQ Sideband MSG is read from the MST DPRX UP_REQ DPCD locations. The MST DPTX shall clear the UP_REQ_MSG_RDY bit to 0 when reading of the message is complete.

The MST DPTX shall not need to support IRQ_HPD signal detection. The MST DPTX can poll the appropriate MST DPRX DPCD locations to determine whether any action is needed. The MST DPRX shall generate the IRQ_HPD signal regardless of whether the MST DPTX supports IRQ_HPD signal detection.

2.14.4.1.5 DOWN_REQ Sideband MSG Buffer

The DOWN_REQ Sideband MSG buffer holds the request Sideband MSG written by an MST DPTX to be processed by the MST DPRX. The first byte of every DOWN_REQ Sideband MSG is written to the start address of the DOWN_REQ Sideband MSG buffer. A DP MST Sink device shall support the DOWN_REQ and DOWN_REP Sideband MSG buffers (DOWN_REQ and DOWN_REP registers (DPCD Addresses 01000h through 011FFh and 01400h through 015FFh, respectively)) if it expects to receive data on the Main-Link using MST packets. All DP MST Branch devices shall support the DOWN_REQ Sideband MSG buffer for each MST DPRX.

2.14.4.1.6 UP_REP Sideband MSG Buffer

The UP_REP Sideband MSG buffer holds the reply Sideband MSG written by an MST DPTX to be processed by the MST DPRX. The first byte of every UP_REP Sideband MSG is written to the start address of the UP_REP Sideband MSG buffer. A DP MST Sink device shall not be required to support the UP_REQ and UP_REP Sideband MSG buffers (UP_REQ and UP_REP registers (DPCD Addresses 01600h through 017FFh and 01200h through 013FFh, respectively) if the device does not originate Sideband MSG transactions. All DP MST Branch devices shall support the UP_REP Sideband MSG buffer for each MST DPRX.

2.14.4.1.7 DOWN_REP Sideband MSG Buffer

The DOWN_REP Sideband MSG buffer holds the reply Sideband MSG written by an MST DPRX to be processed by the MST DPTX. The first byte of the Sideband MSG containing the beginning of the Message Transaction is written to the start address of the DOWN_REP Sideband MSG DPCD locations. A DP MST Sink device shall support the DOWN_REP Sideband MSG buffer (DOWN_REP registers (DPCD Addresses 01400h through 015FFh) if it expects to receive data on the Main-Link using MST packets. All DP MST Branch devices shall support the DOWN_REP Sideband MSG buffer for each MST DPRX.

2.14.4.1.8 UP_REQ Sideband MSG Buffer

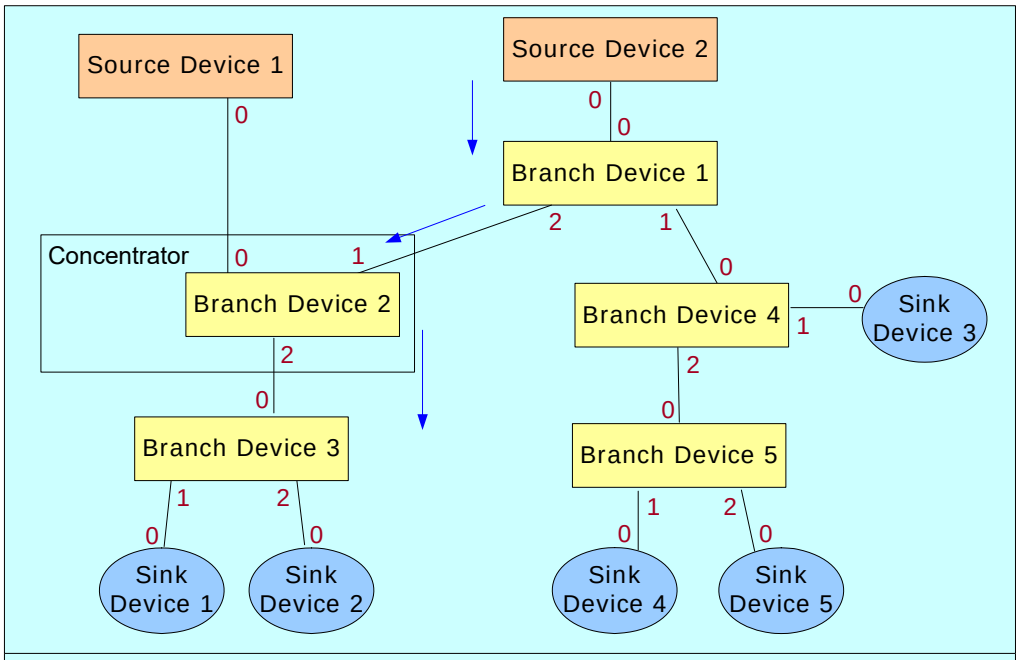
The Sideband UP_REQ Sideband MSG buffer holds the request Sideband MSG written by an MST DPRX to be processed by the MST DPTX. The first byte of the Sideband MSG containing the beginning of the Message Transaction is always written to the start address of the UP_REQ Sideband MSG DPCD locations. A DP MST Sink device shall support the UP_REQ Sideband MSG buffer and corresponding UP_REP Sideband MSG buffer (UP_REQ and UP_REP registers (DPCD Addresses 01600h through 017FFh and 01200h through 013FFh, respectively) if the DP Sink device supports UP_REQ Sideband MSG transactions. All DP MST Branch devices shall support the UP_REQ Sideband MSG buffer for each MST DPRX.

2.14.5 RAD Updated by MST Devices in the Path

The RAD is an array of nibbles of size Link_Count_Total – 1 contained in Sideband MSG Header as described in Section 2.14.3.1. Each nibble of the Relative_Address field specifies the port number of each DPTX or DPRX node to which the message is being transmitted. When the message arrives at a DP node, Relative_Address[0] is the DPTX or DPRX's port number within the node that shall transmit the message. Relative_Address[0] is the first port number transmitted as part of the RAD. Each node modifies the Relative_Address array as described with the following code sample:

```
for (i = 0; i < Link_Count_Remaining - 1; i++)
{
      Relative_Address[i] = Relative_Address[i + 1];
}
Relative_Address[i] = Input_Port_Number;
```

When the Sideband MSG arrives at the target DP node, the Relative_Address array contains the relative address of the Sideband MSG originator. Figure 2-140 illustrates an example of how the RAD is modified as a message traverses the path from originator to target.



Message from Source Device 2 to Branch Device 3 (LCT = 3)

Message arriving at	Relative Address	Link Count Remaining
Branch Device 1	2.2	2
Branch Device 2	2.0	1
Branch Device 3	1.0	0

Figure 2-140: Relative Address Update along the Path Using Example Topology

2.14.6 Broadcast Message Transactions

The Sideband MSG protocol supports the transmission of Broadcast Message transactions.

2.14.6.1 Broadcast Message Syntax

A Sideband MSG with a Broadcast_Message Sideband MSG Header bit set is referred to as a "broadcast message." Broadcast messages are delivered one link at a time until the message reaches an end DP MST device. A Broadcast Sideband MSG does not have a RAD; the LCT equals 1 and the LCR equals 6. Because the broadcast message is transmitted from one DP MST device to another, the LCR value is decremented by one. A broadcast message with an LCR of 0 is removed, and is therefore not transmitted to the adjacent DP device. This mechanism removes broadcast messages when the topology contains loops.

A broadcast message may either be downward-going (originated by an upstream DP MST device) or upward-going (originated by a downstream DP MST device). When the broadcast message is received from an upstream-facing port (UFP), it is to be transmitted from all DFPs. Conversely, if the broadcast message is received from a DFP, the message is transmitted from all UFPs.

A broadcast message can be a path or node request, depending on the Sideband MSG header's Path_Message bit value. If the broadcast message is a node request, only the end devices, DP MST Source or Sink devices (or DP MST Branch devices if Source/Sink devices are not plugged), process the request. If the broadcast message is a path request, all DP MST devices that receive the broadcast message shall process the request.

2.14.6.2 Broadcast Message Reply

Broadcast Message Transactions (consisting of one or multiple broadcast messages) shall be replied to by the adjacent DP MST device that is receiving the message. The Sideband MSG header's validity is verified along with the Sideband MSG body CRC's validity. If an error is found, a NAK message shall be transmitted to the transmitter of the message, indicating the error found. The adjacent DP MST device shall retry forwarding the broadcast message five times before replying with a NAK. The transmitter shall then resolve the error and re-transmit the message. If no error is found, an ACK reply shall be transmitted to the transmitter and no further action is needed from the transmitter.

2.14.7 Message Delivery

The procedures and mandates for delivering Sideband MSGs from one DP device to another are described in the following sections. The procedures and mandates are given based on whether the DP device is the message originating device, message target device, or message forwarding device.

2.14.7.1 Message Originating Device

2.14.7.1.1 Down Request Message

The originator first ensures it has not transmitted a Message Transaction to the same DP device with the next Message Sequence Number (MSN). If a reply has not been received from the two previous Message Transaction requests, the originator shall wait for a reply or timeout from one of the two outstanding requests. Use the freed MSN for the Message Transaction to be transmitted. If it is necessary for message transactions to execute in a defined order, the originator shall ensure message transaction execution by waiting for a reply before transmitting subsequent messages.

The Message Transaction request is split into the needed number of Sideband MSGs. The SMT bit is set in the Sideband MSG header of the first Sideband MSG of the Message Transaction request. The EMT bit is set in the Sideband MSG header of the last Sideband MSG. If the Message Transaction request can be delivered with one Sideband MSG, the SMT and EMT bits are set in the Sideband MSG header.

The originating device shall attempt to write the first Sideband MSG into the DPCD DOWN_REQ Sideband MSG buffer using Native AUX requests. If the receiving device replies with an AUX_DEFER, retry transmitting the Sideband MSG an implementation-specific number of times. If the receiving device replies with an AUX_ACK, continue writing the remaining Message Transaction Sideband MSGs. Wait 4 seconds for a reply from the target after successfully writing the last Message Transaction Sideband MSG.

2.14.7.1.2 Up Request Message

If a reply has not been received from the two previous message transaction requests, wait for a reply or timeout from one of the two outstanding requests. Use the freed MSN for the message transaction to be transmitted. The originator shall ensure that messages are executed in a given order by waiting for a reply before transmitting subsequent messages.

The Message Transaction request is split into the needed number of Sideband MSGs. The SMT bit is set in the Sideband MSG header of the first Sideband MSG of the Message Transaction request, and the EMT bit is set in the Sideband MSG header of the last Sideband MSG. If the Message Transaction request can be delivered with one Sideband MSG, the SMT and EMT bits are set in the Sideband MSG header.

The originating device shall write the first Sideband MSG into the DPCD UP_REQ Sideband MSG buffer, write 1 to the UP_REQ_MSG_RDY bit in the DEVICE_SERVICE_IRQ_VECTOR and DEVICE_SERVICE_IRQ_VECTOR_ESI0 registers (DPCD Addresses 00201h and 02003h, respectively, bit 5) and then generate an IRQ_HPD to the upstream DP device. After 110ms, or after the upstream DP device writes 0 to the UP_REQ_MSG_RDY bit, ensure that the UP_REQ_MSG_RDY bit is cleared before removing the Sideband MSG from the DPCD UP_REQ Sideband MSG buffer. The originating DP device waits 4 seconds for a reply after the upstream DP device reads the last Message Transaction Sideband MSG.

2.14.7.2 Message Forwarding Device (Forward and Execute if Path Message)

2.14.7.2.1 Down Request Message Transaction

If there are at least 48 bytes available for reception of a Sideband MSG, reply with an AUX_ACK to the Native AUX request to write a Sideband MSG into the DPCD DOWN_REQ Sideband MSG buffer. If there is not 48 bytes free when the first Sideband MSG Native AUX write request is performed, reply with an AUX_DEFER until 48 bytes are available.

After the last Sideband MSG Native AUX write, check the validity of the Sideband MSG header by validating the Sideband MSG Header CRC. Check the LCR and Path bit to determine whether the Sideband MSG is to be forwarded or is part of a Message Transaction request to be executed locally. If the Sideband MSG is to be forwarded, attempt to write the Sideband MSG to the DPCD DOWN_REQ Sideband MSG buffer of the downstream DP device using Native AUX requests. After attempting to forward for 20ms, reply to the Message Transaction originator with a Message Transaction NAK reply.

If the Sideband MSG is part of a Path Message Transaction, combine this Sideband MSG with any other Sideband MSGs for the same Message Transaction until the EMT Sideband MSG Header bit is set. After receiving the last Message Transaction Sideband MSG, execute the Message Transaction within 50ms. After executing the Message Transaction, attempt to write the Sideband MSG to the DPCD DOWN_REQ Sideband MSG buffer of the downstream DP device using Native AUX requests. After attempting to forward for 20ms, reply to the Message Transaction originator with a Message Transaction NAK reply.

See Section 2.14.7.3.1 for handling of Node Message Transactions targeted for this DP device.

2.14.7.2.2 Down Reply Message Transaction

Upon detecting an IRQ_HPD, transmit Native AUX requests to read the DOWN_REP_MSG_RDY bit in the DEVICE_SERVICE_IRQ_VECTOR and DEVICE_SERVICE_IRQ_VECTOR_ESI0 registers (DPCD Addresses 00201h and 02003h, respectively, bit 4) to determine if a Down Reply Message Transaction shall be read. If a down reply is available, read the reply from the DPCD DOWN_REP Sideband MSG buffer, and then clear the DOWN_REP_MSG_RDY bit within 100ms of receiving the IRQ_HPD. The downstream DP device shall clear the DOWN_REP_MSG_RDY bit and Sideband MSG from the DPCD DOWN_REP Sideband MSG buffer 110ms after the IRQ_HPD pulse ends.

After the last Sideband MSG Native AUX read, check the validity of the Sideband MSG header by validating the Sideband MSG Header CRC. Check the LCR and Path bit to determine whether the Sideband MSG is to be forwarded or is part of a Message Transaction request to be executed locally. If the Sideband MSG is to be forwarded, write the Sideband MSG to the DPCD DOWN_REP Sideband MSG buffer, write 1 to the DOWN_REP_MSG_RDY bit, and then generate an IRQ_HPD within 5ms of last Sideband MSG Native AUX read request. After 110ms or after the upstream DP device writes 0 to the DOWN_REP_MSG_RDY bit, ensure that the DOWN_REP_MSG_RDY bit is cleared before removing the Sideband MSG from the DPCD DOWN_REP Sideband MSG buffer.

If the Sideband MSG is part of a Path Message Transaction, combine this Sideband MSG with any other Sideband MSGs for the same message transaction until the EMT Sideband MSG Header bit is set. After receiving the last Message Transaction Sideband MSG, execute the Message Transaction within 50ms. After execution is complete, write the Message Transaction Sideband MSG to the DOWN_REP Sideband MSG buffer, write 1 to the DOWN_REP_MSG_RDY bit, and then generate an IRQ_HPD within 5ms of last Sideband MSG Native AUX read request. After 110ms or after the upstream DP device writes 0 to the DOWN_REP_MSG_RDY bit, ensure that the DOWN_REP_MSG_RDY bit is cleared before removing the Sideband MSG from the DPCD DOWN_REP Sideband MSG buffer.

2.14.7.2.3 Up Request Message Transaction

Upon detecting an IRQ_HPD, transmit Native AUX requests to read the UP_REQ_MSG_RDY bit in the DEVICE_SERVICE_IRQ_VECTOR and DEVICE_SERVICE_IRQ_VECTOR_ESI0 registers (DPCD Addresses 00201h and 02003h, respectively, bit 5) to determine whether an Up Request Message Transaction shall be read. If an up request is available, read the request Sideband MSG from the DPCD UP_REQ Sideband MSG buffer, and then clear the UP_REQ_MSG_RDY bit within 100ms of receiving the IRQ_HPD. The downstream DP device shall clear the UP_REQ_MSG_RDY bit and Sideband MSG from the DPCD UP_REQ Sideband MSG buffer 110ms after the IRQ_HPD pulse ends.

After the last Sideband MSG Native AUX is read, check the validity of the Sideband MSG header by validating the Sideband MSG Header CRC. Check the LCR and Path bit to determine whether the Sideband MSG is to be forwarded or is part of a Message Transaction request to be executed locally. If the Sideband MSG is to be forwarded, write the Sideband MSG to the DPCD UP_REQ Sideband MSG buffer, write 1 to the UP_REQ_MSG_RDY bit, and then generate an IRQ_HPD within 5ms of last Sideband MSG Native AUX read request. After 110ms or after the upstream DP device writes 0 to the UP_REQ_MSG_RDY bit, ensure that the UP_REQ_MSG_RDY bit is cleared before removing the Sideband MSG from the DPCD UP_REQ Sideband MSG buffer.

If the Sideband MSG is part of a Path Message transaction, combine this Sideband MSG with any other Sideband MSGs for the same message transaction until the EMT Sideband MSG Header bit is set. After receiving the last Message Transaction Sideband MSG, execute the Message transaction within 50ms. Once execution is complete, write the Message Transaction Sideband MSG to the UP_REQ Sideband MSG buffer, write 1 to the UP_REQ_MSG_RDY bit, and then generate an IRQ_HPD within 5ms of last Sideband MSG Native AUX read request. After 110ms or after the upstream DP device writes 0 to the UP_REQ_MSG_RDY bit, ensure that the UP_REQ_MSG_RDY bit is cleared before removing the Sideband MSG from the DPCD UP_REQ Sideband MSG buffer. If the Up Request Message Transaction Sideband MSG was not read within 110ms by the upstream DP device, transmit a Message Transaction NAK to the originating device.

See Section 2.14.7.3.2 for handling of Up Node Message transactions that are targeted for this DP device.

2.14.7.2.4 Up Reply Message Transaction

If there are at least 48 bytes available for reception of a Sideband MSG, reply with an AUX_ACK to the Native AUX request to write a Sideband MSG into the DPCD UP_REP Sideband MSG buffer. If there are not 48 bytes free when the first Sideband MSG Native AUX write request is performed, reply with an AUX_DEFER until 48 bytes are available.

After the last Sideband MSG Native AUX write, check the validity of the Sideband MSG header by validating the Sideband MSG Header CRC. Check the LCR and Path bit to determine whether the Sideband MSG is to be forwarded or is part of a Message Transaction request to be executed locally. If the Sideband MSG is to be forwarded, attempt to write the Sideband MSG to the DPCD UP_REP Sideband MSG buffer of the downstream DP device using Native AUX requests. Timeout after attempting to forward for 20ms, and then discard the Sideband MSG.

If the Sideband MSG is part of a Path Message Transaction, combine this Sideband MSG with any other Sideband MSGs for the same message transaction until the EMT Sideband MSG Header bit is set. After receiving the last Message Transaction Sideband MSG, execute the Message Transaction within 50ms. After executing the Message Transaction, attempt to write the Sideband MSG reply to the DPCD UP_REP Sideband MSG buffer of the downstream DP device using Native AUX requests. Timeout after attempting to write the Message Transaction Sideband MSG reply for 20ms, and then discard the Message Transaction Sideband MSGs.

2.14.7.3 Message Targeted Device

2.14.7.3.1 Down Request Message

If there are at least 48 bytes available for reception of a Sideband MSG, reply with an AUX_ACK to the Native AUX request to write a Sideband MSG into the DPCD DOWN_REQ Sideband MSG buffer. If there are not 48 bytes free when the first Sideband MSG Native AUX write request is performed, reply with an AUX_DEFER until 48 bytes are available.

After last Sideband MSG Native AUX read, check the validity of the Sideband MSG header by validating the Sideband MSG Header CRC. Check the LCR and Path bit to determine whether the Sideband MSG is to be forwarded or is part of a Message Transaction request to be executed locally. If the Sideband MSG is part of a Node Message Transaction to be executed locally, combine this Sideband MSG with any other Sideband MSGs for the same message transaction until the EMT Sideband MSG Header bit is set. After receiving the last Message Transaction Sideband MSG, execute the message transaction within 50ms. After execution is complete, write the Message Transaction reply Sideband MSG to the DOWN_REP Sideband MSG buffer, write 1 to the DOWN_REP_MSG_RDY bit in the DEVICE_SERVICE_IRQ_VECTOR and DEVICE_SERVICE_IRQ_VECTOR_ESI0 registers (DPCD Addresses 00201h and 02003h, respectively, bit 4), and then generate an IRQ_HPD within 5ms of the last Sideband MSG Native AUX read request. After 110ms, or after the upstream DP device writes 0 to the DOWN_REP_MSG_RDY bit, ensure that the DOWN_REP_MSG_RDY bit is cleared before removing the Sideband MSG from the DPCD DOWN_REP Sideband MSG buffer. If the Down Reply Message Transaction Sideband MSG is not read within 110ms by the upstream DP device, transmit a Message Transaction NAK to the originating device.

If the Message Transaction reply needs to be transmitted using multiple Sideband MSGs, transmit the Sideband MSGs as soon as there is sufficient data to fill each Sideband MSG. Especially in the case of an I^2C read, transmit the Sideband MSGs as soon as there is sufficient data to fill a Sideband MSG without waiting for the entire I^2C data to be read.

2.14.7.3.2 Up Request Message

Upon detecting an IRQ_HPD, transmit Native AUX requests to read the UP_REQ_MSG_RDY bit in the DEVICE_SERVICE_IRQ_VECTOR and DEVICE_SERVICE_IRQ_VECTOR_ESI0 registers (DPCD Addresses 00201h and 02003h, respectively, bit 5) to determine whether an Up Request Message Transaction shall be read. If an Up request is available, read the request Sideband MSG from the DPCD UP_REQ Sideband MSG buffer, and then clear the UP_REQ_MSG_RDY bit within 100ms of receiving the IRQ_HPD. The downstream DP device shall clear the UP_REQ_MSG_RDY bit and Sideband MSG from the DPCD UP_REQ Sideband MSG buffer 110ms after the IRQ_HPD pulse ends.

After the last Sideband MSG Native AUX read, check the validity of the Sideband MSG header by validating the Sideband MSG Header CRC. Check the LCR and Path bit to determine whether the Sideband MSG is to be forwarded or is part of a Message Transaction request to be executed locally. If the Sideband MSG is part of a Node Message Transaction request to be executed locally, combine this Sideband MSG with any other Sideband MSGs for the same Message Transaction until the EMT Sideband MSG Header bit is set. After receiving the last Message Transaction Sideband MSG, execute the Message Transaction within 50ms. After executing the Message Transaction, attempt to write the Sideband MSG reply to the DPCD UP_REP Sideband MSG buffer of the downstream DP device using Native AUX requests. Timeout after attempting to write the Message Transaction Sideband MSG reply for 20ms, and then discard the Message Transaction Sideband MSGs.

If the Message Transaction reply has to be transmitted using multiple Sideband MSGs, transmit the Sideband MSGs as soon as there is sufficient data to fill each Sideband MSG. Especially in the case of an I^2C read, transmit the Sideband MSGs as soon as there is sufficient data to fill a Sideband MSG without waiting for the entire I^2C data to be read.

2.14.8 Error Handling

This section describes error handling of the Messaging AUX Client layers.

2.14.8.1 Message Transaction Layer Error Handling

Other than errors in the Sideband MSG header, errors shall be detected and handled at the Message Transaction Layer. These errors include invalid request syntax, unable to respond to the request within the specified timeout period, and request execution errors. The DP node that detects one or more of the above errors shall reply to the originator with a NAK. The NAK shall indicate the type of error detected. The Message Transaction originator shall perform the AUX Reply Timeout timer check. If an error to a request causes the system to be in an invalid state (e.g., all nodes failed to delete a virtual channel), the Message Transaction originator shall return the system to a valid state. The Message Transaction originator shall also perform retries, as needed.

2.14.8.2 Sideband MSG Layer Error Handling

Sideband MSG Layer shall validate the CRC of the Sideband MSG header. If the Sideband MSG Layer detects a CRC error, it shall abort handling of the Sideband MSG containing the header CRC error. This action causes the Sideband MSG originator to timeout. Upon timeout, the originator Sideband MSG Layer shall inform the Message Transaction Layer of the timeout event. No retries are performed at the Sideband MSG Layer.

2.14.8.3 AUX Layer Error Handling for Sideband MSG

No changes are made to the AUX transactions to support Sideband Messaging.

2.14.8.3.1 AUX Error Handling for Down Message Transactions

A DPTX's AUX Layer uses Native AUX write transactions to write the Sideband MSG into the appropriate DPRX Down Sideband MSG buffer.

When the Native AUX write is unsuccessful within the number of retries allowed, the Sideband MSG Layer shall notify the Message Transaction Layer of the failure. This would be the case when the message buffer is full. The Message Transaction Layer, in turn, should transmit a Message Transaction NAK to the message originator (e.g., Stream Policy Maker) indicating that a WRITE_FAILURE occurred.

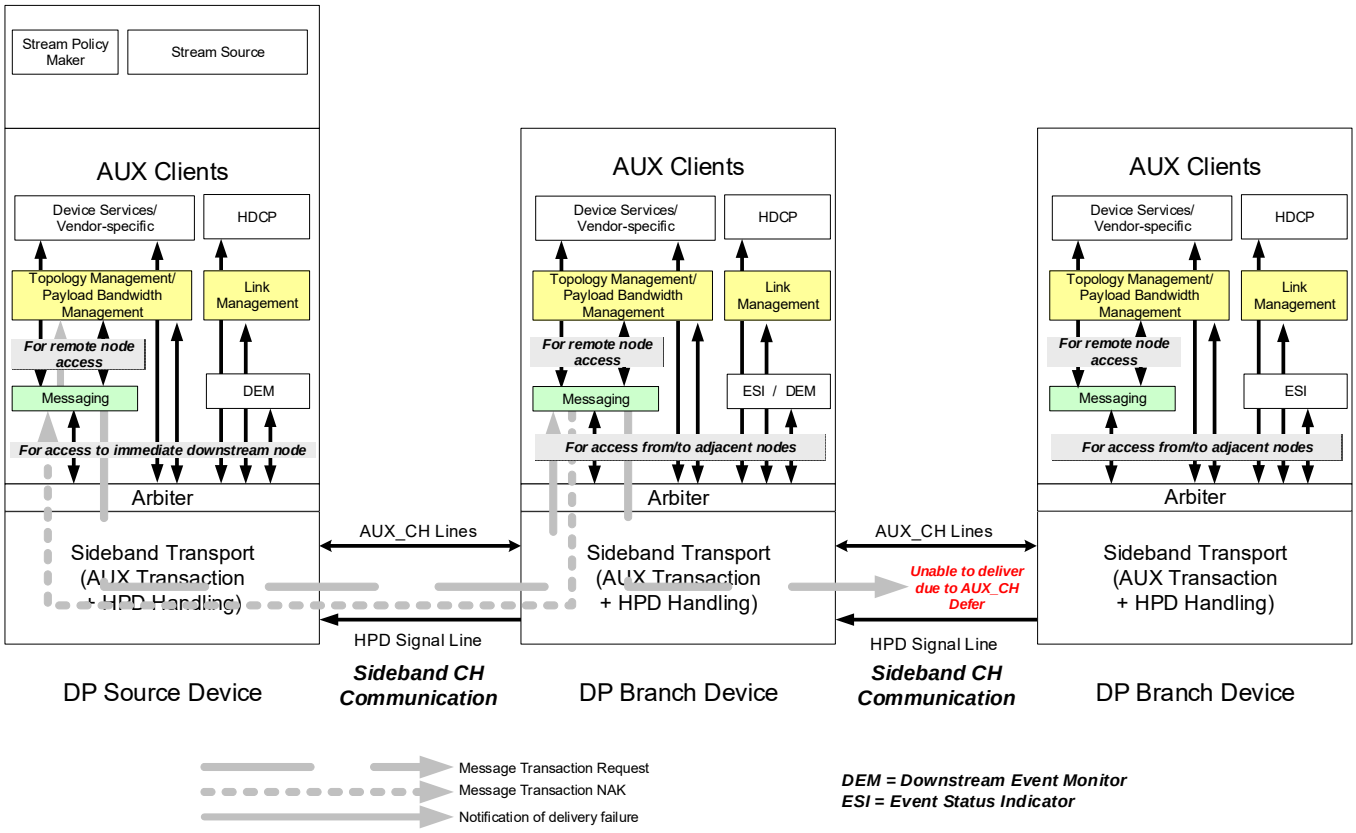


Figure 2-141: AUX Error while Delivering a DOWN_REQ_MSG

2.14.8.3.2 AUX Error Handling for Up Message Transactions

The DPRX's AUX Layer generates an IRQ_HPD to prompt its immediate upstream DP node to initiate Native AUX read transactions and instruct the DPTX to read the Sideband MSG from the appropriate DPRX Up Sideband MSG buffer.

When the DPTX has insufficient room in its internal buffers to read the Sideband MSG, the DPTX shall inform its Message Transaction Layer of the failure. The Message Transaction Layer shall then transmit a Message Transaction NAK Reply to the message originator indicating that a WRITE_FAILURE occurred.

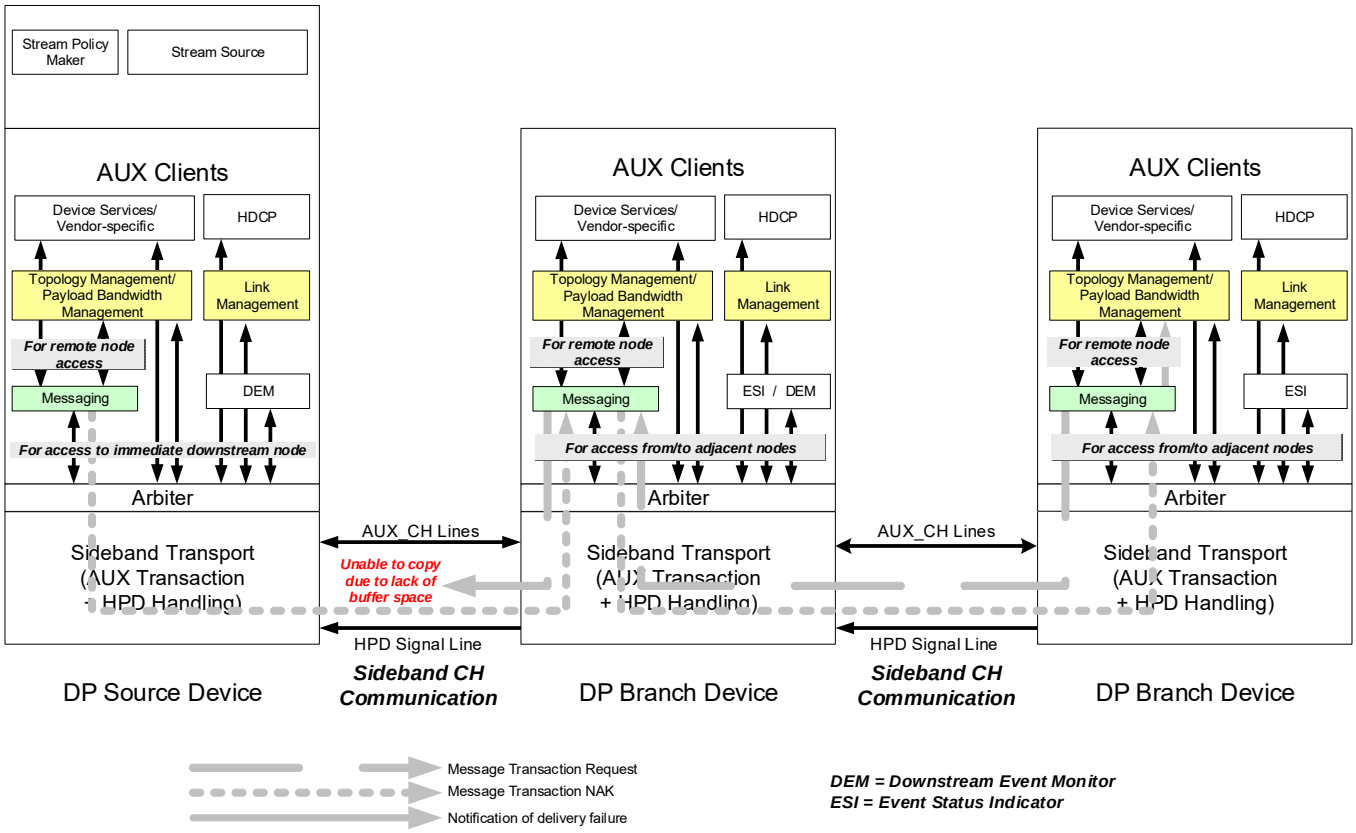


Figure 2-142: AUX Error while Delivering an UP_REQ_MSG

2.14.9 Descriptions of Available Message Transaction Requests

This section describes the available Message Transactions Requests.

2.14.9.1 ALLOCATE_PAYLOAD

The ALLOCATE_PAYLOAD is a path or node request Message Transaction allowing the change of payload allocation for a virtual channel between a DP Source and Sink device. The ALLOCATE_PAYLOAD request is used to allocate a payload for a new virtual channel, change the payload allocation of an existing virtual channel or the deletion the payload allocation of an existing virtual channel.

Table 2-215: ALLOCATE_PAYLOAD Message Syntax

Syntax	# of Bits	Format
ALLOCATE_PAYLOAD_Request()		
{		
zero	1	‘0’
Request_Identifier	7	‘001 0001’
Port_Number	4	
Number_SDP_Streams	4	
zero	1	‘0’
Virtual_Channel_Payload_Identifier	7	
Payload_Bandwidth_Number	16	
for (i = 0; i < Number_SDP_Streams; i++)		
{		
SDP_Stream_Sink[i]	4	
}		
while (!bytealigned())		
{		
zero	1	‘0’
}		
}		
ALLOCATE_PAYLOAD_Ack_Reply()		
{		
Reply_Type	1	‘0’
Request_Identifier	7	‘001 0001’
Port_Number	4	
zeros	5	‘0 0000’
Virtual_Channel_Payload_Identifier	7	
Allocated_Payload_Bandwidth_Number	16	
}		

Link training shall be performed on each DP node from the DP Source device to the immediate upstream node from the DP Sink device if the link needs to be established. After the DP node determines the downstream link can support the requested PBN, Native AUX transactions are used to establish the downstream virtual channel. Each DP node forwards the ALLOCATE_PAYLOAD message to the next downstream device along the path specified by the RAD after the local virtual channel setup is complete. If the DP node changes the virtual channel payload identifier within the DP device, the new virtual channel payload identifier replaces the virtual channel payload identifier in the received ALLOCATE_PAYLOAD request. See Section 2.6.6 for ALLOCATE_PAYLOAD message transaction use.

The path de-allocate payload reply version of the ALLOCATE_PAYLOAD message transaction shall be converted to a node Sideband MSG when the message is received by a DP MST Branch device with the VC Payload allocated to two or more DPTX ports. When the de-allocate payload reply is a node reply, DP MST devices receiving the reply shall convert the VC Payload ID in the message and pass it along to the upstream DP MST device without de-allocating the VC Payload.

2.14.9.1.1 Port_Number

A DP device's target end port number that is to be the virtual channel's endpoint. This field has the same value in the reply as in the request.

2.14.9.1.2 Virtual_Channel_Payload_Identifier

The virtual channel payload identifier of the virtual channel to be added, updated, or deleted. This field has the same value in the reply as in the request.

2.14.9.1.3 Payload_Bandwidth_Number

The Payload Bandwidth Number needed for the virtual channel assigned to the above virtual channel identifier.

2.14.9.1.4 Allocated_Payload_Bandwidth_Number

The Payload Bandwidth Number (PBN) of the time slots actually allocated to the stream. The allocated PBN is the maximum allocated by any DP MST Branching unit. Because the ALLOCATE_PAYLOAD Message Transaction reply is forwarded upstream, each DP MST Branching unit replaces the Allocated_Payload_Bandwidth_Number with its allocated PBN if its allocated PBN is greater than the PBN in the reply.

2.14.9.1.5 Number_SDP_Streams

The Number_SDP_Streams field indicates the number of SDP streams that need to be routed to SDP stream sinks (the size of the SDP stream sink table that follows).

2.14.9.1.6 SDP_Stream_Sink

The SDP Stream Sink table contains mapping of the SDP stream to available SDP stream sinks. The first field of the table is associated with the first SDP stream, the second field is associated with the second SDP stream, etc. Each field's value is the SDP stream sink identifier to which the associated SDP stream is being transmitted. When the SDP_Stream_Sink value is cleared to 0, the SDP stream to which the destination SDP Sink device is transmitted is implementation-specific. It is the decision of the DP Sink device implementer as to how to handle two SDP streams assigned to the same SDP stream sink.

2.14.9.2 CLEAR_PAYLOAD_ID_TABLE

The CLEAR_PAYLOAD_ID_TABLE path broadcast request message transaction is transmitted by a DP MST device to de-allocate all VC Payload ID tables allocated to the port from which the message is received. This broadcast message is not transmitted to all DFPs. The broadcast message is transmitted to those DPTX ports with VC Payloads allocated from the DPRX port being cleared. When the CLEAR_PAYLOAD_ID_TABLE request is received by a concentrator device, the DP MST Concentrator Branch device transmits a NAK reply with the reason set to defer.

The DP MST Concentrator Branch device, ACKs CLEAR_PAYLOAD_ID_TABLE broadcast request message transactions, and converts the CLEAR_PAYLOAD_ID_TABLE request into a series of ALLOCATE_PAYLOAD requests for the VC Payload ID allocated to the DPRX port with the new PBN value cleared to 0 (de-allocate payload) to its downstream DPTX ports.

Table 2-216: CLEAR_PAYLOAD_ID_TABLE Message Syntax

Syntax	# of Bits	Format
CLEAR_PAYLOAD_ID_TABLE_Request()		
{		
zero	1	‘0’
Request_Identifier	7	‘001 0100’
}		
CLEAR_PAYLOAD_ID_TABLE_Ack_Reply()		
{		
Reply_Type	1	‘0’
Request_Identifier	7	‘001 0100’
}		

2.14.9.3 CONNECTION_STATUS_NOTIFY

The CONNECTION_STATUS_NOTIFY node broadcast request message transaction is transmitted by a DP Branch device when it detects a DP or legacy device plug or unplug event. The MST device whose DPTX detected the connection status change shall broadcast the message upstream, while the MST device whose DPRX detected the connection status change shall broadcast the message downstream. All payloads allocated to the disconnected DP ports shall be de-allocated as the broadcast message traverses both upstream and downstream.

The MST device with a branching unit whose DPRX detects the disconnect event shall clear the VC Payload ID table of the disconnected DPRX port while maintaining the VC Payload ID tables of other DPRX/DPTX ports. The MST device then initiates the ALLOCATE_PAYLOAD procedure to its downstream DP nodes to delete the VC Payloads allocated on the disconnected port. (See Section 2.6.)

The MST device with a branching unit whose DPTX detects the disconnect shall clear the DPTX's VC Payload ID table while maintaining the other DPTX/DPRX ports' VC Payload ID tables.

Table 2-217: CONNECTION_STATUS_NOTIFY Message Syntax

Syntax	# of Bits	Format
CONNECTION_STATUS_NOTIFY_Request()		
{		
zero	1	'0'
Request_Identifier	7	'000 0010'
Port_Number	4	
zeros	4	'0000'
Global_Unique_Identifier	128	
zero	1	'0'
Legacy_Device_Plug_Status	1	
DisplayPort_Device_Plug_Status	1	
Messaging_Capability_Status	1	
Input_Port	1	
Peer_Device_Type	3	
}		
CONNECTION_STATUS_NOTIFY_Ack_Reply()		
{		
Reply_Type	1	'0'
Request_Identifier	7	'000 0010'
}		

2.14.9.3.1 Global_Unique_Identifier

The Global Unique Identifier (GUID), of DP device transmitting the CONNECTION_STATUS_NOTIFY Message Transaction.

2.14.9.3.2 Port_Number

The port number on which the connection event was detected.

2.14.9.3.3 Legacy_Device_Plug_Status

This bit is valid if the Peer_Device_Type is set to SST-to-Legacy protocol converter and the DisplayPort_Device_Plug_Status bit is set to 1. This bit indicates the connection status of the legacy device (VGA, DVI, or HDMI device). When the Legacy_Device_Plug_Status bit is set to 1, the legacy device is connected. The Legacy_Device_Plug_Status bit is cleared to 0 when the legacy device is disconnected. This field is valid if the DisplayPort_Device_Plug_Status bit is set to 1.

2.14.9.3.4 DisplayPort_Device_Plug_Status

When set to 1, the DPTX or DPRX is connected to an appropriate micro-packet device and the DPTX or DPRX is initialized.

2.14.9.3.5 Messaging_Capability_Status

When set to 1, the MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0) is enabled for a DPRX, and the UP_REQ_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 1) is enabled by a DPTX. The bit is cleared to 0 if the DPCD MST_CAP or UP_REQ_EN bit is disabled. This field is valid when the DisplayPort_Device_Plug_Status bit is set to 1.

2.14.9.3.6 Input_Port

When set to 1, the port information is for a DPRX; otherwise, the port information is for a DPTX.

2.14.9.3.7 Peer_Device_Type

Peer_Device_Type gives the DP device type connected to the indicated port. Table 2-218 defines the available device types. The Peer_Device_Type number of 010b shall be returned for an SST Branch device connected to a DFP, and for a DP device with MST Branching unit regardless of whether the Branching unit is a part of an MST Branch, Composite Sink, or Sink device.

Table 2-218: Peer_Device_Type

Peer_Device_Type	DP Peer Device Description
000b	No device connected
001b	Source device or SST Branch device connected to a UFP
010b	Device with MST Branching Unit or SST Branch device connected to a DFP
011b	SST Sink device or Stream Sink in an MST Sink/Composite device
100b	DP-to-Legacy protocol converter (DP to VGA, DVI, or HDMI)
101b	DP-to-Wireless protocol converter (DP to WDE or other wireless interfaces)
110b	Wireless-to-DP protocol converter (WDE or other wireless interface to DP)
111b	RESERVED

Table 2-219 provides information on how to determine the Peer_Device_Type and Messaging_Capability_Status fields from the cable plug status and DPCD status.

Table 2-219: Peer_Device_Type Determination[a]

Peer Device Connected to	Peer Device Description	Message Capability/Type		Signal Used for Presence Detection	DPCD Bits Used for Peer_Device_Type Determination			
		Message_ Capability_ Status	Peer_ Device_ Type		DFP_PRESENT[b]	DFP_TYPE[c]	MST_CAP/ UP_REQ_EN[d]	UPSTREAM _IS_SRC[e]
N/A	None	0	000b	No	X	X	X	X
UFP	MST Source Device	1	001b	Powered Source Detect	0	X	UP_REQ_EN = 1	1
UFP	SST-only Source Branch Device	0	001b	Powered Source Detect	0	X	UP_REQ_EN = 0	0
	MST Branch Device	1	010b	Powered Source Detect	0	X	UP_REQ_EN = 1	0
DFP	SST-only Branch Device (DP out)	0	010b	HPD	1	00b	MST_CAP = 0	X
	Device with MST Branching Unit	1	010b	HPD	1	00b	MST_CAP = 1	X
	DP-to-Legacy Protocol Converter	0	100b	HPD	1	01b = VGA 10b = DVI/ HDMI	0	X
	Stream Sink (without Branching Unit)	0	011b	HPD	0	X	0	X
	DP-to-Wireless Protocol Converter	1	101b	HPD	1	11b	1	X
	Wireless-to-DP Protocol Converter	1	110b	Completion of wireless pairing (beyond the scope of this Standard)	1	11b	1	X

a. "X" indicates "don't care."
b. DFP_PRESENT bit in the DOWN_STREAM_PORT_PRESENT register(s) (DPCD Addresses 00005h and 02205h, bit 0).
c. DFP_TYPE field in the DOWN_STREAM_PORT_PRESENT register(s) (DPCD Addresses 00005h and 02205h, bits 2:1).
d. MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0) and UP_REQ_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 1).
e. UPSTREAM_IS_SRC bit in the MSTM_CTRL register (DPCD Address 00111h, bit 2).

2.14.9.4 ENUM_PATH_RESOURCES

ENUM_PATH_RESOURCES is a path request message transaction that is used to determine the minimum available PBN of a path from the DP Source to Sink device.

Table 2-220: ENUM_PATH_RESOURCES Message Syntax

Syntax	# of Bits	Format
ENUM_PATH_RESOURCES_Request()		
{		
zero	1	‘0’
Request_Identifier	7	‘001 0000’
Port_Number	4	
zeros	4	‘0000’
}		
ENUM_PATH_RESOURCES_Ack_Reply()		
{		
Reply_Type	1	‘0’
Request_Identifier	7	‘001 0000’
Port_Number	4	
zeros	3	‘000’
FEC_Capability	1	
Full_Payload_Bandwidth_Number	16	
Available_Payload_Bandwidth_Number	16	
}		

This message is targeted at the downstream DP Branch device of the path to be enumerated. The targeted DP device responds with its downstream available PBN. Each DP node along the path of the reply message replaces the available PBN in the reply message with its available downstream PBN if its available downstream PBN is less than that in the reply message.

2.14.9.4.1 FEC_Capability

New to *DP v1.4*.

Set to 1 if the path from the MST BU that is generating the reply message to the downstream end of the path to be enumerated supports Forward Error Correction (FEC) capability.

2.14.9.4.2 Full_Payload_Bandwidth_Number

The bandwidth of the link at the trained link rate and lane count between the DP Source device and the DP Sink device with no time slots allocated to VC Payloads, represented as a Payload Bandwidth Number. As with the Available_Payload_Bandwidth_Number, this number is determined by the link with the lowest lane count and link rate.

2.14.9.4.3 Available_Payload_Bandwidth_Number

The minimum payload bandwidth number supported by the path. Each node updates this number with its available payload bandwidth number if its payload bandwidth number is less than that in the Message Transaction reply.

2.14.9.4.4 Port_Number

A DP MST device’s target port number that is to be enumerated.

2.14.9.5 LINK_ADDRESS

The LINK_ADDRESS node message transaction is targeted at MST devices that have a branching unit. This transaction is used to determine the resources available of a particular MST device with a branching unit, and the type of devices connected to the branching unit (Peer_Device_Type). The resources reported by an MST device with a branching unit are as follows:

- Number of input and output ports (both physical and logical)
- Whether a peer device is connected to the input or output port
- Whether the peer device is a Branch/Sink/Source (Peer_Device_Type) device
- If the device is a Sink device, how many SDP stream sinks are available
- Whether the peer device supports topology enhancement

Table 2-134 defines the Current_Capabilities_Structure field. This field is available only when the Transaction Message version number is 02h or higher.

Table 2-221: LINK_ADDRESS Message Syntax

Syntax	# of Bits	Format
LINK_ADDRESS_Request()		
{		
zero	1	‘0’
Request_Identifier	7	‘000 0001’
}		
LINK_ADDRESS_Ack_Reply()		
{		
Reply_Type	1	‘0’
Request_Identifier	7	‘000 0001’
Global_Unique_Identifier	128	
zeros	4	‘0000’
Number_Of_Ports	4	
for (i = 0; i < Number_Of_Ports; i++)		
{		
Input_Port[i]	1	
Peer_Device_Type[i]	3	
Port_Number[i]	4	
Messaging_Capability_Status[i]	1	
DisplayPort_Device_Plug_Status[i]	1	
if (Peer_Device_Type[i] == 101b)		
{		
Current_Capabilities_Structure	128	
}		
if (Input_Port[i] == 0)		
{		
Legacy_Device_Plug_Status[i]	1	
zeros	5	‘0 0000’
DPCD_Revision	8	
Peer_Global_Unique_Identifier	128	
Number_SDP_Streams[i]	4	
Number_SDP_Stream_Sinks[i]	4	
}		
else		
{		
zeros	6	‘00 0000’
}		
}		
}		

2.14.9.5.1 Global_Unique_Identifier

The GUID of the targeted DP device.

2.14.9.5.2 Number_Of_Ports

The number of DPTXs/DPRXs that the DP node contains.

2.14.9.5.3 Current_Capabilities_Structure

The CCS of the targeted DP device.

2.14.9.5.4 Input_Port

When set to 1, the port information is for a DPRX. Otherwise, the port information is for a DPTX.

2.14.9.5.5 Peer_Device_Type

Peer_Device_Type gives the DP device type (see Table 2-218) that is connected to the indicated port. The DP Peer Branch device type shall be returned for all branch types, physical, logical, or combined. This field is valid if the DisplayPort_Device_Plug_Status bit is set to 1.

2.14.9.5.6 Port_Number

The port number of the port being reported. Physical port numbers shall be from 0 to 7. Logical port numbers shall be from 8 to 15 (0x0F).

2.14.9.5.7 Messaging_Capability_Status

When set to 1, the MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0) is enabled by a DPRX, and the UP_REQ_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 1) is enabled by a DPTX. The bit shall be cleared to 0 if the MST_CAP or UP_REQ_EN bit is disabled. This field is valid when the DisplayPort_Device_Plug_Status bit is set to 1.

2.14.9.5.8 DisplayPort_Device_Plug_Status

When set to 1, the DPTX or DPRX is connected appropriately and the DPTX or DPRX is initialized.

2.14.9.5.9 Legacy_Device_Plug_Status

This bit is valid if the Peer_Device_Type is set to SST-to-Legacy protocol converter. This bit indicates the connection status of the legacy device (VGA, DVI, or HDMI device).
When the Legacy_Device_Plug_Status bit is set to 1, the legacy device is connected.
The Legacy_Device_Plug_Status bit is cleared to 0 when the legacy device is disconnected.
This field is valid if the DisplayPort_Device_Plug_Status bit is set to 1.

2.14.9.5.10 DPCD_Revision

The DPCD revision number of a DP device's DPRX. Shall be cleared to 0 if a DPRX is not connected to the port.

2.14.9.5.11 Peer_Global_Unique_Identifier

This field is valid if the DPCD revision number of a DP device's DPRX is DPCD r1.2 (or higher). This field shall contain the DPRX's GUID (GUID register (DPCD Addresses 00030h through 0003Fh)). This field shall be cleared to 0 if the DP device's revision is less than DPCD r1.2 –or– a DPRX is not connected to the port.

2.14.9.5.12 Number_SDP_Streams

The Number_SDP_Streams field reports the number of SDP streams that the DP port can simultaneously handle. This field is valid if the DisplayPort_Device_Plug_Status bit is set to 1.

2.14.9.5.13 Number_SDP_Stream_Sinks

The Number_SDP_Stream_Sinks field reports the number of SDP stream sinks associated with the DP port. This field is valid if the DisplayPort_Device_Plug_Status bit is set to 1.

2.14.9.6 POWER_DOWN_PHY

POWER_DOWN_PHY request is a path or node request message transaction.

Table 2-222: POWER_DOWN_PHY Message Syntax

Syntax	# of Bits	Format
POWER_DOWN_PHY_Request() { zero Request_Identifier Port_Number zeros } POWER_DOWN_PHY_Ack_Reply() { Reply_Type Request_Identifier Port_Number zeros }	 1 7 4 4 1 7 4 4	 ‘0’ ‘010 0101’ ‘0000’ ‘0’ ‘010 0101’ ‘0000’

If the message is transmitted as a path request, all DP nodes from the DP device adjacent to the originator and the targeted DP node shall be placed in the D3 power state if none of the payloads allocated to the DPTX contain stream symbol sequences. Each node’s immediate upstream device shall use Native AUX writes to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h) to set the downstream node’s power state. The downstream node is set to the D3 state as the reply message transaction propagates upstream. When a DP device receives the acknowledge message from the downstream device, it uses Native AUX transactions to set the downstream DP device into the D3 power state before transmitting the ACK reply to the upstream DP device specified by the RAD. If setting the downstream to the D3 power state failed, a NAK reply is transmitted to the upstream DP device. The power state does not change if a NAK reply is received.

If the message is a node request, the DP node identified by the RAD shall place the DP device connected to the port specified by the Port_Number parameter in the D3 power state if none of the payloads allocated to the DPTX contain active data, using a Native AUX WR to the SET_POWER & SET_DP_PWR_VOLTAGE register.

For both path and node requests, POWER_DOWN_PHY does **not** affect VC Payload ID table.

2.14.9.6.1 Port_Number

The target DFP number of the DP device to be powered down.

2.14.9.7 POWER_UP_PHY

POWER_UP_PHY request is a path or node request message transaction.

Table 2-223: POWER_UP_PHY Message Syntax

Syntax	# of Bits	Format
POWER_UP_PHY_Request() { zero Request_Identifier Port_Number zeros } POWER_UP_PHY_Ack_Reply() { Reply_Type Request_Identifier Port_Number zeros }	 1 7 4 4 1 7 4 4	 ‘0’ ‘010 0100’ ‘0000’ ‘0’ ‘010 0100’ ‘0000’

If the message is transmitted as a path request, all DP nodes from the source immediate downstream device and the targeted DP node shall be placed in the D0 power state. Each nodes immediate upstream device shall use Native AUX writes to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h) to set the downstream node’s power state.

If the message is a node request, the DP node identified by the RAD shall place the DP device connected to the port specified by the Port_Number parameter in the D0 power state, using a Native AUX write to the SET_POWER & SET_DP_PWR_VOLTAGE register.

For both path and node requests, the POWER_UP_PHY request does **not** affect VC Payload ID table.

2.14.9.7.1 Port_Number

The target port number of the DP device to be powered up.

2.14.9.8 QUERY_PAYLOAD

The QUERY_PAYLOAD request determines the available payload bandwidth number for the virtual channel specified by the Virtual_Channel_Payload_Identifier parameter.

Table 2-224: QUERY_PAYLOAD Message Syntax

Syntax	# of Bits	Format
QUERY_PAYLOAD_Request()		
{		
zero	1	‘0’
Request_Identifier	7	‘001 0010’
Port_Number	4	
zeros	5	‘0 0000’
Virtual_Channel_Payload_Identifier	7	
}		
QUERY_PAYLOAD_Ack_Reply()		
{		
Reply_Type	1	‘0’
Request_Identifier	7	‘001 0010’
Port_Number	4	
zeros	4	‘0000’
Allocated_PBN	16	
}		

2.14.9.8.1 Port_Number

The target port number of the DP device to be queried.

2.14.9.8.2 Virtual_Channel_Payload_Identifier

The virtual channel payload identifier of the virtual channel being queried. Each DP node updates Virtual_Channel_Payload_Identifier parameter as the request traverses.

2.14.9.8.3 Allocated_PBN

The allocated downstream payload bandwidth number for the virtual channel on the DFP specified by the QUERY_PAYLOAD request message transaction parameters.

2.14.9.9 REMOTE_DPCD_READ

The REMOTE_DPCD_READ request reads DPCD location in the targeted DP node. Instead of directly reading DPCD of a remote DPRX, the REMOTE_DPCD_READ request is targeted to the DPTX immediately upstream to the DPRX causing the DPTX to initiate DPCD read accesses, by way of Native AUX transactions.

Table 2-225: REMOTE_DPCD_READ Message Syntax

Syntax	# of Bits	Format
REMOTE_DPCD_READ_Request() {		
zero	1	‘0’
Request_Identifier	7	‘010 0000’
Port_Number	4	
DPCD_Address	20	
Number_Of_Bytes_To_Read	8	
}		
REMOTE_DPCD_READ_Ack_Reply() {		
Reply_Type	1	‘0’
Request_Identifier	7	‘010 0000’
zeros	4	‘0000’
Port_Number	4	
Number_Of_Bytes_Read	8	
for (i = 0; i < Number_Of_Bytes_Read; i++)		
DPCD_Byte_Read[i]	8	
}		

2.14.9.9.1 Port_Number

The target port number of the DP device for the Native AUX transactions.

2.14.9.9.2 DPCD_Address

The 20-bit DPCD address to read or write data.

2.14.9.9.3 Number_Of_Bytes_To_Read

Number of DPCD data bytes to read starting from the DPCD address provided, incrementing the address for each byte read.

2.14.9.9.4 Number_Of_Bytes_Read

The actual number of DPCD data bytes read, starting from the DPCD address given.

2.14.9.9.5 DPCD_Byte_Read

The DPCD data byte read.

2.14.9.10 REMOTE_DPCD_WRITE

The REMOTE_DPCD_WRITE request writes data into DPCD locations in the targeted DP node. Instead of directly writing DPCD of a remote DPRX, the REMOTE_DPCD_WRITE request is targeted to the DPTX immediately upstream to the DPRX causing the DPTX to initiate DPCD write accesses, by way of Native AUX transactions.

Table 2-226: REMOTE_DPCD_WRITE Message Syntax

Syntax	# of Bits	Format
REMOTE_DPCD_WRITE_Request()		
{		
zero	1	‘0’
Request_Identifier	7	‘010 0001’
Port_Number	4	
DPCD_Address	20	
Number_Of_Bytes_To_Write	8	
for (i = 0; i < Number_Of_Bytes_Write; i++)		
DPCD_Byte_To_Write[i]	8	
}		
REMOTE_DPCD_WRITE_Ack_Reply()		
{		
Reply_Type	1	‘0’
Request_Identifier	7	‘010 0001’
zeros	4	‘0000’
Port_Number	4	
}		
REMOTE_DPCD_WRITE_Nak_Reply()		
{		
Reply_Type	1	‘1’
Request_Identifier	7	‘010 0001’
Global_Unique_Identifier	128	
Reason_For_Nak	8	
Number_Of_Bytes_Written_Before_Failure	8	
}		

2.14.9.10.1 Port_Number

The target port number of the DP device for Native AUX transactions.

2.14.9.10.2 DPCD_Address

The 20-bit DPCD address to read or write data.

2.14.9.10.3 Number_Of_Bytes_To_Read

Number of DPCD data bytes to read starting from the DPCD address provided, incrementing the address for each byte read.

2.14.9.10.4 Number_Of_Bytes_To_Write

Number of DPCD data bytes to write, starting from the DPCD address given.

2.14.9.10.5 DPCD_Byte_To_Write

The DPCD data byte to write.

2.14.9.10.6 Number_Of_Bytes_Written_Before_Failure

If the Reason_For_Nak is WRITE_FAILURE, the Number_Of_Bytes_Written_Before_Failure field contains the number of DPCD bytes written before the failure occurred.

2.14.9.10.7 Global_Unique_Identifier

The GUID of the targeted DP device.

2.14.9.11 REMOTE_I2C_READ

The REMOTE_I2C_READ requests the I^2C location attached to a remote DP node. The REMOTE_I2C_READ request is targeted to the DPTX immediately upstream to the DPRX of a DP node to which its I^2C location is attached and causes the DPTX to initiate an I^2C-over-AUX transaction. REMOTE_I2C_READ Message Transaction is capable of transporting multiple I^2C transactions such as an I^2C write followed by an I^2C read with a repeated start.

See Section 2.11 for how to transmit I^2C transactions over the AUX_CH.

Table 2-227: REMOTE_I2C_READ Message Syntax

Syntax	# of Bits	Format
REMOTE_I2C_READ_Request()		
{		
zero	1	‘0’
Request_Identifier	7	‘010 0010’
Port_Number	4	
zeros	2	‘00’
Number_Of_I2C_Write_Transactions	2	
for (i = 0; i < Number_Of_I2C_Transactions; i++)		
{		
zero	1	‘0’
Write_I2C_Device_Identifier[i]	7	
Number_Of_Bytes_To_Write[i]	8	
for (j = 0; j < Number_Of_Bytes_To_Write; j++)		
{		
I2C_Data_To_Write[i][j]	8	
}		
zeros	3	‘000’
No_Stop_Bit[i]	1	
I2C_Transaction_Delay[i]	4	
}		
zero	1	‘0’
Read_I2C_Device_Identifier	7	
Number_Of_Bytes_To_Read	8	
}		
REMOTE_I2C_READ_Ack_Reply()		
{		
Reply_Type	1	‘0’
Request_Identifier	7	‘010 0010’
zeros	4	‘0000’
Port_Number	4	
Number_Of_Bytes_Read	8	
for (i = 0; i < Number_Of_Bytes_Read; i++)		
I2C_Device_Byte_Read	8	
}		
REMOTE_I2C_READ_Nak_Reply()		
{		
Reply_Type	1	‘1’
Request_Identifier	7	‘010 0010’
Global_Unique_Identifier	128	
Port_Number	4	
zeros	4	‘0000’
Reason_For_Nak	8	
zeros	6	‘00 0000’
I2C_NAK_Transaction	2	
}		

2.14.9.11.1 Number_Of_I2C_Write_Transactions

The total number of I^2C write transactions to be transmitted with this Message Transaction.

2.14.9.11.2 Port_Number

The target port number of the DP device to receive the I^2C transactions.

2.14.9.11.3 Write_I2C_Device_Identifier

The I^2C device identifier to receive the write request.

2.14.9.11.4 Number_Of_Bytes_To_Write

The number of data bytes to write to the I^2C device.

2.14.9.11.5 I2C_Data_To_Write

The I^2C write data for the write request.

2.14.9.11.6 No_Stop_Bit

When set to 1, a stop bit is not transmitted at the end of the I^2C transaction; otherwise, when cleared to 0, a stop shall be generated at the end of the I^2C transaction.

2.14.9.11.7 I2C_Transaction_Delay

The amount of delay to insert between this and the next I^2C transaction. The delay unit is 10ms. The delay range is 0 to 150ms.

2.14.9.11.8 Read_I2C_Device_Identifier

The I^2C device identifier to receive the read request.

2.14.9.11.9 Number_Of_Bytes_To_Read

The number of data bytes requested to be read from the I^2C device.

2.14.9.11.10 Number_Of_Bytes_Read

The number of data bytes read from the I^2C device.

2.14.9.11.11 I2C_Device_Byte_Read

A data byte read from the I^2C device.

2.14.9.11.12 Global_Unique_Identifer

The GUID of the targeted DP device.

2.14.9.11.13 Reason_For_Nak

See Section 2.14.2.3.3.

2.14.9.11.14 I2C_NAK_Transaction

The I^2C transaction number in which the NAK was received. The I^2C transaction number is from 1 to 3.

2.14.9.12 REMOTE_I2C_WRITE

The REMOTE_I2C_WRITE request writes data to the I^2C locations attached to a remote DP node. The REMOTE_I2C_WRITE request is targeted to the DPTX immediately upstream to the DPRX of a DP node to which its I^2C location is attached and causes the DPTX to initiate I^2C-over-AUX write transactions.

See Section 2.11 for how to transmit I^2C transactions over the AUX_CH.

Table 2-228: REMOTE_I2C_WRITE Message Syntax

Syntax	# of Bits	Format
REMOTE_I2C_WRITE_Request()		
{		
zero	1	‘0’
Request_Identifier	7	‘010 0011’
Port_Number	4	
zeros	5	‘0 0000’
Write_I2C_Device_Identifier	7	
Number_Of_Bytes_To_Write	8	
for (i = 0; i < Number_Of_Bytes_Write; i++)		
I2C_Data_To_Write	8	
}		
REMOTE_I2C_WRITE_Ack_Reply()		
{		
Reply_Type	1	‘0’
Request_Identifier	7	‘010 0011’
zeros	4	‘0000’
Port_Number	4	
}		

2.14.9.12.1 Port_Number

The target port number of the DP device to receive the I^2C transactions.

2.14.9.12.2 Write_I2C_Device_Identifier

The I^2C device identifier to receive the write request.

2.14.9.12.3 Number_Of_Bytes_To_Write

The number of data bytes to write to the I^2C device.

2.14.9.13 RESOURCE_STATUS_NOTIFY

The RESOURCE_STATUS_NOTIFY node broadcast request message transaction shall be transmitted when either of two events occur. One event is when a link's total available PBN does not support the total number of needed PBN of all allocated payloads. This condition can occur when link training occurs after payloads have been allocated and the new total available PBN value does not support the payloads allocated. After receiving this broadcast message, a DP Source can use the QUERY_PAYLOAD request to determine which streams are still allocated and which were de-allocated. After link training, if the link trains to a new total available PBN, but the available PBN still supports all allocated payloads, this broadcast message shall **not** be transmitted as described in Section 2.6.

The second event is when the available PBN through a DP MST Concentrator Branch device changes. For example, when the available PBN through a DP MST Concentrator Branch device changes due to the ALLOCATE_PAYLOAD request, the RESOURCE_STATUS_NOTIFY node broadcast request is transmitted from all DPRX ports. The RESOURCE_STATUS_NOTIFY node broadcast request message shall be transmitted in response to any request that causes a concentrator payload allocation change.

Table 2-229: RESOURCE_STATUS_NOTIFY Message Syntax

Syntax	# of Bits	Format
RESOURCE_STATUS_NOTIFY_Request()		
{		
zero	1	‘0’
Request_Identifier	7	‘001 0011’
Port_Number	4	
zeros	4	‘0000’
Global_Unique_Identifier	128	
Available_PBN	16	
}		
RESOURCE_STATUS_NOTIFY_Ack_Reply()		
{		
Reply_Type	1	‘0’
Request_Identifier	7	‘001 0011’
}		

2.14.9.13.1 Global_Unique_Identifier

The GUID of DP device reporting resource change.

2.14.9.13.2 Port_Number

DPTX port number of resource change.

2.14.9.13.3 Avaliable_PBN

The newly available PBN for the port where resource allocation changed.

2.14.9.14 SINK_EVENT_NOTIFY

Updated in *DP v2.0*.

Upward-going Broadcast Message Transaction. In *DP v2.0* and higher, the only events that initiate a SINK_EVENT_NOTIFY message transaction are Panel Replay errors – Active Frame CRC or RFB Storage errors.

Table 2-230: SINK_EVENT_NOTIFY Message Syntax

Syntax	# of Bits	Format
SINK_EVENT_NOTIFY_Request()		
{		
zero	1	‘0’
Request_Identifier	7	‘011 0000’
Port_Number	4	
zeros	4	‘0000’
Global_Unique_Identifier	128	
Event_Identifier	16	
}		
SINK_EVENT_NOTIFY_Ack_Reply()		
{		
Reply_Type	1	‘0’
Request_Identifier	7	‘011 0000’
}		

2.14.9.14.1 Global_Unique_Identifier

GUID of the Branching Unit, either physical or virtual, that is reporting a Sink event notification.

2.14.9.14.2 Port_Number

Port number on which the Sink event was detected.

2.14.9.14.3 Event_Identifier

16-bit identifier, used to indicate the type of Sink event that was detected:

- **Bit 0** = Panel Replay Active Frame CRC error
- **Bit 1** = Panel Replay RFB Storage error
- **Bit 2** = DSC_RC_Buffer_Under-run
- **Bit 3** = DSC_RC_Buffer_Overflow
- **Bit 4** = DSC_Chunk_Length_Error
- **Bits 15:5** = RESERVED (all 0s)

2.14.9.15 QUERY_STREAM_ENCRYPTION_STATUS

See Appendix I.

2.15 Audio-to-video and Audio-to-audio Synchronization

2.15.1 Overview

Audio-to-video synchronization is a mechanism that synchronizes the audio stream with the video stream on a single monitor or multi-monitor/daisy-chain configuration. In a multi-monitor configuration, if the same audio stream is transmitted to multiple monitors, audio-to-audio synchronization needs to be controlled to ensure a good user experience. This section describes a mechanism that enables audio-to-video (AV) Sync and audio-to-audio (AA) Sync between DP Source and Sink devices. This section is applicable to DP Source and Sink devices that provide audio capability and to all DP Branch devices.

Commonly followed guidelines are that the sound program should never lead the video program by more than 15ms, or lag the video program by more than 45ms. This tolerance level ensures good user experience while listening to media content. *ITU-R BT.1359*, for example, offers a spectrum of advance/delay threshold.

A Sink device shall internally perform the audio-to-video delay compensation if there is a mismatch between audio-to-video processing delays from the point at which the audio-to-video streams arrive at the DP input connector. A Sink device shall adhere to the commonly followed guidelines mentioned above. The audio-to-video synchronization features provided by this Standard allows synchronization of audio-to-video paths when these streams are transmitted to multiple devices in either a daisy-chain topology or when Branch devices exist within the topology.

Sink devices shall report the processing delay of audio and video through the Audio-Video Sync Data Block (AVSDB). (See Section 2.15.2 for the AVSDB specification.) The Source device shall read the audio and video delay data and calculate the delay compensation that is necessary to synchronize the audio with the video. (See Section 2.15.3.2 for details regarding AV sync delay compensation.)

Audio-to-audio delay compensation is performed when the same audio stream is transmitted to multiple Sink devices. The Source device shall perform coarse delay compensation. The Sink device shall perform fine delay compensation. The Source device shall determine the coarse and fine delay values after enumerating processing/decode delay values from the various connected Sink devices. (See Section 2.15.3.3 for details regarding audio-to-audio delay compensation.)

Figure 2-143 illustrates an example of a DP Source device that is connected to three monitors through different ports that output audio and video through those ports. The Source device reads the processing latency of audio and video through the AUX_CH from the DPCD registers, and then transmits the delay values to the higher-level application where the audio-video latency is compensated. The Source device may generate audio delay values and then write those values to the independent display devices so that the audio delay compensation can be performed in those device endpoints.

Note: *Dependencies on the application itself exist to provide a system-level solution beyond the scope of this Standard, and as such, all Source device mandates described within this section are* ***optional****.*

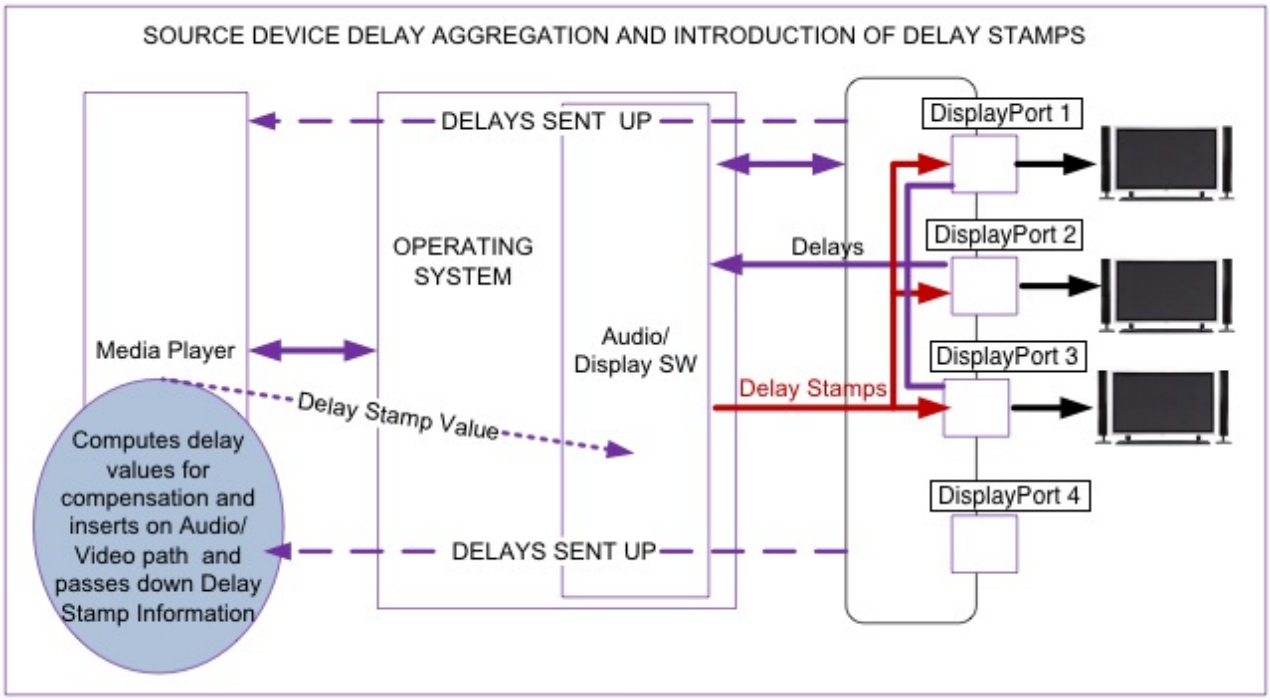


Figure 2-143: Source Device Delay Aggregation and Introduction of Delay Stamps

2.15.2 DP AV Sync Data Block

The Audio-Video Sync Data Block (AVSDB) is a set of DPCD registers that describe the Sink device's audio-to-video decode and post processing delays, and additional delay insertion capability. The values reported by the Sink device shall be static. The Sink device shall meet the reported static delay values and internally compensate for any variation between the operation modes. The AVSDB is allocated to DPCD Addresses 00023h through 0002Dh.

2.15.3 Delay Compensation

2.15.3.1 Audio Delay DPCD Register

The AUDIO_DELAY register (DPCD Addresses 00112h through 00114h) shall be used in Sink devices to allow Source device-based fine-grain control of the audio path delay. The Source device shall calculate the additional audio delay that needs to be introduced in the Sink device and write this value to the AUDIO_DELAY register. Sink devices shall add the specified additional delay on the audio path, based on the delay stamp values. Section 2.15.3.2 and Section 2.15.3.3 describe how the delay stamp values are calculated.

2.15.3.2 AV Sync Delay Compensation

The Sink device shall report the audio and video latency in the AVSDB if the Sink device is capable of rendering audio streams. The Source device shall read the delay values and calculate the necessary delay compensation. It is expected that the Sink device shall internally perform the AV compensation to ensure that the audio-to-video latencies are consistent. In a configuration where the stream is connected to multiple DP Sink devices (e.g., through a repeater or an intermediate Branch device), the Source device shall perform the delay compensation to ensure AV sync. The Source device shall also perform the delay compensation when the same Source device is connected (through its multiple output ports) to multiple DisplayPort devices rendering audio-to-video streams that contain the same data audio-to-video data.

An example of a DisplayPort monitor connected through a repeater device is presented in Figure 2-144. In this example, a repeater device is connected to the Source device and receives an audio-to-video stream through a DP cable. The repeater device then forwards the video stream to a DP monitor which supports only video, while the audio output is driven directly by repeater device that also includes an audio-rendering capability. The monitor and repeater device may have different video and audio processing delays. The Source device shall enumerate each of these delays and determine the Point of Sync (PoS), which is a point in time to which audio and video streams shall be rendered for playback. To meet PoS, the Source device shall add a delay to the video stream. The Source device shall calculate the delay stamp value for audio, and then write the delay stamp value to the Sink device.

Audio delay stamp value =
PoS – (Sink device or Repeater inherent audio delay + delay added to audio in Source device)

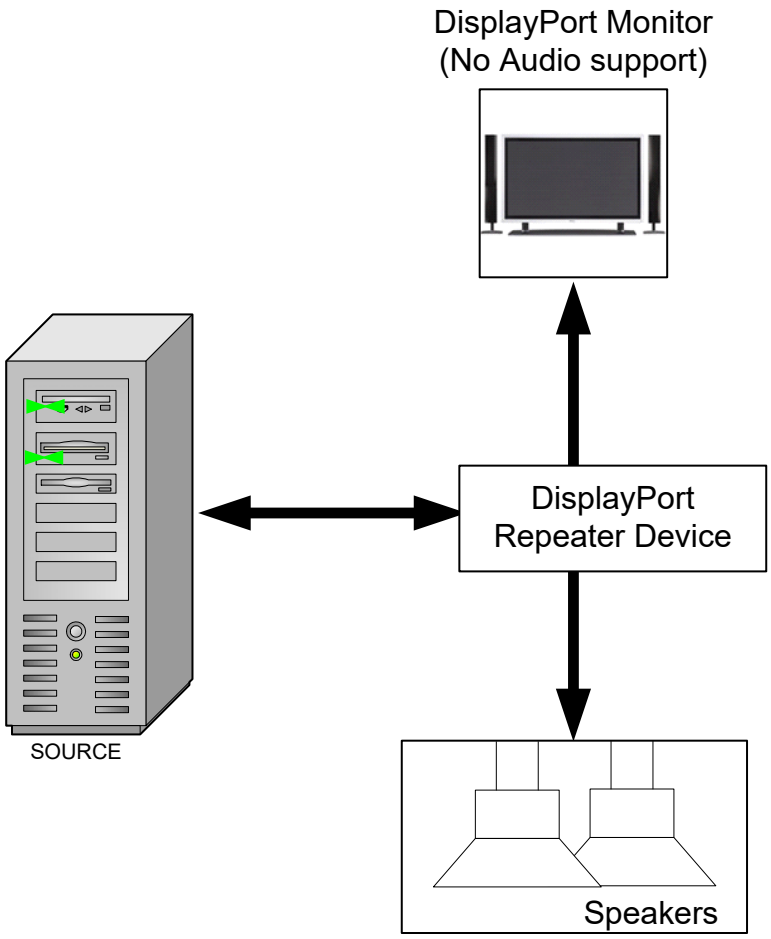


Figure 2-144: DisplayPort Monitor Connected through a Repeater Device

Sink devices shall provide a minimum of 5-ms buffering built-in for fine-grained delay compensation. If the calculated audio delay does not exceed the Sink device's capability, the Source device shall program the AUDIO_DELAY-related registers with the needed delay. If the calculated audio delay exceeds the Sink device's capability, the Source device shall introduce a coarse-grain delay on the audio path, and then recalculate the fine-grained delay needed by the Sink device. The resulting fine-grained delay shall then be programmed into the AUDIO_DELAY-related registers. Figure 2-145 illustrates an example of this delay compensation timing.

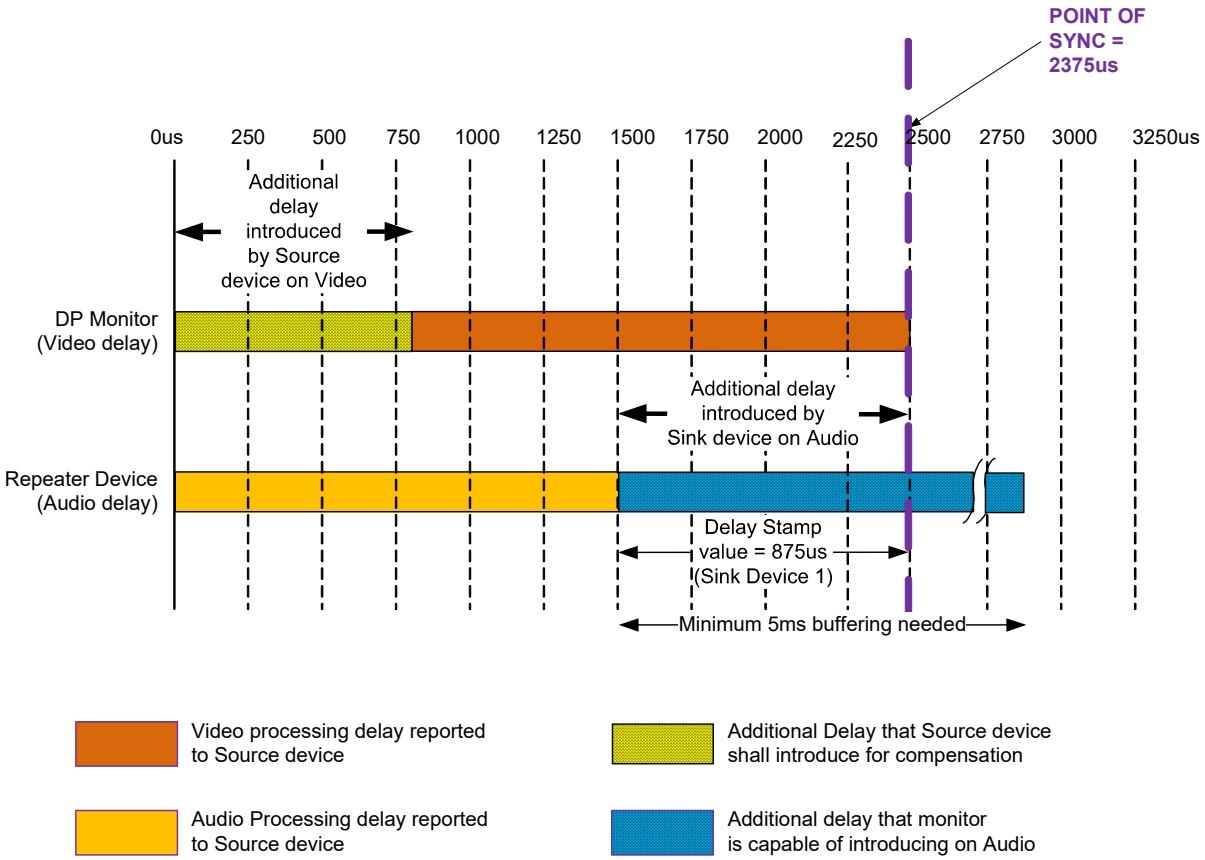


Figure 2-145: Delay Compensation for Audio-to-video Synchronization

In Figure 2-146, the DP Source is streaming the same audio-to-video stream to multiple DP monitors, each of which may have different audio-to-video decode/post processing latencies. The Source device enumerates the delays between each of these monitors, as well as the audio buffering delay that it is capable of inserting. The Source device shall identify the PoS to which all the audio-to-video stream of different monitors shall be rendered at a point in time. The PoS shall be greater than or equal to the maximum audio or video delays introduced by the Sink devices in configuration. The Source device shall compensate for any additional delay needed on the video path on the Source device to meet PoS.

Each Sink device is expected to have a minimum of 5-ms audio delay insertion on its path. The Region Of Overlap (ROO) is defined as a region in which the total audio delay (monitor inherent post processing or decode audio delay + Sink buffer delay) on the audio path between different monitors overlap. If the Source cannot identify ROO, it can add coarse delay on audio path to have a ROO. The fine-grain audio delay adjustments are controlled by writing delay stamp values. The Source can pick any point in time within the ROO and identify that as the PoS. The combined total delay on audio and video should be equal to PoS after compensation.

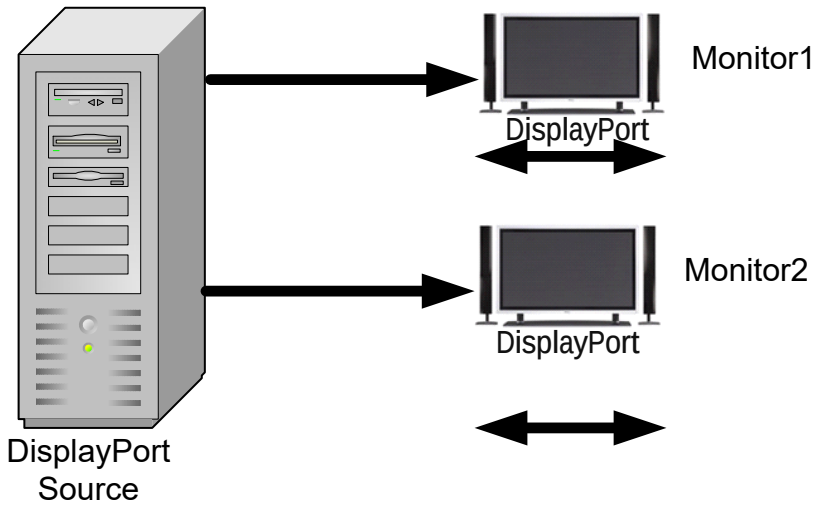


Figure 2-146: DisplayPort Source Device Streaming Audio-to-video Streams to Multiple Monitors

Figure 2-147 illustrates audio and video delays that are incurred within two different Sink devices. The Source device enumerates various delays that are incurred in the Sink device's audio and video paths. The Source device shall compensate for the video delay to meet PoS. Audio delay stamps are calculated to meet the PoS, PoS minus Sink inherent Processing or decode delay gives the "Audio delay stamp value." If this value exceeds the Sink device delay insertion (of 5ms or more), the Source device shall insert coarse delay on the audio path, and fine delay shall be regulated through audio delay stamps. Final audio delay stamps shall be written by the Source device, by way of the AUDIO_DELAY register (DPCD Addresses 00112h through 00114h).

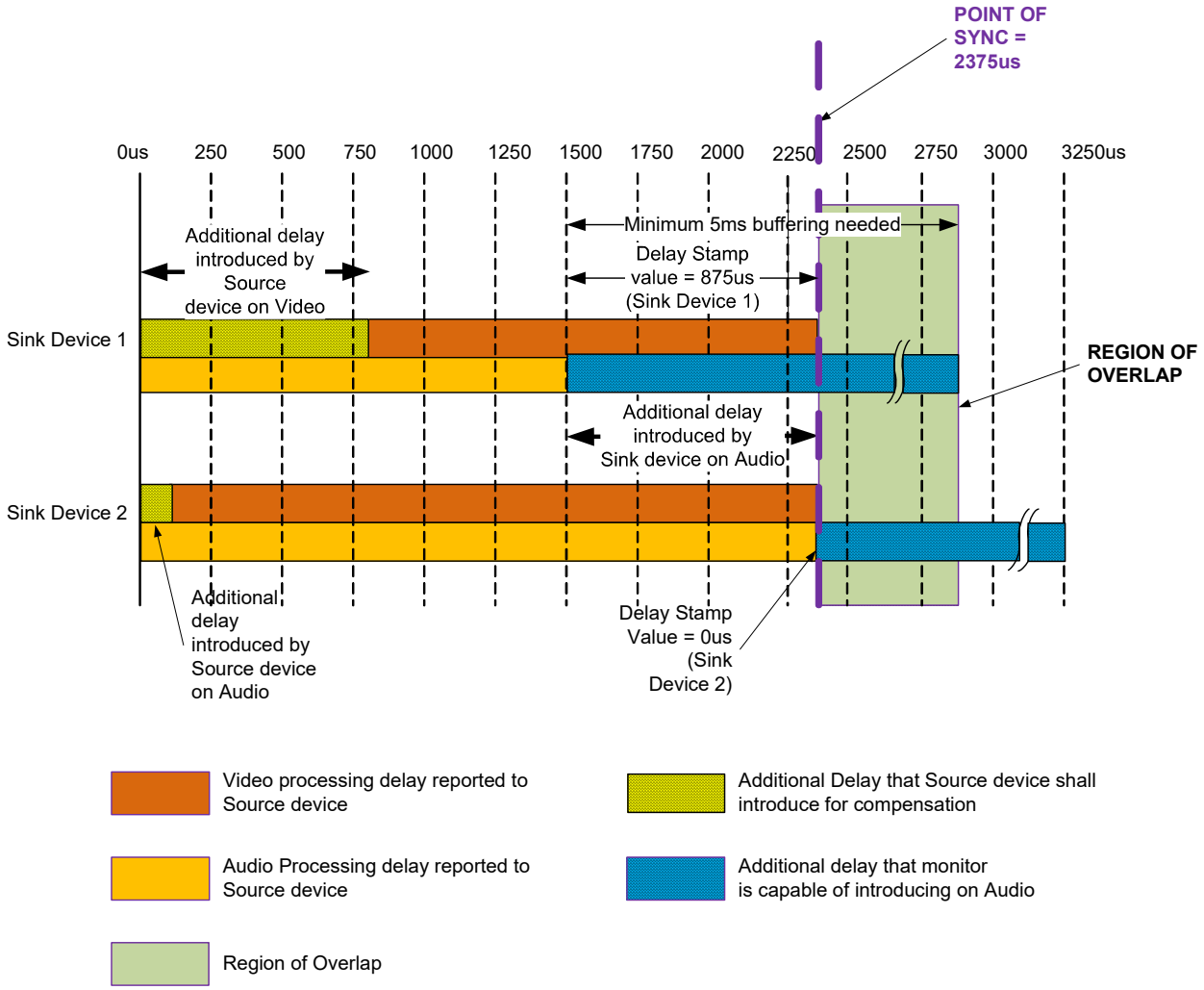


Figure 2-147: Delay Compensation for Audio-to-video Sync in a Multi-monitor Configuration

2.15.3.3 Audio-to-Audio Sync Delay Compensation

In the configuration illustrated in Figure 2-148, a single audio stream is transmitted to multiple DP devices that are capable of playing an audio stream on built-in monitor speakers. These Sink devices can be configured to play audio only (i.e., without video streams being transmitted to the Sink device). The Sink devices shall report the audio post processing or decode latency on the AV Sync data block. The Source device reads these values to calculate how to compensate for the latencies to achieve audio-to-audio synchronization between these devices.

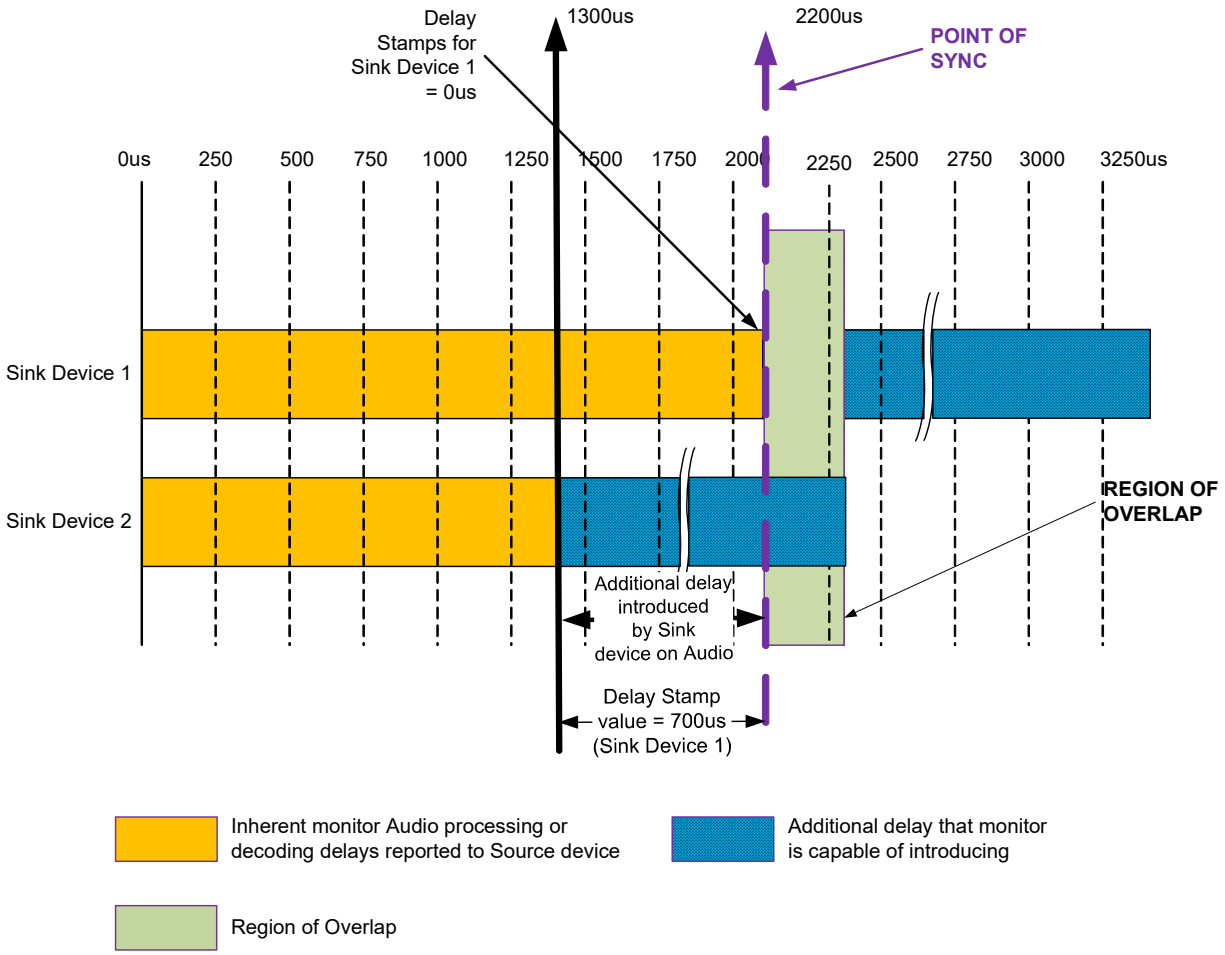


Figure 2-148: Delay Compensation for Audio-to-audio Sync

Sink devices shall support a minimum of 5ms plus the jitter (variance in audio decode or post processing latency in any given mode) incurred on the audio path. Because the Sink devices are expected to report worst case audio delay, the jitter buffer can be used to compensate for jitter incurred in the Sink device.

In the example illustrated in Figure 2-148, Monitors 1 and 2 incur different delays on the audio path. They also support audio buffering for optional audio-to-audio delay compensation. The Source device enumerates the audio latency and additional buffering support in these monitors, and then calculates ROO. If ROO exists, the Source device determines the PoS for delay compensation. If ROO does not exist, coarse delay is inserted to provide ROO. The Source device shall calculate the delay stamp value and write it to the Sink device AVSDB registers (DPCD Addresses 00023h through 0002Dh).

Audio delay stamp value =
PoS – (Sink device inherent delay + any delay added in Source device)

When each of the monitors introduce additional delay as per each delay stamp, the total delay incurred in its Audio path meets PoS and Audio-to-Audio synchronization mandates are satisfied.

2.16 GTC and Audio Inter-channel Sync

This section describes the following two subjects:

- Introduction of the Global Time Code (GTC) of *DP Standard*. The GTC is synchronized between DP devices across a DP link to a 100ns precision. This synchronization is repeated across the entire topology. One end of a link operates as a GTC Master and the other end as a GTC Slave. A GTC Slave synchronizes its GTC value to that of a GTC Master. Each GTC-capable Branch and Sink device shall be able to operate as either a GTC Master or GTC Slave. For a GTC-capable Source device, the ability to operate as a GTC Slave is an **optional** feature.
- Application of GTC for realizing an audio inter-channel synchronization with a 100-ns precision when audio channels are rendered on multiple audio stream sinks connected by DP links.

2.16.1 GTC

The GTC is a 32-bit value, in units of 1ns (the lsb corresponds to 1ns). The GTC FFFFFFFFh value corresponds to just less than 4.3 seconds. A protocol is defined, using a Native AUX transaction for DP devices across a DP link to align GTCs to a 100-ns precision.

GTC shall be supported by DP Sink devices with DPCD r1.2 (or higher) that support audio and all DP Branch devices with DPCD r1.2 (or higher). GTC should be supported by DP Source devices that support audio.

DP Source devices communicate to their downstream devices whether the DP Source devices are GTC-capable and capable of operating as GTC Slaves by setting the TX_GTC_SLAVE_CAP and TX_GTC_CAP bits in the LINK_RATE_SET and TX_GTC_CAPABILITY register (DPCD Address 00115h, bits 4:3, respectively) to 11b.

2.16.1.1 GTC Accumulator Mandate

The GTC generator shall typically be implemented as an accumulator that is driven by a GTC reference clock. How many counts the GTC value increases for each GTC reference clock depends on the GTC reference clock frequency and GTC accumulator's precision. For example, if the GTC accumulator is 32 bits with the lsb corresponding to 1ns and if the GTC reference clock is 100MHz (i.e., 10ns per clock cycle), the value is increased by 10 decimal counts per clock cycle.

GTC synchronization between a GTC Master and GTC Slave consists of two phases:

- **Lock Acquisition** – Initial frequency adjust phase
- **Lock Maintenance** – Ensuing periodic frequency adjust phase

During the Lock Acquisition phase (at the end of which the propagation delay over the DP link is adjusted), the GTC value is transferred from a GTC Master to a GTC Slave every 1ms, while the GTC value transfer takes place every 10ms during the Lock Maintenance phase.

The GTC reference clock on both ends shall be 96MHz or higher during the Lock Acquisition phase, and 24MHz or higher during the Lock Maintenance phase. When the reference clock is switched, care shall be taken to ensure that the switching event does not impact GTC tracking and lock timing mandates. The reference clock shall have a long-term accuracy of ±100ppm from its nominal frequency. SSC is **not** allowed for the GTC reference clock.

As long as a GTC Master's GTC value has no more than 12 error counts during the Lock Acquisition phase and no more than 50 error counts during the Lock Maintenance phase (both resulting from GTC accumulator latching edge uncertainty), a GTC Slave shall be able to settle to the following:

- During the Lock Acquisition phase, the errors should be within ±12 counts of a GTC Master's GTC value on the average (the averaging method described toward the end of the Lock Acquisition Phase description part, right before the Phase Skew Offset part of Section 2.16.1.3.1 and Section 2.16.1.3.2), and shall be no worse than ±25 counts at any time
- During the Lock Maintenance phase, the errors should be within ±50 counts of a GTC Master's GTC value on the average, and shall be no worse than ±100 counts at any time

A GTC Slave shall be able to adjust the rate at which it increases the GTC value by adjusting the reference clock frequency value, increment value, or both.

How to adjust the GTC accumulator increment rate (i.e., a damping factor) during the Lock Maintenance phase is left to the GTC Slave implementer's choice. As a general guideline, a GTC Slave should keep its GTC increment adjustment per 10-ms interval to the following range:

$$|(\text{Next GTC value} - \text{Current GTC value}) - (\text{Current GTC value} - \text{Previous GTC value})| \leq 100$$

Note: *The fact that a GTC Slave increment adjustment guideline is defined per 10-ms interval does not imply that the lock maintenance period shall be exactly 10ms. Although the lock maintenance interval is typically 10ms, the interval is bound to vary from time to time. A GTC Slave compares its own delta (i.e., Current GTC value – Previous GTC value) to a GTC Master's delta. This way, a GTC Slave is tolerant to the lock maintenance interval variation.*

Although the GTC is a 32-bit value with the lsb representing 1ns, the GTC accumulator in a GTC Slave shall be able to increment the GTC accumulator value in precision of well below 1ns in average over lock acquisition/maintenance intervals. For a lock maintenance interval of 10ms and GTC reference clock frequency of 24MHz, there are 240000 GTC accumulation cycles. For example, to adjust the GTC value increment by 25ns per 10-ms period, the average increment rate per GTC accumulation cycle shall be increased by 0.000104 counts (= 25ns / 240000 cycles).

2.16.1.2 DPCD Registers Used for GTC

Table 2-231 lists the DPCD registers that are used for GTC support. (For complete register descriptions, see Table 2-183, Table 2-184, and Table 2-192.)

Table 2-231: DPCD Registers Used for GTC

DPCD Address	Definition	Write/Read Over AUX_CH
00054h through 00057h	**RX_GTC_VALUE** See the RX_GTC_VALUE register's description in Table 2-183 for details.	Read Only
00058h	**RX_GTC_MSTR_REQ** The TX_GTC_VALUE_PHASE_SKEW_EN and RX_GTC_MSTR_REQ bits (bits 1:0, respectively) are used. Bits 7:2 are RESERVED (Read all 0s). See the RX_GTC_MSTR_REQ register's description in Table 2-183 for further details.	Read Only
00059h	**RX_GTC_FREQ_LOCK_DONE** The RX_GTC_FREQ_LOCK_DONE bit (bit 0) is used. Bits 7:1 are RESERVED (Read all 0s). See the RX_GTC_FREQ_LOCK_DONE register's description in Table 2-183 for further details.	Read Only
0005Ah and 0005Bh	**RX_GTC_PHASE_SKEW_OFFSET**	Read Only
00115h	**LINK_RATE_SET and TX_GTC_CAPABILITY** The TX_GTC_SLAVE_CAP and TX_GTC_CAP bits (bits 4:3, respectively) are used. Bits 7:5 are RESERVED (Read all 0s). See the LINK_RATE_SET and TX_GTC_CAPABILITY register's description in Table 2-184 for further details.	Write/Read
00154h through 00157h	**TX_GTC_VALUE** See the TX_GTC_VALUE register's description in Table 2-184 for details.	Write/Read
00158h	**RX_GTC_VALUE_PHASE_SKEW_EN** The RX_GTC_VALUE_PHASE_SKEW_EN bit (bit 0) is used. Bits 7:1 are RESERVED (Read all 0s). See the RX_GTC_VALUE_PHASE_SKEW_EN register's description in Table 2-184 for further details.	Write/Read
00159h	**TX_GTC_FREQ_LOCK_DONE** The TX_GTC_FREQ_LOCK_DONE bit (bit 0) is used. Bits 7:1 are RESERVED (Read all 0s). See the TX_GTC_FREQ_LOCK_DONE register's description in Table 2-184 for further details.	Write/Read

Table 2-231: DPCD Registers Used for GTC (Continued)

DPCD Address	Definition	Write/Read Over AUX_CH
0015Ah and 0015Bh	**TX_GTC_PHASE_SKEW_OFFSET**	Write/Read
02004h	**DEVICE_SERVICE_IRQ_VECTOR_ESI1** The LOCK_ACQUISITION_REQUEST and RX_GTC_MSTR_REQ_STATUS_CHANGE bits (bits 1:0, respectively) are used. See the DEVICE_SERVICE_IRQ_VECTOR_ESI1 register's description in Table 2-192 for further details.	Clearable Read Only (Bit is cleared when 1 is written by way of an AUX write transaction)

2.16.1.3 GTC Lock Acquisition and Maintenance between Adjacent DP Devices with Manchester Transaction Format

A GTC Master transmits its GTC value at the time of the first differential signal edge in the command field (FIRST_COMMAND_EDGE) of a normal Native AUX transaction syntax.

For a Native AUX request transaction, the FIRST_COMMAND_EDGE is the differential signal edge ending the AUX_SYNC pattern, as illustrated in Figure 2-149 (because the msb in the command field is 1).

For a reply transaction, the FIRST_COMMAND_EDGE is later than the SYNC End (because the msb of the reply command to NATIVE AUX transaction is always 0).

The GTC value sampling point applies regardless of whether a DPTX or DPRX is the GTC Master.

A GTC Master shall sample the GTC value at the time FIRST_COMMAND_EDGE leaves its package pins. A GTC Master and GTC Slave shall both measure the FIRST_COMMAND_EDGE position with the accuracy of 10.25ns or better during lock acquisition, and 41ns or better during lock maintenance.

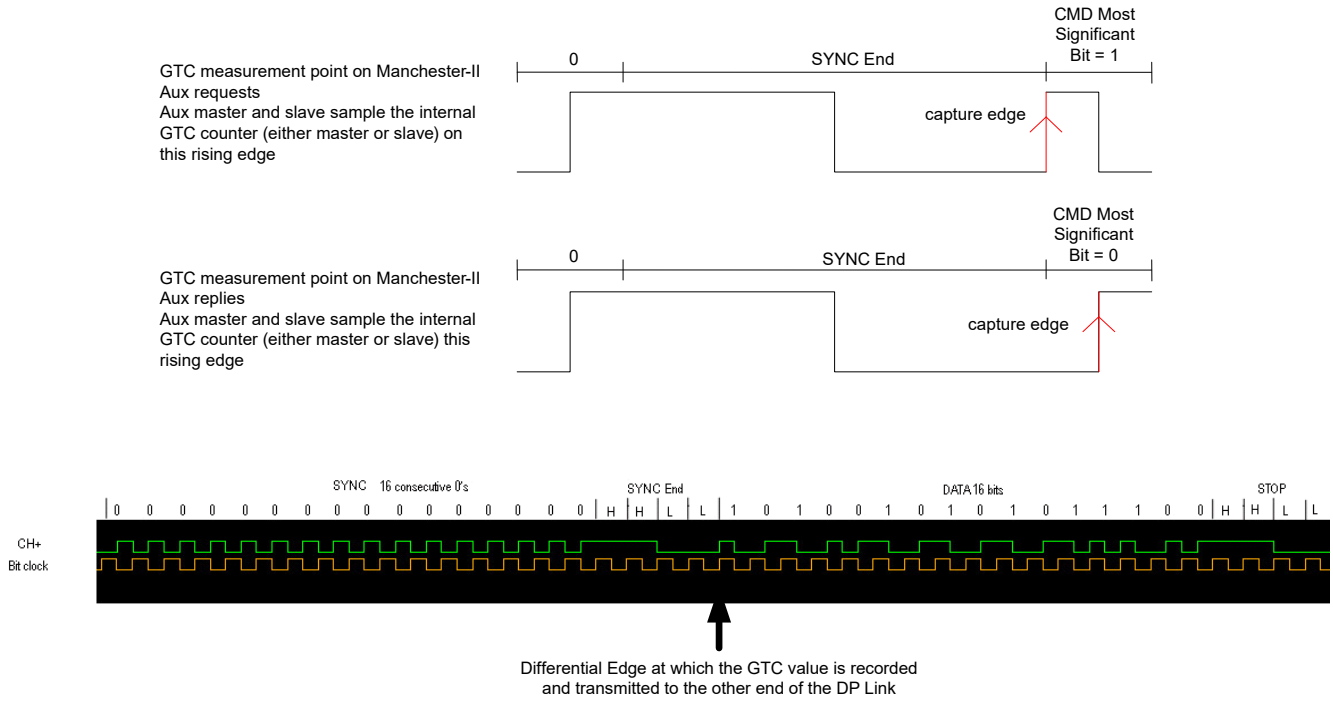


Figure 2-149: GTC Value Measurement Point by GTC Master

The DPTX shall give the GTC-related Native AUX transactions higher priorities than other AUX transaction so that a GTC slave can receive the GTC values at expected intervals. As soon as the other AUX transaction is complete (i.e., AUX_ACK, AUX_DEFER, AUX_NACK, or the AUX Reply Timeout timer times out), the DPTX shall initiate GTC-related Native AUX transaction once lock acquisition interval (1 to 1.5ms, with 1ms typical) has elapsed during lock acquisition and lock maintenance interval (10 to 13ms, with 10ms typical) during lock maintenance.

The lock acquisition and maintenance intervals are defined as the time from the start of one transaction to the start of the next transaction, as illustrated in Figure 2-150.

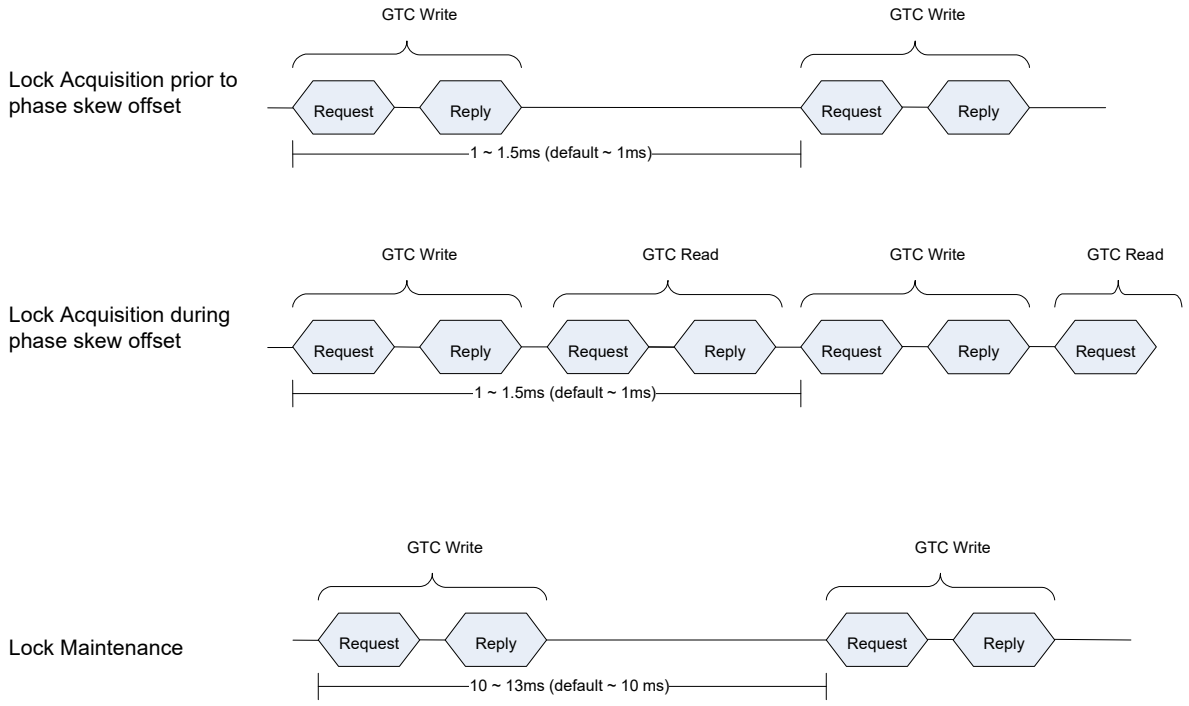


Figure 2-150: Lock Acquisition and Maintenance Intervals

The DPRX shall not reply with AUX_DEFER. The DPRX shall not reply with AUX_NACK except for the following two conditions:

- **Unless the request transaction is corrupted** – The DPRX may return no reply in case the request transaction is corrupted.
- **The DPRX shall be a GTC Master** – The DPRX requests to be a GTC Master by setting the RX_GTC_MSTR_REQ bit in the RX_GTC_MSTR_REQ register (DPCD Address 00058h, bit 0) and RX_GTC_MSTR_REQ_STATUS_CHANGE bit in the DEVICE_SERVICE_IRQ_VECTOR_ESI1 register (DPCD Address 02004h, bit 0) to 1, and then issuing an IRQ_HPD.

Upon AUX_NACK or retry, the DPTX shall retry up to three times, using the GTC value of the FIRST_COMMAND_EDGE position of the retry request transaction, unless it has received an IRQ_HPD with the above bits set.

2.16.1.3.1 GTC Lock Acquisition/Maintenance Procedure when DPTX Is GTC Master

2.16.1.3.1.1 Lock Acquisition Phase

During the Lock Acquisition phase, the DPTX transmits the GTC value at the time of FIRST_COMMAND_EDGE to a DPRX by writing the value to the TX_GTC_VALUE register (DPCD Addresses 00154h through 00157h), by way of a single Native AUX burst write request transaction every lock acquisition interval. A DPTX shall issue the burst write transaction as soon as 1ms has elapsed from the last write and other pending AUX reply transaction is received (or timed out). If the DPTX cannot initiate the Native AUX transaction to the TX_GTC_VALUE registers within 1.5ms after the previous transaction, the DPTX may do one of the following:

- Initiate the transaction after the next interval, which is 2ms from the previous transaction, –or–
- Restart the interval

The DPRX records its own GTC value at the following two timings:

- At the arrival of FIRST_COMMAND_EDGE for every AUX request transaction ("FIRST_COMMAND_EDGE" time value)
- At the time it has finished receiving the 32-bit TX GTC value ("GTC_Reception" time value), if it is a single Native AUX burst write transaction to the TX_GTC_VALUE register

During the Lock Acquisition phase, a DPRX resets its own GTC accumulator to:

$$GTC\_Reset\ value = TX\ GTC\ value + (GTC\_Reception\ value - FIRST\_COMMAND\_EDGE\ value)$$

The delta between the GTC_Reception and FIRST_COMMAND_EDGE values is approximately 64us because there are 64 AUX bit periods (4-bit command, 20-bit address, 8-bit LEN, and 32-bit data) between the FIRST_COMMAND_EDGE to the reception of the 32-bit data.

Starting from the subsequent single Native AUX burst write transaction to the TX_GTC_VALUE register, a DPRX adjusts the GTC accumulator increment rate based on the delta between the GTC_Reset and GTC_Reception values:

- If the GTC_Reset value is larger, the DPRX increases the increment rate
- If the GTC_Reset value is smaller, the DPRX reduces the increment rate

How much to adjust the frequency depends on the absolute amount of delta. A DPRX increases its internal "Lock_Count" value by 1 if the delta is within ±12.5ns. If the delta is within ±25ns, but larger than ±12.5ns, the DPRX keeps the same Lock_Count. If the delta is larger than ±25ns, the DPRX clears the Lock_Count to 0. Only after the Lock_Count is greater than or equal to 5, the DPRX shall set the RX_GTC_FREQ_LOCK_DONE bit to 1.

2.16.1.3.1.2 Phase Skew Offset at the End of Lock Acquisition Phase

After 10 Native AUX write transactions to the TX_GTC_VALUE register (DPCD Addresses 00154h through 00157h) in lock acquisition interval (for each of which it receives AUX_ACK reply), a DPTX reads from the RX_GTC_VALUE register (DPCD Addresses 00054h through 00057h) and the RX_GTC_FREQ_LOCK_DONE bit in the RX_GTC_FREQ_LOCK_DONE register (DPCD Address 00059h, bit 0), by issuing a single Native AUX read burst request transaction to DPCD Addresses 00054h through 00059h.

If the RX_GTC_FREQ_LOCK_DONE bit is set to 1, the DPTX repeats a Native AUX burst write transaction to the TX_GTC_VALUE register, followed by a Native AUX burst read transaction from the RX_GTC_VALUE register and RX_GTC_FREQ_LOCK_DONE bit multiple times at each 1-ms lock acquisition interval.

If the DPTX reads the RX_GTC_FREQ_LOCK_DONE bit cleared to 0, the DPTX has a choice of either re-initiating the Lock Acquisition phase or giving up the lock acquisition.

Note: *A DPRX shall not be designed to depend on the GTC burst read following the GTC burst write, and shall accommodate unrelated AUX transactions in between.*

For each of the above Native AUX read reply transactions with the RX_GTC_FREQ_LOCK_DONE bit set to 1, the DPTX records the delta between its own GTC accumulator value at FIRST_COMMAND_EDGE and the received GTC accumulator value.

Over multiple consecutive read reply transactions for which the RX_GTC_FREQ_LOCK_DONE bit remains set, the DPTX calculates the average of the signed delta value. The phase offset is half of the average of the delta. How many times to read the RX_GTC_VALUE register before calculating the average is left to DPTX implementation choice. A minimum of four reads should be requested.

The DPTX then writes the calculated phase offset value to the TX_GTC_PHASE_SKEW_OFFSET register (DPCD Addresses 0015Ah and 0015Bh) with the RX_GTC_VALUE_PHASE_SKEW_EN bit in the RX_GTC_VALUE_PHASE_SKEW_EN register (DPCD Address 00158h, bit 0) set to 1, by way of a single Native AUX burst write request transaction to DPCD Addresses 00158h through 0015Bh. Upon this Native AUX write transaction, the DPRX increases its GTC accumulator count by TX_GTC_PHASE_SKEW_OFFSET value without adjusting the increment rate. After receiving AUX_ACK to the Native AUX write transaction to DPCD Addresses 00158h through 0015Bh, the DPTX clears the RX_GTC_VALUE_PHASE_SKEW_EN bit with the Native AUX write transaction to DPCD Address 00158h.

2.16.1.3.1.3 Lock Maintenance Phase

The Lock Maintenance phase is entered after a DPTX clears the RX_GTC_VALUE_PHASE_SKEW_EN bit in the RX_GTC_VALUE_PHASE_SKEW_EN register (DPCD Address 00158h, bit 0).

During the Lock Maintenance phase, a DPTX writes the TX_GTC_VALUE register (DPCD Addresses 00154h through 00157h) at every lock maintenance interval. A DPTX shall issue the AUX write transaction as soon as 10ms has elapsed from the last write to the TX_GTC_VALUE register. If the DPTX is waiting for an AUX reply transaction when the 10ms has elapsed, the DPTX shall issue an AUX write transaction as soon as either the reply transaction is received –or– the AUX Response Timeout Timer times out. A DPRX adjusts the GTC accumulator increment rate to maintain the following condition:

Current GTC value – Previous GTC value =
Current TX_GTC_VALUE – Previous TX_GTC_VALUE ±50ns

When the DPRX determines that it is not possible to consistently remain within the above range despite the best effort, the DPRX clears the RX_GTC_FREQ_LOCK_DONE bit in the RX_GTC_FREQ_LOCK_DONE register (DPCD Address 00059h, bit 0), sets the LOCK_ACQUISITION_REQUEST bit in the DEVICE_SERVICE_IRQ_VECTOR_ESI1 register (DPCD Address 02004h, bit 1), and then generates an IRQ_HPD. When to make the judgment is left to each DPRX implementer.

2.16.1.3.2 GTC Lock Acquisition/Maintenance Procedure When DPRX Is GTC Master

For a DPRX interfacing with a DPTX capable of GTC-Slave operation (as indicated by a DPTX's setting the TX_GTC_CAP bit in the LINK_RATE_SET and TX_GTC_CAPABILITY register (DPCD Address 00115h, bit 3) to 1) to request to be a GTC Master, it sets the RX_GTC_MSTR_REQ bit in the RX_GTC_MSTR_REQ register (DPCD Address 00058h, bit 0) and RX_GTC_MSTR_REQ_STATUS_CHANGE bit in the DEVICE_SERVICE_IRQ_VECTOR_ESI1 register (DPCD Address 02004h, bit 0), and then generates an IRQ_HPD.

A DPRX functioning as a GTC Master sets the LOCK_ACQUISITION_REQUEST bit in the DEVICE_SERVICE_IRQ_VECTOR_ESI1 register (DPCD Address 02004h, bit 1), and then generates an IRQ_HPD to request for the start of lock acquisition.

2.16.1.3.2.1 Lock Acquisition Phase

During the Lock Acquisition phase, a DPTX reads the DPRX's GTC value by reading the RX_GTC_VALUE register (DPCD Addresses 00054h through 00057h) and RX_GTC_FREQ_LOCK_DONE bit in the RX_GTC_FREQ_LOCK_DONE register (DPCD Address 00059h, bit 0), by way of a single Native AUX burst read request transaction to DPCD Addresses 00054h through 00059h every lock acquisition interval. Upon the Native AUX read reply transaction, the DPRX stores its GTC value at the FIRST_COMMAND_EDGE differential edge ending the AUX SYNC pattern to the RX_GTC_VALUE register.

A DPTX records its own GTC value at the following two timings:

- At the arrival of FIRST_COMMAND_EDGE for the reply transaction ("FIRST_COMMAND_EDGE" time value)
- At the time it has finished receiving the 32-bit RX GTC value ("GTC_Reception" time value)

During the Lock Acquisition phase, a DPTX resets its own GTC accumulator to:

$$GTC\_Reset\ value = RX\ GTC\ value + (GTC\_Reception\ value - FIRST\_COMMAND\_EDGE\ value)$$

The delta between the GTC_Reception and FIRST_COMMAND_EDGE values is approximately 40us because there are 40 AUX bit periods (8-bit reply command and 32-bit data) between the FIRST_COMMAND_EDGE to the reception of the 32-bit data.

Starting from the subsequent Native AUX burst read from DPCD Addresses 00054h through 00059h every lock acquisition interval, a DPTX adjusts the GTC accumulator increment rate based on the delta between the GTC_Reset and GTC_Reception values:

- If the GTC_Reset value is larger, the DPTX increases the increment rate
- If the GTC_Reset value is smaller, the DPTX reduces the increment rate

How much to adjust the frequency depends on the absolute amount of delta. A DPTX increases its internal "Lock_Count" value by 1 if the delta is within ±12.5ns. If the delta is within ±25ns, but larger than ±12.5ns, the DPTX keeps the same Lock_Count. If the delta is larger than ±25ns, the DPTX clears the Lock_Count to 0. Only after the Lock_Count is greater than or equal to 5, the DPTX shall write its GTC value to the TX_GTC_VALUE register (DPCD Addresses 00154h through 00157h) and set the TX_GTC_FREQ_LOCK_DONE bit in the TX_GTC_FREQ_LOCK_DONE register (DPCD Address 00159h, bit 0) to 1, using a single AUX write burst transaction to DPCD Addresses 00154h through 00159h.

2.16.1.3.2.2 Phase Skew Offset at the End of Lock Acquisition Phase

After setting the TX_GTC_FREQ_LOCK_DONE bit in the TX_GTC_FREQ_LOCK_DONE register (DPCD Address 00159h, bit 0) to 1, a DPTX repeats writing to the following registers:

- TX_GTC_VALUE register (DPCD Addresses 00154h through 00157h)
- RX_GTC_VALUE_PHASE_SKEW_EN register (DPCD Address 00158h)
- TX_GTC_FREQ_LOCK_DONE register (DPCD Address 00159h)

The DPTX then repeats reading of the registers listed below, using a single AUX burst read transaction to DPCD Addresses 00054h through 0005Bh, until it reads that the RX_GTC_FREQ_LOCK_DONE bit is set to 1 every lock acquisition interval:

- RX_GTC_VALUE register (DPCD Addresses 00054h through 00057h)
- RX_GTC_FREQ_LOCK_DONE bit in the RX_GTC_FREQ_LOCK_DONE register (DPCD Address 00059h, bit 0)
- RX_GTC_PHASE_SKEW_OFFSET register (DPCD Addresses 0005Ah and 0005Bh)

The DPRX records the value written to the TX_GTC_VALUE register, as long as the TX_GTC_FREQ_LOCK_DONE bit remains set.

For each of the above Native AUX write transactions with the TX_GTC_FREQ_LOCK_DONE bit set to 1, a DPRX records the delta between its own GTC accumulator value at FIRST_COMMAND_EDGE and the received TX_GTC_VALUE register values. Over multiple consecutive read reply transactions for which the TX_GTC_FREQ_LOCK_DONE bit remains set, the DPRX calculates the average of the signed delta value. The phase offset is half the delta's average. How many times to record the TX GTC value before calculating the average is DPRX implementation-specific. The minimum of four should be requested.

The DPRX then programs the RX_GTC_PHASE_SKEW_OFFSET register to the calculated phase offset value and sets the TX_GTC_VALUE_PHASE_SKEW_EN bit in the RX_GTC_MSTR_REQ register (DPCD Address 00058h, bit 1) to 1. Upon the subsequent Native AUX read transaction from DPCD Addresses 00054h through 00059h, the DPTX increases its GTC accumulator count by the RX_GTC_PHASE_SKEW_OFFSET register value without adjusting the increment rate. After replying with AUX_ACK to this write transaction, the DPRX clears the TX_GTC_VALUE_PHASE_SKEW_EN bit.

Note: *An AUX burst transaction by a DPTX is part of the read/write pair during the phase offset calculation procedure described above, as illustrated in Figure 2-151.*

If a DPTX does not set the TX_GTC_FREQ_LOCK_DONE bit to 1 after 10 reads from DPCD Addresses 00054h through 00059h, a DPRX may prompt the DPTX to stop the lock acquisition by doing the following:

1 Clearing the RX_GTC_MSTR_REQ bit in the RX_GTC_MSTR_REQ register (DPCD Address 00058h, bit 0).

2 Clearing the RX_GTC_MSTR_REQ_STATUS_CHANGE bit in the DEVICE_SERVICE_IRQ_VECTOR_ESI1 register (DPCD Address 02004h, bit 0).

3 Generating an IRQ_HPD.

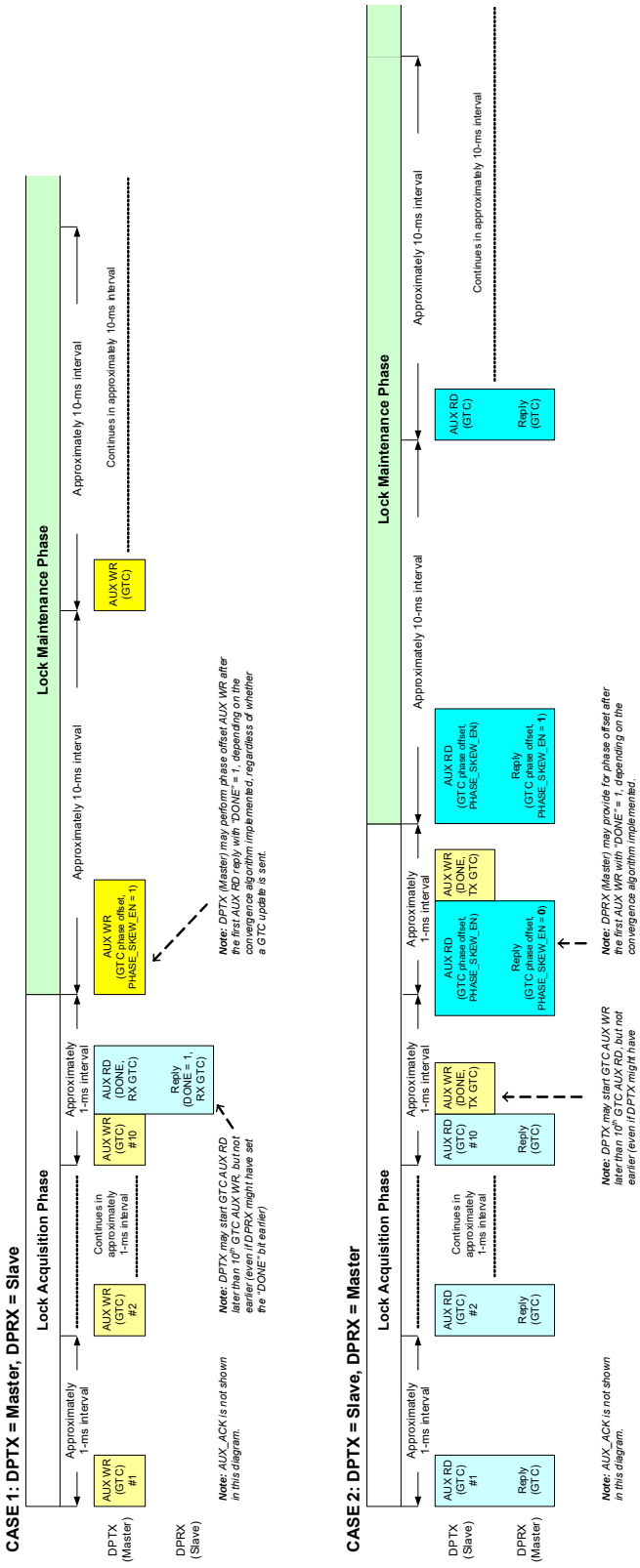


Figure 2-151: AUX Transactions for GTC Synchronization (Informative)

2.16.1.3.2.3 Lock Maintenance Phase

The Lock Maintenance phase is entered after a DPTX reads the TX_GTC_VALUE_PHASE_SKEW_EN bit in the RX_GTC_MSTR_REQ register (DPCD Address 00058h, bit 1) as cleared to 0.

During the Lock Maintenance phase, a DPTX reads the RX_GTC_VALUE register (DPCD Addresses 00054h through 00057h) at every lock maintenance interval. A DPTX shall issue the AUX read transaction as soon as 10ms has elapsed from the last write to the TX_GTC_VALUE register (DPCD Addresses 00154h through 00157h). If the DPTX is waiting for an AUX reply transaction when the 10ms has elapsed, the DPTX shall issue an AUX write transaction as soon as either the reply transaction is received –or– the AUX Response Timeout Timer times out. A DPRX adjusts the GTC accumulator increment rate to maintain the following condition:

Current GTC value – Previous GTC value =
Current RX_GTC_VALUE – Previous RX_GTC_VALUE ±50ns

When a DPRX determines that it is not possible to consistently remain within the above range despite the best effort, the DPRX doing the following:

1 Clears the RX_GTC_FREQ_LOCK_DONE bit in the RX_GTC_FREQ_LOCK_DONE register (DPCD Address 00059h, bit 0).

2 Sets the LOCK_ACQUISITION_REQUEST bit in the DEVICE_SERVICE_IRQ_VECTOR_ESI1 register (DPCD Address 02004h, bit 1).

3 Generates an IRQ_HPD.

When to make the judgment is left to each DPRX implementer.

2.16.1.4 Selection of GTC Grand Master

When multiple GTC-capable DP devices are connected by way of multiple DP links in a given topology, one device shall be selected as a GTC Grand Master. A device connected to the GTC Grand Master becomes a GTC Slave. This GTC Slave device when it conducts the GTC synchronization with another device becomes a GTC Master. As a result of the series of GTC synchronizations, all DP devices in the topology become synchronized to the GTC Grand Master.

By default, an upstream device is a GTC Master of any DP link. When there is only one DP Source device in a topology, therefore, that one DP Source device becomes the GTC Grand Master.

2.16.1.4.1 Selection of GTC Grand Master when Multiple Source Devices Present

When there are multiple Source devices in a topology that has one or multiple Concentrator Branch devices, only one device is chosen as a GTC Grand Master.

When one of the UFPs of a Concentrator (UFP1) has either achieved the GTC Lock or started the GTC lock acquisition with its upstream device (Upstream Device1), and when another upstream device (Upstream Device2) connected to the other UFP (UFP2) starts GTC lock acquisition, the Concentrator port takes the following actions:

1 Sets the RX_GTC_MSTR_REQ bit in the RX_GTC_MSTR_REQ register (DPCD Address 00058h, bit 0) to 1.

2 Sets the RX_GTC_MSTR_REQ_STATUS_CHANGE bit in the DEVICE_SERVICE_IRQ_VECTOR_ESI1 register (DPCD Address 02004h, bit 0) to 1 and generates an IRQ_HPD.

3 Upon IRQ_HPD handling by Upstream Device2, initiates GTC lock acquisition as GTC Master.

4 Subsequently, maintains GTC Lock as a GTC Master.

If Upstream Device2 is another Branch device, that Branch device is to re-initiate GTC lock acquisition as a GTC Master to other downstream and upstream links if those links have already either started or achieved GTC lock acquisition.

If a Concentrator simultaneously receives Native AUX transactions for GTC lock acquisition from multiple upstream devices, the Concentrator accepts one of the upstream devices as a GTC Master. To the upstream device that was not selected, the Concentrator replies with AUX_NACK, and then initiates GTC lock acquisition as a GTC Master as described above. If multiple Source devices support only a GTC Master mode of operation, only one of the Source devices can use GTC.

How a Concentrator selects one upstream device it accepts as a GTC Grand Master is an implementation-specific decision and is beyond the scope of this Standard.

2.16.1.4.1.1 Disabling GTC Synchronization

The Grand Master status is relinquished when an AUX transaction for Lock Acquisition or Maintenance is skipped for five consecutive intervals.

2.16.1.4.1.2 Branch Device GTC Handling Mandates

All Branch device MST-capable DPTX and DPRX ports shall be able to handle GTC in Master mode and Slave mode. Only one Branch device DPTX/DPRX port functions as a GTC Slave, while other ports function as a GTC Master to the adjacent devices.

A Branch device shall have only one GTC value that is to be used for all the ports.

2.16.1.4.1.3 Power Management while GTC Is in Use

AUX_CH should remain powered while GTC is in use; otherwise, GTC operation shall not work.

2.16.2 Application of GTC for Audio Inter-channel Synchronization

Having established a common global time reference across all nodes, the DP audio stream source shall determine the GTC presentation time for each audio frame.

An *IEC 60958* audio frame consists of 192 audio samples. A One Bit audio or DST audio frame consists of the number of samples that occur within $1/75^{th}$ of a second. The DP audio stream Source shall insert the desired GTC presentation time for the audio frame into the "Channel" field ("C" in Figure 2-32 through Figure 2-34) in a bit serial manner in the last 32 samples of an audio frame (Number of Samples/frame – 32 to Number of Samples/frame – 1), starting with the msb of the GTC in the first audio sample of the series.

Of the 32-bit field, the most significant 31 bits of the GTC value (bits 31:1) occupy the most significant 31 bits of the field. The lsb is used to indicate the validity of the field. If the lsb is 0, the field is to be ignored by a stream sink.

The 31-bit GTC value represents the starting time of the presentation of immediately upcoming audio frame.

The DP Source device shall choose GTC presentation values as follows, based on the audio delay capabilities discovered through the mechanism described in Section 2.15:

1 Calculate the propagation delay to each of the audio stream sinks in the topology.

2 Calculate the GTC presentation value that all audio stream sinks can achieve within their audio delay capabilities.

3 Increase the GTC presentation value each frame by the GTC delta between two audio frames.

Note: *The audio sample rate is* ***not*** *synchronized to the GTC rate. The GTC should be used as a "ruler." An audio stream sink device should render the audio within ±500ns of the specified GTC value.*

2.16.2.1 Presentation Time

The presentation time is defined at the points in systems as defined below:

- **Systems with speakers** – At analog speaker terminals
- **Systems with analog audio outputs** – At the analog audio-out jack
- **Systems with digital outputs** – At the digital output jack at the signal edge in that particular digital protocol defining the sample rendering instant.

With the presentation time plane defined as above, one may use an audio test signal that has a well-defined edge (e.g., a sawtooth wave) at a known time to verify that the audio is being rendered at the proper time.

2.16.2.1.1 Dynamic Presentation Time Adjustment

If an audio stream already has embedded GTC values for a presentation time, but there is a need to adjust the playback offset, an audio source device should set the AudioMute_Flag bit in the VB-ID (bit 4) on the link, adjust the presentation time, and then clear the AudioMute_Flag bit.

In case an audio sink device encounters abrupt change in the presentation time received from an audio source device relative to its presentation time based on its current audio sampling rate without preceding the AudioMute_Flag bit, the Sink device should ensure that the change is persistent by checking the presentation time a few extra times, and, if persistent, should make the presentation time change in a manner that results in minimum audio glitch.

2.16.2.1.2 Presentation Time Insertion for Multi-channel Audio

When rendering multi-channel audio on multiple physical audio rendering devices, a Source device, as a rule, shall insert the same presentation time in all audio channels. If a rendering skew is needed among multiple physical audio rendering devices, a Source device shall insert the skew among multiple audio channels before audio stream transmission.

2.17 Panel Replay Mode

New to *DP v2.0*.

This section defines Panel Replay mode, a subset of Panel Self Refresh 2 mode (defined in *eDP v1.4b* and higher (*eDP Standard*)). Panel Replay mode is a subset because it eliminates various Panel Self Refresh mode options. As a prerequisite for understanding Panel Replay mode, it is therefore necessary to understand Panel Self Refresh mode.

2.17.1 Comparison to Panel Self Refresh Mode

The following is a brief summary of Panel Self Refresh 2 mode, as defined in *eDP Standard*:

- DP Source device uses the VSC SDP to prompt entry into and exit from Panel Self Refresh 2 mode
- While entering Panel Self Refresh 2 mode, a DP Source device prompts a DP Sink device to write the “live” active video pixel data that the DP Source device is transmitting over the Main-Link to the DP Sink device’s internal Remote Frame Buffer (RFB)
- In Panel Self Refresh 2 mode, the DP Sink device displays pixel data from the RFB on its screen
- While in Panel Self Refresh 2 mode, the DP Source device may update the display with a full-screen live active video frame or partial-screen live active video (referred to as “Selective Update” (SU)) at or nearly at Panel Self Refresh 2 display timing

Table 2-232 lists the *eDP Standard* Main-Link activity options while in Panel Self Refresh 2 mode.

Table 2-232: Panel Self Refresh 2 Mode Main-Link Activity Options

Option	Description
1-A	DP Source device continues to transmit video timing (i.e., BE and BS control symbols are transmitted to a frame rate-governed micro-packet (or TU)), to be discarded by a DP Sink device.
1-B	DP Source device transmits an Idle Pattern.
1-C	DP Source device disables Main-Link signal transmission.

For Options 1-B and 1-C, *eDP Standard* provides options for syncing the DP Sink device’s Panel Self Refresh 2 display timing with DP Source device timings to minimize the display timing re-synchronization period for transitioning from Panel Self Refresh 2 mode to Live Active Frame mode.

Panel Replay mode in *DP v2.0* mandates Option 1-A, and precludes Options 1-B and 1-C.

2.17.2 Applicability of Panel Replay Mode

Panel Replay is an **optional** feature for DP Source and Sink devices. Panel Replay mode may be enabled in a system only when the DP Source and Sink devices both support Panel Replay. Panel Replay is available for 8b/10b Link Layer in SST and MST modes, and for 128b/132b Link Layer.

Use of RS FEC for Main-Link serial bit signals is mandated in Panel Replay mode:

- **8b/10b Link Layer** – RS(254, 250) FEC (see Section 3.5.1.5)
- **128b/132b Link Layer** – RS(198, 194) FEC (see Section 3.5.2.11)

Note: *Concurrent S3D and Panel Replay support is* ***not*** *defined within this Standard.*

2.17.2.1 Video Frame Terminology and Definition

The term "video frame" refers to the VBlank period, HBlank period, and active pixel data. A video frame spans from the first BS symbol of the VBlank period to the last active pixel of the last active line, as illustrated in Figure 2-152.

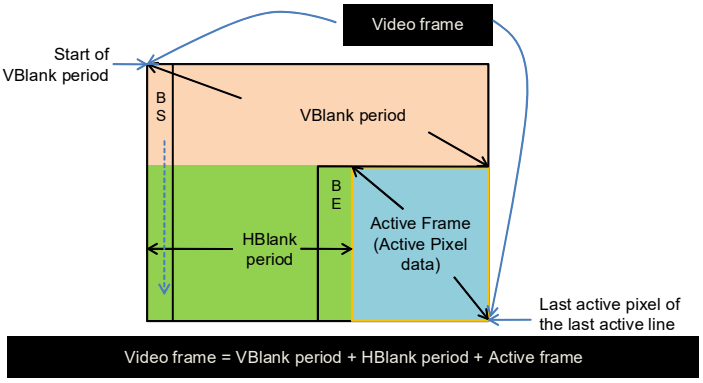


Figure 2-152: Pictorial Representation of Video Frame and Active Frame

An "active frame" is composed of only active pixel data, starting with the first pixel after the first BE symbol at the end of the VBlank period and continuing to the last active pixel of the last active line, excluding the HBlank period of each horizontal line.

The HBlank period starts from the BS symbol sequence and ends with a BE symbol, and includes the BS symbol sequence and BE symbol of each horizontal line.

Video framing remains consistent in Live Active Frame mode and Panel Replay mode.

The term "Live Active Frame mode" is used for normal operation, without Panel Replay mode enabled. Live Active Frame mode may be used with a fixed or variable refresh rate in Adaptive-Sync capable systems. In an Adaptive-Sync configuration, the DP Sink device shall display the video frame received from the DP Source device, at the DP Source device-set refresh rate for that frame, with no delay. During Live Active Frame mode, a DP Source device shall transmit pixel data to be rendered by a DP Sink device. Section 2.17.6 defines the transition between Live Active Frame and Panel Replay modes.

2.17.3 Video Timing, HDCP, and Audio Streaming in Panel Replay Mode

A DP Source and Sink device shall keep their respective Main-Link DPTX and DPRX active during Panel Replay. A DP Source device shall transmit BS/BE symbols that match the video timing at all times, regardless of whether the DP Source device is transmitting active pixels or dummy data. A DP Sink device shall slave itself to the display timings received from the DP Source device and render the new frame, at the DP Source device-set refresh rate for the current video frame, the same as in Live Active Frame mode.

HDCP Cipher clocking and XOR shall continue as in Live Active Frame mode, and are agnostic of Panel Replay mode.

SDP transmission shall continue, uninterrupted by Panel Replay mode. The DP Source device may transmit SDPs during blanking intervals in Panel Replay mode. The DP Sink device shall continue to support SDP reception in Panel Replay mode including Audio_Stream SDPs.

2.17.4 Panel Replay Mode Enumeration and Configuration

A DP Sink device shall declare its Panel Replay capability in the Panel Replay Support bit in the PANEL REPLAY CAPABILITY SUPPORTED register (DPCD Address 000B0h, bit 0). A DP Source device shall read this register to determine whether the DP Sink device is Panel Replay-capable before enabling Panel Replay mode. A DP Source device that is plugged to a Panel Replay-capable DP Sink device and anticipates enabling of Panel Replay shall set the Source Device Enables Panel Replay Mode in Sink Device bit in the PANEL REPLAY ENABLE AND CONFIGURATION register (DPCD Address 001B0h, **bit 0**) to 1 before initiating link training to arm the DP Sink device for Panel Replay mode. The DP Source device shall **not** initiate entry to Panel Replay mode until the DP Source device has received an ACK from the DP Sink device for the Panel Replay mode enable AUX write transaction. After receiving the ACK, the DP Source device may use the VSC SDP to initiate Panel Replay active state entry any time after link training completes.

The DP Sink device may add an additional delay of no more than 3 lines to the pixel stream when the device is armed for the Panel Replay mode. The DP Sink device shall correctly process the first VSC SDP received that carries Panel Replay information after the DP Sink device ACKs a Panel Replay mode enable.

Figure 2-153 illustrates the DP Source and Sink device Panel Replay mode configuration process.

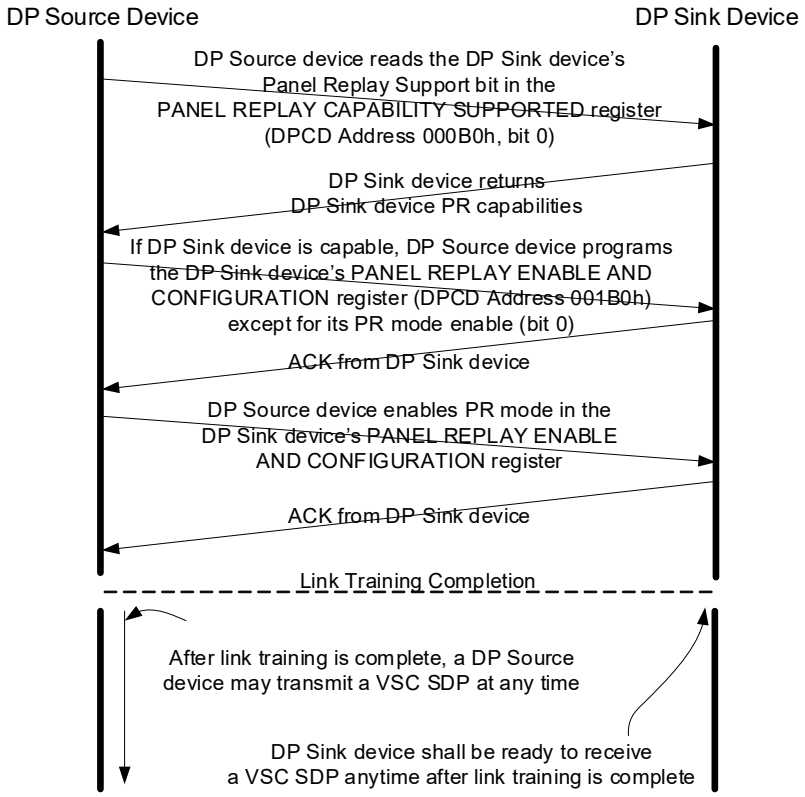


Figure 2-153: Panel Replay Configuration

2.17.5 VSC SDP Use for Panel Replay

Note: *For general VSC SDP use, see Section 2.2.5.6.*

This section defines the VSC SDP format that is needed to support Panel Replay. See Section 2.17.6 through Section 2.17.9 for the transmission timing needs of a VSC SDP that carries Panel Replay information. See Section 2.2.5.6.2 for VSC SDP payload mapping over the Main-Link.

A DP Source device uses VSC SDP in-band signaling to indicate Panel Replay entry and exit:

- Table 2-233 defines the VSC SDP header bytes related to Panel Replay signaling
- Table 2-234 defines bit definitions of the VSC SDP data payload for Panel Replay

Table 2-233: VSC SDP Header Extension Bytes for Panel Replay Mode

Byte #	Bit #	Content
HB0	7:0	**Secondary-data Packet ID** 00h.
HB1	7:0	**Secondary-data Packet Type** 07h.
HB2	4:0	**Revision Number** 01h = VSC SDP supporting 3D stereo only. 06h = VSC SDP supporting 3D stereo + PR. 07h = VSC SDP supporting 3D stereo + PR + Pixel Encoding/Colorimetry Format indication. All other values are RESERVED.
	7:5	**RESERVED** Read all 0s.
HB3	4:0	**Number of Valid Data Bytes** 01h = VSC SDP supporting 3D stereo only (HB2 = 01h). 10h = VSC SDP supporting 3D stereo + PR (HB2 = 06h). 13h = VSC SDP supporting 3D stereo + PR + Pixel Encoding/Colorimetry Format indication (HB2 = 07h).
	7:5	**RESERVED** Read all 0s.

Table 2-234: VSC SDP Payload Extension Bytes for Panel Replay Mode

Byte #	Bit #	Content
DB0	7:0	Used for 3D stereo.
DB1	0	**PR_STATE** 0 = PR Inactive (normal operation mode, Live Active Frame mode). 1 = PR Active (indication to enter PR mode).
	1	**RESERVED** Read 0.
	2	**CRC_VALID** 0 = VSC payload does not contain a valid CRC of the SU region/full active frame. 1 = VSC payload contains a valid CRC of the SU region/full active frame.
	3	**SU_COORDINATES_VALID** 0 = Do not update the RFB. 1 = Update the RFB – Capture the incoming frame/SUs into the RFB.
	7:4	**RESERVED** Read all 0s.
DB2	7:0	**CRC for R or Cr of the Last Transmitted Selective Update Region**
DB3	15:8	
DB4	7:0	**CRC for G or Y of the Last Transmitted Selective Update Region**
DB5	15:8	
DB6	7:0	**CRC for B or Cb of the Last Transmitted Selective Update Region**
DB7	15:8	
DB8	7:0	**Selective Update Region Upper-left Corner X-coordinate (Pixel Count)** Starts with a value of 00h for the first active pixel. When PR SU granularity is **not** needed (Panel Replay Selective Update Granularity Needed bit in the PANEL REPLAY CAPABILITY register (DPCD Address 000B1h, bit 5) is cleared to 0), this X-coordinate value shall be evenly divisible by 16. When PR SU granularity is needed (Panel Replay Selective Update Granularity Needed bit is set to 1), this X-coordinate value shall be evenly divisible by the SU_X_GRANULARITY value.
DB9	15:8	

Table 2-234: VSC SDP Payload Extension Bytes for Panel Replay Mode

Byte #	Bit #	Content
DB10	7:0	**Rectangle Width (Pixel Count)** Value shall be non-zero when the SU_COORDINATES_VALID bit (DB1, bit 3) is set to 1. When PR SU granularity is **not** needed (Panel Replay Selective Update Granularity Needed bit is cleared to 0), the rectangle width shall be evenly divisible by 4. When PR SU granularity is needed (Panel Replay Selective Update Granularity Needed bit is set to 1), the rectangle width shall be evenly divisible by the SU_X_GRANULARITY value.
DB11	15:8	
DB12	7:0	**Selective Update Region First Scan Line Y-coordinate** Starts with a value of 00h for the first active video line. When PR SU granularity is **not** needed (Panel Replay Selective Update Granularity Needed bit is cleared to 0), this Y-coordinate can represent any active line (divisible by 1). When PR SU granularity is needed (Panel Replay Selective Update Granularity Needed bit is set to 1), this Y-coordinate value shall be evenly divisible by 1, 2, 4, 8, or 16, as indicated by SU_Y_GRANULARITY.
DB13	15:8	
DB14	7:0	**Rectangle Height (Pixel Count)** Value shall be non-zero when the SU_COORDINATES_VALID bit (DB1, bit 3) is set to 1. When PR SU granularity is **not** needed (Panel Replay Selective Update Granularity Needed bit is cleared to 0), the rectangle height can represent any integer number of lines (divisible by 1). When PR SU granularity is needed (Panel Replay Selective Update Granularity Needed bit is set to 1), the SU region height shall be evenly divisible by 1, 2, or 4, as indicated by SU_Y_GRANULARITY
DB15	7:0	
DB16	7:0	Used for colorimetry format information.
DB17	7:0	
DB18	7:0	

2.17.6 Transition between Live Active Frame and Panel Replay Modes

To enable Panel Replay mode entry, a DP Source device shall transmit a VSC SDP with the PR_STATE and SU_COORDINATES_VALID bits (DB1, bits 0 and 3, respectively) set to 1, and the X-coordinate, rectangle width, Y-coordinate, and rectangle height indicating the full-screen active frame.

To enable Panel Replay mode with 8b/10b Link Layer, a DP Source device shall enable FEC on the link before initiating Panel Replay. The VSC SDP that initiates Panel Replay entry/exit shall be completely transmitted during the VBlank period, at least 50us before the video frame's first active pixel. When transitioning to Panel Replay mode, the DP Source device shall transmit a full-screen active frame after transmitting the VSC SDP with Panel Replay active indication. The DP Source device may optionally transmit a VSC SDP carrying the active frame's CRC. When transmitting the VSC SDP carrying the active frame's CRC, the DP Source device shall transmit the VSC SDP after transmitting the active frame, and before transmitting the first BE of the next video frame.

After it receives a VSC SDP with Panel Replay active indication, a DP Sink device shall capture the active frame received into its RFB. The DP Sink device shall display the active frame received at the DP Source device-set refresh rate. The DP Sink device shall continue to slave its display timings to the DP Source device display timings, the same as in Live Active Frame mode.
The DP Sink device shall ensure that there are no visible artifacts (e.g., image flickering) that result from the transition in and out of Panel Replay mode.

To exit Panel Replay mode and enter Live Active Frame mode, the DP Source device shall transmit a VSC SDP with the PR_STATE bit cleared to 0.

After it detects a disconnect event, the DP Source device shall reset its PR state. The DP Sink device, after detecting a disconnect event, shall tear down the display, stop rendering from its local frame buffer, and then reset its PR state.

2.17.6.1 DP Source Device Panel Replay States

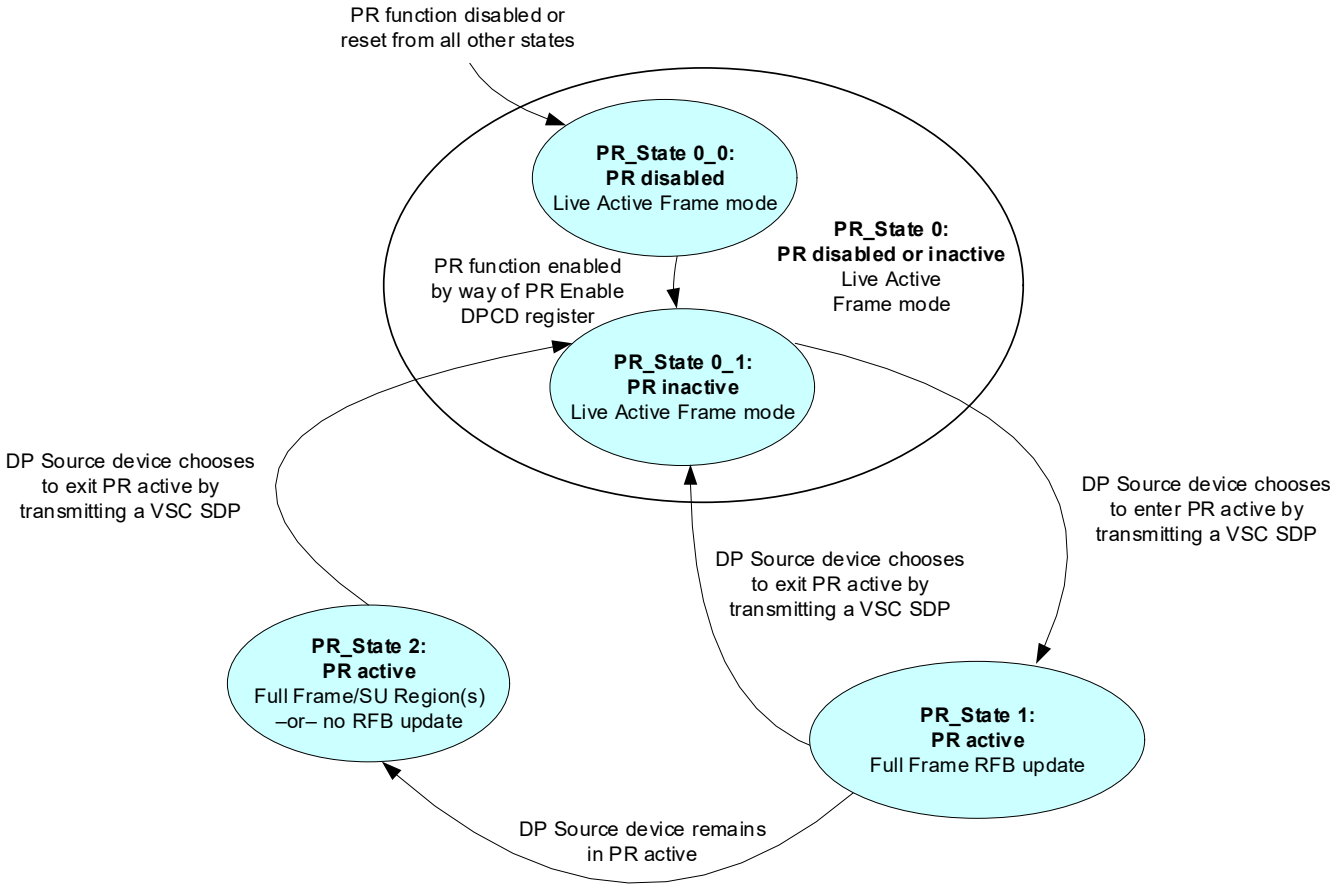


Figure 2-154: DP Source Device Panel Replay States

2.17.6.2 DP Sink Device Panel Replay Mode States

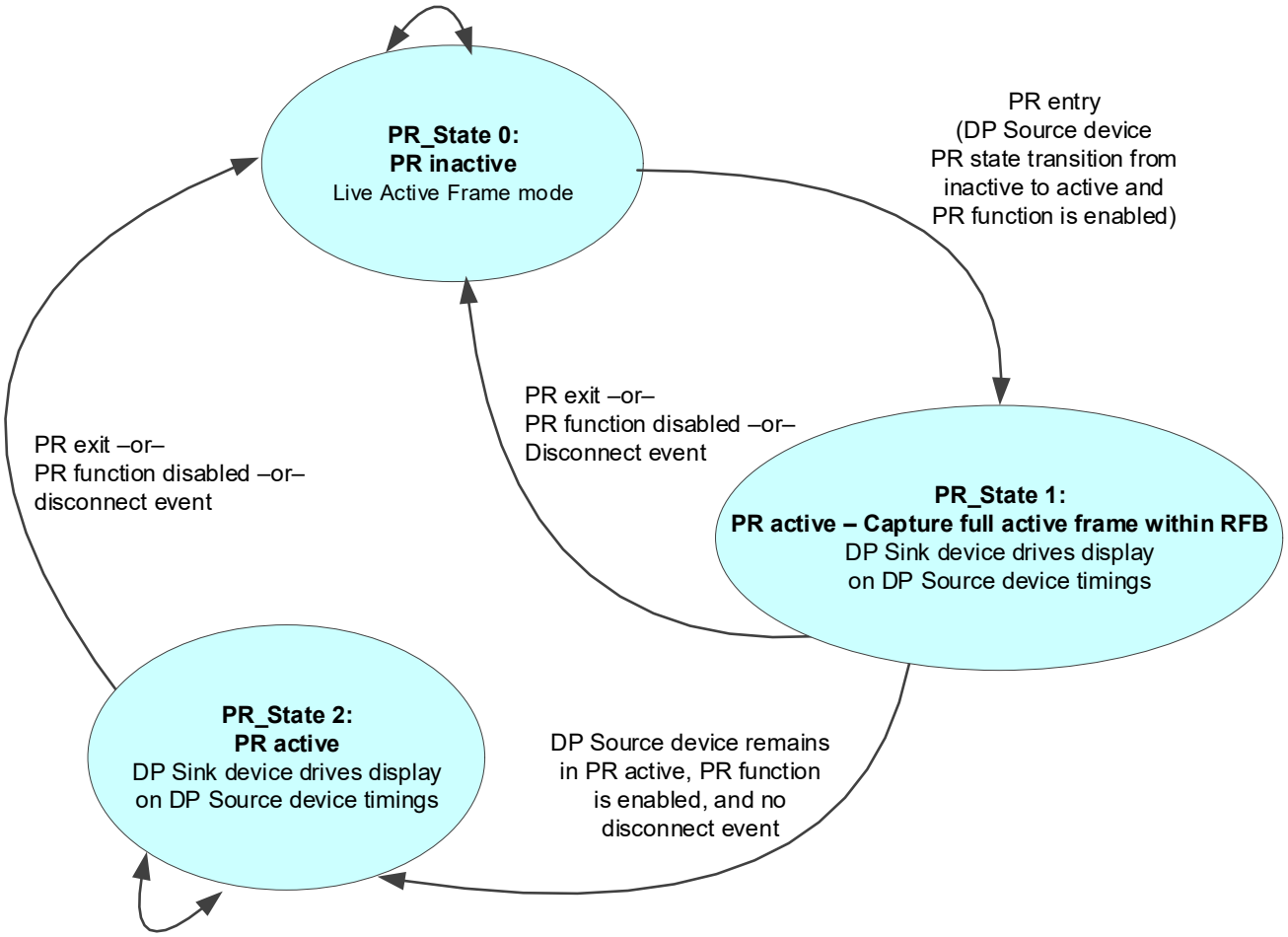


Figure 2-155: DP Sink Device Panel Replay Mode States

2.17.7 Panel Replay with no Live Active Frame Update

While in Panel Replay mode, the DP Source device shall continue to transmit valid MSA and video timing, through BS/BE control link symbols and VB-ID transmission. BS/BE control link symbols shall frame rate-governed micro-packets (or TUs) carrying data that shall be discarded by the DP Sink device. As long as the DP Sink device does not receive a VSC SDP with the SU_COORDINATES_VALID bit (DB1, bit 3) set to 1, the DP Sink device shall replay, from its own frame buffer, at the DP Source device's video timing. The DP Source device may **optionally** transmit a VSC SDP with the PR_STATE bit (DB1, bit 0) set to 1, and SU_COORDINATES_VALID bit cleared to 0, in a video frame with no pixel data update. The DP Sink device shall discard the colorimetry information (VSC SDP DB16 through DB18) that it received during the blanking period of a replayed video frame.

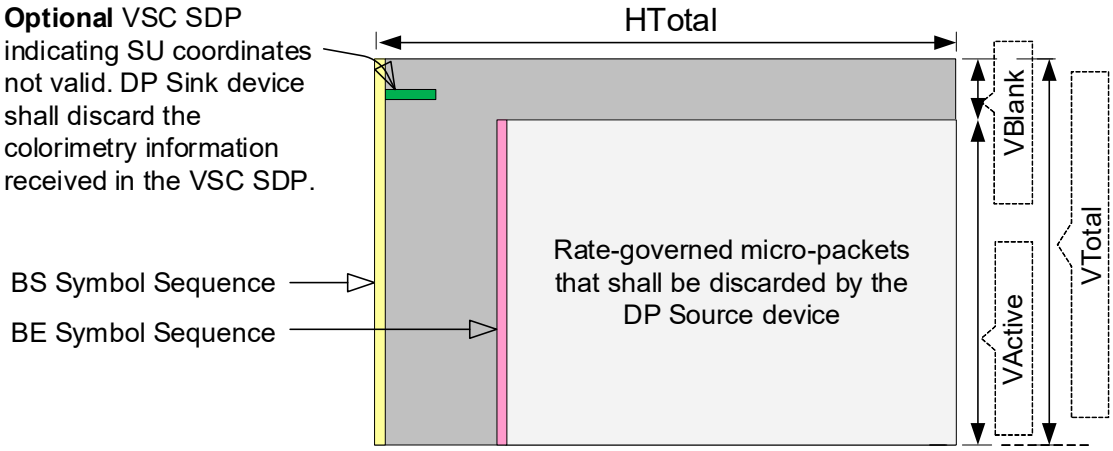


Figure 2-156: Panel Replay with no Live Active Frame Update

2.17.8 Full-screen Live Active Frame Update in Panel Replay Mode

In Panel Replay mode, when the entire frame needs to be updated, a DP Source device shall transmit an active frame with the new pixel data. The DP Source device shall transmit a VSC SDP with the PR_STATE and SU_COORDINATES_VALID bits (DB1, bits 0 and 3, respectively), and the X-coordinate, rectangle width, Y-coordinate, and rectangle height indicating the full-screen active frame. The DP Source device shall completely transmit the VSC SDP, carrying the Panel Replay information, in the VBlank or HBlank period before the first active line, at least 100ns prior to the BE of the SU region's first line. The DP Sink device shall display the active frame received at the DP Source device-set refresh rate, the same as in Live Active Frame mode. The DP Sink device shall also update its RFB with the active frame data received. The DP Source device may transmit a single update frame, –or– a burst of update frames. The active frame shall be available at the time that it needs to be rendered by the DP Sink device, the same as in Live Active Frame mode.

After transmitting the active frame, the DP Source device may **optionally** transmit a VSC SDP that carries the active frame's CRC. Should this occur, the VSC SDP shall be transmitted after the active frame, and before transmitting the next video frame's first BE. Following the VSC SDP carrying the CRC, the DP Source device may transmit a second VSC SDP, carrying the SU coordinates for the upcoming active frame, within the same VBlank period. The DP Source device may transmit the SU coordinates for the upcoming active frame and the CRC for the previous frame within the same VSC SDP.

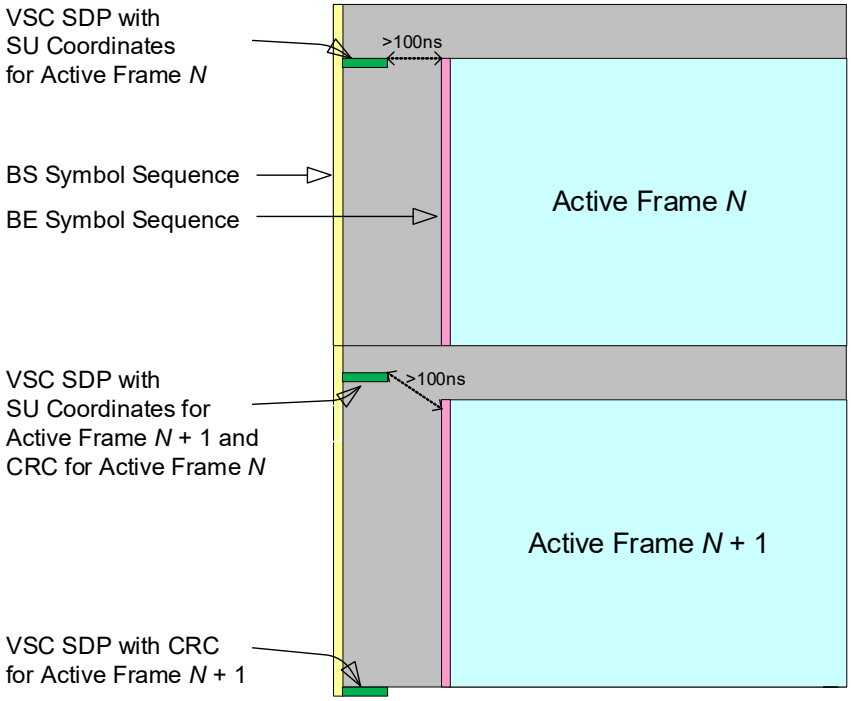


Figure 2-157: Full-screen Live Active Frame Update in Panel Replay Mode

2.17.9 Selective Update in Panel Replay Mode

A modified region within a frame is referred to as a "selective update region" (SU region). During Capability discovery and configuration, a DP Source device may discover the SU capability of a DP Sink device by reading the Selective Update Support bit in the PANEL REPLAY CAPABILITY SUPPORTED register (DPCD Address 000B0h, bit 1) as being set to 1. During Panel Replay mode configuration, the DP Source device may enable SU in an SU-capable DP Sink device by setting the Selective Update Enable bit to 1, and then enabling Panel Replay mode by setting the Source Device Enables Panel Replay Mode in Sink Device bit in the PANEL REPLAY ENABLE AND CONFIGURATION register (DPCD Address 001B0h, bits 6 and 0, respectively) to 1.

The DP Source device may transmit one or multiple SU regions within a video frame. The full-screen active frame displayed by the DP Sink device shall be a combination of SU region(s) and replay pixels that are read from the DP Sink device's local RFB. The DP Sink device shall update its RFB with the SU pixel data received.

The DP Sink device shall discard data received from outside the SU region. The DP Sink device shall display the frame at the DP Source device-set refresh rate for that video frame, with no delay. When DSC is enabled, the SU region's width shall be equal to an integer multiple number of contiguous slices, and the SU region's height shall be equal to an integer multiple number of slices. An SU region shall be transmitted at the time the region's data would normally be rendered by the DP Sink device.

For each SU region, the DP Source device shall transmit a VSC SDP with its PR_STATE and SU_COORDINATES_VALID bits (DB1, bits 0 and 3, respectively) set to 1. The X-coordinate, rectangle width, Y-coordinate, and rectangle height shall indicate the SU region's position and size within the active frame. The DP Source device shall completely transmit the VSC SDP in the blanking period at least 100ns prior to the SU region's first pixel.

After transmitting the active region, the DP Source device may **optionally** transmit a VSC SDP that carries the active region's CRC. Should this occur, the VSC SDP shall be transmitted after the active region, and before transmitting the next video frame's first BE. The CRC shall be generated by accumulating the pixels from all the SU regions within the frame. Dummy data that is located between the SU regions shall **not** be included in the CRC generation. If the DP Source device transmits a second VSC SDP within the same VBlank period or before the next SU region, the second VSC SDP shall also contain a valid CRC.

The DP Source device shall transmit one VSC SDP per SU region with the SU_COORDINATES_VALID bit set to 1 before transmitting the SU region's active pixels. During or after transmitting an SU region, the DP Source device may transmit a second VSC SDP within the HBlank period that carries the SU coordinates of the next SU region that is to be transmitted. After transmitting all the SU regions within a frame, the DP Source device may transmit a VSC SDP that carries the CRC (indicated by the CRC_VALID bit (DB1, bit 2) being set to 1) during the next video frame's VBlank period. The CRC shall be generated by accumulating the transmitted pixels from all the SU regions within the frame. Dummy data between SU regions shall **not** be included in the CRC generation. During the VBlank period, within the same VSC SDP, the DP Source device may transmit the SU coordinates of the first region to be transmitted in the upcoming frame and the CRC for the previous frame.

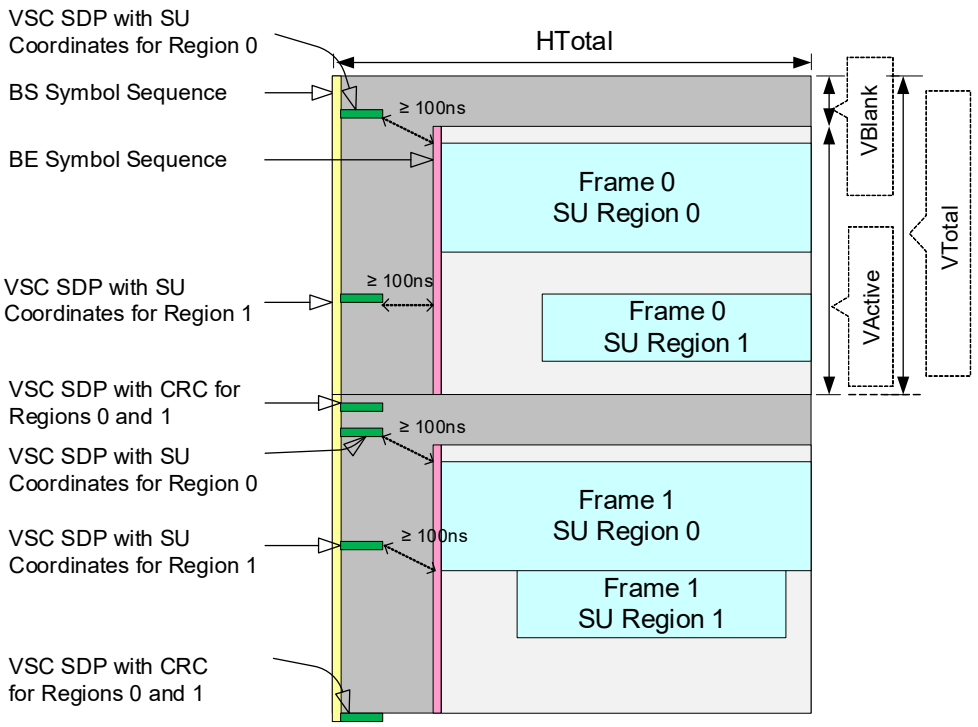


Figure 2-158: Panel Replay with Selective Update

2.17.10 Data Integrity and RFB Storage Error Check and Corrective Action

A DP Source device may **optionally** transmit the active frame/SU region's CRC in the VSC SDP for Panel Replay in which it sets its CRC_VALID bit (DB1, bit 2) to 1. After receiving this SDP, a DP Sink device shall compare the CRCs received from the DP Source device on the Main-Link with internally generated CRCs, and then update the ACTIVE FRAME CRC ERROR bit in the PANEL REPLAY ERROR STATUS register (DPCD Address 02020h, bit 0).

The DP Sink device shall indicate an RFB Storage error by setting the RFB STORAGE ERROR bit in the PANEL REPLAY ERROR STATUS register (DPCD Address 02020h, bit 1). The method that is used to generate the RFB Storage error is implementation-specific.

The DP Source device may **optionally** set the following PANEL REPLAY ENABLE AND CONFIGURATION register (DPCD Address 001B0h) bits to 1 for error checking:

- **IRQ_HPD with Active Frame CRC Errors bit (bit 5)** – When set, indicates to the DP Sink device to generate an IRQ_HPD when an Active Frame CRC mismatch occurs
- **IRQ_HPD with RFB Storage Errors bit (bit 4)** – When set, indicates to the DP Sink device to generate an IRQ_HPD when an RFB Storage error occurs

A SYNC_EVENT_NOTIFY message transaction shall be used for Active Frame CRC and RFB Storage error notification in a multi-stream topology. (See Section 2.14.9.14 for details regarding the SYNC_EVENT_NOTIFY message transaction for PR error notification.) When to read the PANEL REPLAY ERROR STATUS register is a DP Source device implementation-specific. After it detects an error, the DP Source device can take implementation-specific corrective action.

2.17.11 DPCD Registers Used for Panel Replay

Table 2-235 lists the DPCD registers that are used for Panel Replay support. (For complete register descriptions, see Table 2-183, Table 2-184, and Table 2-192).

Table 2-235: DPCD Registers Used for Panel Replay

Type	DPCD Address	Register
Capability	000B0h	PANEL REPLAY CAPABILITY SUPPORTED
	000B1h	PANEL REPLAY CAPABILITY
	000B2h and 000B3h	PANEL REPLAY SELECTIVE UPDATE X GRANULARITY CAPABILITY
	000B4h	PANEL REPLAY SELECTIVE UPDATE Y GRANULARITY CAPABILITY
Configuration	001B0h	PANEL REPLAY ENABLE AND CONFIGURATION
Status	02004h	DEVICE_SERVICE_IRQ_VECTOR_ESI1 The PANEL_REPLAY_ERROR_STATUS bit (bit 3) is used.
	02020h	PANEL REPLAY ERROR STATUS
	02021h	SU/PR EVENT STATUS INDICATOR
	02022h	SINK DEVICE PANEL REPLAY STATUS
	02024h	DEBUG 1_LAST RECEIVED VSC SDP CARRYING PANEL REPLAY INFORMATION

3 PHY Layer Specifications

3.1 Introduction

The DP PHY Layer specified the physical properties of a direct connection between a port on an upstream device (i.e., an AV output port on a DP Source or Branch device) and a port on a downstream device (i.e., an AV input port on a DP Sink or Branch device). The DP PHY Layer de-couples the data transmission electrical specifications from the DP Link Layer, thereby allowing modularity for future Link Layer-specific design enhancements and also future changes to the transport media type, such as the use of Hybrid devices. The PHY Layer is further sub-divided into logical and electrical functional sub-blocks, as illustrated in Figure 3-1.

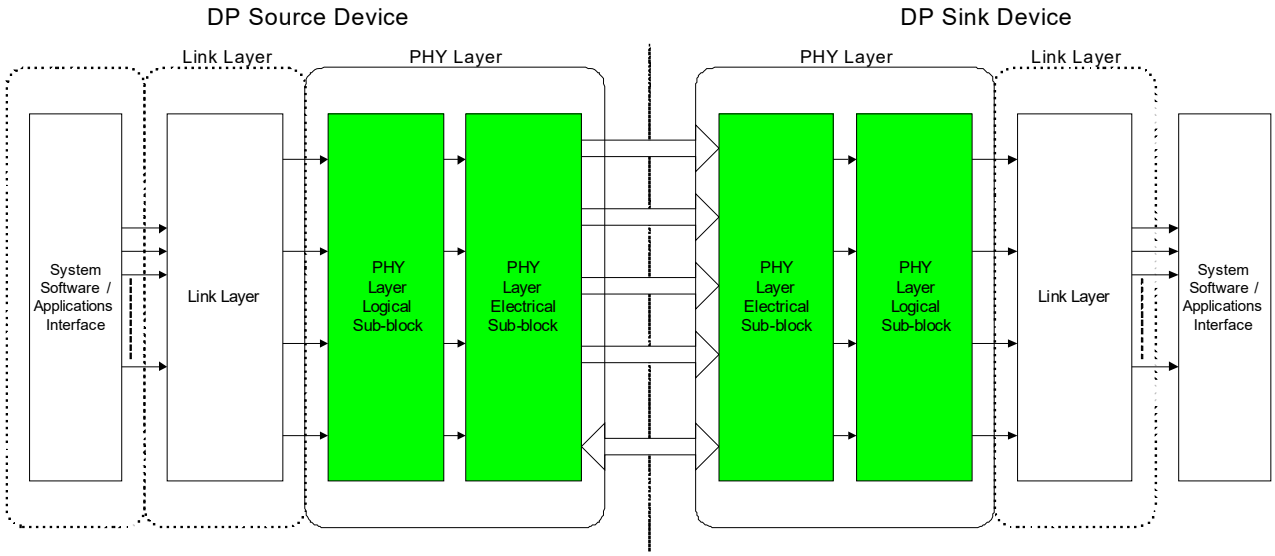


Figure 3-1: DP PHY Layer

3.1.1 PHY Layer Functions

This section summarizes the functionalities of the DP PHY Layer.

3.1.1.1 Hot Plug/Unplug Detection Circuitry

The PHY Layer shall detect Hot Plug/Unplug events and notify the Link Layer of the events, as follows:

- **Logical Sub-block** – Notifies Hot Plug/Unplug events to the upper layer
- **Electrical Sub-block** – Detects a Hot Plug/Unplug event

3.1.1.2 AUX_CH Circuitry

The PHY Layer provides the half-duplex, bidirectional AUX_CH for services such as Link Configuration or Maintenance and DisplayID or legacy EDID access, using 1-Mbps Manchester-II coding.

- Logical Sub-block
  - Supports Manchester-II coding
  - Generates and detects Start/Stop condition, and locks to the synchronization pattern for the appropriate encoding
  - Encoding and decoding of data for the appropriate encoding
- Electrical Sub-block
  - Consists of a single differential pair, both ends of the link equipped with driver and receiver for half-duplex bidirectional operation
    - Driving end
      - Drives a doubly terminated, AC-coupled differential pair in a manner compliant with the AUX_CH electrical specification for encoding
    - Receiving end
      - Receives the incoming differential signal and extracts the data

3.1.1.3 Main-Link Circuitry

The PHY Layer provides the unidirectional Main-Link for the transport of isochronous streams and secondary-data packets.

- Logical Sub-block
  - Scrambling and de-scrambling
  - Channel encoding/decoding
  - Reed-Solomon (RS) FEC encoding/decoding
  - Serialization and de-serialization
  - Link Training and Link Status Monitor
  - Adjusts link rate, spreading, drive current level, and pre-emphasis level, as needed
    - Link Quality Measurement for testability
- Electrical Sub-block
  - Consists of up to four differential pairs
  - Transmitter
    - Drives doubly terminated, AC-coupled differential pairs in a manner compliant with the Main-Link Transmitter electrical specification
  - Receiver
    - Receives the incoming differential signals and extract the data with its link CDR (clock and data recovery) circuits

3.1.2 Link-PHY Layer Interface Signals

This section summarizes the interface signals between the Link and PHY Layers.

3.1.2.1 Main-Link

The interface signal for the Main-Link between the Link and PHY Layers consists of either an 8- or 32-bit data signal (for 8b/10b or 128b/132b channel coding, respectively) per Main-Link lane, plus a 1-bit control signal. The control signal is used for special symbols such as BS and BE (Blank Start and Blank End, respectively) for framing an isochronous data stream. Use of the 1-bit control signal is implementation-specific and is beyond the scope of this Standard.

3.1.2.2 AUX_CH

The AUX_CH's interface signal between the Link and PHY Layers shall consist of an 8-bit data signal plus a 1-bit control signal. The control signal shall be used to indicate the AUX transaction's Start or Stop. Use of the 1-bit control signal to indicate Start/Stop conditions is implementation-specific and is beyond the scope of this Standard.

3.1.2.3 Hot Plug/Unplug Detection

Hot Plug/Unplug Detection circuitry provides for the Hot Plug/Unplug Status signal to Link Layer.

The de-bouncing timer shall belong to the Link Layer and **not** to the PHY Layer.

3.1.3 PHY Layer and Link Media Interface Signals

This section summarizes the interface signals between the PHY Layer and Link Media consisting of PCB, connector, and cable. (Connector and cable may be absent for certain link configurations, such as a chip-to-chip connection.)

3.1.3.1 DP_PWR/DP_PWR_RETURN

A DP Source, Sink, or locally self-powered Branch device shall provide power on the DP_PWR pin of the box-to-box DP connector. Branch devices that are not self-powered[a] need not supply DP_PWR. Power provided at DP_PWR is intended to power consumer devices that are connected directly to the power provider's connector.

3.1.3.2 Hot Plug/Unplug Detection

One signal, Hot Plug Detect (HPD), is used by a device (an upstream device) to detect that a downstream-facing port (DFP) on the device has been connected to another device (the downstream device). HPD may be implemented for an embedded link configuration. For a Hot Plug event to be detected, at least trickle power shall be present in both the upstream and downstream devices.

Downstream devices shall be ready for an AUX transaction whenever the devices assert (drive high) the HPD signal. Even in power-saving state(s) (see Section 5.2.5), a downstream device that keeps its HPD signal asserted shall be able to detect the presence of an AUX_CH differential signal input. The downstream device shall exit the power-saving state within 1ms of the differential signal being detected.

---

a. *Self-powered capable Branch devices that are physically disconnected from their independent power source are effectively "not self-powered," and need not supply DP_PWR.*

3.1.3.3 AUX_CH

The AUX_CH is composed of one differential pair, AUX_CH_P and AUX_CH_N.

For the AUX_CH to be functional, at least trickle power shall be present in both the upstream and downstream devices.

A downstream device that supports the optional upstream device detection feature shall monitor the DC voltage of the AUX_CH lines between the AC-coupling capacitors and its upstream connector.

3.1.3.4 Main-Link

The Main-Link is composed of up to four differential pairs:

- ML_Lane_0_P and ML_Lane_0_N
- ML_Lane_1_P and ML_Lane_1_N
- ML_Lane_2_P and ML_Lane_2_N
- ML_Lane_3_P and ML_Lane_3_N

Both the upstream and downstream device shall be fully powered for the Main-Link to be functional.

3.1.4 Main-Link Compliance Configurations

Updated in *DP v2.0*.

Table 3-1 describes the Main-Link PHY Layer compliance test points. For the Main-Link PHY Layer compliance configuration, see *PHY CTS*.

Table 3-1: Main-Link PHY Layer Compliance Test Points

Test Point	Definition
TP1	Located at the transmitter device's pins.
TP2	Located at the test interface on a Test Point Access fixture, as close as possible to the DP-mated connection to a DP Source device.
TP2'	RX JTOL signal injection point for DUT with Plug connector.
TP2_CTLE	RX Jitter Tolerance calibration and testing interface point of DUT with plug.
TP3	Located at the test interface on a Test Point Access fixture, as close as possible to the DP-mated connection to a DP Sink device.
TP3'	Used for signal injection point to a DP Sink device (receptacle DUT).
TP3_EQ	TP3 using a defined cable model with an equalizer applied. There are two defined cable models: • Worst-case cable model • Zero-length, zero-loss cable
TP3_CTLE	TP3 using a defined cable model with CTLE applied.
TP3_DFE	TP3 using a defined cable model with CTLE and DFE applied.
TP4	Located at the receiver's package pins.
TPRX	Located at the receiver IC's pads.
TPRX_CTLE	TPRX using a defined cable model and a defined DPRX device model with CTLE applied.
TPRX_DFE	TPRX using a defined cable model and a defined DPRX device model with CTLE and DFE applied.

3.1.5 Electrical Signal Definitions

The following definitions apply to both Main-Link and AUX_CH signaling.

3.1.5.1 Differential Voltage for up to HBR3 Bit Rate

A differential signal is defined by taking the voltage difference between two conductors. In this Standard, a differential signal or differential pair is composed of a voltage on a positive conductor, V_{D+}, and a negative conductor, V_{D-}. The differential voltage (V_{DIFF}) is defined as the difference of the positive and negative conductor voltages ($V_{DIFF} = V_{D+} - V_{D-}$), as illustrated in Figure 3-2.

The Common Mode Voltage (V_{CM}) is defined as the average or mean voltage present on the same differential pair ($V_{CM} = [V_{D+} + V_{D-}] / 2$).

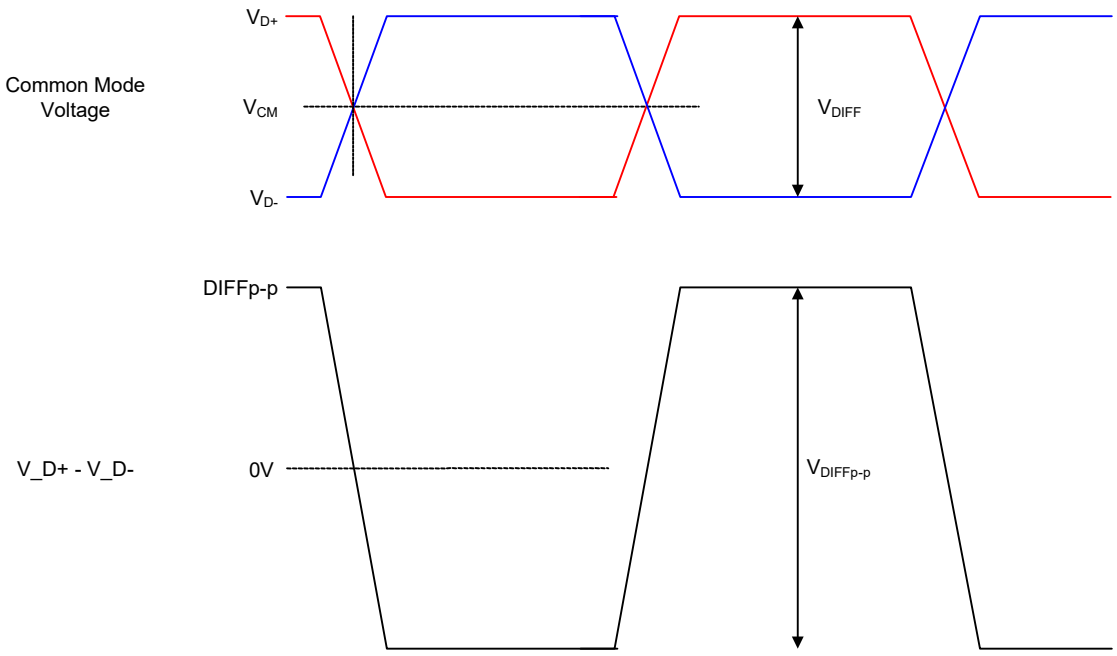


Figure 3-2: Differential Voltage and Differential Voltage Peak-to-peak Definition

This Standard's electrical specifications often refer to peak-to-peak measurements or peak measurements, which are defined by the following equations:

- Symmetrical Differential Voltage Swing

  $$V_{DIFFp\text{-}p} = (2 \times max\,|V_{D+} - V_{D-}|)$$

- Asymmetrical Differential Voltage Swing

  $$V_{DIFFp\text{-}p} = (max\,|V_{D+} - V_{D-}|\ \{V_{D+} > V_{D-}\} + max\,|V_{D+} - V_{D-}|\ \{V_{D+} < V_{D-}\})$$

- Common-Mode Voltage

  $$V_{CMp} = (max\,|V_{D+} + V_{D-}|\ / 2)$$

3.1.5.2 Voltage Swing and Pre-emphasis for up to HBR3 Bit Rate

The Main-Link's DPTX specification allows four differential peak-peak voltage swing levels, and four pre-emphasis levels.

Certain combinations of voltage swing and pre-emphasis levels result in differential peak-to-peak voltages that are beyond the allowable range, and thus are **not** allowed. Table 3-2 defines the allowable combinations of voltage swing and TX emphasis levels, by bit rate.

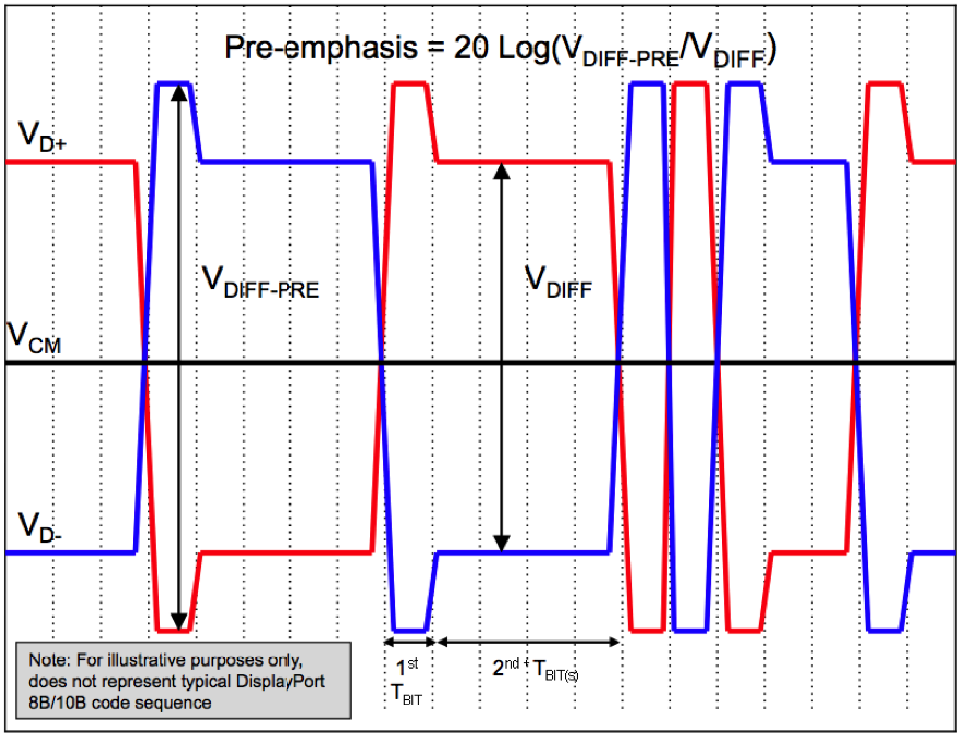
Table 3-2: Allowed Voltage Swing and TX Emphasis Level Combinations

Bit Rate	Voltage Swing Level	TX Emphasis Level			
		0	1	2	3
HBR3/HBR2[a]	0	Shall be supported	Shall be supported	Shall be supported	Shall be supported
	1	Shall be supported	Shall be supported	Shall be supported	Not allowed
	2	Shall be supported	Shall be supported	Not allowed	Not allowed
	3	Shall be supported	Not allowed	Not allowed	Not allowed
HBR/RBR[b]	0	Shall be supported	Shall be supported	Shall be supported	May be supported
	1	Shall be supported	Shall be supported	Shall be supported	Not allowed
	2	Shall be supported	Shall be supported	Not allowed	Not allowed
	3	May be supported	Not allowed	Not allowed	Not allowed

a. ***HBR3 and HBR2*** *– See Table 3-39 for DP Main-Link TX TP2 parameters.*
b. ***HBR and RBR*** *– See Table 3-40 for DP Main-Link TX TP2 parameters.*

Note: *Pre-emphasis, as used in this Standard, is defined as 20 multiplied by $\log_{10}$ of the ratio of the amplitude for the first T_{BIT} immediately following a transition divided by the amplitude for the subsequent bits until the next transition ($20 \times \log (V_{DIFF\text{-}PRE} / V_{DIFF})$).*

Figure 3-3 illustrates an example of pre-emphasis. When there are consecutive single bits of opposite values being transmitted, all the consecutive bit transitions shall be pre-emphasized to the voltage swing of $V_{DIFF-PRE}$.



Note: *For illustrative purposes only; does* ***not*** *represent typical DP 8b/10b code sequence.*

Figure 3-3: Pre-emphasis Example

where:

- $V_{DIFF-PRE\_v\_p}$ indicates the $V_{DIFF-PRE}$ measured at voltage level *v* and pre-emphasis level *p* (i.e., the voltage measured on a transition bit)
- $V_{DIFF\_v\_p}$ indicates the V_{DIFF} measured at voltage level *v* and pre-emphasis level *p* (i.e., the voltage measured on the non-transition bits)
- T_{BIT} indicates the time that is taken to transmit a single bit

$V_{DIFF-PRE\_2\_0}$ and $V_{DIFF\_2\_0}$ are measured and used as a baseline for the needs of all other $V_{DIFF-PRE\_v\_p}$ and $V_{DIFF\_v\_p}$ values.

3.1.6 8b/10b Scrambling

Note: *128b/132b channel coding, including scrambling, is defined in Section 3.5.2.*

Scrambling of the Main-Link data is performed for EMI reduction prior to 8b/10b encoding on the transmitter. De-scrambling of the data symbols is performed following 8b/10b decoding at the receiver. Scrambling should result in an approximate 7-dB reduction in peak spectrum.

Each of the Main-Link lanes is scrambled and de-scrambled independently, each with a 16-bit internal LFSR, as follows:

$$G(x) = x^{16} + x^5 + x^4 + x^3 + 1$$

Each byte of data is scrambled/de-scrambled with the most significant 8 bits of the LFSR in reverse bit order:

{D'[7], D'[6], D'[5], D'[4], D'[3], D'[2], D'[1], D'[0]}
= {D[7], D[6], D[5], D[4], D[3], D[2], D[1], D[0]} ^ {LFSR[8]. LFSR[9], LFSR[10], LFSR[11], LFSR[12], LFSR[13], LFSR[14, LFSR[15]}

In Single-Stream Transport (SST) mode, the UFP shall replace every 512th BS BF BF BS or BS CP CP BS symbol sequence with an SR BF BF SR or SR CP CP SR symbol sequence. In Multi-Stream Transport (MST) mode, the UFP shall transmit an SR symbol as the MTPH every 1024 Multi-stream packets (thus, an SR symbol is transmitted every 65536 symbols). The SR symbol or SR BF BF SR or SR CP CP SR symbol sequence is used to reset the LFSR to FFFFh (or FFFEh for eDP Alternate Scrambler Seed), so that the first byte of data following the scrambler reset is scrambled/de-scrambled with FFh. The scrambler is then advanced to contain E817h (or E917h for eDP Alternate Scrambler Seed).

The data scrambling rules shall be as follows:

- LFSR advances on all symbols, both data symbols (D), and special symbols (K).
- Special symbols (K) are not scrambled.
- Data symbols, including “fill data” are scrambled. Fill data is normally zero before scrambling.
- Multi-stream indexed control link symbols are scrambled before being encoded as special symbols (K).

Scrambling shall be disabled during Link Training and Recovered Link Clock Quality Measurement.

Receivers should implement appropriate robustness to ensure that bit errors that generate a false SR symbol do not result in the de-scrambler LFSR being reset.

A C code reference implementation of the scrambler/de-scrambler is provided in Appendix E. This includes an implementation of methods that should be used for robust detection of scrambler reset.

3.1.7 8b/10b Symbol Coding and Serialization/De-serialization

Note: *128b/132b channel coding, including scrambling, is defined in Section 3.5.2.*

Updated in *DP v1.4a*.

The DP interface uses 8b/10b[a] channel coding to provide symbol-level DC balancing. It also provides high transition density for link clock phase tracking at the receiver. With 8b/10b channel coding, 8-bit data characters are treated as three bits and five bits mapped onto a 4-bit code group and a 6-bit code group, respectively.

The control bit, in conjunction with the data character, is used to identify when to encode one of the Special Symbols included in the 8b/10b transmission code.

Symbols are referred to using the notation *Zxx.y*, where:

- *Z* = Control bit for the symbol
  - D = Data symbol
  - K = Special symbol
- *xx* = Least significant five bits of the 8-bit coded character (EDCBA)
- *y* = Most significant three bits of the 8-bit coded character (HGF)

Mapping of the 8-bit characters to 10-bit symbols is performed according to *ANSI INCITS 230* rules. For each 8-bit character and control bit, there are different 10-bit sequences that are used, depending on the current running disparity (RD). Under most conditions, choosing of the correct 10-bit symbol is automatically performed based on the current RD. However, whenever a specific 10-bit sequence is required in this Standard, it is referred to as follows:

- "*Zxx.y*+" for the 10-bit mapping that would be used when the current RD is positive (corresponding to the **RD +** values listed in *ANSI INCITS 230*, *Table 22* and *Table 23*). A *Zxx.y*+ character will have either five 0 bits and five 1 bits, –or– six 0 bits and four 1 bits.
- "*Zxx.y*-" for the 10-bit mapping that would be used when the current RD is negative (corresponding to the **RD -** values listed in *ANSI INCITS 230*, *Table 22* and *Table 23*). A *Zxx.y*- character will have either five 0 bits and five 1 bits, –or– four 0 bits and six 1 bits.

a. 8b/10b channel coding is defined in ANSI INCITS 230.

As illustrated in Figure 3-4, ABCDE maps to abcdei and FGH maps to fghj.

After coding, the 8b/10b symbols are serialized so that the least significant bit (lsb) is transported first, and the most significant bit (msb) is transported last.

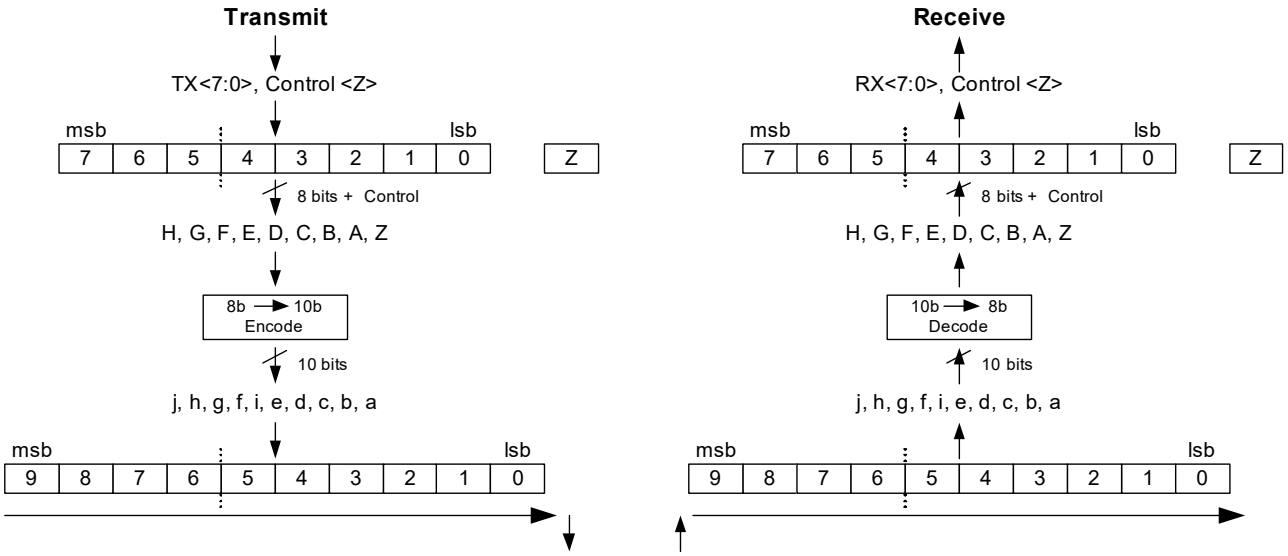


Figure 3-4: Character-to-Symbol Mapping

3.2 DP_PWR for Box-to-Box DP Connection

DP connectors on DP Source, Sink, and self-powered Branch devices have one power pin and one return current pin on the receptacle connector. This power shall be provided by the Source, Sink, or self-powered Branch device whenever DP output ports of those devices are enabled. Branch devices that are not self-powered[a] are allowed, which may not provide DP_PWR at its connectors.

The DP_PWR consumer shall be connected directly to the power provider's connector. The consumer may be a Branch Device (with or without an additional power source), an active cable assembly or Sink device with a permanently attached cable.

A downstream device with a permanently attached cable may provide DP_PWR on the plug connector's DP_PWR pin. The downstream device with an attached cable that is capable of providing DP_PWR on the plug connector shall verify whether a device that uses DP_PWR is connected to the plug connector. The DP_PWR output of a downstream device with a permanently attached cable may only be enabled after the downstream device has determined that a DP_PWR-using device is attached. The method that is used for detecting a DP_PWR-using device is described in Section 3.2.1.

The upstream device's DP_PWR pin's voltage shall be within the range of 2.89 to 3.6V (3.3V ±10% less fuse voltage drop = 0.076V). The minimum power available at the upstream DP_PWR pin shall be 1.5W. A downstream device that consumes more than 1.5W of power shall have means of getting power from an alternate power source.

The voltage on the DP_PWR pin of the downstream device shall be within the range of 2.89 to 3.6V, by default. The higher voltage settings listed in Table 3-3 are optionally available for the downstream DP_PWR pin, as declared in the *x*V_DP_PWR_CAP bits in the NORP & DP_PWR_VOLTAGE_CAP register (DPCD Address 00004h, bits 7:5). These higher voltage settings are enabled by an upstream device when the device sets the corresponding voltage's SET_DN_DEVICE_DP_PWR_*x*V bit in the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h, bits 7:5), by way of an AUX write transaction.

Upon detecting an upstream device disconnect event (which can be detected by monitoring the AUX_CH_P common mode voltage transitioning from a low-to-high level, a downstream DP device generating DP_PWR voltage higher than the default +2.89 to +3.6V shall reset its output voltage to the default setting. Box-to-box connector DP_PWR and RETURN pins shall support the maximum current rating of 0.65A.

a. *Self-powered capable Branch devices that are physically disconnected from their independent power source are effectively "not self-powered," and need not supply DP_PWR.*

Table 3-3: DP_PWR Specification for Box-to-Box DisplayPort Connection

Parameter	Min	Nominal	Max	Unit	Comment
Voltage Range for Upstream DP_PWR	2.89	3.3	3.6	V	
Voltage Range for downstream device DP_PWR	2.89	3.3	3.6	V	Default DP_PWR voltage value for a downstream device
	4.9	5.0	5.5	V	"5V setting" enabled through AUX transaction[a]
	10.8	12	13.2	V	"12V setting" enabled through AUX transaction[a]
	16.2	18	19.8	V	"18V setting" enabled through AUX transaction[a]
Noise voltage for downstream device DP_PWR			100	mV	Peak-to-peak
Power Capacity per Upstream DP_PWR pin	1.5			W	• Full-height PC add-in card with multiple upstream DP connectors shall power at least 3.0W per card • Half-height PC add-in card with multiple upstream DP connectors shall power at least 1.5W per card • Upstream DP connector on PC motherboard shall power 1.5W per connector, regardless of the number of connectors on the motherboard
Current drawn by a downstream device from upstream DP_PWR pin			0.5	A	
Power Capacity per downstream DP_PWR pin	1.5			W	3.3V (default) setting
	3.2			W	5V setting
	7.0			W	12V setting
	10.5			W	18V setting
Current drawn by an upstream device from Downstream DP_PWR pin			0.5	A	3.3V (default) setting
			0.65	A	5V/12V/18V setting

a. Self-powered capable Branch devices that are physically disconnected from their independent power source are effectively "not self-powered," and need not supply DP_PWR.

3.2.1 DP_PWR User Detection Method

Pins CONFIG1 and CONFIG2 of the box-to-box receptacle connector of upstream and downstream DP devices shall be weakly pulled down with resistors. CONFIG1 shall always use 1MΩ resistors. CONFIG2 shall always use a 5MΩ (or larger) resistor if the upstream device is a dual-mode device and supports HDMI. In other cases, CONFIG2 can use either a 1MΩ or larger resistor. For more information, see *DP Interoperability Guideline*, *Section 5.1.1*.

Those two pins of a DP device with an upstream function that uses power from DP_PWR shall be shorted by a ≤ 100Ω resistor.

A downstream device with a permanently attached cable that is capable of supplying power on the DP_PWR pin of the plug connector shall verify that pins CONFIG1 and CONFIG2 are shorted before enabling its DP_PWR output.

To detect the presence of a DP_PWR User, a downstream device with a permanently attached cable shall provide a probe power to Pin CONFIG2. If the Pin CONFIG1 voltage follows the probe power voltage applied to Pin CONFIG2, a DP_PWR User is present.

There shall be a group of cable adapters that pulls up Pin CONFIG1. Those cable adapters with DP receptacle connectors that pull up Pin CONFIG1 shall not be a DP_PWR User. When a downstream device with a permanently attached cable detects H level on Pin CONFIG1 before providing a probe power to Pin CONFIG2, it determines that the attached cable adapter is not a DP_PWR User.

3.2.2 DP_PWR Wire

A standard DP cable shall have no wire for the DP_PWR pin.

Only captive cables supplied with cable powered Branch devices or cables permanently attached to downstream devices or resizing adapters or extension cables are permitted to have the wire for DP_PWR. These captive/attached/resizing/extension cables shall have a full-size or mDP plug connector (as specified in Section 4.2.1) on one end only. The other end shall either be permanently attached or have a DP receptacle connector or a custom connector.

3.2.3 Inrush Energy

DP devices that consume DP_PWR shall limit the inrush energy during Hot Plug to 0.4mJ, to be measured over the time period that the inrush exceeds 0.6A, and measured at the nominal voltage for a given voltage level +10% (the maximum voltage for DP_PWR). The peak current should be limited to ≤ 13.5A during the inrush energy window. SCALE_FACT is equal to:

DEFAULT_VOLTAGE_SETTING / SELECTED_VOLTAGE_SETTING

For example, the SCALE_FACTOR is 1 when the 3.3V setting is selected, and 0.66 when the 5V setting is selected.

3.2.4 Voltage Droop

DP devices that provide power at DP_PWR pin should have sufficient bypass capacitance per DP connector to be able to charge 56uF of low ESR capacitance plus 7.2Ω constant load across DP_PWR on hot plug of this load. Power provider devices should exhibit no obvious system failure and should ensure that any resulting voltage droop is no more than 10% of the DP_PWR supply voltage on any other DP connectors (measured at the connector) on the system on hot plug of this load. Additionally, the device should, under the same condition, be able to support a momentary 12-A outrush peak current.

3.2.4.1 DP_PWR Loss and Recovery on Branch Device

If a Branch device that controls the HPD signal loses its ability to function normally (such as may happen due to an momentary out-of-spec droop in DP_PWR), before resuming normal operation, the device should either de-assert or disconnect its HPD signal (leaving the HPD signal terminated to GND, as per the HPD Downstream Device Termination mandate) until the device has fully recovered and can resume normal operation.

If and when the device resumes normal operation, the device should behave as if it is coming out of reset or initial power-on with its DPCD registers set accordingly. Before resuming normal operation, the HPD signal should be de-asserted for a minimum of HPD_Timeout and then re-asserted after the device returns to normal functionality and can receive AUX communications.

3.2.5 Over-current Protection

User accessible powered connectors shall implement over-current protection for safety and regulatory reasons. Optional detection of an over-current condition and reporting of this condition to the system software is implementation-specific.

The preset trip limit shall not exceed 3A at the upstream device connector DP_PWR pin and 1.5A at the downstream device connector DP_PWR pin. Limit shall be above allowable current transients to avoid false trips. An over-current protection device shall be resettable without user mechanical intervention.

A DP device with multiple DP_PWR outputs is permitted to use a single over-current protection device to protect all outputs. For devices that use a single over-current protection device, the preset trip limit shall be 3A per device with upstream device connectors and 1.5A per device with downstream device connectors. There is no mandate to maintain the DP_PWR specification on one port in the presence of a fault condition on another port.

3.3 Hot Plug/Unplug Detect Circuitry

The downstream DP device asserts the HPD signal whenever the downstream device is connected to either its main power supply or trickle power. Table 3-4 defines the HPD signal specification.

Table 3-4: Hot Plug Detect Signal Specification

Parameter	Minimum	Nominal	Maximum	Unit	Comment
HPD Voltage	2.25		3.6	V	HPD signal to be driven by the downstream device.
Hot Plug Detection Threshold	2.0			V	HPD signal to be detected by the upstream device.
Hot Unplug Detection Threshold			0.8	V	
HPD Upstream Device Termination	100			kΩ	Upstream device shall pull down its HPD input with a ≥ 100kΩ resistor.
HPD Downstream Device Termination	100			kΩ	When a downstream device is off, it shall pull down its HPD output with a ≥ 100kΩ resistor.
IRQ_HPD Pulse Width Driven by Downstream Device	0.5		1.0	ms	Downstream device generates a low-going pulse within this range for IRQ (interrupt request) to the upstream device.
IRQ_HPD Pulse/ Glitch Detection Threshold for Upstream Device	0.25			ms	When the HPD pulse width is narrower than this threshold, the upstream device shall ignore the pulse as a glitch.
IRQ_HPD Minimum Spacing	2.0			ms	Minimum time after asserting HPD at the end of IRQ_HPD before de-asserting HPD at the start of the next IRQ_HPD.

Table 3-4: Hot Plug Detect Signal Specification (Continued)

Parameter	Minimum	Nominal	Maximum	Unit	Comment
IRQ_HPD Pulse/ Hot Unplug Event Detection Threshold for Upstream Device	2.0			ms	When the HPD pulse width is wider than this threshold, it is likely to be an actual cable unplug/re-plug event. After detecting HPD high, the upstream device shall read the Link/Sink Capability field of the DPCD before initiating link training. When the HPD pulse width is narrower than this threshold but wider than the Glitch Detection Threshold minimum listed in this table, the upstream device shall first read the DPCD registers (either Link/Sink Device Status field registers at DPCD Addresses 00200h through 00205h, –or– ESI registers at DPCD Addresses 02002h through 02005h, and 0200Ch through 0200Fh; an MST device shall read the ESI registers) listed below, and then take corrective action: • SINK_COUNT or SINK_COUNT_ESI register (DPCD Address 00200h or 02002h, respectively) • DEVICE_SERVICE_IRQ_VECTOR or DEVICE_SERVICE_IRQ_VECTOR_ESI0 register (DPCD Address 00201h or 02003h, respectively) • LANE*x_y*_STATUS register(s) (DPCD Address(es) 00202h and 00203h) or LANE*x_y*_STATUS_ESI register(s) (DPCD Address(es) 0200Ch and 0200Dh) • LANE_ALIGN_STATUS_UPDATED or LANE_ALIGN_STATUS_UPDATED_ESI register (DPCD Address 00204h or 0200Eh, respectively) • SINK_STATUS or SINK_STATUS_ESI register (DPCD Address 00205h or 0200Fh, respectively) • DEVICE_SERVICE_IRQ_VECTOR_ESI1 register (DPCD Address 02004h) • LINK_SERVICE_IRQ_VECTOR_ESI0 register (DPCD Address 02005h) On device reset, a downstream device shall de-assert the HPD signal for a duration that is longer than the minimum IRQ_HPD Pulse/Hot Unplug Event Detection Threshold for Upstream Device.

The upstream device shall monitor the HPD pin's voltage level. Transistor-transistor logic (TTL) levels shall be used for the detection.

The downstream device may detect the upstream device's presence by monitoring the AUX_CH line DC voltage levels. For a detachable downstream device whose power is not provided by the upstream device's DP_PWR, the upstream device detection feature shall be supported.

Upstream implementations should implement HPD signal de-bouncing on an external connection. A period of 100ms should be used for detecting an HPD connect event (i.e., the event, "HPD high," is confirmed only after HPD has been continuously asserted for 100ms). Care should be taken to not implement de-bouncing on an IRQ_HPD and on a downstream device-generated pair of HPD disconnect/reconnect events (typically HPD shall be de-asserted for more than 2ms, but less than 100ms in this case). To cover these cases, HPD de-bounce should be implemented only after HPD low has been detected for 100ms. Timing mandates in this Standard that are related to the detection of HPD high are to be interpreted as applying from the completion of an implementation-specific de-bounce period.

If the downstream device has been placed in a low-power state (see Section 5.1.5) but detects an event that it needs to notify to the upstream device, the downstream device asserts IRQ_HPD. The upstream device shall attempt to perform AUX transactions to wake the downstream device. It is possible for the upstream device to already be making AUX transactions to wake up the downstream device. In this case, the upstream device shall complete the actions that it was already executing (e.g., waking the link and initiating link training), and then perform appropriate DPCD register reads to determine what caused the IRQ_HPD.

3.4 AUX_CH

The AUX_CH is a half-duplex, bidirectional channel consisting of one differential pair, as illustrated in Figure 3-5, supporting the bit rate of approximately 1Mbps.

Note: *The 50-Ω termination resistors may be integrated on-chip. The AUX_CH is doubly terminated with 50-Ω termination resistors on both ends, and AC-coupled on the DPTX end.*

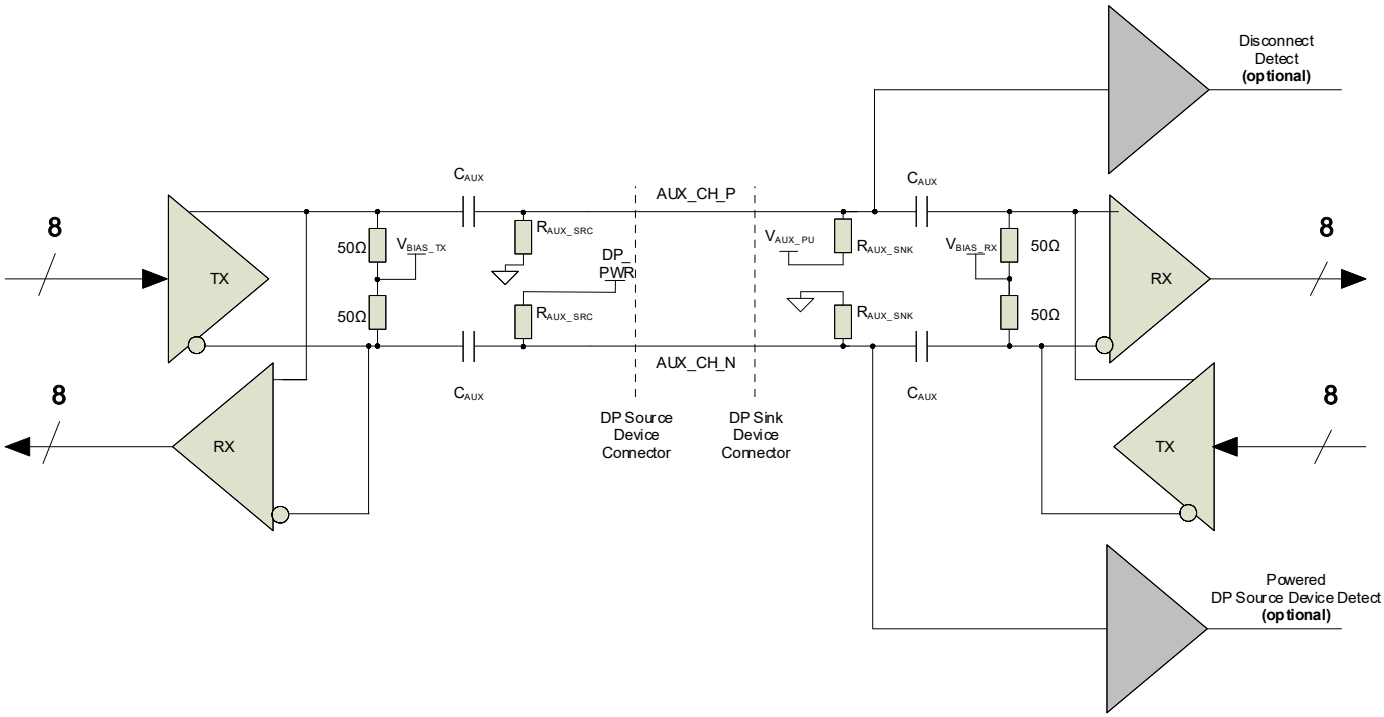


Figure 3-5: AUX_CH Differential Pair

The upstream DP device shall weakly pull down the AUX_CH_P line to GND and weakly pull up the AUX_CH_N line to DP_PWR, each with an R_{AUX_SRC} resistor between the AC-coupling capacitor and the upstream device connector to enable detection of the upstream DP device and powered upstream DP device by the downstream device.

All downstream devices shall have AC-coupling capacitors, regardless of whether they implement upstream DP device detection. The downstream devices shall weakly pull up the AUX_CH_P line and weakly pull down the AUX_CH_N line with R_{AUX_SNK} resistors between the downstream device connector and the AC-coupling capacitors.

A downstream device may implement the ability to detect whether an upstream DP device is physically connected by examining the common mode level on the capacitively coupled AUX_CH_P line. AUX_CH_N line DC voltage that is less than or equal to the $V_{AUX\_SRC\_CONN}$ level indicates that an upstream DP device is connected. When implementing connected upstream device detection, the downstream device shall use the $V_{AUX\_SRC\_CONN}$ negative threshold after filtering for detecting the connected upstream device. Filtering shall be used to avoid false disconnect detects during AUX signaling.

A downstream device may implement the ability to detect whether an upstream DP device is connected and powered by examining the common mode level on the capacitively coupled AUX_CH_N line. AUX_CH_N line DC voltage that is greater than or equal to the $V_{AUX\_SRC\_PWRD}$ level indicates that a powered upstream DP device is connected. When implementing powered upstream device detection, the downstream device shall use the $V_{AUX\_SRC\_PWRD}$ threshold after filtering for detecting the connected and powered upstream device. Filtering shall be used to avoid false disconnect detects during AUX signaling.

A downstream device can detect the presence of either of the two conditions described above to implement the Upstream Device Detection feature.

The AUX_CH uses Manchester-II coding for self-clocked signal transmission, as illustrated in Figure 3-6.

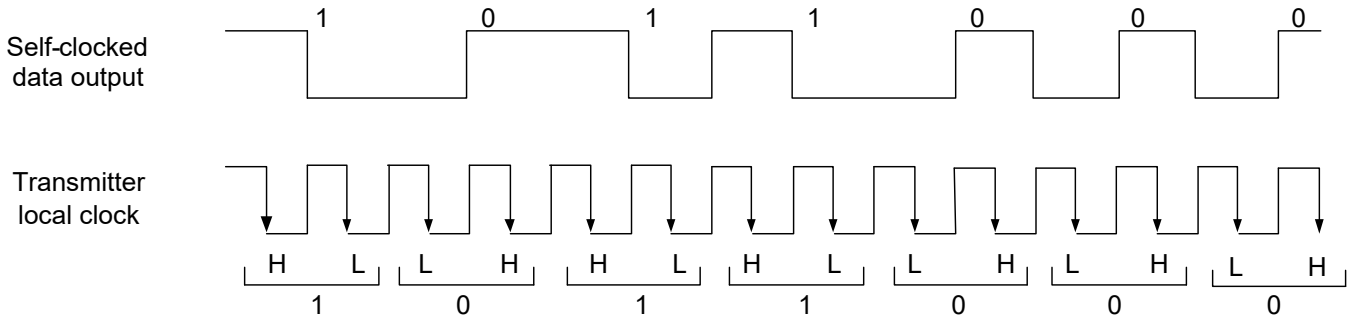


Figure 3-6: AUX_CH Self-clocking with Manchester-II Coding

3.4.1 AUX_CH Logical Sub-block

Between transactions, the AUX_CH is in an electrical idle state. In the electrical idle state, neither device is driving the AUX_CH. Therefore, both AUX_CH_P and AUX_CH_N are at the termination voltage.

AUX_CH transactions are initiated by the DPTX, which functions as an AUX_CH requester. The DPTX, which is the driving end for a request transaction, pre-charges AUX_CH_P and AUX_CH_N to a common mode voltage by transmitting 10 to 16 consecutive 0s in Manchester-II code.

After the active pre-charge, the DPTX transmits an AUX_SYNC pattern. The AUX_SYNC pattern shall be as follows:

- Start with 16 consecutive 0s in Manchester-II code, which results in a transition from low to high in the middle of each bit period. Including active pre-charge pulses, there shall be 26 to 32 consecutive 0s before the end of the AUX_SYNC pattern.
- End with AUX_CH_P being driven to high for a 2-bit period (which is 2us when the bit rate is 1Mbps) and then low for a 2-bit period, which is illegal in Manchester-II code. AUX_CH_N shall be driven to the opposite polarity.

The receiving end, which is the DPRX for the request transaction, shall lock to this AUX_SYNC pattern.

Following the AUX_SYNC pattern, the driving end shall transmit data according to the AUX_CH syntax, as described in Section 2.11. When the AUX_CH transmitter has finished transmitting data, the driving node shall assert the AUX STOP condition. The AUX STOP condition shall be as follows:

- Drives AUX_CH_P to high and AUX_CH_N to low for a 2-bit period, and then AUX_CH_P to low and AUX_CH_N to high for a 2-bit period, which is an illegal sequence for Manchester-II
- Releases the AUX_CH immediately after the AUX STOP condition

Figure 3-7 illustrates the AUX_SYNC pattern and AUX STOP condition.

The DPRX (the AUX_CH replier) replies to this request transaction. The DPRX, now functioning as a driving end, shall let the bus park for at least 10ns, pre-charge the bus to the common mode voltage with 10 to 16 pre-charge pulses, and then initiate the reply transaction. The AUX_SYNC pattern and AUX STOP condition are the same for request and reply transactions.

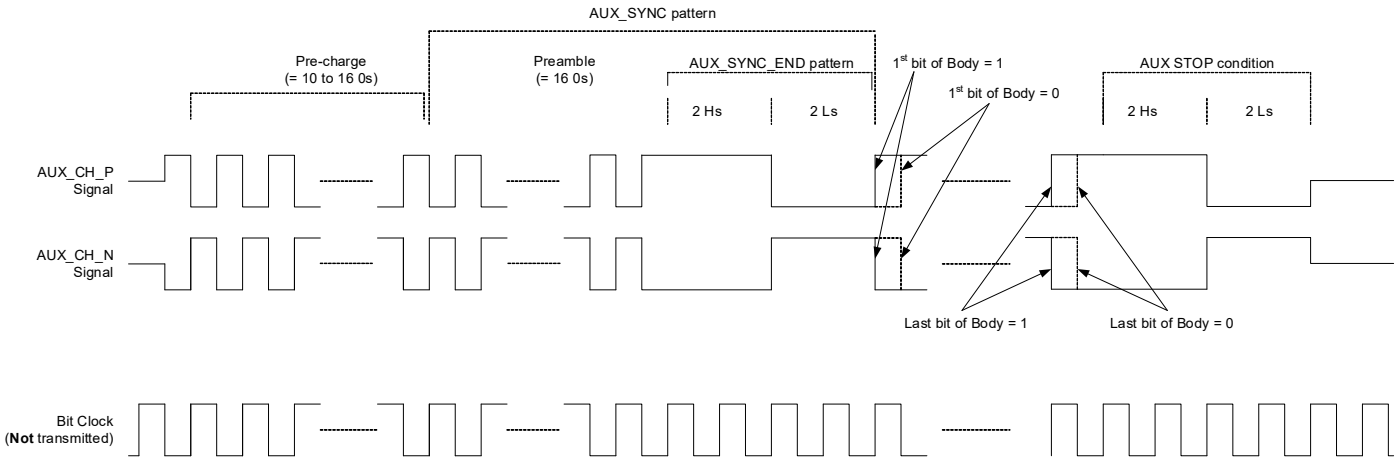


Figure 3-7: AUX_SYNC Pattern and AUX STOP Condition

3.4.2 AUX_CH Electrical Sub-block

Updated in *DP v1.4a*.

Table 3-5 defines the AUX_CH electrical specifications.

Table 3-5: AUX_CH Electrical Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI_{MAN}	Manchester transaction unit interval	0.4		0.6	us	Results in the bit rate of 1Mbps, which includes coding overhead.
Pre-charge Pulses	Number of pre-charge pulses	10		16		Each pulse is a 0.
$T_{AUX-BUS-PARK}$	AUX_CH bus park time	10			ns	Period after the AUX_CH STOP condition for which the bus is parked.
$T_{cycle-to-cycle\ jitter}$	Maximum allowable UI variation within a single transaction at connector pins of a transmitting device			0.08	UI	Equal to 48ns maximum. The transmitting device is an upstream device for a Request Transaction and a downstream device for a Reply Transaction.
	Maximum allowable variation for adjacent bit times within a single transaction at connector pins of a transmitting device			0.04	UI	Equal to 24ns maximum. The transmitting device is an upstream device for a Request Transaction and a downstream device for a Reply Transaction.
	Maximum allowable UI variation within a single transaction at connector pins of a receiving device			0.10	UI	Equal to 60ns maximum. The transmitting device is an upstream device for a Request Transaction and a downstream device for a Reply Transaction.
	Maximum allowable variation for adjacent bit times within a single transaction at connector pins of a receiving device			0.05	UI	Equal to 30ns maximum. The transmitting device is an upstream device for a Request Transaction and a downstream device for a Reply Transaction.
$V_{AUX-DIFFp-p\_TX}$	AUX peak-to-peak voltage from Main-Link Source/ Sink when transmitting	0.29	0.40	1.38	V	$V_{AUX-DIFFp-p} = 2 \times \lvert V_{AUX\_CH\_p} - V_{AUX\_CH\_n} \rvert$
$V_{AUX-DIFFp-p\_RX}$	AUX peak-to-peak voltage received by Main-Link Source, TP2	0.27		1.36	V	
	AUX peak-to-peak voltage received by Main-Link Sink, TP3	0.27		1.36	V	
$V_{AUX\_TERM\_R}$	AUX_CH termination DC resistance		100		Ω	Informative.

Table 3-5: AUX_CH Electrical Specifications (Continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{AUX-DC-CM}$	AUX DC common mode voltage	0		2.0	V	Common mode voltage is equal to V_{BIAS_TX} (or V_{BIAS_RX}) voltage.
$V_{AUX-TURN-CM}$	AUX turnaround common mode voltage			0.3	V	Steady state common mode voltage shift between Transmit and Receive modes of operation.
I_{AUX_SHORT}	AUX short circuit current limit			90	mA	Transmitter's total drive current when the transmitter is shorted to ground.
C_{AUX}	AUX AC-coupling capacitor	75		200	nF	AUX_CH AC-coupling capacitor placed on both the DP upstream and downstream devices.
SR_{AUX_20-80}	AUX slew rate, 20 to 80%			375[a]	mV/ns	Slew rate measured 20 to 80% of the rising and falling edge. (See Figure 3-8.)
V_{AUX_PU}	DP Sink device pull-up voltage on AUX_CH_P	2.25[b]		3.6	V	Includes ±10% tolerance.
$V_{AUX\_SRC\_CONN}$	Connected DP Source device voltage at DP Sink device				0.375 × V_{AUX_PU}	Voltage lower than this value indicates a physically connected DP Source device. The logic low threshold for detecting a connected DP Source device shall be between max($V_{AUX\_SRC\_CONN}$) and V_{AUX_PU}. After filtering.
$V_{AUX\_SRC\_PWRD}$	Powered DP Source device voltage at DP Sink device	0.8 × min (DP_PWR)				Voltage higher than this value indicates a connected and powered DP Source device. The threshold for detecting a powered DP Source device shall be between 0V and min($V_{AUX\_SRC\_PWRD}$). After filtering.
R_{AUX_SRC}	AUX biasing resistor at DP Source device	10	100	105	kΩ	Nominal 100-kΩ resistor should be used.
R_{AUX_SNK}	AUX biasing resistor at DP Sink device	950		1050	kΩ	

a. To reduce the near-end crosstalk (NEXT) to Main-Link differential signals from AUX reply transactions, the maximum slew rate of the AUX_CH differential Voltage Swing at the AUX transmitter (at TP2) has been specified as 375mV/ns. The slew rate specification applies to both Main-Link Source and Sink. For DPTX and DPRX testing, the test point is located at their respective connector pins.

b. Set by the 100-MHz USB Type-C-to-Type-C cable crosstalk mandate (i.e., 0.22 / 100MHz = 2.2ns). This specification applies to all DP devices, regardless of the connector type.

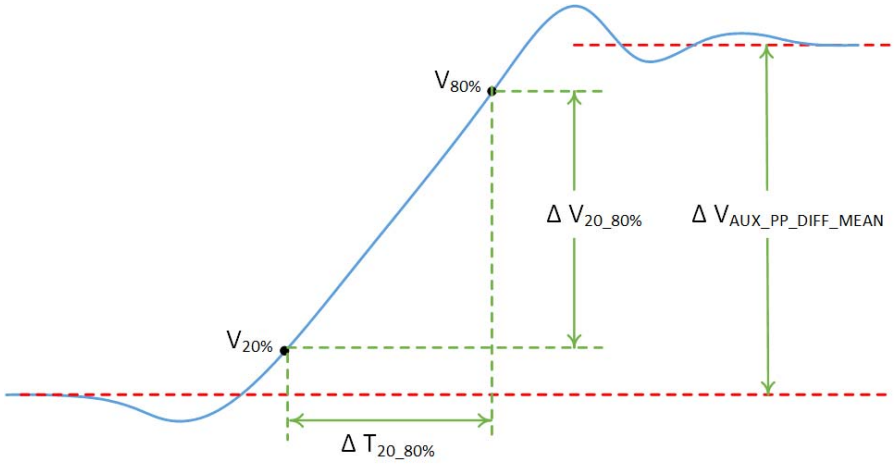


Figure 3-8: $V_{AUX\_PP\_MEAN}$ Measurement

where:

- $V_{AUX\_PP\_DIFF\_MEAN}$ is the V_{p-p} mean of the AUX voltage level, ignoring any overshoot or ringing that follows the positive or negative transition
- Rise Time/Fall Time Measurement oscilloscopes implement built-in rise and fall time measurements with typical options of 10 to 90% –or– 20 to 80%
- RT/FT_{20_80} is the time that it takes for the AUX voltage to rise or fall between the $V_{20\%}$ and $V_{80\%}$ levels (value is $\Delta T_{20\_80\%}$)

For worst-case slew rate, the minimum rise or fall time (in ns) will be used ($\Delta T_{20\_80\%\_min}$).

To calculate the $\Delta V_{20\_80\%}$ term, multiply $V_{AUX\_PP\_DIFF\_MEAN}$ by 60%.

To determine the slew rate between the $V_{20\%}$ and $V_{80\%}$ vertices, calculate the rate of change, as follows:

$$\begin{aligned}\text{Slew Rate} &= \text{Rate of change} = \text{Rise} / \text{Run} \\ &= \Delta V_{20\_80\%} / \Delta T_{20\_80\%} \\ &= (V_{AUX\_PP\_DIFF} \times 0.6) / \Delta T_{20\_80\%\_min}\ (\text{V/ns})\end{aligned}$$

Figure 3-9 indicates the topologies and test points for Table 3-6. Table 3-6 provides design guidance for AUX TX and RX designs, and guidance for the range of series resistance of a plug orientation switch in a DisplayPort Alt mode application.

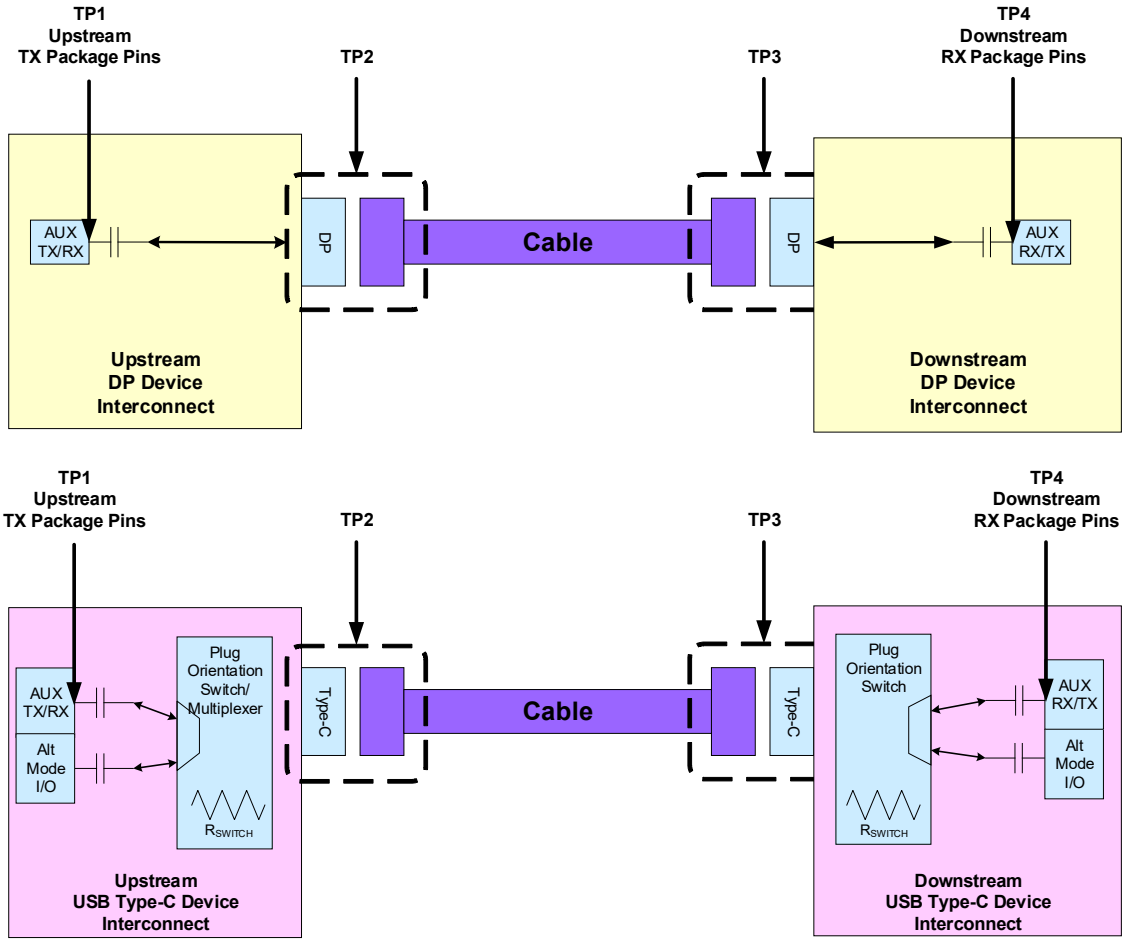


Figure 3-9: DP AUX IC Connections

Table 3-6: DP AUX IC Design Guidance (Informative)

Symbol	Parameter	Min	Nom	Max	Units	Comments
R_{SWITCH}[a]	Plug Orientation Switch/Multiplexer Resistance	0		20	Ω	Not required for legacy DP connector. Required for DisplayPort Alt mode. Integrated or external.
$V_{AUX\_TERM\_R\_PKG}$	AUX_CH differential termination DC resistance at TP1 and TP4	80	100	120	Ω	
$V_{AUX\text{-}DC\text{-}CM\_PKG}$	AUX DC common mode voltage at TP1 and TP4	0		2.0	V	Common mode voltage is equal to V_{BIAS_TX} (or V_{BIAS_RX}) voltage.
$V_{AUX\text{-}TURN\text{-}CM\_PKG}$	AUX turnaround common mode voltage at TP1 and TP4			0.3	V	Steady state common mode voltage shift between Transmit and Receive modes of operation.
$I_{AUX\_SHORT\_PKG}$	AUX short circuit current limit at TP1 and TP4			90	mA	Transmitter's total drive current when the transmitter is shorted to ground.
$V_{AUX\text{-}DIFFp\text{-}p\_TX\_PKG}$	AUX peak-to-peak voltage from Source IC when transmitting AUX at TP1	0.29		1.38	V	100Ω differential receiver, 75-nF AC-coupling capacitor. To meet $V_{AUX\text{-}DIFFp\text{-}p\_TX}$ at TP2, Voltage Swing must be increased as switch/multiplexer resistance is increased.
	AUX peak-to-peak voltage from Sink IC when transmitting AUX at TP4	0.29		0.40	V	100Ω differential receiver, 75-nF AC-coupling capacitor. To meet $V_{AUX\text{-}DIFFp\text{-}p\_TX}$ at TP3, Voltage Swing must be increased as switch/multiplexer resistance is increased.

Table 3-6: DP AUX IC Design Guidance (Informative) (Continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{AUX-DIFFp-p\_RX\_PKG}$	AUX peak-to-peak voltage to Source IC when receiving AUX at TP1	0.087		1.5	V	**Minimum Swing** – 75-nF TX and RX AC-coupling capacitor, maximum TX termination, minimum RX termination, switch/multiplexer resistance on receiver per design. **Maximum Swing** – 200-nF TX and RX AC-coupling capacitor, minimum TX termination, maximum RX termination, switch/multiplexer resistance on receiver per design. Droop due to AC-coupling with AUX_SYNC_END and longest UI should be considered.
	AUX peak-to-peak voltage to Sink IC when receiving AUX at TP4					
$T_{RISE/FALL\_20-80\_PKG}$	Rise/Fall time, 20 to 80%	2.2			ns	Rise and Fall time scale with Voltage Swing level.

a. Plug orientation switch/multiplexer may include a multiplexer for other alternate modes that also use the SBU wires.

3.4.2.1 AC-coupling

The AUX_CH shall be AC-coupled. The minimum and maximum values for the capacitance are defined in Table 3-5. The mandate for including AC-coupling capacitors on the interconnect media is specified at the DPTX.

3.4.2.2 Termination

The AUX_CH should meet the termination resistance defined in Table 3-5 whenever the link is active.

3.4.2.3 DC Common Mode Voltage

To facilitate the minimum bus turnaround delay, the transmitting side shall provide between 10 and 16 Manchester-II code 0s as pre-charge pulses at the start of a Manchester-II transaction. The steady state common mode voltage between transmit and receive modes of operation shall **not** exceed $V_{AUX-TURN-CM}$, as defined in Table 3-5.

Upstream and downstream devices shall be designed to tolerate a power-on, power-off, or Hot Plug event presenting the maximum charge redistribution of 720nC caused by $V_{AUX-DC-CM}$ (2.0V maximum) and C_{AUX} (200nF maximum) for the maximum period of maximum Pre-charge Pulses × UI_{MAN} (Manchester transaction Unit Interval) or greater.

3.4.2.4 Short Circuit Mandates

AUX_CH block driver and receiver circuits shall survive the worst-case short-circuit current of 90mA (3.6V over 40Ω).

3.4.2.5 Differential Voltage/Timing (EYE) Diagram

Figure 3-10 illustrates the AUX_CH EYE mask at the TX device connector pins, and Table 3-7 lists the minimum voltage at each pin. Figure 3-11 illustrates the AUX_CH EYE mask at the RX device connector pins, and Table 3-8 lists the minimum voltage at each pin.

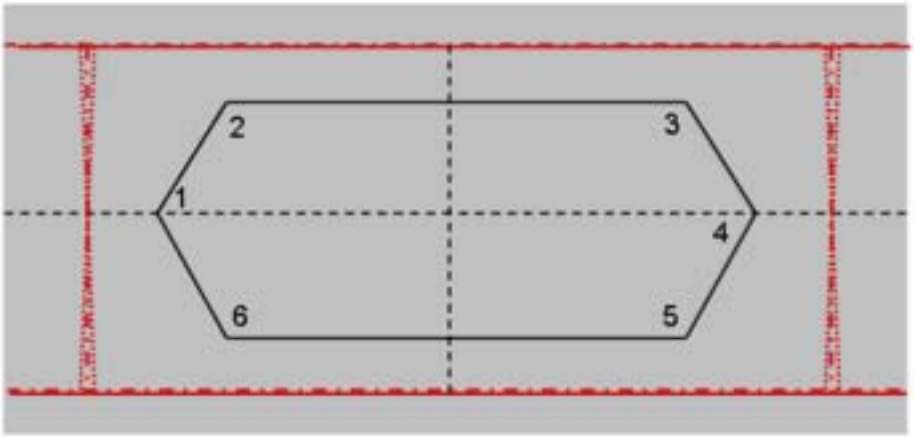


Figure 3-10: AUX_CH EYE Mask at TX Device Connector Pins

Table 3-7: AUX_CH EYE Mask Minimum Voltage Values at TX Device Connector Pins

Point	Time (from EYE Center) (ns)	Minimum Voltage Value (mV)
1	-185	0
2	-135	145
3	135	145
4	185	0
5	135	-145
6	-135	-145

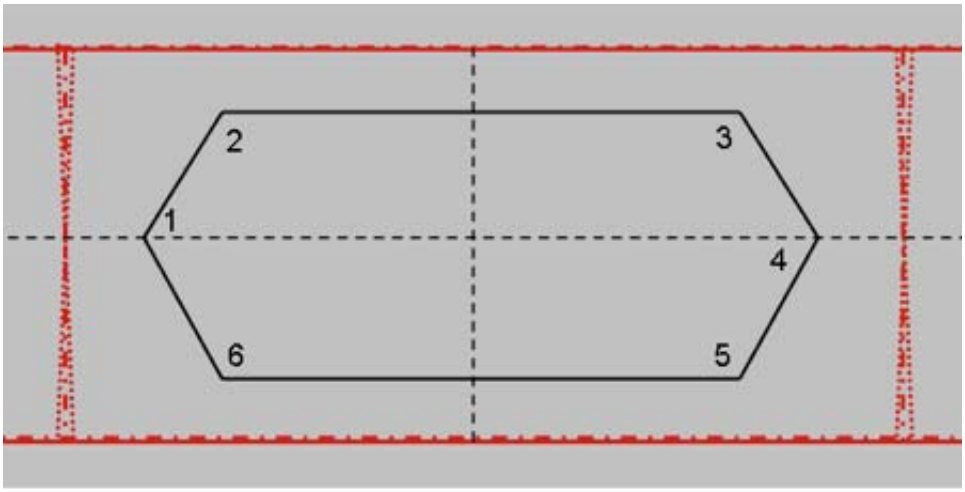


Figure 3-11: AUX_CH EYE Mask at RX Device Connector Pins

Table 3-8: AUX_CH EYE Mask Minimum Voltage Values at RX Device Connector Pins

Point	Time (from EYE Center) (ns)	Minimum Voltage Value (mV)
1	-185	0
2	-135	135
3	135	135
4	185	0
5	135	-135
6	-135	-135

3.5 Main-Link

This section describes the functions of the DP Main-Link PHY Layer.

3.5.1 Main-Link 8b/10b PHY Logical Sub-layer

The Main-Link 8b/10b PHY Logical Sub-layer performs the following functions:

- Scrambling and de-scrambling (see Section 3.1.6)
- 8b/10b encoding/decoding (see Section 3.1.7 and Section 3.5.1.1)
- Serialization and de-serialization (see Section 3.1.7)
- Link Training and Link Status Monitor (see Section 3.5.1.2 and Section 3.5.1.3)
- Link Quality Measurement (Testability; see Section 3.5.1.4)
- Forward Error Correction (FEC; see Section 3.5.1.5)

3.5.1.1 8b/10b Special Characters used for DisplayPort

In this Standard, various control link symbols are defined in the Link Layer for use on the Main-Link lanes in SST and MST modes.

Table 3-9 defines which 8b/10b special characters are used for those control link symbols. Unused special characters are reserved for future use and shall **not** be used by a DP-compliant link.

Table 3-9: 8b/10b Special Character-to-Control Link Symbol Mapping

Special Character	Control Link Symbol in SST Enhanced Mode[a]	Control Link Symbol in SST Enhanced Mode with FEC[b]	Control Link Symbol in MST Mode[c]
K23.7	FE	FE[d]	Indexed 0[d]
K27.7	BE	BE	Indexed 1
K28.0	SR	SR	Indexed 2
K28.1	CP	PM[d]	PM[d]
K28.2	SS	SS	Indexed 3
K28.3	BF	BF	Indexed 4
K28.4	RESERVED	CP	Direct RESERVED[e]
K28.5	BS	BS	Direct SR
K28.6	EOC[f]	EOC[f]	Indexed 5
K28.7	**Optionally** mapped to BE for tunneling Panel Replay symbols[g]	RESERVED	Direct RESERVED
K29.7	SE	SE	Indexed 6
K30.7	FS	FS	Indexed 7[d]

a. See Section 2.2.1.1 and Section 2.2.1.2 for definitions of these control link symbols in SST mode.
b. This column applies when a DPTX sets the FEC_READY bit in the FEC_CONFIGURATION register (DPCD Address 00120h, bit 0).
c. See Table 2-144 for definitions of these control link symbols in MST mode.
d. Parity Marker (PM) is used when FEC is enabled. K23.7 and K30.7 are used in FEC_DECODE_EN and FEC_DECODE_DIS control link symbol sequences. (For details regarding FEC, see Section 3.5.1.5.)

e. In MST mode, some 8b/10b K-codes are directly mapped from LL control link symbols, while others are index-mapped for indexed control link symbol scrambling for EMI reduction. "Direct RESERVED" means that the K character is reserved for future non-indexed control link symbol usage.

f. End of Chunk (EOC) is used for DSC Transport. (For details regarding DSC Transport, see Section 2.8.) In MST mode, EOC is mapped to C2-C2-C2-C2, as listed in Table 2-144.

g. See Section 5.14.1.1 for details.

3.5.1.2 Link Training

For an open, box-to-box connection, the upstream DP device configures the link through a link training sequence. One exception is when the upstream DP device resumes a transmission. In this condition, the upstream device may skip the link training AUX transactions, as described in Section 2.12.4.3.

For a closed, embedded connection, the DPTX and DPRX may be set to pre-calibrated parameters without going through the full link training sequence. In this mode, the upstream DP device may start a normal operation without the link training AUX transactions, as described in Section 2.12.4.3.

Table 3-10 lists the DPCD registers that are used for 8b/10b link training. (For complete register descriptions, see Table 2-183, Table 2-184, Table 2-185, Table 2-192, and Table 2-193.)

Table 3-10: DPCD Registers Used for 8b/10b Link Training

DPCD Address	Register
0000Eh	8b/10b_TRAINING_AUX_RD_INTERVAL
00100h	LINK_BW_SET
00101h	LANE_COUNT_SET
00102h	TRAINING_PATTERN_SET
00103h	TRAINING_LANE0_SET
00104h	TRAINING_LANE1_SET
00105h	TRAINING_LANE2_SET
00106h	TRAINING_LANE3_SET
00107h	DOWNSPREAD_CTRL
00108h	MAIN_LINK_CHANNEL_CODING_SET
00202h	LANE0_1_STATUS
00203h	LANE2_3_STATUS
00204h	LANE_ALIGN_STATUS_UPDATED
00206h	ADJUST_REQUEST_LANE0_1
00207h	ADJUST_REQUEST_LANE2_3
0200Ch	LANE0_1_STATUS_ESI
0200Dh	LANE2_3_STATUS_ESI
0200Eh	LANE_ALIGN_STATUS_UPDATED_ESI
0220Eh	8b/10b_TRAINING_AUX_RD_INTERVAL

Link training consists of two distinct tasks that shall be successfully completed in sequence to establish the link:

- **LANE*x*_CR_DONE** – Locks the DPRX Clock Recovery (CR) PLL to the repetition of D10.2 data symbols
- **LANE*x*_CHANNEL_EQ_DONE/LANE*x*_SYMBOL_LOCKED/ INTERLANE_ALIGN_DONE** – When successful, LANE*x*_SYMBOL_LOCKED and INTERLANE_ALIGN_DONE shall be achieved by the end of this sequence

The link training sequence is initiated by the Link Policy Maker in the upstream device to establish a link with the downstream device. The Link Policy Maker shall first detect that the HPD signal is asserted high by the downstream device. Before initiating the link training sequence, the Link Policy Maker of a DPTX that supports LT-tunable PHY Repeaters (LTTPRs) shall perform LTTPR recognition, as described in Section 3.6.6.6.1. Link Policy Maker shall then read the downstream device's Receiver Capability field (DPCD Addresses 00000h through 000FFh; see Table 2-183), –or– Extended Receiver Capability field (DPCD Addresses 02200h through 022FFh; see Table 2-193) registers (if the downstream device supports the Extended Receiver Capability field), for the following two conditions:

- Hot Plug Detect event (i.e., HPD low-going pulse that exceeds 2ms)
- With a downstream device whose DPCD r1.2 (or higher), an IRQ_HPD pulse with the RX_CAP_CHANGED bit in the LINK_SERVICE_IRQ_VECTOR_ESI0 register (DPCD Address 02005h, bit 0) set to 1

Link Policy Maker shall read the Receiver Capability and Extended Receiver Capability fields by way of the AUX_CH. Link Policy Maker shall then determine the link configuration based on the DPRX's capability and its own needs, and then write the following Link Configuration parameters:

- LINK_BW_SET register (DPCD Address 00100h)
- LANE_COUNT_SET field in the LANE_COUNT_SET register (DPCD Address 00101h, bits 4:0)
- DOWNSPREAD_CTRL register (DPCD Address 00107h)
- MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h)

After writing Link Configuration parameters, Link Policy Maker shall start link training by writing 21h to the TRAINING_PATTERN_SET register (DPCD Address 00102h) by way of the AUX_CH, while instructing its transmitter's logical PHY Layer to start transmitting link training pattern sequences.

Link Configuration parameters written to by Link Policy Maker shall not be changed after training has commenced until the next time the link is trained, except as described below for falling back to lower link bandwidth and/or reduced lane count on training failure.

An upstream DP device's writing of 21h to the TRAINING_PATTERN_SET register (DPCD Address 00102h) by way of the AUX_CH shall be preceded by the change of transmitted training pattern over the Main-Link. Whenever the TRAINING_PATTERN_SET register is written to, the TRAINING_LANE*x*_SET register(s) (DPCD Addresses 00103h through 00106h) of the enabled lane(s) shall also be written to.

Note: *The number of enabled lanes is written to the LANE_COUNT_SET field in the LANE_COUNT_SET register (DPCD Address 00101h, bits 4:0) before initiating link training. The AUX_CH burst write shall be used for writing to TRAINING_LANEx_SET register(s) of the enabled lane(s). An upstream device may write to the TRAINING_PATTERN_SET and TRAINING_LANEx_SET registers in one AUX_CH burst write transaction.*

A per-lane drive setting adjustability is an optional feature of a DPTX of an upstream device. If a DPRX requests different drive settings among multiple (two or four) lanes, a DPTX may use the setting of highest pre-emphasis level and voltage swing of all the requested settings.

When the combination of the requested pre-emphasis level and voltage swing exceeds the capability of a DPTX, the DPTX shall set the pre-emphasis level according to the request and use the highest voltage swing level that it can output with the given pre-emphasis level.

A DPRX shall issue a drive setting adjustment request within limits defined in this Standard.

When a DPTX reads a request beyond the limits of this Standard, the DPTX shall set the pre-emphasis level according to the request and set the highest voltage swing level that it can output with the given pre-emphasis level. If a DPTX is requested for 9.5dB of pre-emphasis level (may be supported for a DPTX) and cannot support that level, it shall set the pre-emphasis level to the next highest level, 6dB.

Table 3-11 defines the link training symbol patterns. All devices shall support TPS1 and TPS2. An HBR2-capable device shall also support TPS3. See Section 3.1.7 for the *Zxx.y-* and *Zxx.y+* notation definition.

Table 3-11: Link Training Symbol Patterns

Pattern Number	Purpose	Name
TPS1	For locking a DPRX's clock recovery circuit	Repetition of D10.2 characters without scrambling
TPS2	For setting equalization, determining symbol boundary, and achieving INTERLANE_ALIGN_DONE[a]	K28.5-, D11.6, K28.5+, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2 without scrambling
TPS3	For setting equalization, determining symbol boundary, and achieving INTERLANE_ALIGN_DONE[a]	K28.5-, K28.5+, K28.5-, K28.5+, D10.2-, D10.2-, D10.2-, D10.2-, D10.2-, D10.2-, D10.2-, D10.2-, K28.5-, K28.5+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3- without scrambling
TPS4	For setting equalization, determining symbol boundary, and achieving INTERLANE_ALIGN_DONE[a]	Same as CP2520 Pattern 3 defined in *PHY CTS* K28.0-, K28.5-, K28.5+, K28.0-, 248 00hs after data symbol scrambling and 8b/10b coding (252 of 10 binary bits listed in Section 3.5.1.2.1 for clarity; the rightmost bit is the least significant bit that is transmitted first, and the leftmost bit is the most significant bit that is transmitted last)

a. INTERLANE_ALIGN_DONE bits in the LANE_ALIGN_STATUS_UPDATED and LANE_ALIGN_STATUS_UPDATED_ESI registers (DPCD Addresses 00204h and 0200Eh, bit 0, respectively).

An HBR3-capable device shall also support TPS4. A downstream device that is capable of supporting TPS4 shall advertise this capability by setting the TPS4_SUPPORTED bit in the MAX_DOWNSPREAD register (DPCD Address 00003h, bit 7). An upstream device that supports TPS4 shall verify the TPS4_SUPPORTED bit in the connected downstream device. If the upstream device finds the bit set, the upstream device shall write 07h to the TRAINING_PATTERN_SET register (DPCD Address 00102h) and transmit TPS4 during the link training LANE*x*_CHANNEL_EQ_DONE sequence (regardless of the speed at which the link is being trained).

In all other cases, the upstream device shall transmit TPS2 (or TPS3 in case a downstream device supports TPS3) during the link training LANE*x*_CHANNEL_EQ_DONE sequence. If training without AUX transactions, the use of TPS4 is determined either as the result of a previous training sequence on the same connection, or by implementation-specific system configuration means (e.g., on eDP).

A DPTX shall transition from TPS2/3/4 to a non-training pattern at a link symbol boundary without any gap in between. The DPTX is allowed to transition to a non-training pattern in the middle of a link training pattern.

Unless training without AUX transactions, a DPRX may request for adjustment of differential voltage swing, pre-emphasis, or both during the link training LANE*x*_CR_DONE and LANE*x*_CHANNEL_EQ_DONE sequences, as illustrated in Figure 3-12 on page 745 and Figure 3-13 on page 750.

3.5.1.2.1 TPS4 Bit Sequence

0010111100

0101111100

1010000011

0010111100

1000110101

0010010111

0110111001

0010110100

0101110010

0111000111

1101010010

1011010010

1100110010

1100001110

1001011000

0101100110

0101011110

1100001101

0101001010

1011001101

0101100001

1010111001

0101111000

1000100110

1001101100

0110010011

1000101101

0101110010

1101000111

1101010010

0011101000

1001101010

0110001101

1001110100

0101011110

0111000110

0101111000

1010100010

1001101011

0101110001

1011100100

0101010001

0101011101

1001010010

0110110100

1010100101

0010011101

0110010011

0110010111

1000101010

0011010110

0111001110

1001101100

0110011010

0010011010

0111011010

1001011000

1001001101

1001010110

1001011011

1001011010

0010001110

1100111010

1100111000

0110000101

1101100110

1010101100

1001100110

0110010011

1000101001

1001011010

0110001101

1001000111

0011010110

1001110110

1000011100

1011110100

0100001011

1101100011

0110100001

0110010011

1101100110

1010110010

1000010110

1010111010

1011011000

1011000110

0100010101

0110101011

1100101010

1100100110

1000110010

0100110101

1101101100

0101010001

1001010101

1000101101

1010101110

0110000101

1001000111

0011110100

1010111001

0011100001

0100011110

0101100101

1010110011

0111100001

1011010100

0010101001

1100111001

1101011000

0101101001

1000110001

1101001011

0011000101

1100101101

1101101000

1010100011

1010011100

0001001101

1010100111

1001011001

1001001010

0110110100

1010011010

0111010101

0010001110

0101010011

0110000111

1101100011

1011100010

1011100100

0100001011

1101001101

0100001110

1010011100

1001010011

0100110011

1100010111

0101001110

1001001101

0101101100

0010001011

1001011110

0110011010

0010001011

1010101101

1100011010

1100011100

0110110001

0110000101

0101100111

0010011100

1101110010

0001001110

1010101110

0110010010

1001110101

1001001100

0011011010

1101001101

1100101001

1000110100

0010101110

0110011010

1001110001

0011110010

0110100101

0101111001

0110101000

1011010011

0010001110

0110011100

0101111010

0101010100

1010010101

0111000111

0111001001

1100110010

0010010110

1100100111

0110010101

1001001100

0100101011

0110011101

1101000110

0110001101

1101001100

1011100001

0110101010

1001001001

1010011001

1010101100

0011010101

0010011011

1100010111

1001110001

0110100101

0001001101

0110111010

0100110001

1100101011

1100001110

1001100010

1000011110

1000100111

1001101001

0010101011

0110111010

1100101100

1000011100

0110101011

0010001011

1010011110

0110011010

0011010010

0101011010

1010011011

0101001011

0110001010

1010011001

0101010111

0011100010

1001010111

1010100001

0111100011

0010011010

0110100110

0100100111

1101110100

1000010101

1010111010

0100001011

0110100111

1010010110

0110001011

0110010011

1101001001

1010010010

0011100011

0010101011

1011101010

0101110100

0111101000

1011010100

1101010001

0101000110

0010101110

1011100011

1010101001

1100111000

0001001110

The link training sequence, regardless of whether there is an accompanying AUX transaction, shall always start with negative disparity. The Link Training Symbol Pattern of the LANE*x*_CHANNEL_EQ_DONE sequence shall start with K28.5-, K28.5-, and K28.0- for TPS2, TPS3, and TPS4, respectively.

For complete DPCD address mapping, see Table 2-182.

3.5.1.2.2 LANE*x*_CR_DONE Sequence

Link training begins with the LANE*x*_CR_DONE sequence. The link symbols transmitted in this sequence are a repetition of D10.2 data symbols with scrambling disabled (TPS1). In this sequence, the transmitter shall normally start signaling at Voltage Swing Level 0 and Pre-emphasis Level 0. The upstream device commences transmission of TPS1, and then writes 21h to the TRAINING_PATTERN_SET register (DPCD Address 00102h) and the current drive setting to the TRAINING_LANE*x*_SET register(s) (DPCD Address(es) 00103h through 00106h).

The upstream device may start Full Link Training with non-minimum differential voltage swing and/or non-zero pre-emphasis if the optimal setting is already known, for example, as is the case in an embedded application. In this case, the upstream device shall write the voltage swing and pre-emphasis settings at which it is starting training to the TRAINING_LANE*x*_SET register(s) as part of the burst write in which it writes 21h to the TRAINING_PATTERN_SET register.

In the LANE*x*_CR_DONE sequence, the transmitter shall wait for at least 100us before issuing a read request AUX transaction for reading the Lane's LANE*x*_CR_DONE bit in the following registers, which are set by the receiver:

- LANE*x_y*_STATUS register(s) (DPCD Address 00202h, bits 0 and 4, and DPCD Address 00203h, bits 0 and 4, for Lanes 0, 1, 2, and 3, respectively, as appropriate)
- LANE*x_y*_STATUS_ESI register(s) (DPCD Address 0200Ch, bits 0 and 4, and DPCD Address 0200Dh, bits 0 and 4, for Lanes 0, 1, 2, and 3, respectively, as appropriate)

Unless all the LANE*x*_CR_DONE bits are set, the transmitter shall do the following:

1 Read the ADJUST_REQUEST_LANE*x_y* register(s) (DPCD Address(es) 00206h and 00207h).

2 Adjust the voltage swing and/or pre-emphasis level according to the request.

3 Update the TRAINING_LANE*x*_SET register(s) to match the new voltage swing and/or pre-emphasis settings.

The receiver sets the LANE*x*_CR_DONE bit(s) only when its link clock and data recovery (CDR) unit has achieved and maintained LANE*x*_CR_DONE. To optimize the transmitter's drive setting, the receiver may defer setting LANE*x*_CR_DONE bits until optimization is complete.

The receiver shall set the LANE*x*_CR_DONE bit(s) on those lanes for which CR lock is achieved in the DPCD. Otherwise, the receiver shall keep the LANE*x*_CR_DONE bits cleared and request an adjustment of the differential voltage swing and/or an adjustment of the pre-emphasis level, by updating the value in the ADJUST_REQUEST_LANE*x_y* register(s).

The transmitter shall downshift to the lower link rate, and then repeat the LANE*x*_CR_DONE sequence when any of the following conditions exist:

- Receiver keeps the same value in the ADJUST_REQUEST_LANE*x_y* register(s) while one or more of the LANE*x*_CR_DONE bit(s) remain unset after five AUX_ACKs for read request transactions for reading LANE*x*_CR_DONE bit(s) and ADJUST_REQUEST_LANE*x_y* registers.
- Receiver fails to set all the LANE*x*_CR_DONE bit(s) after the transmitter transmits the maximum voltage swing level, which is the sum of the VOLTAGE_SWING_LANE*x* and PRE_EMPHASIS_LANE*x* field values in the ADJUST_REQUEST_LANE*x_y* register(s).
- Receiver fails to set all the LANE*x*_CR_DONE bit(s) on the enabled lanes following a total of 10 AUX_ACKs for read request transactions for reading LANE*x*_CR_DONE bit(s) and ADJUST_REQUEST_LANE*x_y* register(s).

See Section 3.1.5.2 for the voltage swing levels that the transmitter shall support.

To re-initiate training at a lower link rate, the upstream device does the following:

1 Clears the TRAINING_PATTERN_SET register (DPCD Address 00102h) to 00h.

2 Starts transmitting TPS1 (D10.2) at the lower rate at the default voltage swing and pre-emphasis (400mV, no pre-emphasis).

3 Writes 21h to the TRAINING_PATTERN_SET register (and appropriate values to the TRAINING_LANE*x*_SET register(s) (DPCD Addresses 00103h through 00106h)) to initiate training

After the transmitter's Link Policy Maker reads the LANE*x*_CR_DONE bit(s) as set for all enabled lanes, the Link Policy Maker shall move on to the next stage (i.e., the Channel Equalization (EQ) sequence).

3.5.1.2.2.1 Fallback Mandates for LANE*x*_CR_DONE Failure on Lower-count Lanes

Figure 3-12 updated in *DP v2.0*.

There is a possibility that the number of physical connections between a transmitter in an upstream device and a receiver in a downstream device is lower than the maximum number of lanes that the receiver supports. For example, only Lanes 0 and 1 can be connected even when a receiver supports up to four lanes. In this case, the link training LANE*x*_CR_DONE sequence is likely to fail on higher-count lanes that have no physical connections (Lanes 2 and 3 in the above example).

Figure 3-12 describes the necessary behavior of an upstream DP device with DPTX's Link Policy Maker in the above scenario.

If a DPRX sets the LANE*x*_CR_DONE bit(s) on all enabled lanes, but fails in the link training EQ sequence, the upstream DP device shall follow the fallback mandate described in Section 3.5.1.2.3.1.

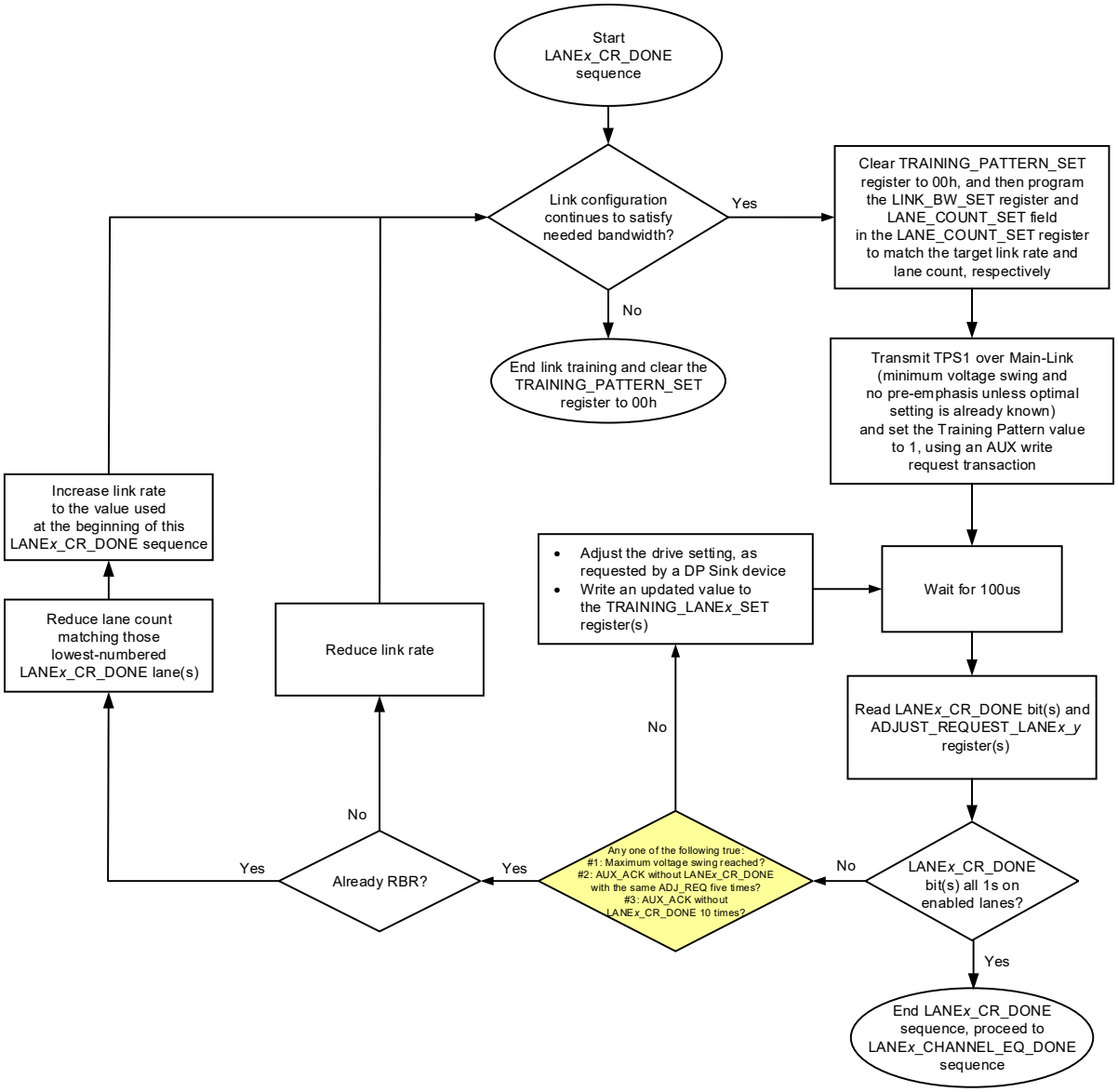


Figure 3-12: Link Training LANE*x*_CR_DONE Sequence

Note: *The minimum video format is DP Source implementation-specific, and might be the same as, or different from, the video fallback format. DP Branch devices shall consider 1-lane RBR to be the minimum acceptable link configuration when training their DFPs.*

The upstream device, after reducing the link rate to RBR upon failure of the LANE*x*_CR_DONE bit on all enabled lanes, shall check whether it is the lowest numbered lanes that have the LANE*x*_CR_DONE bit(s) set to 1:

- LANE*x*_*y*_STATUS register(s) (DPCD Address 00202h, bits 0 and 4, and DPCD Address 00203h, bits 0 and 4, for Lanes 0, 1, 2, and 3, respectively, as appropriate)
- LANE*x*_*y*_STATUS_ESI register(s) (DPCD Address 0200Ch, bits 0 and 4, and DPCD Address 0200Dh, bits 0 and 4, for Lanes 0, 1, 2, and 3, respectively, as appropriate)

If that is the case, the upstream device shall reduce the lane count to match those LANE*x*_CR_DONE lanes, program the link rate to the highest link rate needed, and then continue with the link training LANE*x*_CR_DONE sequence.

Note that with the reduced lane count, only the following lane combinations are valid:

- 2-lane configuration = Lanes 0 and 1 enabled, and Lanes 2 and 3 disabled
- 1-lane configuration = Lane 0 enabled, and Lanes 1, 2, and 3 disabled

The Source device may abort training if the LANE*x*_CR_DONE or LANE*x*_CHANNEL_EQ_DONE sequence fails at all link configurations that would provide sufficient bandwidth for the Source device's needed video format. The Source device shall clear the TRAINING_PATTERN_SET register to 00h when training is aborted.

3.5.1.2.3 LANE*x*_CHANNEL_EQ_DONE Sequence

The LANE*x*_CHANNEL_EQ_DONE sequence starts with the transmitter drive setting as set at the end of the LANE*x*_CR_DONE sequence.

In the LANE*x*_CHANNEL_EQ_DONE sequence, the upstream device transmits the appropriate pattern (TPS2, TPS3, or TPS4) with scrambling disabled for TPS2 and TPS3 and enabled for TPS4. The upstream device then writes 22h, 23h, or 07h for TPS2, TPS3, or TPS4, respectively, to the TRAINING_PATTERN_SET register (DPCD Address 00102h) and the current drive setting to the TRAINING_LANE*x*_SET register(s) (DPCD Addresses 00103h through 00106h).

The transmitter shall wait at least the period of time specified in the TRAINING_AUX_RD_INTERVAL field in the 8b/10b_TRAINING_AUX_RD_INTERVAL register (DPCD Address 0000Eh, bits 6:0) after programming 22h, 23h, or 07h for TPS2, TPS3, or TPS4, respectively, to the TRAINING_PATTERN_SET register before reading the link status bits.

The bits are transported from the leftmost bit first (lsb) to the rightmost bit last (msb). The transmitter shall insert a two-link-symbol inter-lane skew between adjacent lanes, as illustrated in Figure 2-15.

The receiver shall use the recognition of this training pattern to decide whether the channel equalization is successful. How to measure the equalization result is implementation-specific.

Section 3.1.5.2 gives the voltage swings and pre-emphasis level combinations that the transmitter shall support. The receiver shall indicate success by setting the following register bits:

- Lane's LANE*x*_CHANNEL_EQ_DONE bit(s), as appropriate
  - LANE*x*_*y*_STATUS register(s) (DPCD Address 00202h, bits 1 and 5, and DPCD Address 00203h, bits 1 and 5, for Lanes 0, 1, 2, and 3, respectively)
  - LANE*x*_*y*_STATUS_ESI register(s) (DPCD Address 0200Ch, bits 1 and 5, and DPCD Address 0200Dh, bits 1 and 5, for Lanes 0, 1, 2, and 3, respectively)
- Lane's LANE*x*_SYMBOL_LOCKED bit(s), as appropriate
  - LANE*x*_*y*_STATUS register(s) (DPCD Address 00202h, bits 2 and 6, and DPCD Address 00203h, bits 2 and 6, for Lanes 0, 1, 2, and 3, respectively)
  - LANE*x*_*y*_STATUS_ESI register(s) (DPCD Address 0200Ch, bits 2 and 6, and DPCD Address 0200Dh, bits 2 and 6, for Lanes 0, 1, 2, and 3, respectively)
- INTERLANE_ALIGN_DONE bits in the LANE_ALIGN_STATUS_UPDATED and LANE_ALIGN_STATUS_UPDATED_ESI registers (DPCD Addresses 00204h and 0200Eh, bit 0, respectively)

The receiver sets the LANE*x*_SYMBOL_LOCKED bit(s) only when it has properly detected and aligned the 8b/10b symbol boundaries. Given the bit error rate target of $1E^{-9}$ and the duration of the link training period (which can be 10ms or less, though it might take a few hundreds of milliseconds, depending on the number of iterations needed for completion), the receiver should detect no more than a single symbol error during the link training to set the LANE*x*_SYMBOL_LOCKED bits. To optimize the DPTX's drive setting, the DPRX may defer setting the LANE*x*_SYMBOL_LOCKED bits until optimization is complete.

The receiver sets the INTERLANE_ALIGN_DONE bits only when its PHY Layer digital sub-block has successfully aligned the symbol boundaries of all the enabled lanes with one another so that the Link Layer block can handle the incoming symbol patterns. To optimize the DPTX's drive setting, the DPRX may defer setting the INTERLANE_ALIGN_DONE bit until optimization is complete.

During the normal operation following the link training, the receiver shall clear the LANE*x*_SYMBOL_LOCKED and INTERLANE_ALIGN_DONE bits when its Link Layer block can no longer process the incoming symbol patterns due to symbol errors, which causes noticeable visible/audible glitches to the regenerated streams. The receiver shall otherwise maintain these bits during normal operation. The receiver shall not clear these bits upon isolated Symbol errors. Guidelines for Symbol-error resiliency of the receiver are provided in Appendix C.

The transmitter shall read the LANE*x*_SYMBOL_LOCKED and INTERLANE_ALIGN_DONE bits, as well as the ADJUST_REQUEST_LANE*x*_*y* register(s) (DPCD Address(es) 00206h and 00207h). Unless all status bits are set to 1, the transmitter shall adjust the drive setting according to the receiver's request, and then write the new setting to the TRAINING_LANE*x*_SET register(s) (DPCD Addresses 00103h through 00106h).

The minimum loop count in this sequence is one, while the maximum loop count in this sequence (see Figure 3-13) is five. When not training at RBR and one or more of the LANE*x*_SYMBOL_LOCKED and INTERLANE_ALIGN_DONE bits remain unset in the sixth loop, the transmitter shall reduce the lane count, and then re-initiate training at the same link rate. Only after failing with a lane count of 1, the transmitter shall set the lane count to the quantity needed (within the maximum supported by the DPRX), and then downshift to the next lower bit rate. To re-initiate training at a lower bit rate, the upstream device does the following:

1 Clears the TRAINING_PATTERN_SET register (DPCD Address 00102h).

2 Starts transmitting TPS1 (D10.2) at the lower rate at the default voltage swing and pre-emphasis (400mV, no pre-emphasis).

3 Writes 21h to the TRAINING_PATTERN_SET register (and appropriate values to the TRAINING_LANE*x*_SET register(s) (DPCD Addresses 00103h through 00106h)) to initiate training.

At the end of the successful LANE*x*_CHANNEL_EQ_DONE sequence (with all the LANE*x*_SYMBOL_LOCKED and INTERLANE_ALIGN_DONE bits set by the receiver), the transmitter shall clear the TRAINING_PATTERN_SET register to 00h.

The receiver, with its own equalizer (**optional**), may adjust its equalizer setting(s) in each training loop. The receiver may issue up to seven consecutive AUX_DEFERs, if needed. However, use of AUX_DEFER should be minimized to meet the Link Training completion time target of 10ms. When the transmitter receives more than seven consecutive AUX_DEFERs, it may terminate link training.

The receiver should not set the following register bits immediately after successfully receiving the training patterns:

- Lane's LANE*x*_CHANNEL_EQ_DONE bit(s), as appropriate
  - LANE*x*_*y*_STATUS register(s) (DPCD Address 00202h, bits 1 and 5, and DPCD Address 00203h, bits 1 and 5, for Lanes 0, 1, 2, and 3, respectively)
  - LANE*x*_*y*_STATUS_ESI register(s) (DPCD Address 0200Ch, bits 1 and 5, and DPCD Address 0200Dh, bits 1 and 5, for Lanes 0, 1, 2, and 3, respectively)
- Lane's LANE*x*_SYMBOL_LOCKED bit(s), as appropriate
  - LANE*x*_*y*_STATUS register(s) (DPCD Address 00202h, bits 2 and 6, and DPCD Address 00203h, bits 2 and 6, for Lanes 0, 1, 2, and 3, respectively)
  - LANE*x*_*y*_STATUS_ESI register(s) (DPCD Address 0200Ch, bits 2 and 6, and DPCD Address 0200Dh, bits 2 and 6, for Lanes 0, 1, 2, and 3, respectively)
- INTERLANE_ALIGN_DONE bits in the LANE_ALIGN_STATUS_UPDATED and LANE_ALIGN_STATUS_UPDATED_ESI registers (DPCD Addresses 00204h and 0200Eh, respectively, bit 0)

Rather, the receiver should either increase its own equalization level or request a stronger pre-emphasis. When such action results in loss of successful reception, the receiver shall restore or request the last setting. The purpose of this methodology is to ensure the maximum operating margin.

3.5.1.2.3.1 Fallback Mandates for LANE*x*_SYMBOL_LOCKED Failures in 2- and 4-lane Configurations

Figure 3-13 updated in *DP v2.0*.

There is a possibility for LANE*x*_SYMBOL_LOCKED failure in a 2- or 4-lane configuration because only one lane (2-lane configuration) or two lanes (4-lane configuration) are available for a DP Main-Link. In such a condition, the LANE*x*_CR_DONE sequence over two or four lanes should have failed. However, it is known that there are DPRX implementations that erroneously set the LANE*x*_CR_DONE bit(s) on all lanes.

In the event of LANE*x*_SYMBOL_LOCKED failure in a 2-lane configuration, the DPTX shall attempt to return to the LANE*x*_CR_DONE sequence after reducing the lane count to one (i.e., writing 01h to the LANE_COUNT_SET field in the LANE_COUNT_SET register (DPCD Address 00101h, bits 4:0) at the same link rate, as illustrated in Figure 3-13.

In the event of LANE*x*_SYMBOL_LOCKED failure in a 4-lane configuration, the DPTX shall attempt to return to the LANE*x*_CR_DONE sequence after reducing the lane count to two (i.e., writing 02h to the LANE_COUNT_SET field) at the same link rate, as illustrated in Figure 3-13.

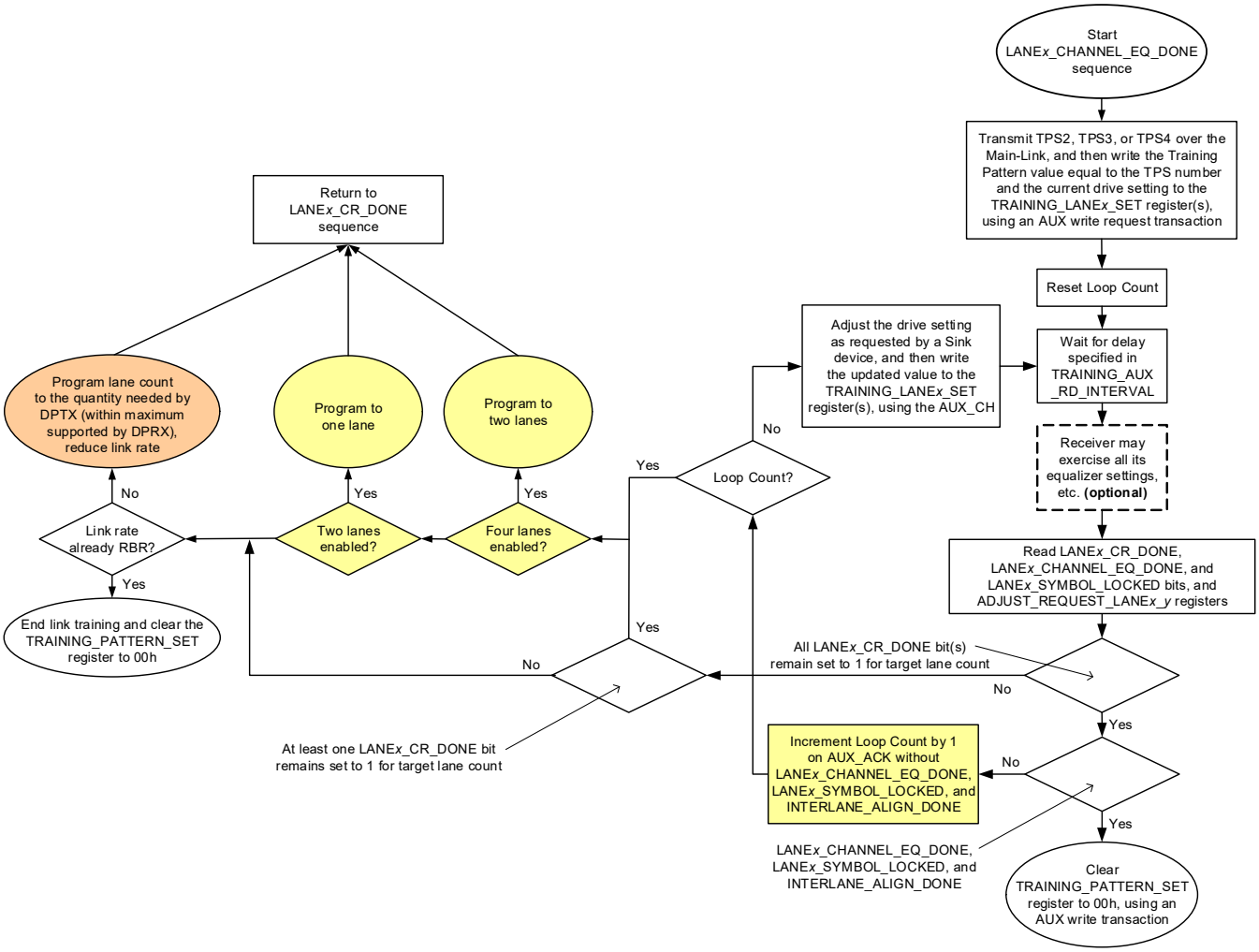


Figure 3-13: Link Training LANE*x*_CHANNEL_EQ_DONE Sequence

Note: *The minimum video format is DP Source implementation-specific, and might be the same as, or different from, the video fallback format. DP Branch devices shall consider 1-lane RBR to be the minimum acceptable link configuration when training their DFPs.*

After verifying that LANE*x*_CHANNEL_EQ_DONE, LANE*x*_SYMBOL_LOCKED, and INTERLANE_ALIGN_DONE are achieved, the transmitter shall write 00h to the TRAINING_PATTERN_SET register (DPCD Address 00102h) to indicate the end of training, and then start transmitting stream data.

If the Clock Recovery circuit loses lock during the LANE*x*_CHANNEL_EQ_DONE sequence, the receiver shall clear the lane's LANE*x*_CR_DONE bit(s) to 0:

- LANE*x*_*y*_STATUS register(s) (DPCD Address 00202h, bits 0 and 4, and DPCD Address 00203h, bits 0 and 4, for Lanes 0, 1, 2, and 3, respectively, as appropriate)
- LANE*x*_*y*_STATUS_ESI register(s) (DPCD Address 0200Ch, bits 0 and 4, and DPCD Address 0200Dh, bits 0 and 4, for Lanes 0, 1, 2, and 3, respectively, as appropriate)

If the DP Sink device has cleared all LANE*x*_CR_DONE bits to 0 and link training is conducted in HBR or higher, the transmitter shall reduce the bit rate and return to the LANE*x*_CR_DONE sequence. If link training is already conducted in RBR, the transmitter shall end link training by writing 00h to the TRAINING_PATTERN_SET register, without establishing the link. If at least one LANE*x*_CR_DONE bit remains set to 1 for the current lane count, the transmitter shall reduce the lane count to the next-lowest setting and return to the LANE*x*_CR_DONE sequence.

3.5.1.2.4 Link Training Flow with Maximum Link Data Bandwidth Policy

New to *DP v2.0*.

If the initial target link configuration fails link training, a DPTX device may use a link training link configuration flow that maximizes the link data bandwidth. Figure 3-14 and Figure 3-15 illustrate the LANE*x*_CR_DONE and LANE*x*_CHANNEL_EQ_DONE sequence flows, respectively.

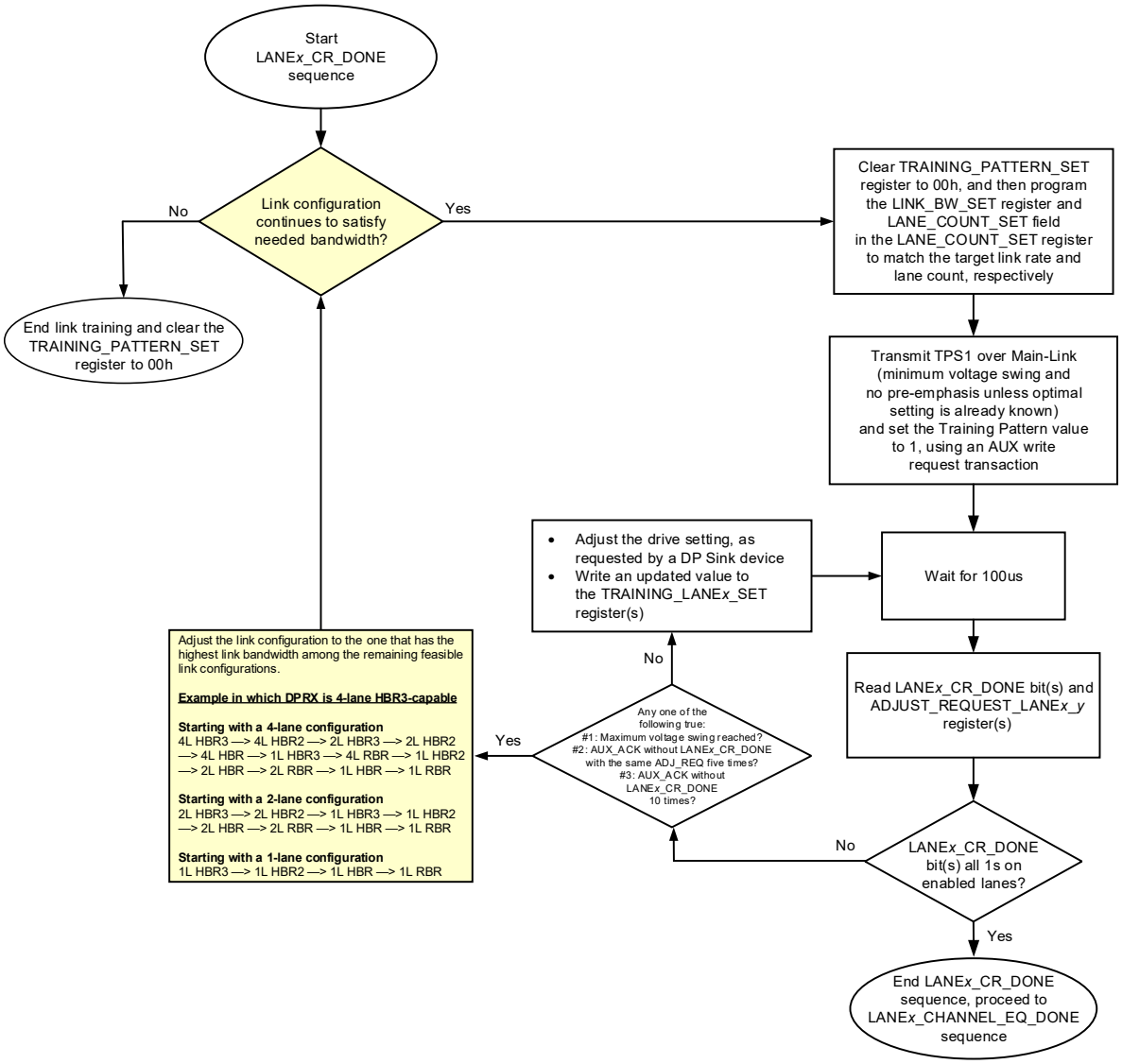


Figure 3-14: Link Training LANE*x*_CR_DONE Sequence for Maximum Link Data Bandwidth Policy

Note: *The minimum video format is DP Source implementation-specific, and might be the same as, or different from, the video fallback format. DP Branch devices shall consider 1-lane RBR to be the minimum acceptable link configuration when training their DFPs.*

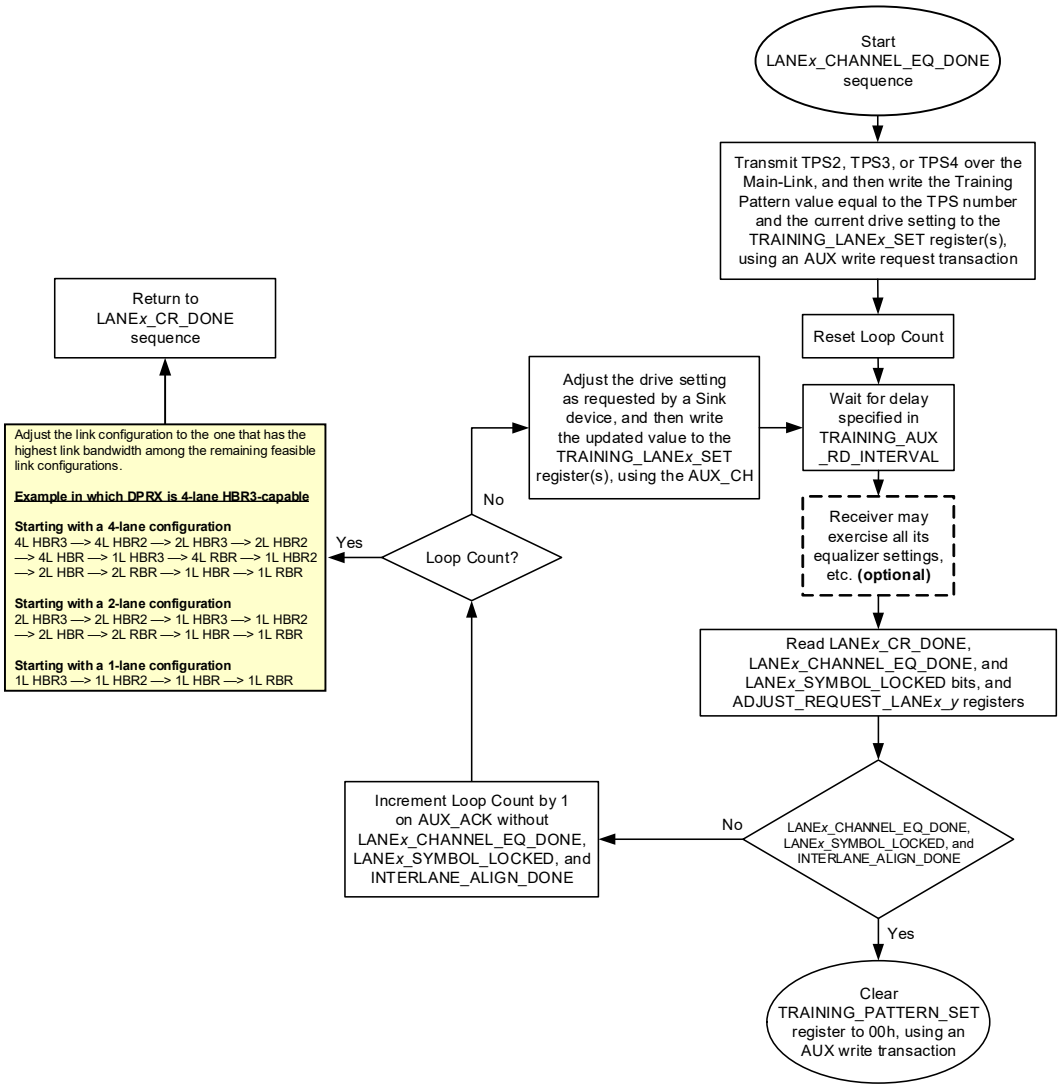


Figure 3-15: Link Training LANE*x*_CHANNEL_EQ_DONE Sequence for Maximum Link Data Bandwidth Policy

Note: *The minimum video format is DP Source implementation-specific, and might be the same as, or different from, the video fallback format. DP Branch devices shall consider 1-lane RBR to be the minimum acceptable link configuration when training their DFPs.*

3.5.1.2.5 POST_LT_ADJ_REQ Sequence

Updated in *DP v1.4a*.

A downstream device may support the POST_LT_ADJ_REQ sequence to further fine-tune the TX drive setting and its own RX EQ setting in case the upstream device does not support TPS4. POST_LT_ADJ_REQ uses a randomized 8b/10b transmission pattern instead of TPS2 or TPS3.

A downstream device that supports the POST_LT_ADJ_REQ sequence sets the POST_LT_ADJ_REQ_SUPPORTED bit in the MAX_LANE_COUNT register (DPCD Address 00002h, bit 5) to declare the support to the upstream device. The upstream device then grants the POST_LT_ADJ_REQ sequence by setting the POST_LT_ADJ_REQ_GRANTED bit in the LANE_COUNT_SET register (DPCD Address 00101h, bit 5) to 1.

The downstream device, after setting the Link/Sink Device Status registers (DPCD Addresses 00202h through 00204h and DPCD Addresses 0200Ch through 0200Eh) to indicate that link training is complete, sets the POST_LT_ADJ_REQ_IN_PROGRESS bits in the LANE_ALIGN_STATUS_UPDATED and LANE_ALIGN_STATUS_UPDATED_ESI registers (DPCD Addresses 00204h and 0200Eh, respectively, bit 1) to initiate the POST_LT_ADJ_REQ sequence, as illustrated in Figure 3-16.

The downstream device may clear the Link/Sink Device Status registers during the POST_LT_ADJ_REQ sequence to indicate that the downstream device is unable to synchronize to the training pattern that was transmitted by the upstream device. When the upstream device detects this condition, the upstream device shall abort the POST_LT_ADJ_REQ sequence and return to the LANE*x*_CR_DONE sequence (as defined in Section 3.5.1.2.2) after reducing the link rate to the next-lowest rate. Link training shall be terminated if the link rate has already been reduced to the lowest supported link rate, 1.62Gbps/lane (RBR).

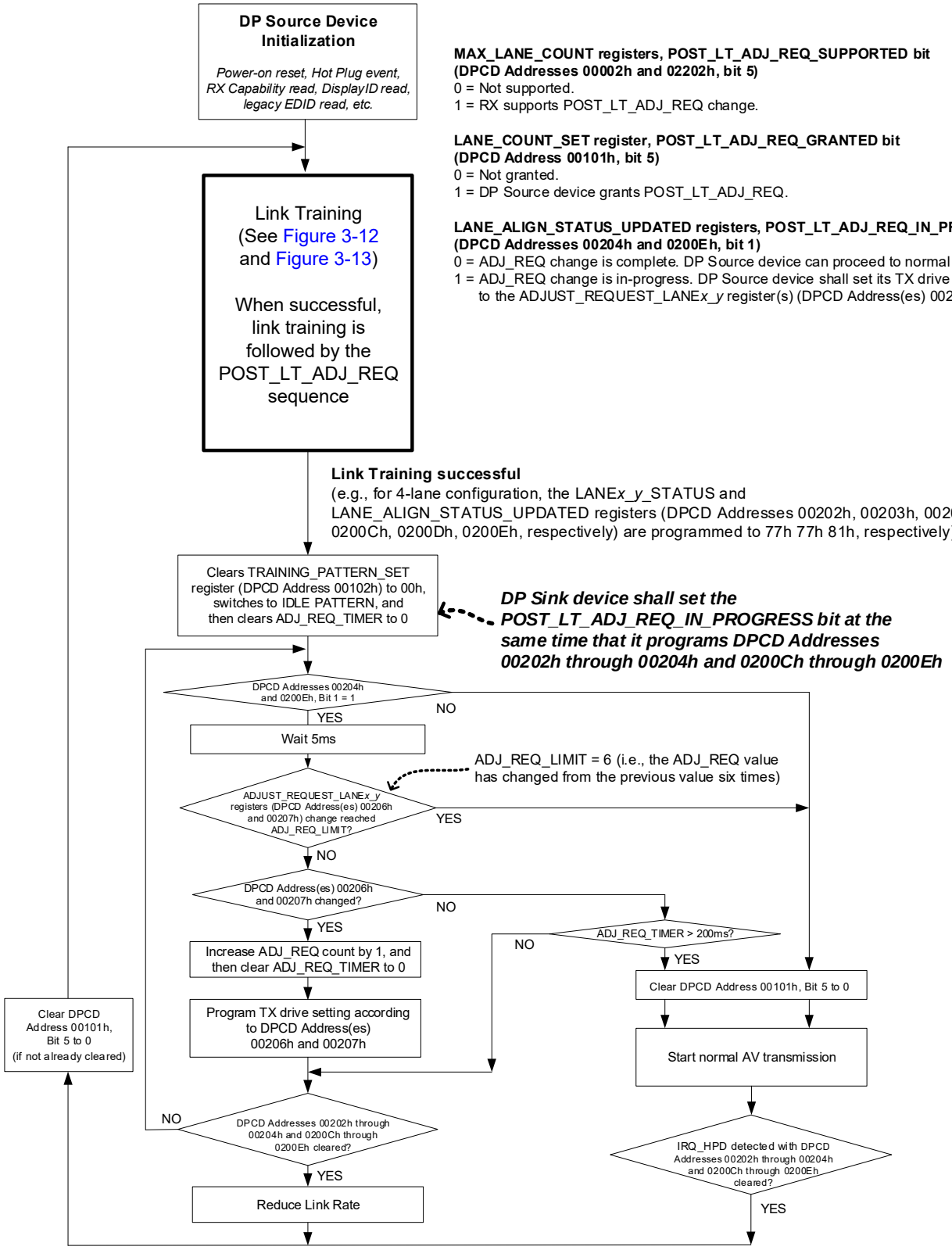


Figure 3-16: POST_LT_ADJ_REQ Sequence

3.5.1.3 Link Maintenance

During normal operation, the downstream device shall maintain the Link Status flags in the following registers:

- LANE*x_y*_STATUS register(s) (DPCD Address(es) 00202h and 00203h)
- LANE*x_y*_STATUS_ESI register(s) (DPCD Address(es) 0200Ch and 0200Dh)
- LANE_ALIGN_STATUS_UPDATED register (DPCD Address 00204h)
- LANE_ALIGN_STATUS_UPDATED_ESI register (DPCD Address 0200Eh)

After losing synchronization with the upstream device for any reason other than after receiving a request to program the SET_POWER_STATE field in the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h, bits 2:0) to 10b, –or– to request link retraining, the downstream device shall do the following:

1 Clear the INTERLANE_ALIGN_DONE bit in the LANE_ALIGN_STATUS_UPDATED and LANE_ALIGN_STATUS_UPDATED_ESI register(s) (DPCD Address(es) 00204h and 0200Eh, respectively, bit 0).

2 Issue a distinct IRQ_HPD (i.e., distinct from an IRQ_HPD issued for any other reason).

The transmitter shall check the link status whenever it detects a low-going IRQ_HPD pulse during normal operation, and perform link retraining as needed. The link status check is performed by reading status-related registers located at DPCD Addresses 00200h through 00205h –or– 02002h, 02003h, and 0200Ch through 0200Fh.

See Appendix C for Link Quality Management recommendations.

3.5.1.4 Link Quality Measurement (Testability)

The DPTX shall be able to transmit test patterns for link quality measurement purposes as indicated in Section 2.12.4.5. The DPTX indicates which test pattern (if any) is currently active on each lane, by writing to the Lane's LINK_QUAL_PATTERN_SET field in the LINK_QUAL_LANE*x*_SET register(s) (DPCD Address(es) 0010Bh through 0010Eh, bits 6:0). Using these registers to determine which test pattern is being received, the DPRX shall support the following:

- **Recovered Link Clock Quality Measurement** – Outputs the recovered link clock from a test pad when the upstream DP device writes to the RECOVERED_CLOCK_OUT_EN bit in the TRAINING_PATTERN_SET register (DPCD Address 00102h, bit 4). The output clock frequency shall be 1/40 of the link clock frequency.

  The purpose of this test output is to enable a simple EYE test for jitter measurements with minimal equipment for embedded applications using the recovered clock from the CDR circuits in the receiver. This output is not intended to be used for compliance purposes. Such testing is specified in *PHY CTS*.

  This test output should support a minimum of 10pF of parasitic capacitance including the capacitance of the test probe. The test output should add no more than the following peak-to-peak jitter, accumulated for a period of 250UI to facilitate 3% measurement accuracy (±1.5%):

  - **HBR3** – 4ps
  - **HBR2** – 6ps
  - **HBR** – 11ps
  - **RBR** – 18ps

  For example, if a single-ended output pad is desired, the test pad would need a minimum slew rate of 1.82V/ns into the maximum expected capacitive load, and can have no more than 20mVp-p of total power supply noise. If the same pad can support 3.64V/ns, then 40mVp-p power supply noise can be tolerated.
- **Link Symbol Error Rate Measurement** – Count of the number of unscrambled data symbols that are not 00h when the upstream DP device writes 010b to each enabled lane's LINK_QUAL_LANE*x*_SET register, and stores that count in the SYMBOL_ERROR_COUNT_LANE*x* registers (DPCD Addresses 00210h through 00217h; each register is composed of two bytes, within which the error count is stored in the 15 least significant bits). Link quality can be estimated using the procedure listed in Section 2.12.4.5.
- When the downstream device is receiving the PRBS7 pattern or CP2520 PHY Layer Compliance EYE pattern, it shall count the number of bits (PRBS7) or symbols (CP2520 PHY Layer Compliance EYE pattern) that do not match the appropriate pattern. This count is also stored in the SYMBOL_ERROR_COUNT_LANE*x* registers.

Any time that the link is trained and the downstream device is not receiving the Symbol Error Rate Measurement, PRBS7, or CP2520 PHY Layer Compliance EYE pattern, the downstream device shall increment the counter(s) in the SYMBOL_ERROR_COUNT_LANE*x* registers when an invalid 8b/10b symbol is received. The SYMBOL_ERROR_COUNT_SEL field in the TRAINING_PATTERN_SET register (DPCD Address 00102h, bits 7:6) values determine which errors to include:

- 00b = Count Disparity and Illegal Symbol errors.
- 01b = Count Disparity errors only.
- 10b = Count Illegal Symbol errors only.
- 11b = RESERVED.

3.5.1.5 8b/10b Channel Coding RS (254, 250) Forward Error Correction

New to *DP v1.4*, the RS(254, 250) Forward Error Correction (FEC) function, with a symbol size of 10 bits that is capable of correcting up to two RS symbol errors per FEC block of 254 RS symbols, is an optional feature that can be added to the Main-Link PHY Logical Sub-block.

FEC shall be used for transporting DSC bitstreams. Because FEC is a Main-Link PHY Logical Sub-block function, it is agnostic to the contents of link symbols. Therefore, FEC is applicable to:

- SST mode
- MST mode
- Uncompressed video stream transport
- DSC bitstream transport

The DPTX shall **not** enable FEC encoding until after link training completes.

3.5.1.5.1 DPTX FEC Encoding

New to *DP v1.4*. Updated in *DP v1.4a*.

FEC encoding in a DPTX is a DP Main-Link PHY Logical Sub-block function that occurs after 8b/10b encoding, as illustrated in Figure 3-17. The 10-bit input to the FEC encoder is the 8b/10b encoder's 10-bit output, as illustrated in Figure 3-4. Note that bit *j* is the msb and bit *a* is the lsb. When FEC encoding is enabled, a DPTX's Link Layer block generates the following symbols:

- Link Layer (LL) link symbols (either Stream Valid/Stuffing data link symbols, –or– Stream Framing control link symbols)
- FEC_PM link symbols
- FEC_PARITY_PH (FEC parity place holder) link symbols

Neither an HDCP encryption cipher nor scrambler LFSR (including the DP MST Control Link Symbol Index scrambler) advances in link symbol clock cycles carrying FEC_PARITY_PH link symbols that are replaced with FEC parity codes in the FEC encoder within the Main-Link PHY Logical Sub-block. Besides, neither the HDCP cipher nor scrambler LFSR (including the DP MST Control Link Symbol Index scrambler) advances in link symbol clock cycles carrying FEC_DECODE_EN and/or FEC_DECODE_DIS control link symbol sequences. Furthermore, FEC_PARITY_PH link symbols shall be dropped before the 8b/10b encoder. The scrambler LFSR shall advance in the link symbol clock cycle, carrying the FEC_PM. The HDCP cipher shall **not** advance in the link symbol clock cycle carrying the FEC_PM. (See Figure 3-17.)

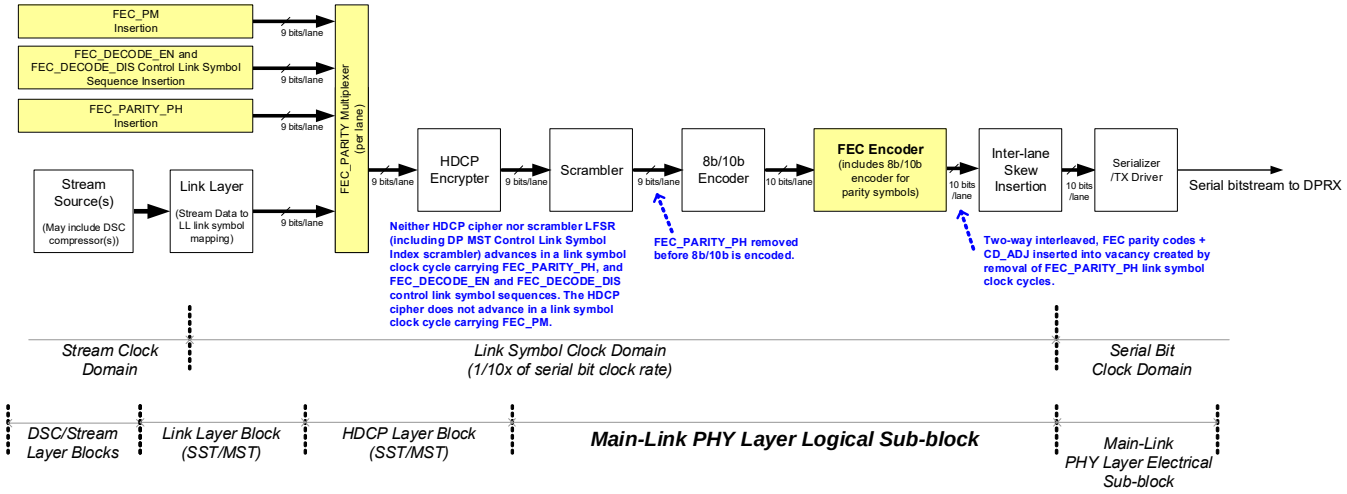


Figure 3-17: DPTX FEC Encoding (Logical View)

3.5.1.5.2 DPRX FEC Decoding

New to *DP v1.4*. Updated in *DP v1.4a*.

FEC decoding in a DPRX is a DP Main-Link PHY Logical Sub-block function that occurs before 8b/10b decoding, as illustrated in Figure 3-18. When FEC decoding is enabled, a DPRX's Main-Link PHY Logical Sub-block performs FEC decoding and removes the FEC parity codes and CD_ADJ code. After 8b/10b decoding, the Main-Link PHY Logical Sub-block inserts FEC_PARITY_PH link symbols into the vacancy created by removing the FEC parity codes and CD_ADJ code. Neither an HDCP encryption cipher nor scrambler LFSR (including the DP MST Control Link Symbol Index scrambler) advances in link symbol clock cycles carrying FEC_PARITY_PH link symbols that are discarded by the Link Layer block. Similarly, neither the HDCP encryption nor the scrambler LFSR (including the DP MST Control Link Symbol Index scrambler) advance during the FEC_DECODE_EN and/or FEC_DECODE_DIS control link symbol sequences. Additionally, the HDCP cipher shall **not** advance in the link symbol clock cycle carrying the FEC_PM.

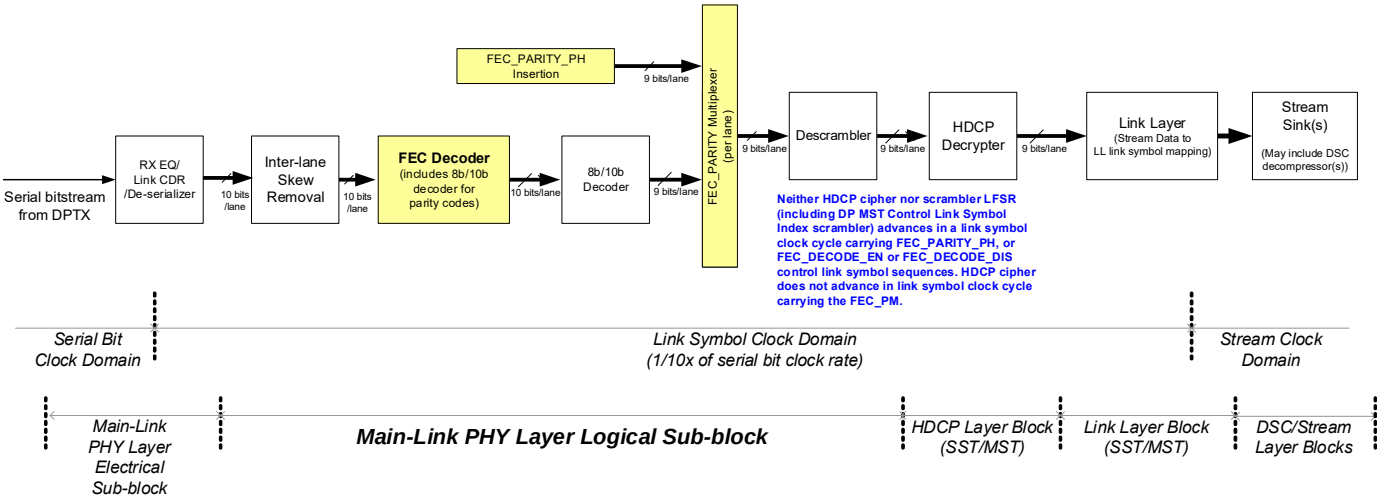


Figure 3-18: DPRX FEC Decoding (Logical View)

3.5.1.5.3 RS(254, 250) FEC Polynomial and Test Vectors

New to *DP v1.4*.

The following equation represents the polynomial of *DP v1.4a* and higher RS(254, 250) FEC:

$$G(x) = (x - 1)(x - \alpha)(x - \alpha^2)(x - \alpha^3) = x^4 + g_3 \times x^3 + g_2 \times x^2 + g_1 \times x + g_0$$

where:

- $G(x) = x^{10} + x^3 + 1$ is a primitive polynomial over $GF(2^{10})$
- α is a root of the primitive polynomial
- $g_3 = 15$, $g_2 = 54$, $g_1 = 120$, and $g_0 = 64$ (all in decimal)

Figure 3-19 illustrates the schematic RS encoder representation. Before starting the calculation, a DPTX shall initialize all registers to 0s, and then transmit the register contents when the data ends. In Figure 3-19, Data0 is the first 10 bits and Data249 is the last 10 bits. P3 is the most significant parity symbol and P0 the least significant parity symbol.

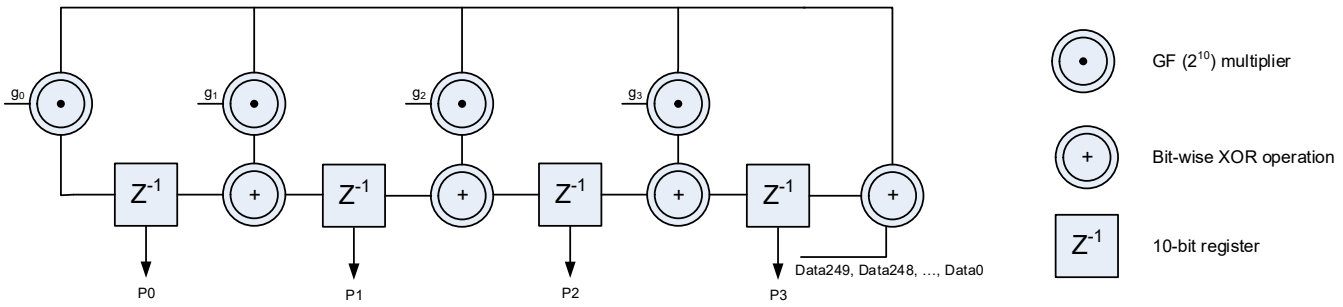


Figure 3-19: Schematic RS Encoder Representation for 8b/10b (Informative)

Table 3-12 lists four test vectors, which are provided for informative purposes. All values listed are in decimal. The leftmost is Data0. The rightmost is Data249.

Table 3-12: RS(254, 250) FEC Test Vectors (Informative)

Test Vector 1	Test Vector 2	Test Vector 3	Test Vector 4
FEC_ENC_D = [0,0,…,0,1]	FEC_ENC_D = [1,0,…,0]	FEC_ENC_D = [1,2,3,4,…,249,250]	FEC_ENC_1ST_D = [251,252,253,254…,499,500]
FEC_ENC_P3 = 15	FEC_ENC_P3 = 40	FEC_ENC_P3 = 77	FEC_ENC_P3 = 311
FEC_ENC_P2 = 54	FEC_ENC_P2 = 447	FEC_ENC_P2 = 905	FEC_ENC_P2 = 356
FEC_ENC_P1 = 120	FEC_ENC_P1 = 252	FEC_ENC_P1 = 863	FEC_ENC_P1 = 836
FEC_ENC_P0 = 64	FEC_ENC_P0 = 362	FEC_ENC_P0 = 96	FEC_ENC_P0 = 536

3.5.1.5.4 Two-way Interleaving

New to *DP v1.4*. Updated in *DP v1.4a*.

To improve immunity against transport bit errors that can become bursty errors due to the DPRX's Decision Feedback Equalizer (DFE), DisplayPort shall use two-way interleaving for RS(254, 250) FEC.

For 2- and 4-lane configurations, a DPTX shall generate an interleaved FEC block consisting of 256 8b/10b codes.

For 1-lane configuration, a DPTX shall combine two FEC blocks of 254 RS symbols each to formulate an interleaved FEC block consisting of 512 8b/10b codes, as listed in Table 3-13.

A DPTX shall insert an FEC parity marker (FEC_PM, K28.1) every 256th interleaved FEC block for 2- and 4-lane configurations, and every 128th interleaved FEC block for 1-lane configuration.

The resulting total FEC overhead is 2.4% (i.e., an FEC-enabled DP link has 2.4% less link bandwidth available for transport of stream(s)).

Table 3-13: Interleaved FEC Block for 4-, 2-, and 1-lane Configurations

Configuration	Interleaved FEC Block Generated	Interleaved FEC Block Transported	FEC_PM Insertion
2- or 4-lane	250 RS data symbols + 4 RS parity symbols	250 LL codes[a] + 5 FEC parity codes + CD_ADJ code	Every 256th interleaved FEC block transported (= every 65537th 8b/10b code[b])
1-lane	2 × 250 RS data symbols + 2 × 4 RS parity symbols	2 × 250 LL codes[a] + 11 FEC parity codes + CD_ADJ code	Every 128th interleaved FEC block transported (= every 65537th 8b/10b code[b])

a. 8b/10b-encoded LL link symbols.
b. Every 81us at 8.1Gbps/lane and every 121us at 5.4Gbps/lane.

Figure 3-20 illustrates the interleaved FEC block transport for 2- and 4-lane configurations.
Figure 3-21 illustrates the interleaved FEC block transport for 1-lane configuration.

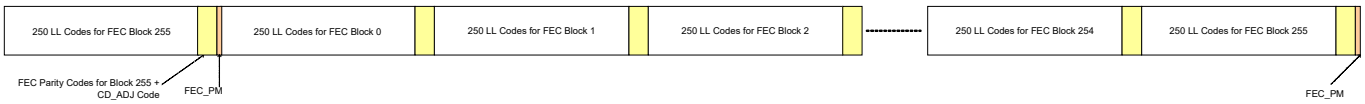


Figure 3-20: Interleaved FEC Block Transport for 2- and 4-lane Configurations

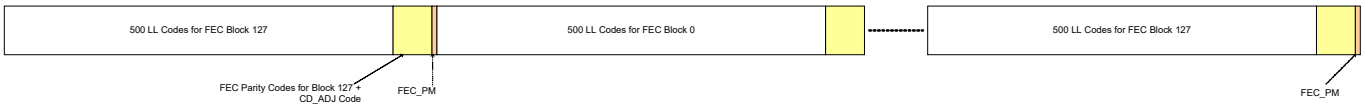


Figure 3-21: Interleaved FEC Block Transport for 1-lane Configuration

Figure 3-22 and Figure 3-23 illustrate two-way interleaving in a DPTX and DPRX, respectively, for 2- and 4-lane configurations. For 4-lane configuration, the diagram illustrated in those figures is duplicated.

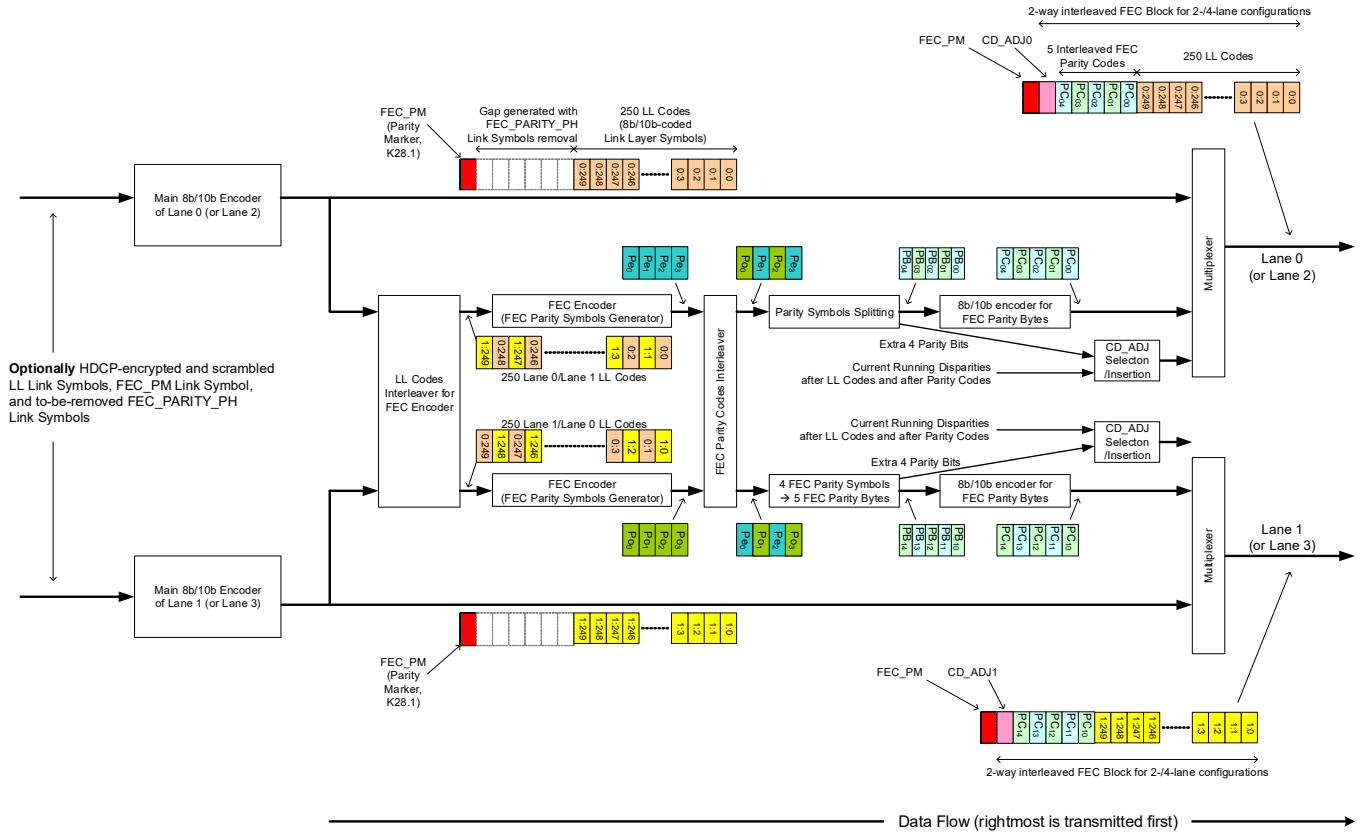


Figure 3-22: Two-way FEC Interleaving for 2- and 4-lane Configurations in DPTX

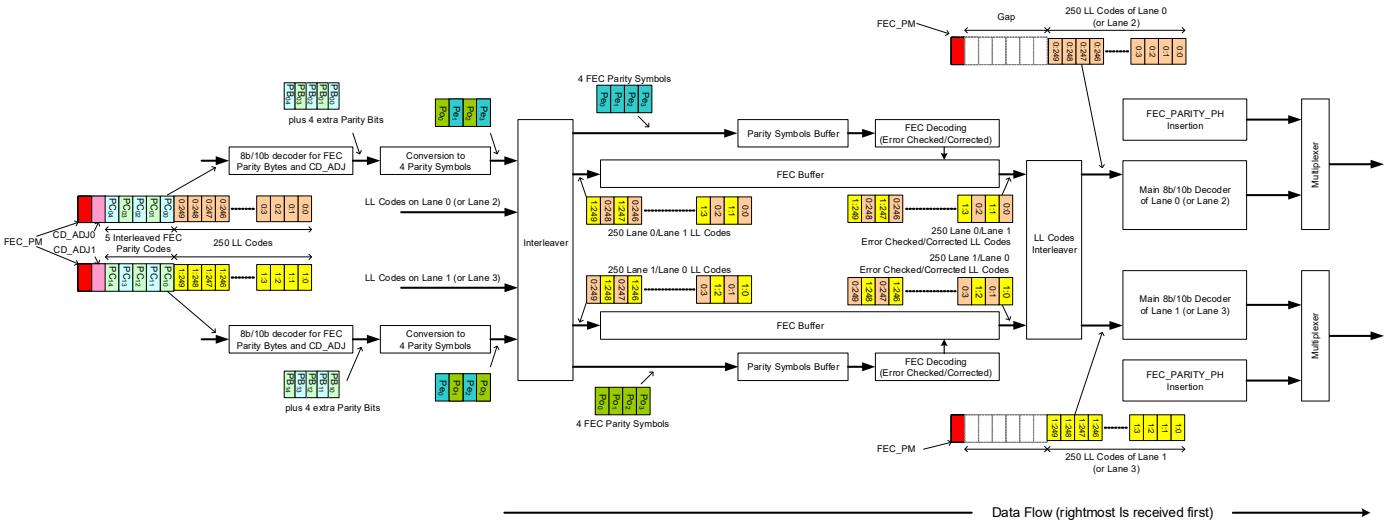


Figure 3-23: Two-way FEC Interleaving for 2- and 4-lane Configurations in DPRX

Figure 3-24 and Figure 3-25 illustrate two-way interleaving in a DPTX and DPRX, respectively, for a 1-lane configuration.

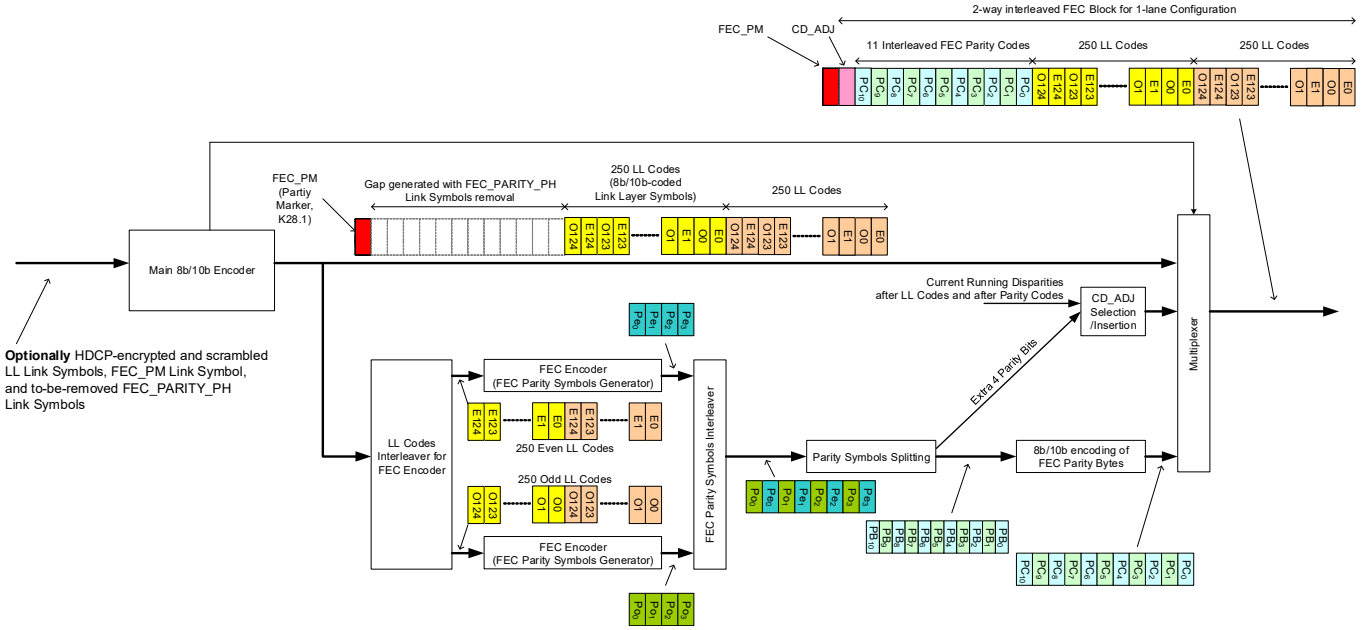


Figure 3-24: Two-way FEC Interleaving for 1-lane Configuration in DPTX

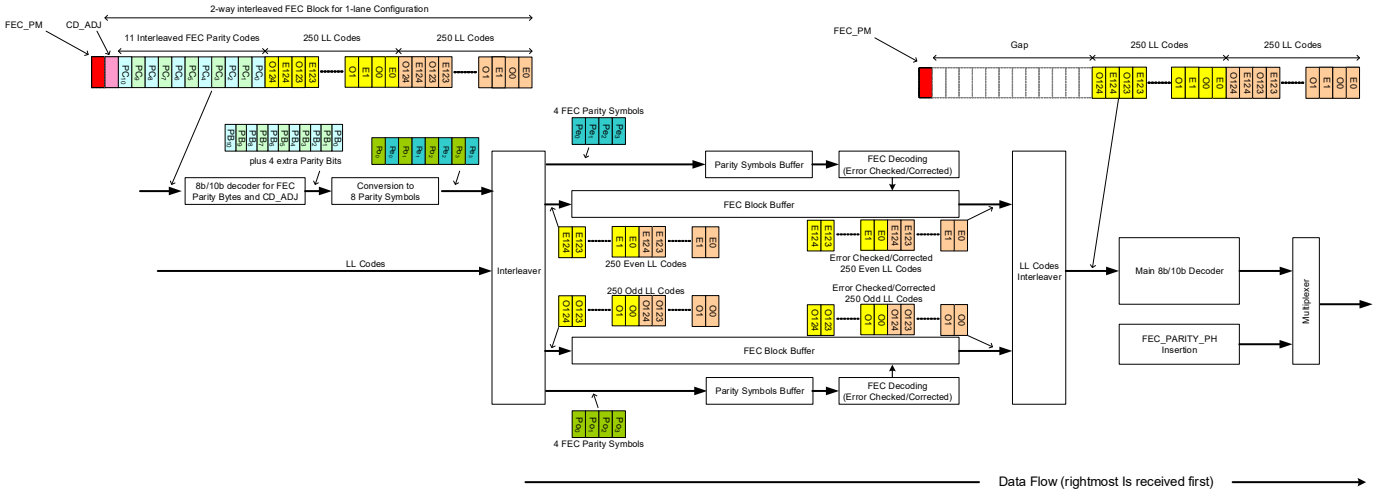


Figure 3-25: Two-way FEC Interleaving for 1-lane Configuration in DPRX

As illustrated in Figure 3-22 through Figure 3-25, a DPTX shall interleave LL codes to be transported for FEC encoding. For FEC parity symbols:

- **2- and 4-lane configurations** – A DTPX shall interleave the four FEC parity symbols from two FEC Encoders, split each to five parity bytes and four extra parity bits as listed in Table 3-14, and 8b/10b-encode for transport.
- **1-lane configuration** – A DPTX shall interleave the four FEC parity symbols from two FEC encoders, split them into 11 parity bytes and four extra parity bits as listed in Table 3-15, and 8b/10b-encode for transport.

Four 10-bit RS(254, 250) parity symbols are mapped to PE*x* and PO*x* (where *x* is 0, 1, 2, or 3) in Table 3-14 and Table 3-15, as follows:

- P3 → PE3 and PO3
- P2 → PE2 and PO2
- P1 → PE1 and PO1
- P0 → PE0 and PO0

Note: *Prior to RS(254, 250) error detection/correction, the DPRX will strip out the 0 bits that the DPTX inserted into the parity bytes. As a result, bit errors that affect these bits on the link will* ***not*** *be counted as part of the FEC Error Counters described in Section 3.5.3.3.*

When a single FEC parity byte has parity symbol bits from multiple parity symbols, the bits from one parity symbol may affect both sub-blocks (the 3- and 5-bit sub-blocks) of the 8b/10b data code word.

The initial disparity of the first Parity Code (i.e., PC0) after the RS data block shall be the current running disparity of the last LL code in the RS data block. The disparity of parity codes thereafter shall follow standard 8b/10b encoding rules. See also the CD_ADJ code selection table (see Table 3-16) used for the CD_ADJ 8b/10b code selection to avoid having the current disparity error start at the next RS data block.

Table 3-14: Parity Symbols Interleaving and Splitting in 2- and 4-lane Configurations

Parity Bytes and Extra Bits	Parity Symbols Bits Contained	Parity Codes
Lane 0 (or Lane 2)		
PB00	PE3[9:2]	PC00
PB01	0 | PO2[9:3]	PC01
PB02	PE1[9:5] | PO2[2:0]	PC02
PB03	PE1[4:0] | 000	PC03
PB04	PO0[7:0]	PC04
Extra four bits	PO0[9:8] | PE3[1:0]	Part of CD_ADJ0
Lane 1 (or Lane 3)		
PB10	PO3[9:2]	PC10
PB11	0 | PE2[9:3]	PC11
PB12	PO1[9:5] | PE2[2:0]	PC12
PB13	PO1[4:0] | 000	PC13
PB14	PE0[7:0]	PC14
Extra four bits	PE0[9:8] | PO3[1:0]	Part of CD_ADJ1

Table 3-15: Parity Symbols Interleaving and Splitting in 1-lane Configuration

Parity Bytes and Extra Bits	Parity Symbols Bits Contained	Parity Codes
PB0	PE3[9:2]	PC0
PB1	PO3[9:5] | PE3[1:0] | 0	PC1
PB2	PO3[4:0] | 000	PC2
PB3	PE2[9:2]	PC3
PB4	PO2[9:5] | PE2[1:0] | 0	PC4
PB5	PO2[4:0] | 000	PC5
PB6	PE1[9:2]	PC6
PB7	0 | PO1[9:3]	PC7
PB8	PE0[9:5] | PO1[2:0]	PC8
PB9	PE0[4:0] | 000	PC9
PB10	PO0[7:0]	PC10
Extra four bits	PO0[9:8] | PE1[1:0]	Part of CD_ADJ

For CD_ADJ code determination, a DPTX shall incorporate the four extra parity bits into CD_ADJ, as listed in Table 3-16. The case number is defined by the currently running disparity (i.e., the number of accumulated 1s relative to the number of accumulated 0s, the disparity is either two extra 1s or equal as per the 8b/10b coding rule) at the end of LL codes and parity codes. (See Table 3-17.) See Section 3.1.7 for the *Zxx.y*- and *Zxx.y*+ notation definition.

Table 3-16: CD_ADJ Code Selection

Extra Four Bits (PXx[9:8] | PYy[1:0])[a]		Case Number[b]			
		1	2	3	4
00	00	D3.1	D3.0+	D3.1	D3.0-
00	01	D5.1	D5.0+	D5.1	D5.0-
00	10	D10.1	D10.0+	D10.1	D10.0-
00	11	D12.1	D12.0+	D12.1	D12.0-
01	00	D3.2	D2.3+	D3.2	D2.3-
01	01	D5.2	D4.3+	D5.2	D4.3-
01	10	D10.2	D8.3+	D10.2	D8.3-
01	11	D12.2	D15.3+	D12.2	D15.3-
10	00	D3.5	D3.4+	D3.5	D3.4-
10	01	D5.5	D5.4+	D5.5	D5.4-
10	10	D10.5	D10.4+	D10.5	D10.4-
10	11	D12.5	D12.4+	D12.5	D12.4-
11	00	D3.6	D3.7+	D3.6	D3.7-
11	01	D5.6	D5.7+	D5.6	D5.7-
11	10	D10.6	D10.7+	D10.6	D10.7-
11	11	D12.6	D12.7+	D12.6	D12.7-

a. See Table 3-14 and Table 3-15 for parity symbol bit mapping.
b. See Table 3-17 for case number definitions.

Table 3-17: CD_ADJ Selection Case Definition

Description	Case Number			
	1	2	3	4
Current Running Disparity after the Last LL Code	Two extra 1s	Equal	Equal	Two extra 1s
Current Running Disparity after the Last Parity Code	Two extra 1s	Two extra 1s	Equal	Equal

The extra two bits, P*Xx*[9:8], have been mapped to CD_ADJ's HG bits. The other two extra bits, P*Yy*[1:0], have been mapped to CD_ADJ's DC bits. The remaining CD_ADJ bits have been chosen to keep the running disparity consistent with the state at the end of the LL codes.

With the FEC parity code interleaving and splitting method described above, only one FEC parity symbol per RS(254, 250) block becomes corrupted when two consecutive FEC parity codes are corrupted over the DP link.

To account for the overhead of FEC parity codes and CD_ADJ code per interleaved FEC block, a DPTX shall insert FEC_PARITY_PH link symbols in the Link Layer block, as follows:

- **4- and 2-lane configurations** – 6 FEC_PARITY_PH symbols after every 250 LL link symbols
- **1-lane configuration** – 12 FEC_PARITY_PH symbols after every 500 LL link symbols

Additionally, a DPTX shall insert an FEC_PM link symbol in the Link Layer block, as follows:

- **4- and 2-lane configurations** – Once every 256th interleaved FEC block
- **1-lane configuration** – Once every 128th interleaved FEC block

A DPTX shall **not** advance either HDCP cipher or scrambler LFSR (both Data Link Symbol scrambler and MST Control Link Symbol Index scrambler) in those link symbol clock cycles for FEC_PARITY_PH link symbols. Furthermore, a DPTX shall remove the FEC_PARITY_PH link symbols before the main 8b/10b encoding to generate a gap in which to insert FEC parity codes and the CD_ADJ code.

A DPRX shall interleave the received LL codes and FEC parity codes for FEC decoding. It shall then 8b/10b decode the five FEC parity codes per FEC decoder to five FEC parity bytes and four FEC parity symbols for FEC decoding.

As part of the FEC decoding, a DPRX shall remove FEC parity codes and the CD_ADJ code. Consequently, the gap left by removing these symbols shall have no effect on the 8b/10b decoding, including any running disparity calculation. After the 8b/10b decoder, the DPRX shall insert FEC_PARITY_PH link symbols into the vacancy created by removing the FEC parity codes and CD_ADJ code. A DPRX shall **not** advance either scrambler LFSR (both Data Link Symbol scrambler and MST Control Link Symbol Index scrambler) or HDCP cipher into those link symbol clock cycles for FEC_PARITY_PH link symbols.

A DPRX Link Layer block shall discard both FEC_PARITY_PH link symbols and the FEC_PM link symbol.

3.5.1.5.5 Enabling/Disabling FEC Encoding/Decoding

New to *DP v1.4*. Updated in *DP v2.0*.

An FEC-capable DPTX discovers whether a plugged DPRX is FEC-capable by reading the FEC_CAPABLE bit in the FEC_CAPABILITY_0 register (DPCD Address 00090h, bit 0).

A DPTX that is plugged to an FEC-capable DPRX and anticipates enabling FEC encoding shall set the FEC_READY bit in the FEC_CONFIGURATION register (DPCD Address 00120h, bit 0) to 1 before initiating link training.

The DPTX may switch from SST to MST mode (or vice versa) after link training is complete, as described in Section 2.6.10.3. The DPTX shall disable FEC encoding by transmitting an FEC_DECODE_DIS control link symbol sequence over the Main-Link before the SST/MST mode switch.

The DPTX may disable the Main-Link without transmitting an FEC_DECODE_DIS control link symbol sequence. After link training is complete, the DPTX, if it needs to enable FEC encoding, shall transmit an FEC_DECODE_EN control link symbol sequence to indicate the start of FEC encoding, regardless of whether the DPTX transmitted an FEC_DECODE_DIS control link symbol sequence before disabling the Main-Link.

A DPRX that supports this new capability (FEC_ERROR_REPORTING_POLICY_SUPPORTED bit in the FEC_CAPABILITY_0 register (DPCD Address 00090h, bit 6) is set to 1) shall increase the FEC_RUNNING_INDICATOR (i.e., set bit 2 in the FEC_STATUS register (DPCD Address 00280h)) within an upper time limit of 5ms from the moment that the FEC circuit was enabled (i.e., immediately after an FEC_DECODE_EN control link symbol sequence was detected). The DPRX shall hold the FEC_RUNNING_INDICATOR asserted until one of the following conditions exists:

- FEC_DECODE_DIS control link symbol sequence was detected, –or–
- DPRX was placed in Low Power mode by the SET_POWER_STATE field in the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h, bits 2:0) being programmed to 001b
- Link loss occurred

After the FEC_READY bit is set, the DPRX shall delay LL code forwarding to the main 8b/10b decoder and descrambler block by the same amount of time needed for FEC decoding, even when it is not performing FEC decoding (that is, the DPRX shall ensure that enabling and disabling of FEC decoding is transparent to its HDCP decryption block and Link Layer block). Furthermore, although there are no FEC-related non-LL 8b/10b codes transmitted on the link until the FEC_DECODE_EN control link symbol sequence is transmitted, the DPTX shall **not** use more than 97.6% of the available link bandwidth for transmitting Stream Valid data link symbols and Stream Framing control link symbols after it starts transmitting one or more stream(s) to avoid the link bandwidth oversubscription on FEC_DECODE_EN control link symbol sequence transmission. Reduction of the peak Stream Valid data link symbols/Stream Framing control link symbols transmission rate causes a reduction in the number of link symbol clock cycles (or time slots) occupied by those link symbols per micro-packet, and a corresponding increase in the number of Stream Stuffing link symbols. For video stream transport, the DPTX may spread the Stream Valid data link symbol transmission by delaying the BS symbol sequence transmission to transmit the same number of Stream Valid data link symbols per video horizontal line period during the video vertical active period.

An FEC-capable LTTPR shall snoop AUX requests that address the FEC_CONFIGURATION register. When the register's FEC_READY bit is set, the FEC-capable LTTPR shall delay LL-code forwarding to the main 8b/10b decoder and descrambler block by the same amount of time that is needed for FEC decoding, even when it is not performing FEC decoding, to ensure that enabling and disabling of FEC decoding is transparent to the DPRX's HDCP decryption and Link Layer blocks.

To prompt a DPRX and LTTPR to enable FEC decoding, a DPTX shall insert the FEC_DECODE_EN control link symbol sequence listed in Table 3-18 into the FEC_PARITY multiplexer (see Figure 3-17 on page 759). Neither HDCP cipher nor scrambler LFSR (including the DP MST Control Link Symbol Index scrambler) advances in a link symbol clock cycle carrying the FEC_DECODE_EN control link symbol sequence. The symbol immediately following the FEC_DECODE_EN control link symbol sequence is the first LL code of the first FEC-encoded block. Following the FEC_DECODE_EN control link symbol sequence, each interleaved FEC block should be transmitted along with the associated FEC parity codes and CD_ADJ. The next FEC_PM should occur after the 256^{th} interleaved FEC block (4- or 2-lane configuration), or 128^{th} interleaved block (1-lane configuration). The FEC_DECODE_EN control link symbol sequence can first be transmitted anytime after 1000 LL codes have been transmitted on the link after training completion. Figure 3-26 illustrates the FEC_DECODE_EN control link symbol sequence for 4- and 2-lane configurations.

FEC decoding can be disabled only at the end of an FEC block that immediately precedes what would normally be the insertion of the FEC_PM symbol (i.e., after an integer number of multiples of 256 interleaved FEC blocks (4- and 2-lane configurations), or an integer number of multiples of 128 interleaved FEC blocks (1-lane configurations). To prompt a DPRX and LTTPR to disable FEC decoding, a DPTX shall transmit the FEC_DECODE_DIS control link symbol sequence listed in Table 3-18 into the FEC_PARITY multiplexer (see Figure 3-17 on page 759) instead of the normal FEC_PARITY_PH and FEC_PM codes for that interleaved FEC block. The interleaved FEC block whose FEC_PARITY_PH is replaced by the FEC_DECODE_DIS control link symbol sequence (instead of FEC parity codes and the CD_ADJ) are **not** protected by FEC parity, and therefore are **not** to be FEC-corrected. Again, neither HDCP cipher nor scrambler LFSR (including DP MST Control Link Symbol Index scrambler) advances in a link symbol clock cycle carrying the FEC_DECODE_DIS control link symbol sequence. After the FEC_DECODE_DIS control link symbol sequence is transmitted, no further FEC-related non-LL 8b/10b codes are transmitted on the link unless FEC decoding is re-enabled at a later time. Figure 3-27 illustrates the FEC_DECODE_DIS control link symbol sequence for 4- and 2-lane configurations.

The DPTX shall **not** transmit an FEC_DECODE_EN control link symbol sequence within 1000 LL codes of the last FEC_DECODE_DIS control link symbol sequence. FEC decoding may be re-enabled anytime after the 1000 LL-code delay by transmitting the FEC_DECODE_EN control link symbol sequence.

The FEC_DECODE_EN and FEC_DECODE_DIS control link symbol sequences are inserted on all lanes to enable and disable decoding, respectively. For all lane counts and for both enabling and disabling of FEC encoding/decoding, a DPTX shall place the last K28.1 of the sequence to coincide with FEC_PM.

Neither the FEC_DECODE_EN nor FEC_DECODE_DIS control link symbol sequence shall be interrupted by the insertion of LL Link Symbols.

Table 3-18: FEC_DECODE_EN and FEC_DECODE_DIS Control Link Symbol Sequences

Configuration	Control Link Symbol Sequence	
	FEC_DECODE_EN	FEC_DECODE_DIS
4- and 2-lane	K28.1 – K30.7 – K30.7 – K30.7 – K23.7 – K23.7 – K28.1	K28.1 – K23.7 – K23.7 – K23.7 – K30.7 – K30.7 – K28.1
1-lane	K28.1 – K30.7 – K30.7 – K30.7 – K23.7 – K23.7 – K28.1 – K30.7 – K30.7 – K28.1 – K23.7 – K23.7 – K28.1	K28.1 – K23.7 – K23.7 – K23.7 – K30.7 – K30.7– K28.1 – K23.7 – K23.7 – K28.1 – K30.7 – K30.7 – K28.1

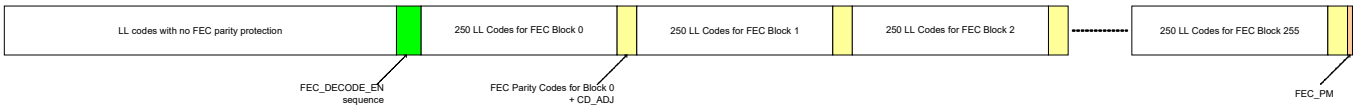


Figure 3-26: FEC_DECODE_EN Control Link Symbol Sequence Transmission (4- and 2-lane Configuration Example)

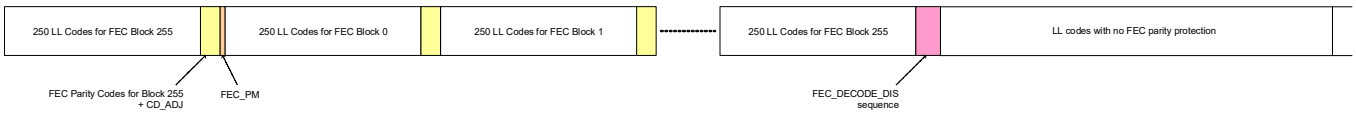


Figure 3-27: FEC_DECODE_DIS Control Link Symbol Sequence Transmission (4- and 2-lane Configuration Example)

3.5.2 Main-Link 128b/132b PHY Logical Sub-layer

New to *DP v2.0*.

This section defines the Main-Link 128b/132b PHY Logical Sub-layer (**green** boxes in Figure 3-28), including 128b/132b capability discovery and configuration through AUX transactions.

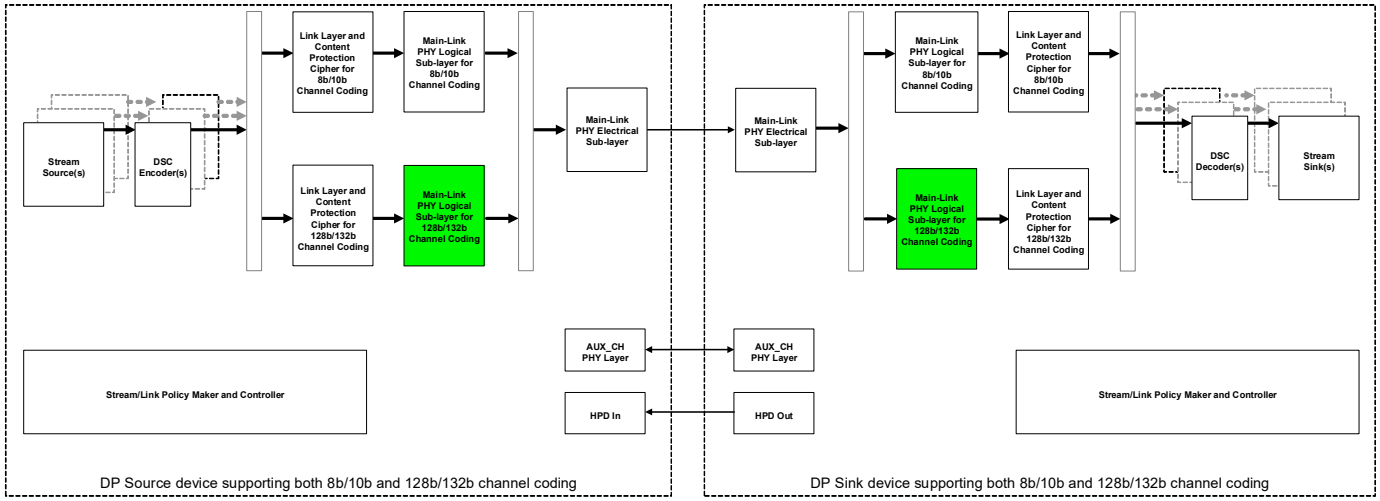


Figure 3-28: 128b/132b Link Layer-capable DP Source and Sink Device Connection, Highlighting PHY Logical Sub-layer Blocks

3.5.2.1 DPCD Registers Used for 128b/132b PHY Logical Sub-layer Capability Discovery and Configuration

Table 3-19 lists the DPCD registers that a DPRX uses for 128b/132b PHY Logical Sub-layer capability discovery and configuration. The DPRX shall revert to 8b/10b Link Layer when a power-on reset or upstream device disconnect occurs. (For complete register descriptions, see Table 2-183, Table 2-184, and Table 2-193.)

Table 3-19: DPCD Registers Used for 128b/132b PHY Logical Sub-layer Capability Discovery and Configuration

DPCD Address	Register
00000h	DPCD_REV
00002h	MAX_LANE_COUNT
00006h	MAIN_LINK_CHANNEL_CODING_CAP
00100h	LINK_BW_SET
00101h	LANE_COUNT_SET
00102h	TRAINING_PATTERN_SET
00108h	MAIN_LINK_CHANNEL_CODING_SET
02206h	MAIN_LINK_CHANNEL_CODING_CAP
02215h	128b/132b_SUPPORTED_LINK_RATES

3.5.2.2 128b/132b PHY Logical Sub-layer Operating Sequence

This section defines the high-level DPTX and DPRX 128b/132b PHY Logical Sub-layer operating sequence.

Note: *An alternate approach to the place holder method can be found in Appendix M. The resulting bitstream from both approaches will be identical.*

3.5.2.2.1 DPTX 128b/132b PHY Logical Sub-layer Operating Sequence

The operating sequence occurs in the following order (see Figure 3-29):

1 Link Layer-to-PHY Logical Sub-layer Main-Link lane count conversion.

2 Intra super symbol shifting.

3 Scrambling.

4 Control Data Indicator (CDI) field insertion.

5 RS FEC encoding.

6 2-way interleaving of RS parity bytes.

7 Pre-coding.

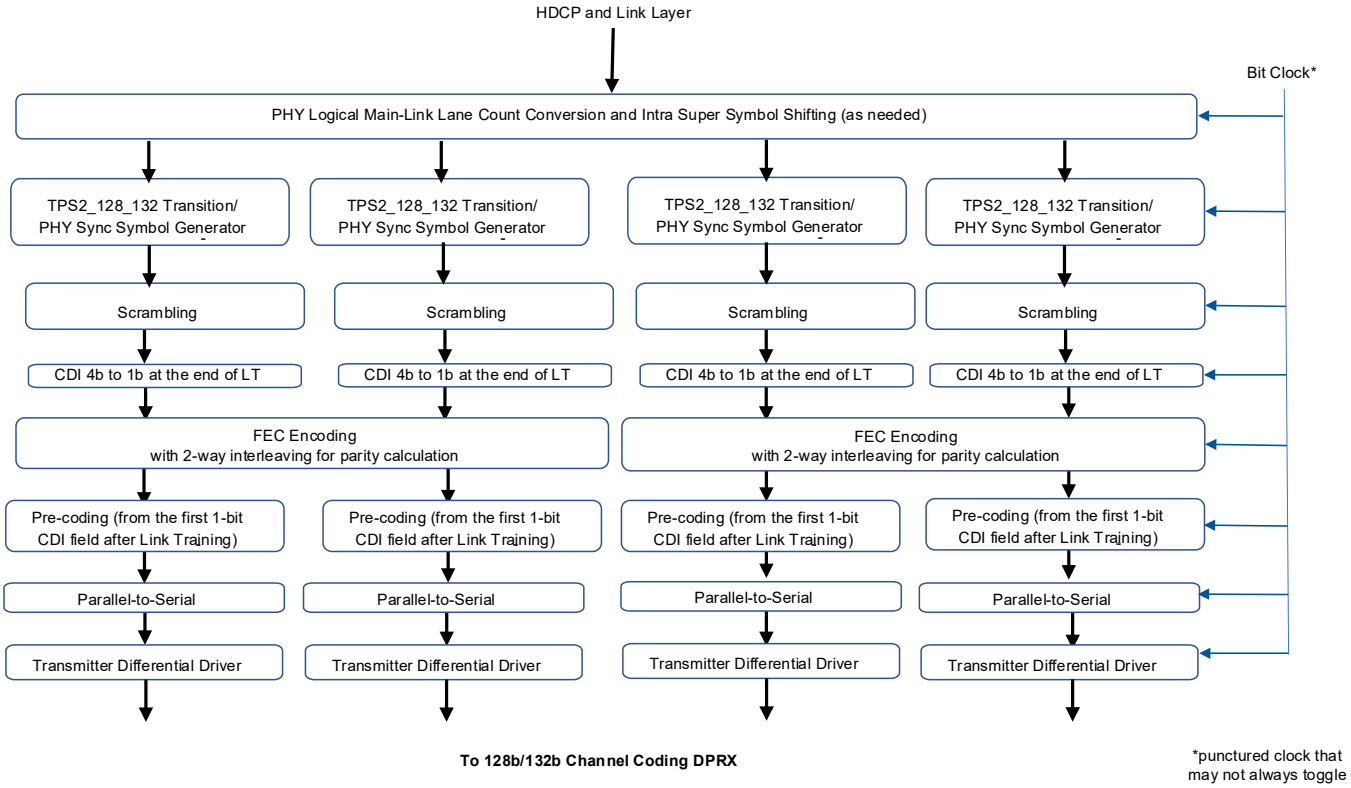


Figure 3-29: DPTX 128b/132b PHY Logical Sub-layer Diagram (Informative)

3.5.2.2.2 DPRX 128b/132b PHY Logical Sub-layer Operating Sequence

The operating sequence occurs in the following order (see Figure 3-30):

1 Pre-coding removal.

2 2-way de-interleaving of RS parity bytes.

3 RS FEC decoding.

4 CDI field parsing.

5 De-scrambling.

6 Intra super symbol reverse shifting.

7 PHY Logical Sub-layer-to-Link Layer Main-Link lane count conversion.

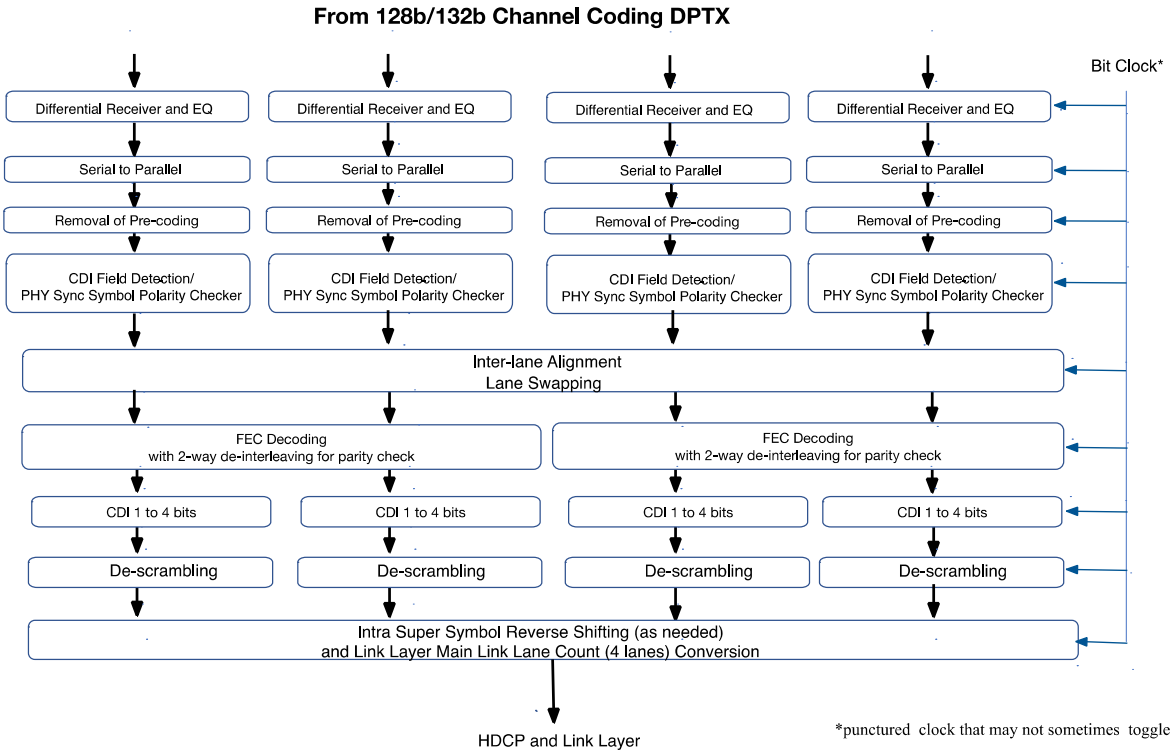


Figure 3-30: DPRX 128b/132b PHY Logical Sub-layer Diagram (Informative)

3.5.2.3 Link Symbols to 128b/132b PHY Logical Sub-layer Mapping

The 128b/132b Link Layer link symbol size is 32 bits, as defined in Section 2.7.
For 128b/132b PHY Logical Sub-layer, the 1-bit CDI field plus four 32-bit link symbols (128 bits total, referred to as "super symbol") comprises 129 information bits, per lane, as illustrated in Figure 3-31.

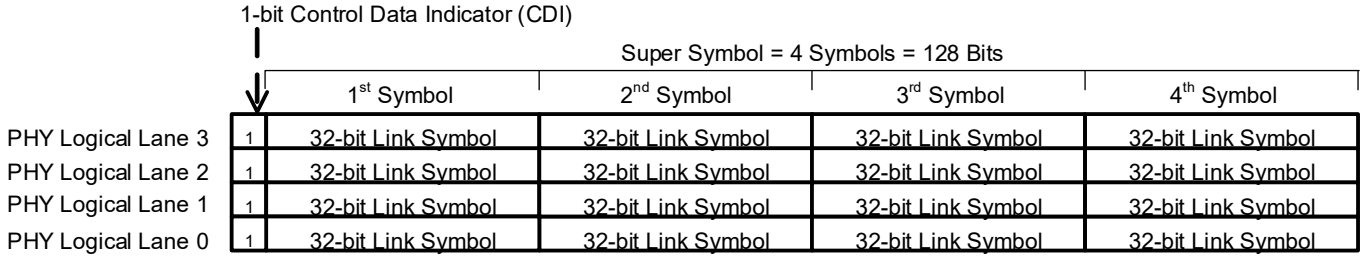


Figure 3-31: Super Symbols – 128b/132b PHY Logical Sub-layer

The CDI field size is as follows:

- Four bits during link training with link training pattern sequence 128b/132b_TPS2
- One bit after link training is complete
- Not applicable during PHY Layer electrical test patterns, –or– with link training pattern sequence 128b/132b_TPS1

When the super symbol has four data link symbols, the CDI field value is 0 or 0011b; otherwise, the value is 1 or 1100b.

3.5.2.4 Symbol Types

Table 3-20 defines the four 128b/132b PHY Logical Sub-layer 32-bit symbol types. 128b/132b Link Layer inserts place holder (PH) symbols that are either replaced with PHY sync symbols, –or– account for the channel coding overhead (CDI fields and RS symbols) in the DPTX's PHY Logical Sub-layer (see Section 3.5.2.8 for further details).

Table 3-20: 128b/132b PHY Logical Sub-layer 32-bit Symbol Types

Symbol Type	Generated By	Description
Control Link Symbol	Link Layer	• Transmitted after successful LT completion.
Data Link Symbol	Link Layer	• Transmitted during LT (fixed value of 00000000h, scrambled) and after LT • Data link symbol generation is defined in Section 2.7
RS Parity Symbol	PHY Logical Sub-layer	• Transmitted when RS FEC is enabled at LT completion • Composed of four RS(198, 194) parity bytes • Transmitted on all enabled physical lanes, once per RS block, composed of 1552 bits of RS data block (twelve 129-bit information bits (1548 bits total) plus four padded bits) and a 32-bit RS parity symbol
PHY Sync Symbol	PHY Logical Sub-layer	• Three symbol sub-types • **LT_SCRAMBLER_RESET** – Transmitted during LT • **POST_LT_SCRAMBLER_RESET** – Transmitted after LT to mark LT completion • **PHY_SYNC_ONLY** – Transmitted during and after LT • Transmitted on all enabled lanes, once every PHY Logical Frame (in total, the PHY Logical Frame has 383 link symbols and one PHY sync symbol) • PHY sync symbol is always the first symbol in a super symbol

3.5.2.5 Control Link Symbol Bit Mapping

Figure 3-32 illustrates and Table 3-21 defines the control link symbol bit mapping that is used by the 128b/132b PHY Logical Sub-layer.

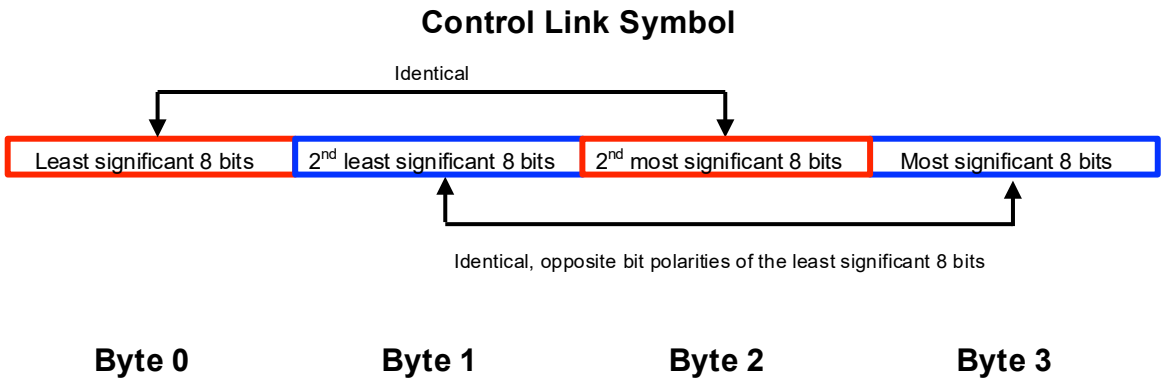


Figure 3-32: Control Link Symbol Bit Mapping – 128b/132b PHY Logical Sub-layer

Table 3-21: Control Link Symbol Bit Mapping – 128b/132b PHY Logical Sub-layer

Byte #	Bit #	Field Description
0 or 2	3:0 or 19:16	**CONTROL_LINK_SYMBOL_VALUE** 0010b = BS. 1000b = BE. 0011b = EOC. 1001b = VCPF. 0101b = SE. 1010b = LLCP_MARKER. 0110b = SS. 1011b = Active Video Fill. 0111b = SF. 0000b, 0001b, 0100b, 1100b = Used or RESERVED for PHY sync symbols. (See Section 3.5.2.6.) 1101b, 1110b, 1111b = RESERVED.
	7:4 or 23:20	**Symbol Type Vector** Valid only for the control link symbol that is mapped to the first symbol of a super symbol. See Section 3.5.2.9 for details.
1 or 3	15:8 or 31:24	Identical to Byte 0 or 2, with the bit polarities swapped. For example, if CONTROL_LINK_SYMBOL_VALUE (bits 3:0) have a value of 0001b, bits 11:8 and Bits 27:24 each have a value of 1110b.

3.5.2.6 PHY Sync Symbol Bit Mapping

A PHY sync symbol, transmitted once per PHY Logical Frame, is always placed in the 1st symbol of a super symbol. PHY sync symbol bit mapping is as follows:

- Bits 31:24 ("XY" in the hex values for the symbols listed below; see also Table 3-22) indicate the link symbol types of the 2nd, 3rd, and 4th symbols that follow the PHY sync symbol within the super symbol
- LT_SCRAMBLER_RESET symbol
  - 33CCCCCCh marks the training pattern sequence boundary
- POST_LT_SCRAMBLER_RESET symbol after LT completion
  - 33F0F0F0h marks the end of the training pattern sequence and PHY Logical Frame boundary
  - XY111111h marks the PHY Logical Frame boundary
  - Replaces every 64th PHY_SYNC_ONLY symbol after LT completion
- PHY_SYNC_ONLY symbol
  - 333C3C3Ch marks the PHY Logical Frame boundary during LT
  - XY444444h marks the PHY Logical Frame boundary after LT completion

Table 3-22 defines the bit 31:24 value (XYh) mapping of PHY sync symbols to 2nd, 3rd, and 4th symbol types.

Table 3-22: PHY Sync Symbol Bit [31:24] XYh Value to 2nd, 3rd, and 4th Symbol Type Mapping

XYh Value	Symbol Type		
	2nd	3rd	4th
54h	Data	Data	Data
5Eh	Control	Data	Data
AAh	Data	Control	Data
22h	Control	Control	Data
ABh	Data	Data	Control
FFh	Control	Data	Control
55h	Data	Control	Control
89h	Control	Control	Control

3.5.2.7 Conversion to PHY Logical Main-Link Lane Count

As defined in Section 2.7, the Link Layer always performs stream data-to-link symbol mapping for a 4-lane Main-Link. The PHY Logical Sub-layer converts the lane count to a physical lane count, as illustrated in Figure 3-33, Figure 3-34, Figure 3-35 for four, two, and one physical lane configurations, respectively. The interval between link symbols in the Link Layer is inversely proportional to the physical lane count, as illustrated in the figures.

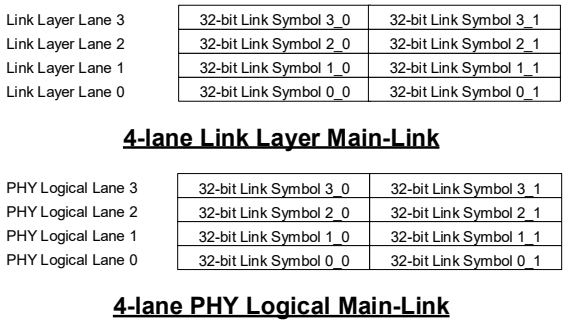


Figure 3-33: Four Physical Lanes (Link Symbols Shown)

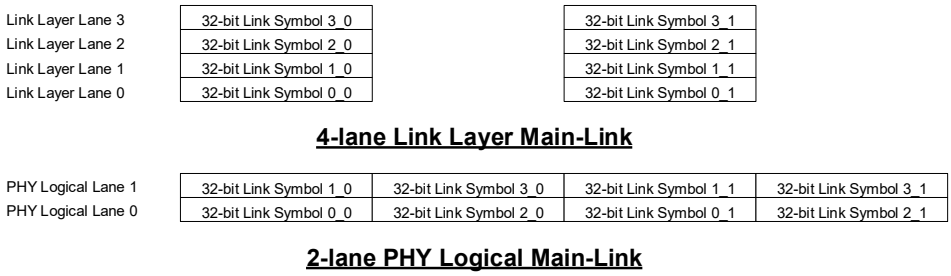


Figure 3-34: Conversion to Two Physical Lanes (Link Symbols Shown)

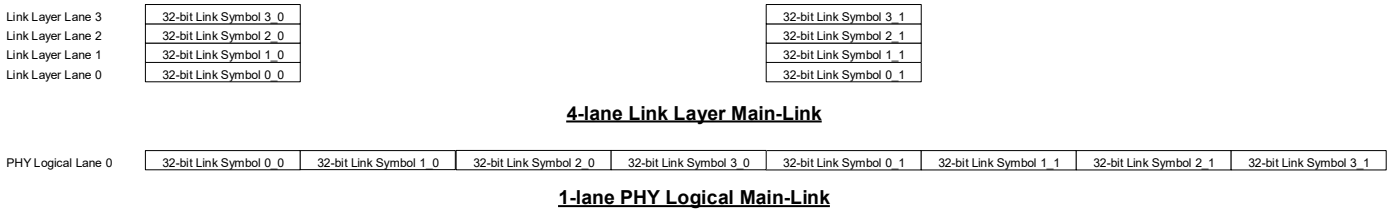


Figure 3-35: Conversion to One Physical Lane (Link Symbols Shown)

Link Symbols 0_*N* through 3_*N* are either all control link symbols or all data link symbols. When there is a transition from control to data (or vice versa), the first symbol on PHY logical Lane 0 after the transition is from Link Layer Lane 0. DPRX 128b/132b PHY Logical Sub-layer shall use this rule for PHY logical to Link Layer lane count conversion.

3.5.2.8 Place Holder Symbol Mapping to PHY Logical Main-Link

As defined in Section 2.7, 128b/132b Link Layer inserts place holder symbols to be replaced with PHY sync symbols and to account for the channel coding overhead, as follows:

- Insert one PHY sync place holder symbol for every 383 link symbols
- Insert one coding overhead place holder symbol for either every one PHY sync place holder symbol plus 31 link symbols, –or– 32 link symbols

Figure 3-36 through Figure 3-38 are informative diagrams that illustrate the mapping of place holder symbols to a 4-/2-/1-lane PHY logical Main-Link, respectively. The three figures are informative because the phase relationship between the PHY sync and coding overhead place holder symbols is implementation-specific.

Note: *An alternate approach to the place holder method can be found in Appendix M. The resulting bitstream from both approaches will be identical.*

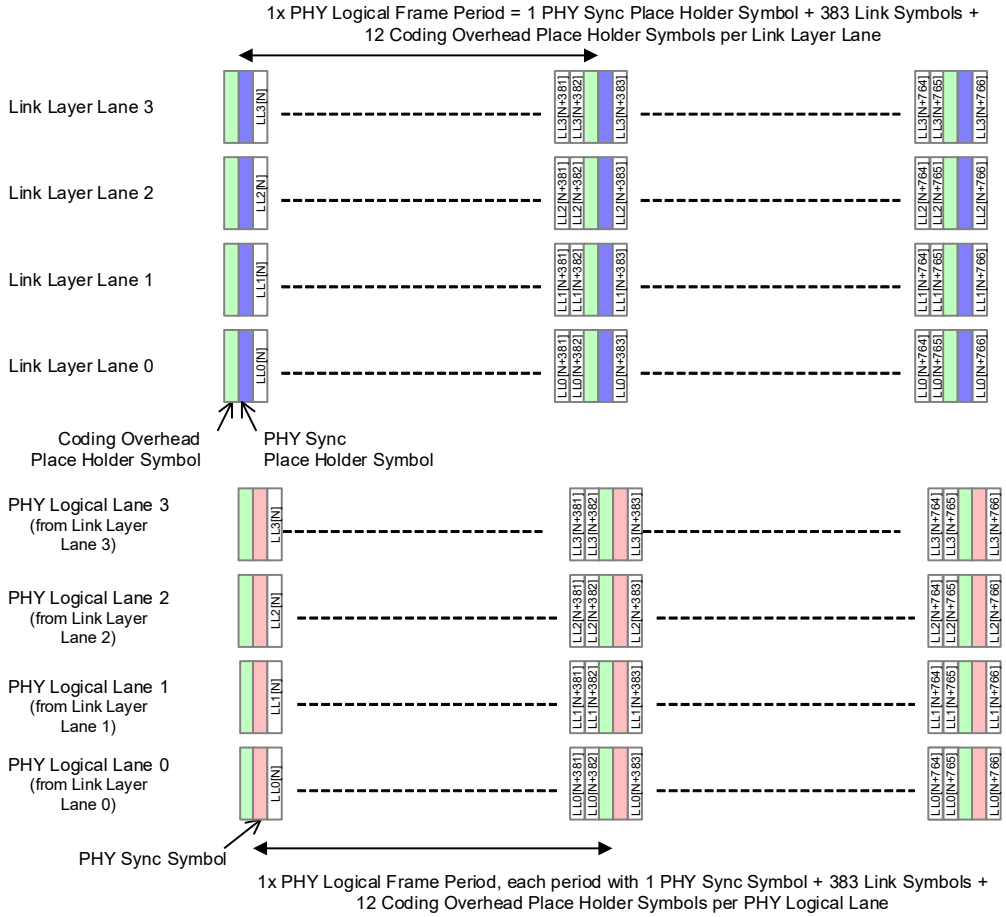


Figure 3-36: Place Holder Symbol Mapping to 4-lane PHY Logical Main-Link (Informative)

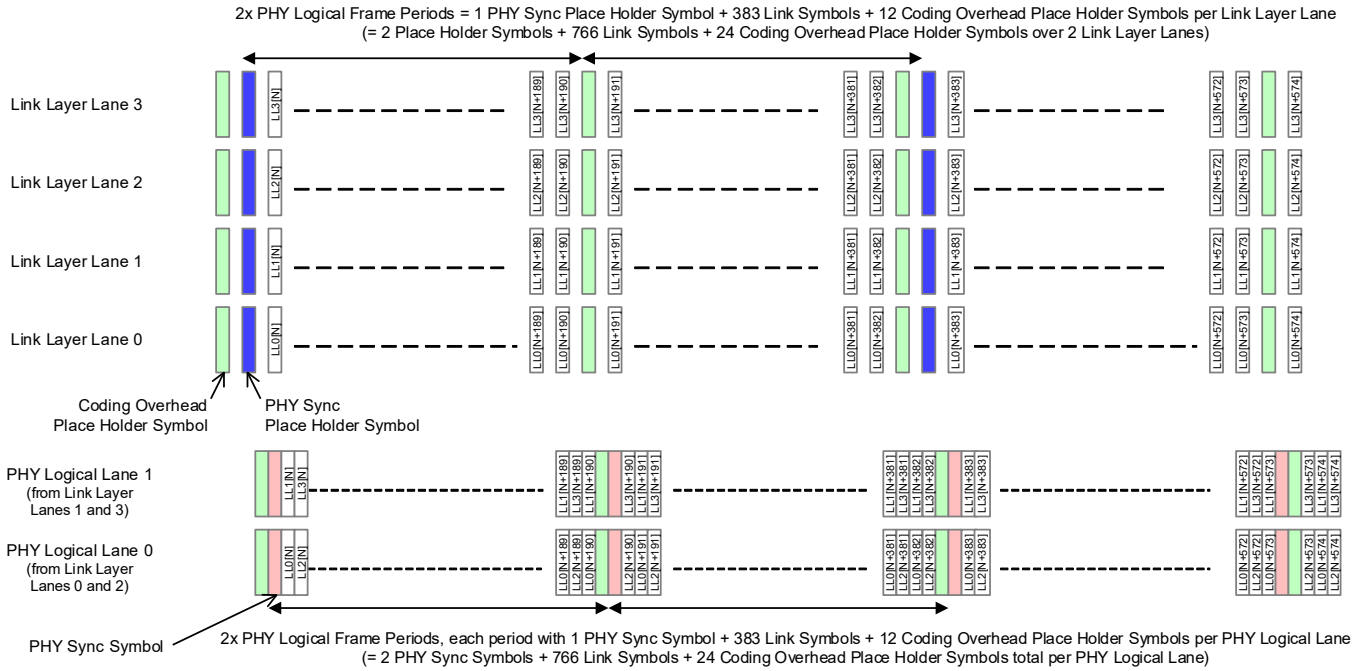


Figure 3-37: Place Holder Symbol Mapping to 2-lane PHY Logical Main-Link (Informative)

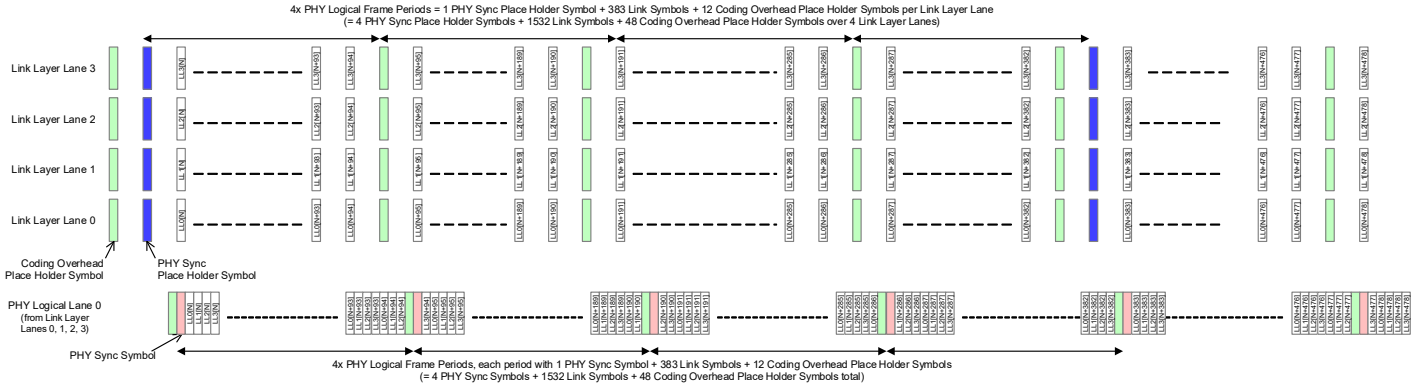


Figure 3-38: Place Holder Symbol Mapping to 1-lane PHY Logical Main-Link (Informative)

3.5.2.9 CDI Field Intra-super-symbol Shifting

When the CDI field value is 1 or 1100b, the ensuing super symbol has at least one non-link data symbol, PHY sync symbol –or– control link symbol(s), as defined in Table 3-23.

Table 3-23: CDI Field Intra-super-symbol Shifting When CDI Field Value is 1 or 1100b

Non-Link Data Symbol Type	Quantity	Location within Super Symbol
PHY sync symbol	One	Always placed within the first symbol of a super symbol.
Control link symbol	One or more	Position is arbitrary within the super symbol.

When a super symbol contains control link symbol(s), but **not** a PHY sync symbol, –and– the first symbol is **not** a control link symbol, a DPTX shall perform intra-super-symbol shifting to shift the nearest control link symbol to the first symbol position prior to transmission. Figure 3-39, Figure 3-40, and Figure 3-41 illustrate the intra-super-symbol shifting operation Symbol Type Vector field values of 1000b, *X*100b, and *XX*10b (where *X* is "don't care"), respectively. Although all three figures show only PHY Logical Lane 0, the same intra-super-symbol shifting operation occurs on all enabled PHY Logical lanes. As illustrated in the three figures, only the nearest to the first symbol is shifted; the subsequent control link symbols are not shifted. In parallel, the DPTX shall program the Symbol Type Vector field in the control link symbol(s) to describe the link symbol types of the four link symbols prior to the shifting, as follows:

- Bit 4 = 1st symbol type, Bit 5 = 2nd symbol type,
  Bit 6 = 3rd symbol type, Bit 7 = 4th symbol type
  - 1 = Control link symbol
  - 0 = Data link symbol

Note: *The Symbol Type Vector field is valid only for the control link symbol that is mapped to the first symbol of a super symbol.*

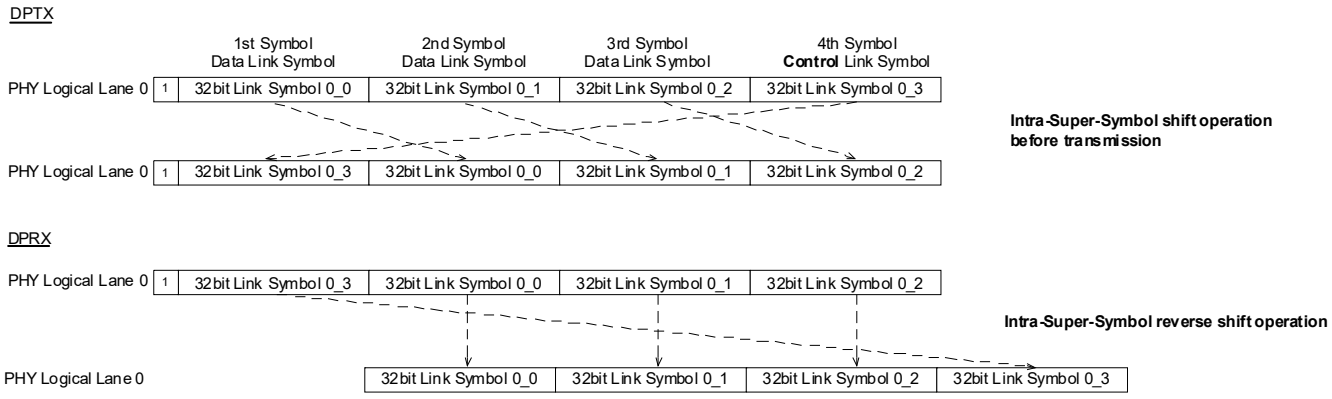


Figure 3-39: Intra-super-symbol Shifting and Reverse Shifting with Symbol Type Vector Field Value = 1000b

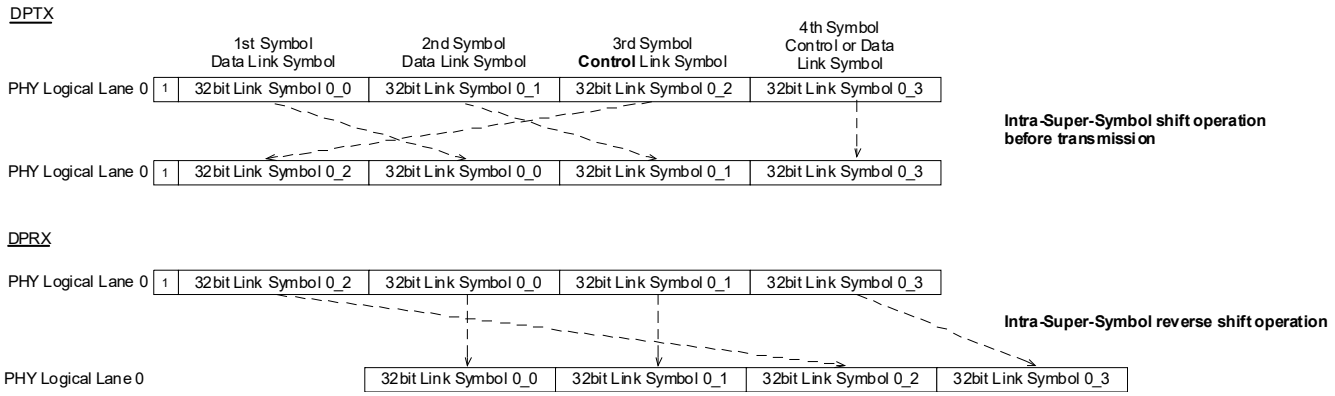


Figure 3-40: Intra-super-symbol Shifting and Reverse Shifting with Symbol Type Vector Field Value = *X*100b

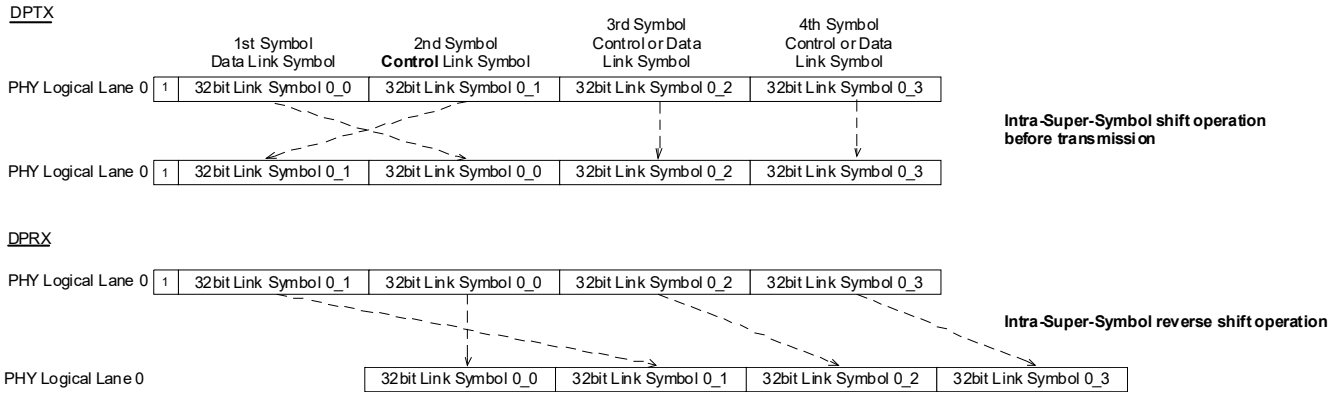


Figure 3-41: Intra-super-symbol Shifting and Reverse Shifting with Symbol Type Vector Field Value = *XX*10b

3.5.2.10 128b/132b PHY Logical Sub-layer Scrambling

The PHY Logical Sub-layer uses the LFSR, with the following polynomial and seed values:

- Polynomial
  - $G(x) = x^{23} + x^{21} + x^{16} + x^{8} + x^{5} + x^{2} + 1$
- Seed values
  - **Lane 0** – 1DBFBCh
  - **Lane 1** – 1DBFBDh
  - **Lane 2** – 1DBFBEh
  - **Lane 3** – 1DBFBFh

The scrambling rules are as follows:

- Conversion to PHY Logical Main-Link lane count and intra-super-symbol shifting occurs before scrambling on the DPTX 128b/132b PHY Logical Sub-layer.
  - DPRX 128b/132b PHY Logical Sub-layer shall perform intra-super-symbol reverse shifting after de-scrambling.
- LT_SCRAMBLER_RESET and POST_LT_SCRAMBLER_RESET PHY sync symbols bypass and then initialize the scrambling LFSR. The first bit after the LT_SCRAMBLER_RESET or POST_LT_SCRAMBLER_RESET PHY sync symbol "sees" the LFSR seed value.
- PHY_SYNC_ONLY PHY sync symbol advances the scrambling LFSR, but bypasses the scrambler.
- Control link and data link symbols advance the scrambling LFSR. The first byte of LFSR output is XOR'd with the first byte of the 32-bit control or data link symbol, etc. The first LFSR output bit maps to bit 0 of the first byte.
- CDI field (either four bits during LT or one bit after LT), four padded bits (after LT), and RS parity symbol (after LT) are added after scrambling on the DPTX.
  - These bits bypass the de-scrambler and do **not** advance the scrambling LFSR on the DPRX.

See Section 3.5.2.17 for LFSR output bit examples, both during and immediately after LT. Note that the bit sequences listed in that section are pre-coded (see Section 3.5.2.12), starting from the first 1-bit CDI field immediately after LT completion.

3.5.2.11 8-bit Symbol RS(198, 194) FEC

RS(198, 194), with an 8-bit symbol size, is used for FEC when 128b/132b PHY Logical Sub-layer is enabled. This is capable of correcting up to two RS symbol errors per RS data block of 194 RS symbols (194 × 8 = 1552 bits). The RS data block is composed of 12 super symbols, the 12 associated CDI bits, and four padding bits.

The polynomials are as follows:

- **Generator polynomial** – $G(x) = x^4 + 15 \times x^3 + 54 \times x^2 + 120 \times x + 64$
- **Primitive polynomial** – $P(x) = x^8 + x^4 + x^3 + x^2 + 1$

Figure 3-42 illustrates the schematic RS encoder representation. Before starting the calculation, a DPTX shall initialize all registers to 0s, and then transmit the register content when the data ends. In Figure 3-42, Data0 is the first data byte and Data193 is the last data byte. P3 is the most significant parity byte and P0 the least significant parity byte.

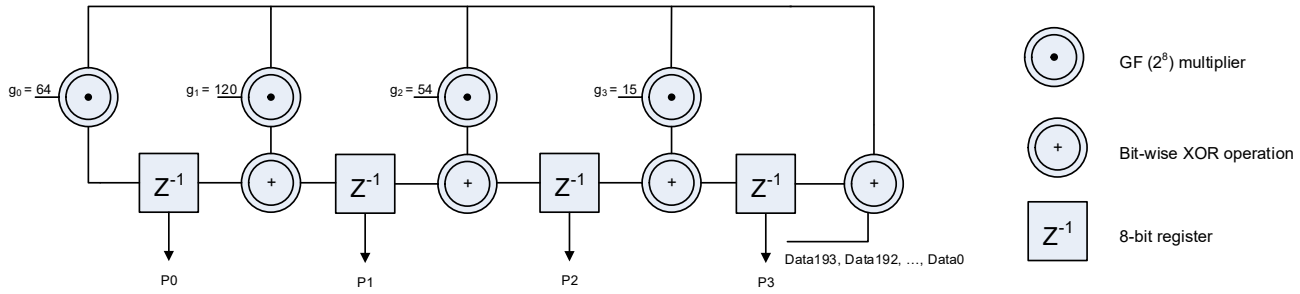


Figure 3-42: Schematic RS Encoder Representation for 128b/132b (Informative)

Table 3-24 lists four sets of test vectors of the RS(198, 194) FEC encoder. All values listed are in decimal.

- Test Vector 1 consists of 193 bytes of 0s (Bytes 0 through 192) and one byte of 1 (Byte 193)
- Test Vector 2 consists of one byte of 1 (Byte 0) and 193 bytes of 0s (Bytes 1 through 193)
- Test Vector 3 has Byte 0 equal to 1, the byte data value increasing by one for each byte, with Byte 193 having the value of 194
- Test Vector 4 has Byte 0 equal to 194, the byte data value decreasing by one for each byte, with Byte 193 having the value of 1

Table 3-24: RS(198, 194) FEC Test Vectors

Test Vector 1	Test Vector 2	Test Vector 3	Test Vector 4
FEC_ENC_D = [0,0,0,…,0,1]	FEC_ENC_D = [1,0,0,…,0]	FEC_ENC_D = [1,2,3,…,193,194]	FEC_ENC_D = [194,193,192,…,2,1]
FEC_ENC_P3 = 15	FEC_ENC_P3 = 34	FEC_ENC_P3 = 6	FEC_ENC_P3 = 182
FEC_ENC_P2 = 54	FEC_ENC_P2 = 67	FEC_ENC_P2 = 41	FEC_ENC_P2 = 107
FEC_ENC_P1 = 120	FEC_ENC_P1 = 164	FEC_ENC_P1 = 69	FEC_ENC_P1 = 231
FEC_ENC_P0 = 64	FEC_ENC_P0 = 196	FEC_ENC_P0 = 169	FEC_ENC_P0 = 249

The DPTX PHY Logical Sub-layer XOR's 12 of the 1-bit CDIs with 333h for DC balancing (because the 1-bit CDI value is predominantly 0), and then programs the four padded bits to 0011b prior to RS FEC encoding. The 12-bit 333h value's lsb and msb that are used to XOR 12 of 1-bit CDI fields (comprising the 12-bit CDI group field) are XOR'd as defined in Table 3-25.

Table 3-25: 12-bit CDI Group Field lsb and msb

Bit	Value	Comment
lsb (0)	1	XOR'd with the **first** of the 12-bit CDI group field (i.e., the CDI that precedes the 1st super symbol).
msb (11)	0	XOR'd with the **last** of the 12-bit CDI group field (i.e., the CDI that precedes the last, or 12th, super symbol).

The RS parity bytes are calculated for each 8-bit RS data byte in the order that they are transmitted over the cable. Because the CDI is included in the RS data block, the 8-bit RS data bytes will **not** align to byte boundaries in most link symbols, as illustrated in Figure 3-43.

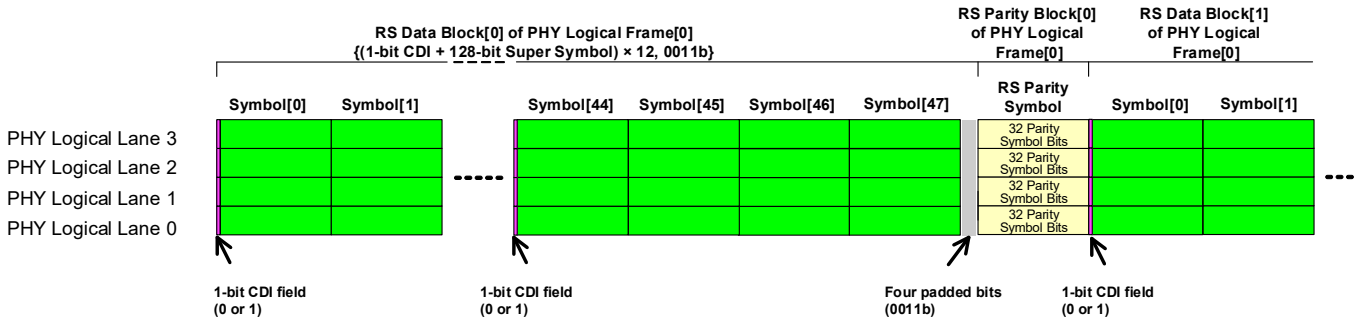


Figure 3-43: 32-bit RS Parity Symbol Insertion (for 4-lane PHY Logical Main-Link) Example

The DPTX PHY Logical Sub-layer 2-way interleaves RS parity bytes, as illustrated in Figure 3-44 and Figure 3-45 for a 4-/2-lane and 1-lane PHY Logical Main-Link, respectively.

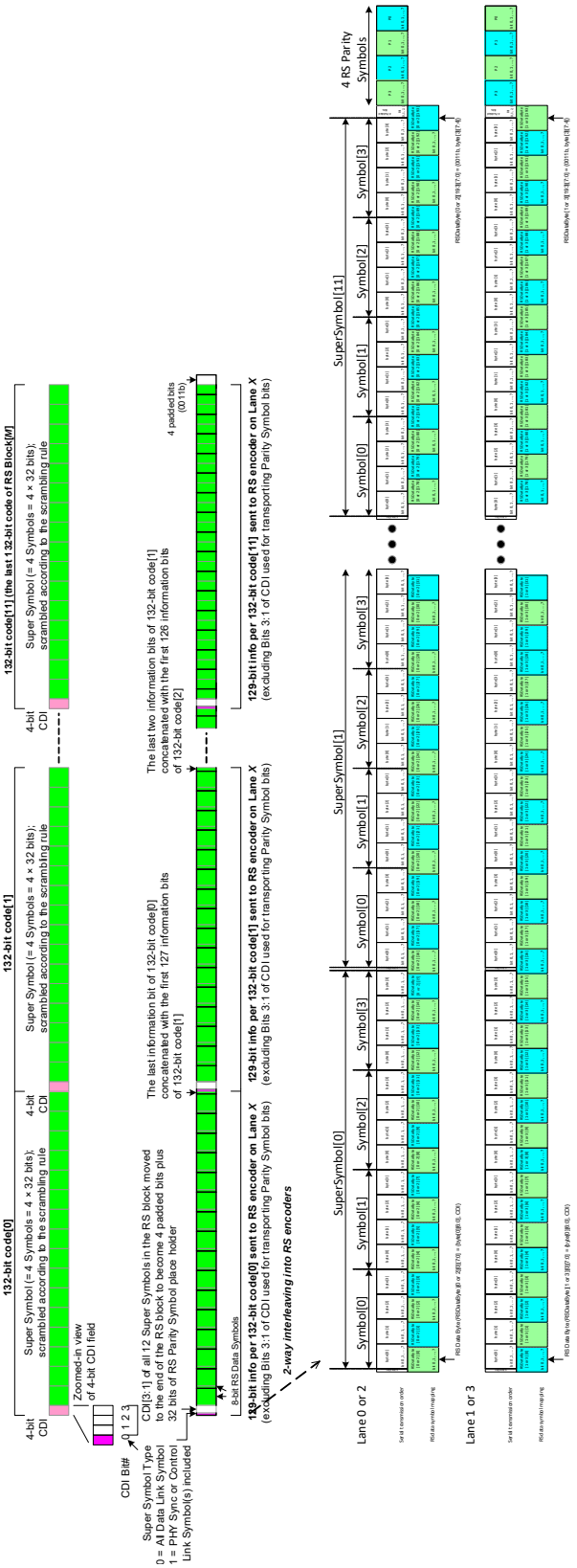


Figure 3-44: RS FEC Parity Bytes Mapping for 4-/2-lane PHY Logical Main-Link

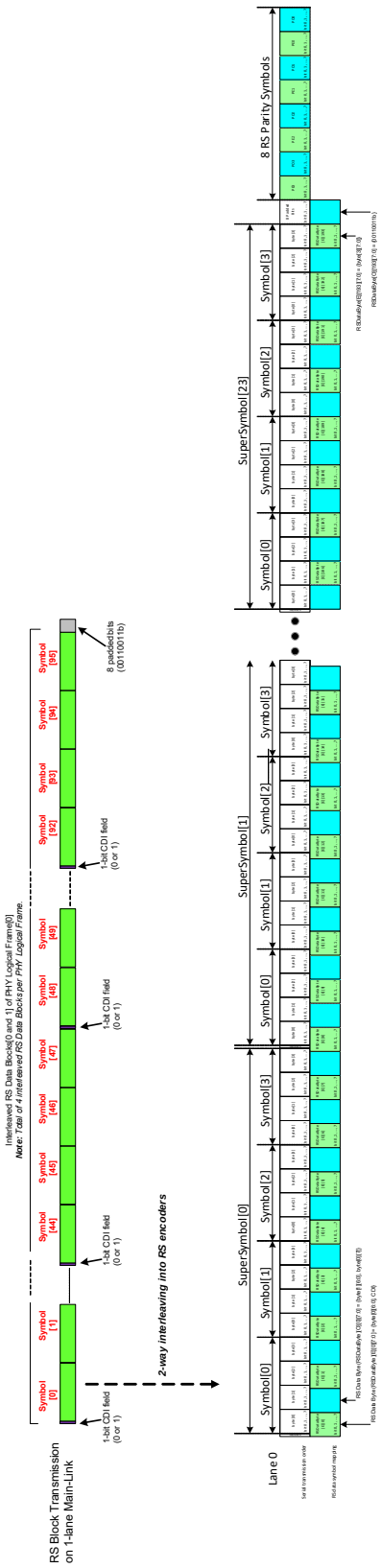


Figure 3-45: RS FEC Parity Bytes Mapping for 1-lane PHY Logical Main-Link

Figure 3-45 illustrates the mapping of a 1-lane PHY Logical Main-Link symbol sequence to RS data bytes for the first interleaved RS data block of a PHY Logical Frame. As indicated in the figure, two RS data blocks are interleaved together over 24 super symbols, 24 associated CDI bits, and eight padded bits. The eight padded bits consist of two sets of four padded bits, and are appended to the end of the 24 super symbol plus associated CDI bit set. Because two RS data blocks are interleaved together, there are a total of four interleaved RS data blocks per PHY Logical Frame. Two RS encoders, even and odd, are needed to calculate the RS parity bytes for an interleaved RS data block, as follows:

- Even RS encoder shall calculate RS parity bytes over the even-numbered RS data bytes (RSDataBytes[E][0…193]), and then output four even-numbered RS parity bytes (PE3, PE2, PE1, and PE0)
- Odd RS encoder shall calculate the RS parity bytes over the odd-numbered RS data bytes (RSDataBytes[O][0…193]), and then output four odd-numbered RS parity bytes (PO3, PO2, PO1, and PO0)

The RS parity bytes from the even and odd RS encoder shall then be transmitted in interleaved order, with PE3 transmitted first and PO0 transmitted last.

See Section 3.5.2.17 for an RS parity symbol value example. Note that the bit sequences listed in that section are pre-coded (see Section 3.5.2.12), starting from the first 1-bit CDI field immediately after LT completion. Therefore, the listed RS parity symbol value is also pre-coded.

3.5.2.12 Pre-coding

DPTX 128b/132b PHY Logical Sub-layer pre-coding and DPRX 128b/132b PHY Logical Sub-layer pre-coding removal convert bursts of errors that exist in received serial bits into two isolated errors (as indicated by the **red** 0s and 1s in $b_{rx}[n]$ and $a_{rx}[n]$ in Figure 3-46). This conversion facilitates error correction by the DPRX's RS FEC decoder.

Pre-coding starts with the first bit of PHY Logical Frame[0], which is the first 1-bit CDI of RS Block[0] (see Figure 3-48).

The initial $b_{tx}[-1]$ and $b_{rx}[-1]$ values (to be XOR'd with a[0] and $a_{rx}[0]$, respectively, as illustrated in Figure 3-46), shall both be cleared to 0.

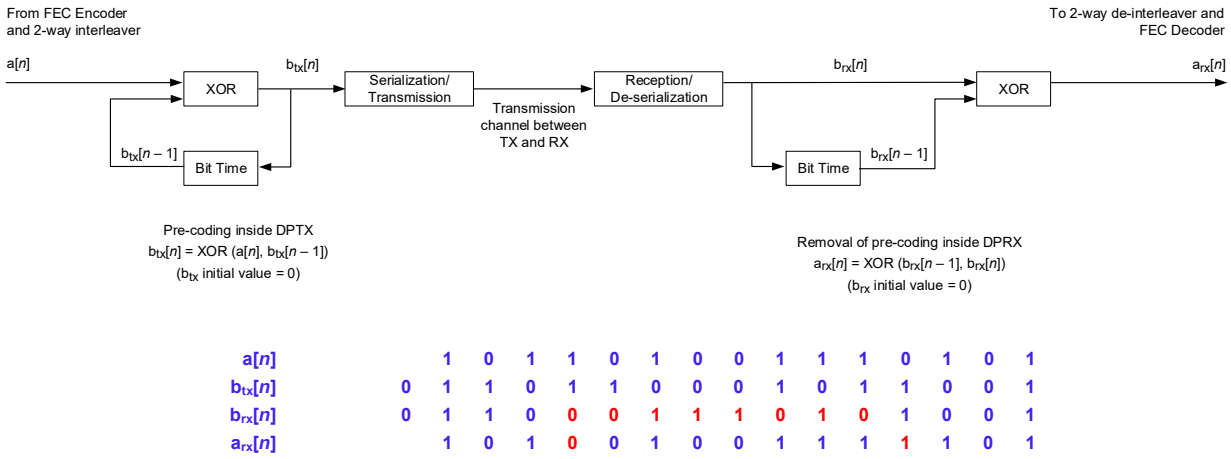


Figure 3-46: Logical Diagrams of Pre-coding/Pre-coding Removal and Bit Pattern Example

3.5.2.13 Link Training Pattern Sequences (TPSs)

DPTX 128b/132b PHY Logical Sub-layer shall conduct LT RS FEC disabled.

Table 3-26 defines the two TPSs that are used by 128b/132b PHY Logical Sub-layer.

Table 3-26: 128b/132b PHY Logical Sub-layer Link TPSs

TPS	Description
128b/132b_TPS1	• Every serial bit has a transition, resulting in a clock pattern that toggles at UHBR Nyquist frequencies (5GHz for UHBR10, 6.75GHz for UHBR13.5, and 10GHz for UHB20)
128b/132b_TPS2	• Conducted with a 4-bit CDI field inserted • PHY sync symbol is transmitted once every 96 of 132-bit codes • Starts with LT_SCRAMBLER_RESET PHY sync symbol; subsequently, every 16th PHY_SYNC_ONLY PHY sync symbol is replaced with an LT_SCRAMBLER_RESET PHY sync symbol • Ends with a POST_LT_SCRAMBLER_RESET PHY sync symbol, which replaces the LT_SCRAMBLER_RESET PHY sync symbol • All other symbols are data link symbols that are filled with 0s and with scrambling enabled

As is the case with 8b/10b PHY Logical Sub-layer, DPTX 128b/132b PHY Logical Sub-layer shall write to and read from DPCD registers as it conducts and completes LT, as illustrated in Figure 3-47.

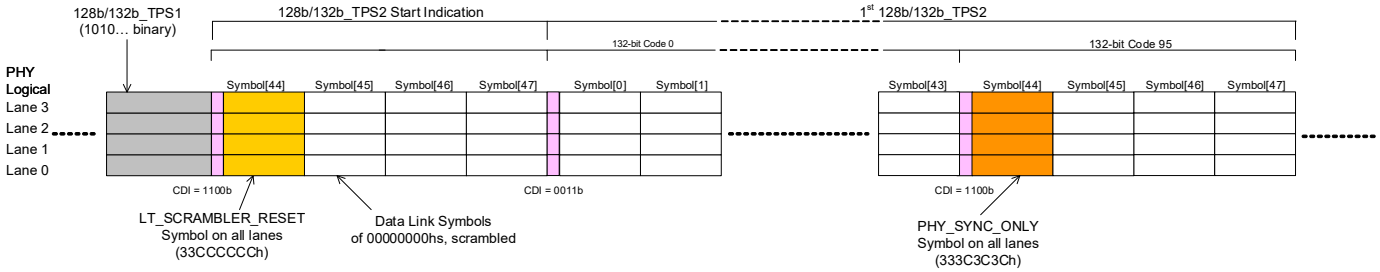


Figure 3-47: 128b/132b PHY Logical Sub-layer Link TPSs

3.5.2.13.1 128b/132b_TPS2 to Normal Operation Transition

After successful LT completion, a DPTX shall collapse the CDI field to one bit, and then enable RS FEC and pre-coding, starting from the 1-bit CDI field of RS Block[0] of PHY Logical Frame[0] before transmission, as illustrated in Figure 3-48.

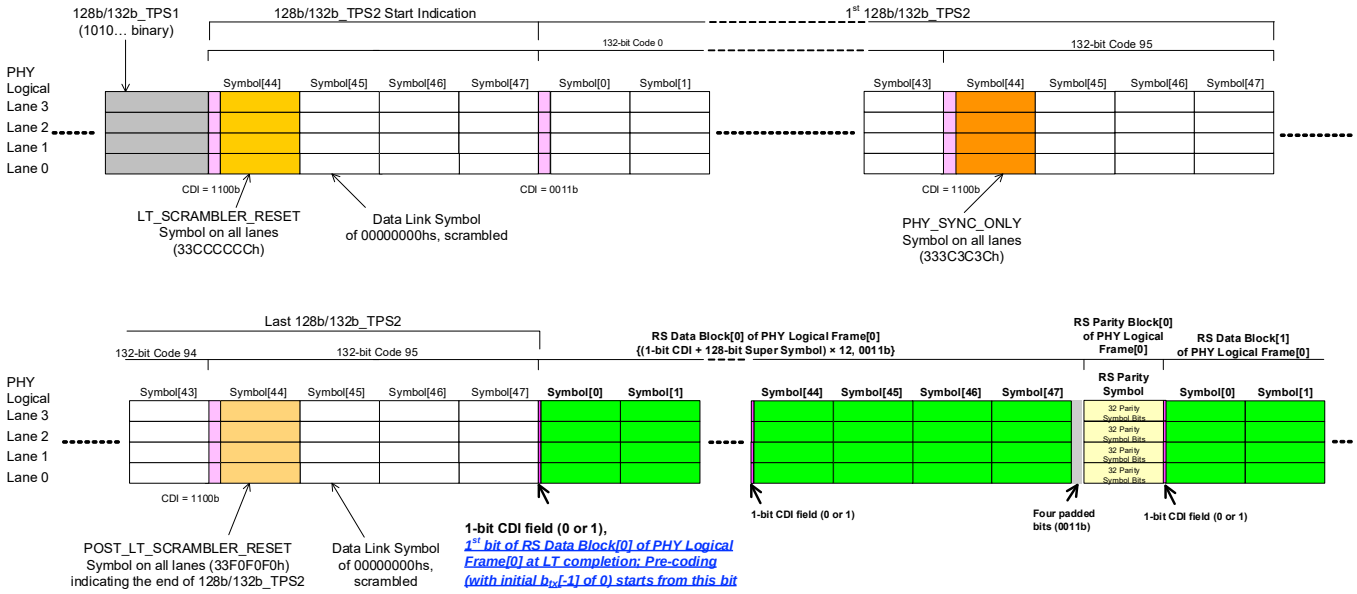


Figure 3-48: Link Training Completion and RS FEC/Pre-coding Enablement

3.5.2.13.2 PHY Sync Symbol Transmission Interval Consistency in Transition from 128b/132b_TPS2 to Normal Operation

The PHY sync symbol transmission interval remains consistent while transitioning from LT to normal operation. During LT, the PHY Logical Frame is composed of 8 times 12 of 132-bit codes, each of which is composed of a 4-bit CDI field plus a super symbol. A super symbol is composed of four symbols, as follows:

- Four data link symbols, –or–
- One PHY sync symbol plus three data link symbols

Therefore, 12 of the 132-bit codes have 48 symbols total (Symbol[0]) through Symbol[47]). In every 8th instance of those 48 symbols, a PHY sync symbol is transmitted as Symbol[44].

When RS FEC is enabled after LT completion, the PHY Logical Frame is composed as defined in Table 3-27.

Table 3-27: PHY Logical Frame Composition when RS FEC Is Enabled after LT Completion

Main-Link Lane Count	Description
4 or 2	• PHY Logical Frame is composed of 8 RS blocks, each of which includes the following: • 12 of 129 information bits (= 1-bit CDI + super symbol) • 4 padded bits • 32 bits of RS parity symbols • Total number of Link or PHY sync symbols per RS block is 48, which is 12 of 4 symbols/super symbol, Symbol[0] through Symbol[47] • PHY sync symbol is transmitted as the Symbol[44] location, the 1st symbol of the last super symbol of the PHY Logical Frame's last RS block
1	• PHY Logical Frame is composed of 4 interleaved RS blocks[0, 1], [2, 3], [4, 5], and [6, 7] • Each interleaved block includes the following: • 24 of 129 information bits (= 1-bit CDI + super symbol) • 8 padded bits • 2 of 32 bits of RS parity symbols • Total number of Link or PHY sync symbols per the interleaved RS blocks is 96, which is 24 of 4 symbols/super symbol, Symbol[0] through Symbol[95] • PHY sync symbol is transmitted as the Symbol[44] location and the Symbol[92]

3.5.2.14 128b/132b Channel Coding Serial Bit Transmission Order

The serial bit transmission order is as follows (see Figure 3-49):

1 CDI

- 4-bit CDI, bits 3:0 transmitted during LT
  - Bit 0 is transmitted first
  - Bit 3 is transmitted last
  - Binary values are indicated in the bit 3:0 sequence (e.g., a value of 0011b indicates that bits 3 and 2 are 0s and bits 1 and 0 are 1s)
- 1-bit CDI, bit 0 transmitted after LT

2 Four 32-bit link symbols

- Bit 0 of the least significant eight bits is transmitted first
- Bit 7 of the most significant eight bits is transmitted last
- Binary values are indicated in the bit 7:0 sequence (e.g., a value of 10100110b indicates that bit 7, transmitted last within each 8-bit symbol, is 1, and bit 0, transmitted first within each 8-bit symbol, is 0)

3 RS data block padded bits

- Four padded bits in 4- and 2-lane configurations
  - Bit 0 is transmitted first
  - Bit 3 is transmitted last
  - Binary values are indicated in the bit 3:0 sequence (e.g., a value of 0011b indicates that bits 3 and 2 are 0s and bits 1 and 0 are 1s)
- Eight padded bits in 1-lane configuration
  - Bit 0 is transmitted first
  - Bit 7 is transmitted last
  - Binary values are indicated in the bit 7:0 sequence (e.g., a value of 00110011b indicates that bit 7 is 0 and bit 0 is 1)

4 One (in 4- and 2-lane configurations; see Figure 3-44) or two (in 1-lane configuration; see Figure 3-45) 32-bit RS parity symbols

- Bit 0 of the most significant eight bits is transmitted first
- Bit 7 of the least significant eight bits is transmitted last
- Binary values are indicated in the bit 7:0 sequence (e.g., a value of 10100110b indicates that bit 7, transmitted last within each 8-bit symbol, is 1, and bit 0, transmitted first within each 8-bit symbol, is 0)

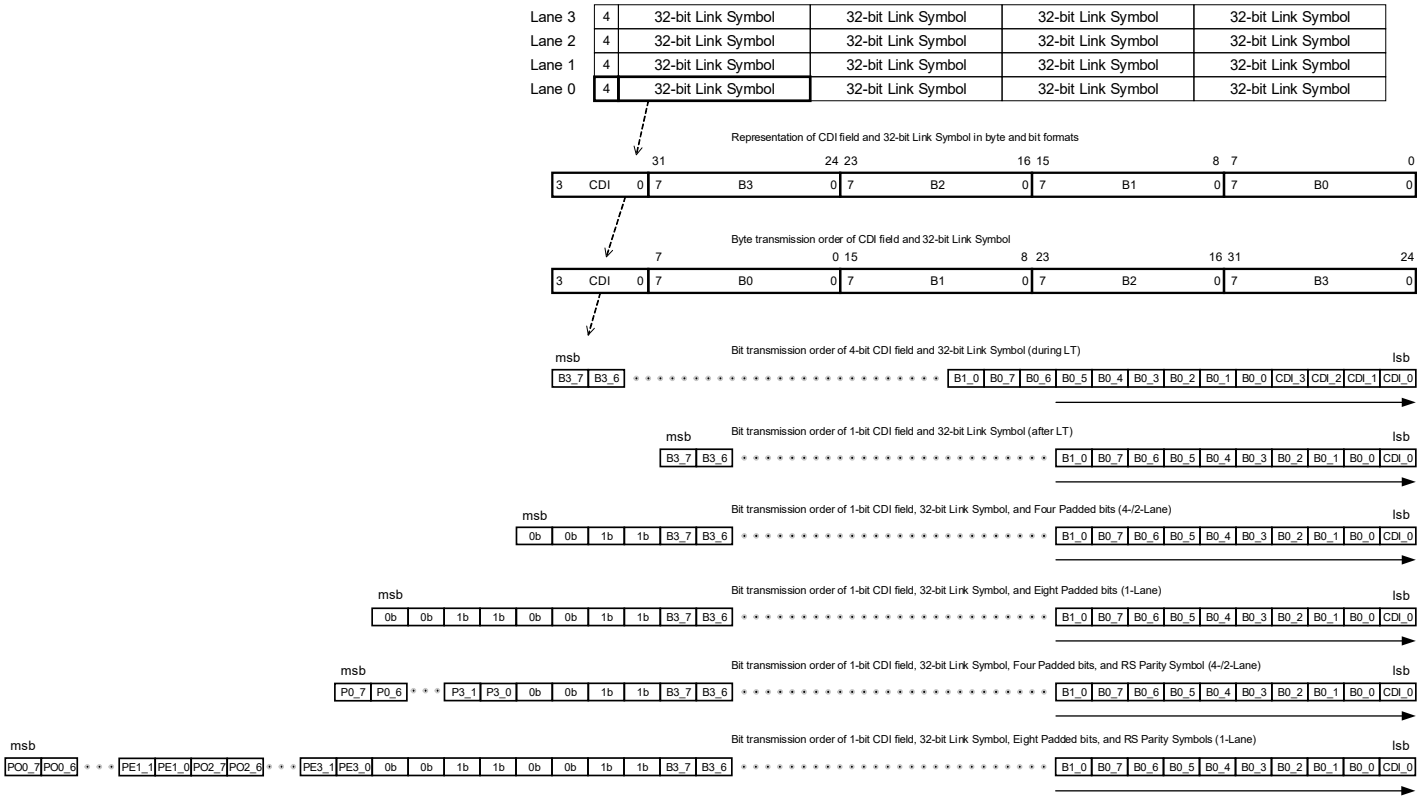


Figure 3-49: Serial Bit Transmission Order of CDI field and 32-bit Link Symbols

3.5.2.14.1 Bit Listing within Multi-bit Field

A multi-bit field is listed with the msb to the leftmost (transmitted last within the field) and the lsb to the rightmost (transmitted first within the field).

3.5.2.14.2 Byte Ordering within Multi-byte Field

There are some multi-byte fields in which the MSB is are transmitted first and the LSB is transmitted last, such as multi-byte fields with an MSA packet or an AFREQ field within an Audio_TimeStamp SDP. These exceptions are clearly articulated in text and/or tables. Unless stated otherwise, multi-byte fields are transmitted in the order of the LSB first and the MSB last.

3.5.2.15 128b/132b PHY Logical Sub-layer Inter-lane Skew Specification

Table 3-28 defines the 128b/132b PHY Logical Sub-layer inter-lane skew specification.

Table 3-28: 128b/132b PHY Logical Sub-layer Inter-lane Skew Specification

Parameters	Inter-lane Skew Specification (Maximum)	Comments
DPTX IC or PHY Repeater IC DFP at package pins	32UI	PHY Repeater IC shall de-skew the inter-lane skew of incoming serial bit signals to avoid inter-lane skew accumulation over cascaded PHY Repeaters.
DPTX device traces between DPTX IC package pins and connector pins	0.1ns	
Cable connector assembly	0.9ns	
DPRX or PHY Repeater UFP inter-lane skew tolerance at DPRX/PHY Repeater device UFP connector pins	32UI + 1.2ns	

Unlike DPTX 8b/10b PHY Logical Sub-layer, DPTX 128b/132b PHY Logical Sub-layer shall **not** insert any inter-lane link-symbol-cycle skew. However, DPRX 128b/132b PHY Logical Sub-layer is likely to encounter inter-lane skew in the incoming serial bit signals, and shall tolerate the worst-case inter-lane skew that is measured at the receiver device's connector, using a PHY sync symbol as a de-skewing marker.

Table 3-29 defines the inter-lane skew sources.

Table 3-29: 128b/132b PHY Logical Sub-layer Inter-lane Skew Sources

Inter-lane Skew Source	Description
Inter-lane skew at the DPTX IC output, coming from uncertainty of the phase relationship of bit 0 of 32-bit symbols among PHY Logical Main-Link lanes at the serializer's output	• DPTX 128b/132b PHY Logical Sub-layer shall maintain a 32-serial bit (or 32-UI) maximum inter-lane skew at the package pins (e.g., at the slowest 128b/132b channel coding link rate of 10Gbps/lane (UHBR10), the 32-UI maximum corresponds to 3.2ns)
Latency difference among PHY Logical Main-Link lanes (1-ns maximum), regardless of raw bit rate	• 0.1-ns maximum over transmitter device PCB traces • 0.9-ns maximum over a cable connector assembly

3.5.2.16 128b/132b PHY Logical Sub-layer LT Operation

The 128b/132b PHY Logical Sub-layer LT operating flow is the same as that for 8b/10b PHY Logical Sub-layer, as defined in Section 3.5.1.2. Table 3-30 lists the DPCD registers that are used for 128b/132b LT. (For complete register descriptions, see Table 2-183, Table 2-184, Table 2-185, Table 2-192, and Table 2-193.)

Table 3-30: DPCD Registers Used for 128b/132b Link Training

DPCD Address	Register
00100h	LINK_BW_SET
00101h	LANE_COUNT_SET
00102h	TRAINING_PATTERN_SET
00103h	TRAINING_LANE0_SET
00104h	TRAINING_LANE1_SET
00105h	TRAINING_LANE2_SET
00106h	TRAINING_LANE3_SET
00107h	DOWNSPREAD_CTRL
00108h	MAIN_LINK_CHANNEL_CODING_SET
00202h	LANE0_1_STATUS
00203h	LANE2_3_STATUS
00204h	LANE_ALIGN_STATUS_UPDATED
00206h	ADJUST_REQUEST_LANE0_1
00207h	ADJUST_REQUEST_LANE2_3
0200Ch	LANE0_1_STATUS_ESI
0200Dh	LANE2_3_STATUS_ESI
0200Eh	LANE_ALIGN_STATUS_UPDATED_ESI
02216h	128b/132b_TRAINING_AUX_RD_INTERVAL

A DPTX shall write to the MAIN_LINK_CHANNEL_CODING_SET register to select the channel coding type, and then program the target link rate and lane count by way of an AUX write transaction to LINK_BW_SET and LANE_COUNT_SET registers. The DPTX shall be transmitting a Link TPS over the Main-Link by the time it writes to the TRAINING_PATTERN_SET register and TRAINING_LANE*x*_SET register(s).

The DPTX shall then adjust its drive setting according to the LANE*x*_*y*_STATUS, LANE_ALIGN_STATUS_UPDATED, and ADJUST_REQUEST_LANE*x*_*y* registers, and then update the TRAINING_LANE*x*_SET register(s) accordingly.

During the LANE*x*_CHANNEL_EQ_DONE sequence of 128b/132b PHY Logical Sub-layer LT, the DPTX shall honor the 128b/132b_TRAINING_AUX_RD_INTERVAL register value. To help the DPRX improve the equalization optimization for the UHBR rates that are used for 128b/132b PHY Logical Sub-layer, the register supports 32- and 64-ms read intervals (values 05h and 06h, respectively) during the LANE*x*_CHANNEL_EQ_DONE sequence.

3.5.2.16.1 Channel Coding Change during LT

A DPTX may change the channel coding between 128b/132b channel coding and 8b/10b channel coding during LT. For example, a DPTX that has the policy of configuring the link for the highest link data bandwidth may switch from four lanes at UHBR10 with 128b/132b channel coding to four lanes at HBR3 with 8b/10b channel coding, and then to two lanes at UHBR10 with 128b/132b channel coding in case the link fails to be established.

Before writing to the MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) to indicate the channel coding change, the DPTX shall:

1 Disable Main-Link signal transmission.

2 Clear the TRAINING_PATTERN_SET register (DPCD Address 00102h) to 00h.

3 Write default values to the TRAINING_LANE*x*_SET registers (DPCD Addresses 00103h through 00106h).

When switching channel coding during normal operation, the DPTX shall perform the following before initiating LT:

1 Write 02h to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h).

2 Disable Main-Link signal transmission.

3 Write default values (or last-known good values) to the TRAINING_LANE*x*_SET registers.

3.5.2.17 Bit Sequences during and Immediately after LT (Informative)

This section defines the bit sequences that occur both during and immediately after LT as the bits are transmitted over a differential pair. This information is provided as an informative reference for scrambling LFSR output bits, RS parity bytes, and pre-coding. As noted in Section 3.5.2.14.1, the lsb is transmitted first within a multi-bit field, and in Section 3.5.2.14.2, the LSB is transmitted first within a multi-byte field. See Section 3.5.2.14 for the serial bit transmission order of the bit sequences provided in this section.

3.5.2.17.1 Bit Sequences on 4-lane PHY Logical Main-Link

Bit Sequence Lists #1 through #4, as highlighted in Figure 3-50, are provided for Lanes 0 through 3 in the sections that follow. The link symbols that follow LT are all programmed to be data link symbols with a value of all 0s prior to scrambling.

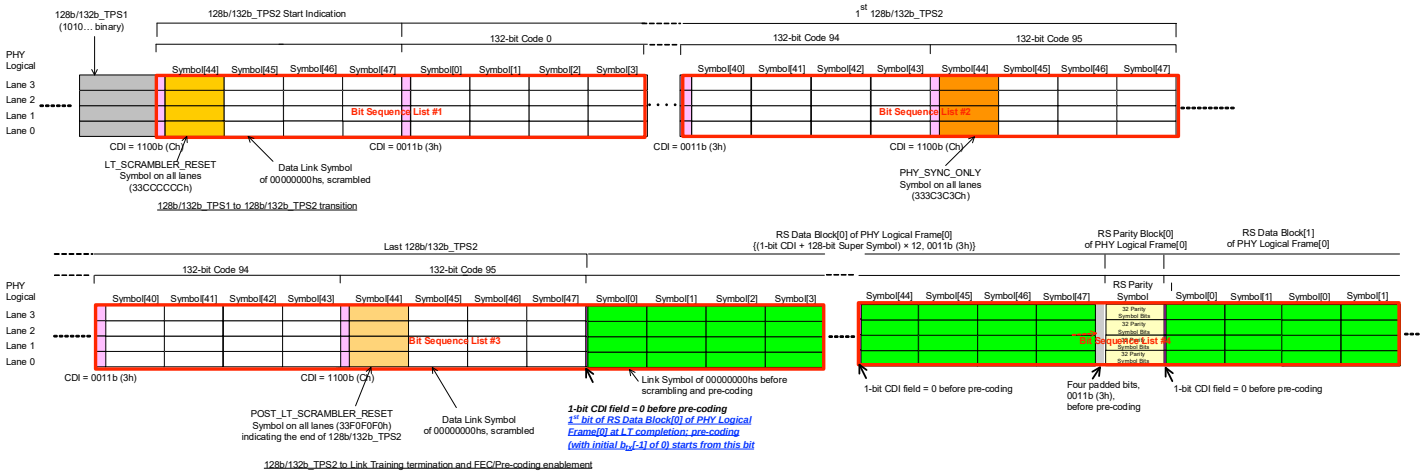


Figure 3-50: Bit Sequence Lists Illustration for 4-lane PHY Logical Main-Link

3.5.2.17.1.1 Bit Sequence that Includes RS(198, 194) FEC Parity Bytes before Pre-coding for 4-/2-lane Main-Link

Table 3-31 illustrates a bit sequence for 4- and 2-lane configurations that includes RS(198, 194) FEC parity bytes (in hex) before pre-coding is applied for the 1st RS block, starting with 1st 1-bit CDI field that immediately follows link training completion. All symbols are data link symbols with raw data of all 0s that have been scrambled.

Table 3-31: Bit Sequence for 4-/2-lane Configurations that Includes RS(198, 194) FEC Parity Bytes before Pre-coding[a]

Symbol #	Lane 0		Lane 1		Lane 2		Lane 3	
	CDI	Data	CDI	Data	CDI	Data	CDI	Data
0	1	07C34F04	1	A41C574B	1	D62CC323	1	75F3DB6C
1		06C62675		F5B08BD6		7F7D70A4		8C0BDD07
2		ABB4B0A3		545D5CDB		D440469F		2BA9AAE7
3		57CC1105		CD00BE31		9AAA469F		0066E9AB
4	1	7342694E	1	DED8F5A3	1	258F2738	1	8815BBD5
5		03B70F1D		AADD0E2B		D7020F86		7E680EB0
6		5EBA45E0		30491037		69C3EF0B		0730BADC
7		43D7EB30		7E25D2DA		5D2EF7C5		60DCCE2F
8	0	D0F55D2C	0	7B6F4EC8	0	053854DE	0	AEA2473A
9		8E764115		74DFFE18		F3229E93		098B219E
10		57D19DC3		2FDB0B77		EBD4D699		93DE402D
11		A176FFCD		1C700F1A		FFF587A6		42F37771
12	0	2E644C7A	0	F64E4530	0	C27148DF	0	1A5B4195
13		24A30587		D13CCF7C		DE6CE0FA		2BF32A01
14		4BA2FF89		EDB34798		18AA2381		BEBB9B90
15		621D7C46		2D8A2622		45D6D174		0A418B10
16	1	2FA51912	1	7CD70DDC	1	861C1375	1	D56E07BB
17		33CAB3E6		89BA7C63		6EF2D424		D4821BA1
18		882BF3ED		484F0E7F		68198D24		A87D70B6
19		96AB3E67		9FA831B8		122AB988		1B29B657
20	1	5D6A9EE8	1	C5A8BB8B	1	910B8C59	1	09C9A93A
21		1D641C5C		7E6CFD39		ACE06CEE		CFE88D8B
22		C8512CF5		F2E0A412		D509E886		EFB86061
23		4DF4A8D8		2348BB96		FAAAA17F		9416B231
24	0	7A5DAC96	0	077C03B9	0	C4CD7B01	0	B9ECD42E
25		092FF42B		B07CC53C		D5866CA0		6CD55DB7
26		C90E2E08		9816C3C9		618258E8		309AB529
27		D9AF4B02		19D4200B		3992FE86		F9E9958F
28	0	E7784E3D	0	CC65260A	0	72F6FA26	0	59EB9211

Table 3-31: Bit Sequence for 4-/2-lane Configurations that Includes RS(198, 194) FEC Parity Bytes before Pre-coding[a] (Continued)

Symbol #	Lane 0		Lane 1		Lane 2		Lane 3	
	CDI	Data	CDI	Data	CDI	Data	CDI	Data
29		75657F7F		51D19264		673F09F2		438BE4E9
30		2B547CFC		3E13D24C		A1F7ABA4		B4B00514
31		831A0F93		AFF216C2		156E033B		39861A6A
32	1	75137A60	1	82C9DD89	1	0EFE2994	1	F9248E7D
33		D9977F89		8BB4B311		708699C5		22A5555D
34		9067EC5D		B52E0180		82C31AB3		A78AF76E
35		3589AF49		103E505B		275250C0		02E5AFD2
36	1	36F30552	1	2E6A89FC	1	BABFC305	1	A2264FAB
37		242027BC		D2015DF9		DF309A9E		2911E0DB
38		F4A0F351		C348C562		EF54E848		D8BCDE7B
39		918407E9		1D407D53		57E63AB4		DB22400E
40	0	4928D987	0	1C725A86	0	E3859807	0	B6DF1B06
41		50580061		9ED7B178		B71FD8ED		799069F4
42		549CB361		F320E5EE		87429826		20FECEA9
43		1DC70D38		FBECC42B		EED2E9B1		08F920A2
44	0	9C47712E	0	B5C2AF15	0	08859E33	0	21004008
45		A99049F4		EAFF54A5		8827C75C		CB48DA0D
46		2D7A6B9A		58219C24		17D79045		628C67FB
47		539D17F2		BAFF81BE		A72C5CD4		4E4ECA98
Pad		3		3		3		3
	FEC_ENC_P3 = 9B		FEC_ENC_P3 = 47		FEC_ENC_P3 = F6		FEC_ENC_P3 = 2A	
	FEC_ENC_P2 = 9B		FEC_ENC_P2 = EF		FEC_ENC_P2 = 31		FEC_ENC_P2 = 45	
	FEC_ENC_P1 = 83		FEC_ENC_P1 = B2		FEC_ENC_P1 = 7D		FEC_ENC_P1 = 4C	
	FEC_ENC_P0 = E2		FEC_ENC_P0 = 3C		FEC_ENC_P0 = 69		FEC_ENC_P0 = B7	

a. 1st RS block, starting with 1st 1-bit CDI field immediately following Link Training completion.
All symbols are data link symbols with raw data of all 0s, scrambled.
1-bit CDIs are all 0s, but XOR'd with 333h before RS(198, 194) FEC encoding.
All values listed are in hex.

3.5.2.17.1.2 Lane 0 of 4-lane Main-Link

3.5.2.17.1.2.1 Lane 0 of 4-lane Main-Link Bit Sequence List #1

```
CDI     8b_0,    8b_1,    8b_2,    8b_3
3  0  7      0,7      0,7      0,7      0
1100  11001100,11001100,11001100,00110011; CDI = Ch, LT_SCRAMBLER_RESET Symbol (8b_3 ~ 8b_0 = 33CCCCCCh)
      01101100,10111101,10010100,10011000; 8b_3 ~ 8b_0 = 9894BD6Ch
      01010011,11000110,11011000,11001110; 8b_3 ~ 8b_0 = CED8C653h
      01010000,01101010,01110101,11000001; 8b_3 ~ 8b_0 = C1756A50h
0011  00000100,01001111,11000011,00000111; CDI = 3h, 8b_3 ~ 8b_0 = 07C34F04h
      01110101,00100110,11000110,00000110; 8b_3 ~ 8b_0 = 06C62675h
      10100011,10110000,10110100,10101011; 8b_3 ~ 8b_0 = ABB4B0A3h
      00000101,00010001,11001100,01010111; 8b_3 ~ 8b_0 = 57CC1105h
```

3.5.2.17.1.2.2 Lane 0 of 4-lane Main-Link Bit Sequence List #2

```
CDI     8b_0,    8b_1,    8b_2,    8b_3
3  0  7      0,7      0,7      0,7      0
0011  11100010,11111111,10001001,10010111; CDI = 3h, 8b_3 ~ 8b_0 = 9789FFE2h
      11100010,10111010,01011001,00001110; 8b_3 ~ 8b_0 = 0E59BAE2h
      00001011,11101100,01110010,10110010; 8b_3 ~ 8b_0 = B272EC0Bh
      00101010,10011010,10110011,01110110; 8b_3 ~ 8b_0 = 76B39A2Ah
1100  00111100,00111100,00111100,00110011; CDI = Ch, PHY_SYNC_ONLY Symbol, 8b_3 ~ 8b_0 = 333C3C3Ch
      11001010,01010100,01000010,10100001; 8b_3 ~ 8b_0 = A14254CAh
      11010010,00001110,10100000,10111001; 8b_3 ~ 8b_0 = B9A00ED2h
      10101000,10101000,10110111,10110110; 8b_3 ~ 8b_0 = B6B7A8A8h
```

3.5.2.17.1.2.3 Lane 0 of 4-lane Main-Link Bit Sequence List #3

```
CDI     8b_0,    8b_1,    8b_2,    8b_3
3  0  7      0,7      0,7      0,7      0
0011  11011011,10011111,00000000,01011110; CDI = 3h, 8b_3 ~ 8b_0 = 5E009FDBh
      10110000,11101001,01000010,10101100; 8b_3 ~ 8b_0 = AC42E9B0h
      00111011,11101111,01110100,10000010; 8b_3 ~ 8b_0 = 8274EF3Bh
      01000000,01111001,10010110,11111000; 8b_3 ~ 8b_0 = F8967940h
1100  11110000,11110000,11110000,00110011; CDI = Ch, POST_LT_SCRAMBLER_RESET Symbol, 8b_3 ~ 8b_0 = 33F0F0F0h)
      01101100,10111101,10010100,10011000; 8b_3 ~ 8b_0 = 9894BD6Ch
      01010011,11000110,11011000,11001110; 8b_3 ~ 8b_0 = CED8C653h
      01010000,01101010,01110101,11000001; 8b_3 ~ 8b_0 = C1756A50h
   1  00000011,11000101,10111110,00000010; CDI = 1, 8b_3 ~ 8b_0 = 02BEC503h
      11010011,00011101,01000010,00000010; 8b_3 ~ 8b_0 = 02421DD3h
      01100001,10010000,10010011,01100110; 8b_3 ~ 8b_0 = 66939061h
      00000011,00001111,01000100,11001101; 8b_3 ~ 8b_0 = CD440F03h

Starting from the first 1-bit CDI field on, all bits are pre-coded prior to transmission
(e.g., CDI field value 0 is pre-coded to 1).
```

3.5.2.17.1.2.4 Lane 0 of 4-lane Main-Link Bit Sequence List #4

```
CDI     8b_0,    8b_1,    8b_2,    8b_3
3  0  7      0,7      0,7      0,7      0
   0  00011010,00101111,00111101,01110100; CDI = 0, 8b_3 ~ 8b_0 = 743D2F1Ah
      10101100,00111000,01110000,01100111; 8b_3 ~ 8b_0 = 677038ACh
      01110110,11011001,00101001,00011011; 8b_3 ~ 8b_0 = 1B29D976h
      10101110,11110010,01110100,00110001; 8b_3 ~ 8b_0 = 3174F2AEh
      0001                               ; Pre-coded four padded bits = 1h
      10001001,01110110,10000001,10100001; Pre-coded RS Parity Symbol,
                                         ; 8b_0 = P3_L0 = 89h, 8b_1 = P2_L1 = 76h,
                                         ; 8b_2 = P1_L0= 81h, 8b_3 = P0_L1 = A1h
   0  10011101,10110010,00100000,00110101; CDI = 0, 8b_3 ~ 8b_0 = 3520B29Dh
      11011000,11100010,11111001,11101001; 8b_3 ~ 8b_0 = E9F9E2D8h
      01000110,11101001,10101101,01100101; 8b_3 ~ 8b_0 = 65ADE946h
      00110100,00001010,00000011,10000011; 8b_3 ~ 8b_0 = 83030A34h
```

3.5.2.17.1.3 Lane 1 of 4-lane Main-Link

3.5.2.17.1.3.1 Lane 1 of 4-lane Main-Link Bit Sequence List #1

```
CDI     8b_0,    8b_1,    8b_2,    8b_3
3  0  7      0,7      0,7      0,7      0
1100  11001100,11001100,11001100,00110011; CDI = Ch, 8b_3 ~ 8b_0 = 33CCCCCCh
      01101100,10111101,11010100,11101101; 8b_3 ~ 8b_0 = EDD4BD6Ch
      01010100,01110010,00100010,01010101; 8b_3 ~ 8b_0 = 55227254h
      00010100,10010101,10001111,01001111; 8b_3 ~ 8b_0 = 4F8F9514h
0011  01001011,01010111,00011100,10100100; CDI = 3h, 8b_3 ~ 8b_0 = A41C574Bh
      11010110,10001011,10110000,11110101; 8b_3 ~ 8b_0 = F5B08BD6h
      11011011,01011100,01011101,01010100; 8b_3 ~ 8b_0 = 545D5CDBh
      00110001,10111110,00000000,11001101; 8b_3 ~ 8b_0 = CD00BE31h
```

3.5.2.17.1.3.2 Lane 1 of 4-lane Main-Link Bit Sequence List #2

```
CDI     8b_0,    8b_1,    8b_2,    8b_3
3  0  7      0,7      0,7      0,7      0
0011  00000110,10110001,10000101,10110011; CDI = 3h, 8b_3 ~ 8b_0 = B385B106h
      10110101,00011001,01100011,00001110; 8b_3 ~ 8b_0 = 0E6319B5h
      10010001,01111101,11010001,01101101; 8b_3 ~ 8b_0 = 6DD17D91h
      11010111,00100111,01100110,10100011; 8b_3 ~ 8b_0 = A36627D7h
1100  00111100,00111100,00111100,00110011; CDI = Ch, 8b_3 ~ 8b_0 = 333C3C3Ch
      01110000,00000110,11110011,10101110; 8b_3 ~ 8b_0 = AEF30670h
      01111111,10110001,10001101,10111101; 8b_3 ~ 8b_0 = BD8DB17Fh
      01101010,10110111,11000011,00001100; 8b_3 ~ 8b_0 = 0CC3B76Ah
```

3.5.2.17.1.3.3 Lane 1 of 4-lane Main-Link Bit Sequence List #3

```
CDI     8b_0,    8b_1,    8b_2,    8b_3
3  0  7      0,7      0,7      0,7      0
0011  01111101,01000010,01100100,11100010; CDI = 3h, 8b_3 ~ 8b_0 = E264427Dh
      00011000,10000010,10010101,10010110; 8b_3 ~ 8b_0 = 96958218h
      11110100,00110000,10011101,11001111; 8b_3 ~ 8b_0 = CF9D30F4h
      01100000,10010001,00101011,01010100; 8b_3 ~ 8b_0 = 542B9160h
1100  11110000,11110000,11110000,00110011; CDI = Ch, 8b_3 ~ 8b_0 = 33F0F0F0h
      01101100,10111101,11010100,11101101; 8b_3 ~ 8b_0 = EDD4BD6Ch
      01010100,01110010,00100010,01010101; 8b_3 ~ 8b_0 = 55227254h
      00010100,10010101,10001111,01001111; 8b_3 ~ 8b_0 = 4F8F9514h
   1  11000110,00110010,11110100,01100011; CDI = 1, 8b_3 ~ 8b_0 = 63F432C6h
      10110010,10000110,01101111,01010011; 8b_3 ~ 8b_0 = 536F86B2h
      01001001,00110100,11001011,00110011; 8b_3 ~ 8b_0 = 33CB3449h
      11101111,10010101,11111111,01000100; 8b_3 ~ 8b_0 = 44FF95EFh
```

3.5.2.17.1.3.4 Lane 1 of 4-lane Main-Link Bit Sequence List #4

```
CDI     8b_0,    8b_1,    8b_2,    8b_3
3  0  7      0,7      0,7      0,7      0
   1  00001100,01100101,10111110,01101100; CDI = 1, 8b_3 ~ 8b_0 = 6CBE650Ch
      01100011,11001100,10101010,01011001; 8b_3 ~ 8b_0 = 59AACC63h
      00011100,01110100,00011111,11001000; 8b_3 ~ 8b_0 = C81F741Ch
      10010101,10000000,10101010,01101001; 8b_3 ~ 8b_0 = 69AA8095h
      0001                               ; Pre-coded four padded bits = 1h
      00111101,10100101,10010001,11101011; Pre-coded RS Parity Symbol,
                                         ; 8b_0 = P3_L1 = 3Dh, 8b_1 = P2_L0 = A5h,
                                         ; 8b_2 = P1_L1 = 91h, 8b_3 = P0_L0 = EBh
   0  00010010,01100111,01010111,10110110; CDI = 0, 8b_3 ~ 8b_0 = B6576712h
      10110000,10001101,00101111,11111101; 8b_3 ~ 8b_0 = FD2F8DB0h
      10011111,00110001,01011101,10101001; 8b_3 ~ 8b_0 = A95D319Fh
      11011010,01010010,11110110,01011100; 8b_3 ~ 8b_0 = 5CF652DAh
```

3.5.2.17.1.4 Lane 2 of 4-lane Main-Link

3.5.2.17.1.4.1 Lane 2 of 4-lane Main-Link Bit Sequence List #1

```
CDI     8b_0,    8b_1,    8b_2,    8b_3
3  0  7      0,7      0,7      0,7      0
1100  11001100,11001100,11001100,00110011; CDI = Ch, 8b_3 ~ 8b_0 = 33CCCCCCh
      01101100,10111101,00110100,00100010; 8b_3 ~ 8b_0 = 2234BD6Ch
      01010000,10011100,00100101,10000011; 8b_3 ~ 8b_0 = 83259C50h
      11110010,00010101,00001000,00000110; 8b_3 ~ 8b_0 = 060815F2h
0011  00100011,11000011,00101100,11010110; CDI = 3h, 8b_3 ~ 8b_0 = D62CC323h
      10100100,01110000,01111101,01111111; 8b_3 ~ 8b_0 = 7F7D70A4h
      10011111,01000110,01000000,11010100; 8b_3 ~ 8b_0 = D440469Fh
      10011111,01000110,10101010,10011010; 8b_3 ~ 8b_0 = 9AAA469Fh
```

3.5.2.17.1.4.2 Lane 2 of 4-lane Main-Link Bit Sequence List #2

```
CDI     8b_0,    8b_1,    8b_2,    8b_3
3  0  7      0,7      0,7      0,7      0
0011  10010000,11011000,10001111,00000101; CDI = 3h, 8b_3 ~ 8b_0 = 058FD890h
      01001001,11101011,01000100,00001110; 8b_3 ~ 8b_0 = 0E44EB49h
      11000110,00100100,10100011,01011101; 8b_3 ~ 8b_0 = 5DA324C6h
      11010100,01000100,01011001,00011100; 8b_3 ~ 8b_0 = 1C5944D4h
1100  00111100,00111100,00111100,00110011; CDI = Ch, 8b_3 ~ 8b_0 = 333C3C3Ch
      10010111,11111101,10011010,00100110; 8b_3 ~ 8b_0 = 269AFD97h
      00000100,11010001,10110110,10111011; 8b_3 ~ 8b_0 = BBB6D104h
      01001001,10100111,10001101,01101011; 8b_3 ~ 8b_0 = 6B8DA749h
```

3.5.2.17.1.4.3 Lane 2 of 4-lane Main-Link Bit Sequence List #3

```
CDI     8b_0,    8b_1,    8b_2,    8b_3
3  0  7      0,7      0,7      0,7      0
0011  00001000,11110001,00110010,00000000; CDI = 3h, 8b_3 ~ 8b_0 = 0032F108h
      01100100,01011100,00101001,00110001; 8b_3 ~ 8b_0 = 31295C64h
      11011100,00000000,10000000,10100100; 8b_3 ~ 8b_0 = A48000DCh
      01010000,10001101,11001000,10101110; 8b_3 ~ 8b_0 = AEC88D50h
1100  11110000,11110000,11110000,00110011; CDI = Ch, 8b_3 ~ 8b_0 = 33F0F0F0h
      01101100,10111101,00110100,00100010; 8b_3 ~ 8b_0 = 2234BD6Ch
      01010000,10011100,00100101,10000011; 8b_3 ~ 8b_0 = 83259C50h
      11110010,00010101,00001000,00000110; 8b_3 ~ 8b_0 = 060815F2h
   1  00011110,01000001,11100100,01001101; CDI = 1, 8b_3 ~ 8b_0 = 4DE4411Eh
      10011100,00101111,00101011,11010101; 8b_3 ~ 8b_0 = D52B2F9Ch
      10001010,00111101,11000000,10110011; 8b_3 ~ 8b_0 = B3C03D8Ah
      10001010,00111101,01100110,01110110; 8b_3 ~ 8b_0 = 76663D8Ah
```

3.5.2.17.1.4.4 Lane 2 of 4-lane Main-Link Bit Sequence List #4

```
CDI     8b_0,    8b_1,    8b_2,    8b_3
3  0  7      0,7      0,7      0,7      0
   1  11101110,01110101,10000011,00000111; CDI = 1, 8b_3 ~ 8b_0 = 078375EEh
      00110100,10111101,11100010,10000111; 8b_3 ~ 8b_0 = 87E2BD34h
      00111100,01110000,01001101,00001101; 8b_3 ~ 8b_0 = 0D4D703Ch
      01001100,00110100,11100100,01100010; 8b_3 ~ 8b_0 = 62E4344Ch
      0001                               ; Pre-coded four padded bits = 1h
      01010010,11101111,11010100,11011000; Pre-coded RS Parity Symbol,
                                         ; 8b_0 = P3_L2 = 52h, 8b_1 = P2_L3 = EFh,
                                         ; 8b_2 = P1_L2 = D4h, 8b_3 = P0_L3 = D8h
   0  10100101,10100111,01100100,10001011; CDI = 0, 8b_3 ~ 8b_0 = 8B64A7A5h
      10010011,00101010,01101101,10011100; 8b_3 ~ 8b_0 = 9C6D2A93h
      11010101,01111010,00101010,11111100; 8b_3 ~ 8b_0 = FC2A7AD5h
      10111100,01011001,00000110,10010011; 8b_3 ~ 8b_0 = 930659BCh
```

3.5.2.17.1.5 Lane 3 of 4-lane Main-Link

3.5.2.17.1.5.1 Lane 3 of 4-lane Main-Link Bit Sequence List #1

```
CDI     8b_0,    8b_1,    8b_2,    8b_3
3  0  7      0,7      0,7      0,7      0
1100  11001100,11001100,11001100,00110011; CDI = Ch, 8b_3 ~ 8b_0 = 33CCCCCCh
      01101100,10111101,01110100,01010111; 8b_3 ~ 8b_0 = 5774BD6Ch
      01010111,00101000,11011111,00011000; 8b_3 ~ 8b_0 = 18DF2857h
      10110110,11101010,11110010,10001000; 8b_3 ~ 8b_0 = 88F2EAB6h
0011  01101100,11011011,11110011,01110101; CDI = 3h, 8b_3 ~ 8b_0 = 75F3DB6Ch
      00000111,11011101,00001011,10001100; 8b_3 ~ 8b_0 = 8C0BDD07h
      11100111,10101010,10101001,00101011; 8b_3 ~ 8b_0 = 2BA9AAE7h
      10101011,11101001,01100110,00000000; 8b_3 ~ 8b_0 = 0066E9ABh
```

3.5.2.17.1.5.2 Lane 3 of 4-lane Main-Link Bit Sequence List #2

```
CDI     8b_0,    8b_1,    8b_2,    8b_3
3  0  7      0,7      0,7      0,7      0
0011  01110100,10010110,10000011,00100001; CDI = 3h, 8b_3 ~ 8b_0 = 21839674h
      00011110,01001000,01111110,00001110; 8b_3 ~ 8b_0 = 0E7E481Eh
      01011100,10110101,00000000,10000010; 8b_3 ~ 8b_0 = 8200B55Ch
      00101001,11111001,10001100,11001001; 8b_3 ~ 8b_0 = C98CF929h
1100  00111100,00111100,00111100,00110011; CDI = Ch, 8b_3 ~ 8b_0 = 333C3C3Ch
      00101101,10101111,00101011,00101001; 8b_3 ~ 8b_0 = 292BAF2Dh
      10101001,01101110,10011011,10111111; 8b_3 ~ 8b_0 = BF9B6EA9h
      10001011,10111000,11111001,11010001; 8b_3 ~ 8b_0 = D1F9B88Bh
```

3.5.2.17.1.5.3 Lane 3 of 4-lane Main-Link Bit Sequence List #3

```
CDI     8b_0,    8b_1,    8b_2,    8b_3
3  0  7      0,7      0,7      0,7      0
0011  10101110,00101100,01010110,10111100; CDI = 3h, 8b_3 ~ 8b_0 = BC562CAEh
      11001100,00110111,11111110,00001011; 8b_3 ~ 8b_0 = 0BFE37CCh
      00010011,11011111,01101001,11101001; 8b_3 ~ 8b_0 = E969DF13h
      01110000,01100101,01110101,00000010; 8b_3 ~ 8b_0 = 02756570h
1100  11110000,11110000,11110000,00110011; CDI = Ch, 8b_3 ~ 8b_0 = 33F0F0F0h
      01101100,10111101,01110100,01010111; 8b_3 ~ 8b_0 = 5774BD6Ch
      01010111,00101000,11011111,00011000; 8b_3 ~ 8b_0 = 18DF2857h
      10110110,11101010,11110010,10001000; 8b_3 ~ 8b_0 = 88F2EAB6h
   1  11011011,10110110,10101110,00101100; CDI = 1, 8b_3 ~ 8b_0 = 2CAEB6DBh
      11111101,10110100,00000110,10000100; 8b_3 ~ 8b_0 = 8406B4FDh
      10100010,10011001,10011000,11100110; 8b_3 ~ 8b_0 = E69899A2h
      01100110,10100111,11011101,11111111; 8b_3 ~ 8b_0 = FFDDA766h
```

3.5.2.17.1.5.4 Lane 3 of 4-lane Main-Link Bit Sequence List #4

```
CDI     8b_0,    8b_1,    8b_2,    8b_3
3  0  7      0,7      0,7      0,7      0
   0  11111000,00111111,00000000,00011111; CDI = 0, 8b_3 ~ 8b_0 = 1F003FF8h
      11111011,01001001,00111000,10111001; 8b_3 ~ 8b_0 = B93849FBh
      01010110,11011101,01111011,11011110; 8b_3 ~ 8b_0 = DE7BDD56h
      01110111,01000110,00111010,00111010; 8b_3 ~ 8b_0 = 3A3A4677h
      0001                               ; Pre-coded four padded bits = 1h
      11100110,00111100,11000100,10010010; Pre-coded RS Parity Symbol,
                                         ; 8b_0 = P3_L3 = E6h, 8b_1 = P2_L2 = 3Ch,
                                         ; 8b_2 = P1_L3 = C4h, 8b_3 = P0_L2 = 92h
   0  00101010,01110010,00010011,00001000; CDI = 0, 8b_3 ~ 8b_0 = 0813722Ah
      11111011,01000101,10111011,10001000; 8b_3 ~ 8b_0 = 88BB45FBh
      00001100,10100010,11011010,00110000; 8b_3 ~ 8b_0 = 30DAA20Ch
      01010010,00000001,11110011,01001100; 8b_3 ~ 8b_0 = 4CF30152h
```

3.5.2.17.2 Bit Sequences on 1-lane PHY Logical Main-Link

Bit Sequence Lists #1 through #4, as highlighted in Figure 3-51, are provided in the sections that follow. The link symbols that follow LT are all programmed to be data link symbols with a value of all 0s prior to scrambling.

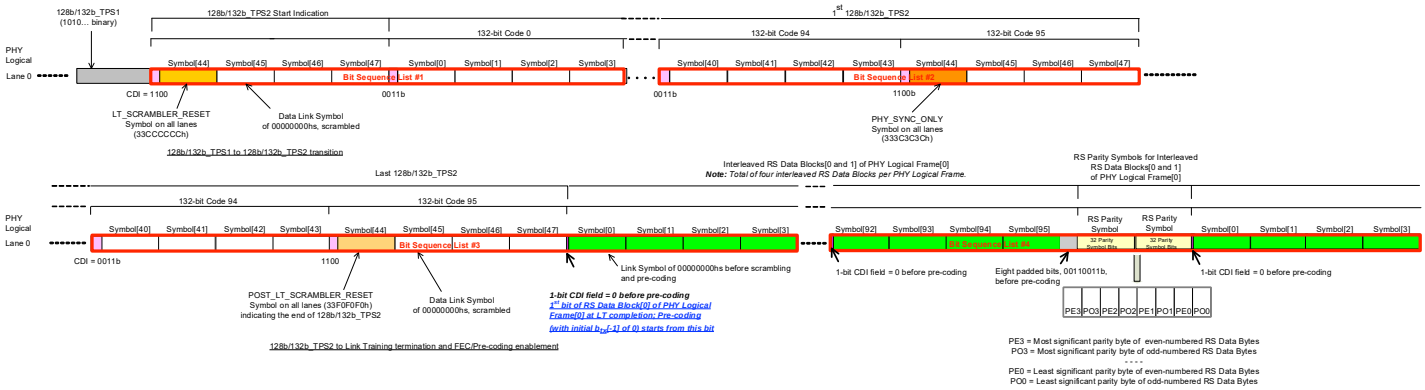


Figure 3-51: Bit Sequence Lists Illustration for 1-lane PHY Logical Main-Link

3.5.2.17.2.1 Bit Sequence that Includes RS(198, 194) FEC Parity Bytes before Pre-coding for 1-lane Main-Link

Table 3-32 illustrates a bit sequence for 1-lane configurations that includes RS(198, 194) FEC parity bytes (in hex) before pre-coding is applied for the 1st RS block, starting with 1st 1-bit CDI field that immediately follows link training completion. All symbols are data link symbols with raw data of all 0s that have been scrambled.

Table 3-32: Bit Sequence for 1-lane Configurations that Includes RS(198, 194) FEC Parity Bytes before Pre-coding[a]

Symbol #	Lane 0	
	CDI	Data
0	1	07C34F04
1		06C62675
2		ABB4B0A3
3		57CC1105
4	1	7342694E
5		03B70F1D
6		5EBA45E0
7		43D7EB30
8	0	D0F55D2C
9		8E764115
10		57D19DC3
11		A176FFCD

Table 3-32: Bit Sequence for 1-lane Configurations that Includes RS(198, 194) FEC Parity Bytes before Pre-coding[a] (Continued)

Symbol #	Lane 0	
	CDI	Data
12	0	2E644C7A
13		24A30587
14		4BA2FF89
15		621D7C46
16	1	2FA51912
17		33CAB3E6
18		882BF3ED
19		96AB3E67
20	1	5D6A9EE8
21		1D641C5C
22		C8512CF5
23		4DF4A8D8
24	0	7A5DAC96
25		092FF42B
26		C90E2E08
27		D9AF4B02
28	0	E7784E3D
29		75657F7F
30		2B547CFC
31		831A0F93
32	1	75137A60
33		D9977F89
34		9067EC5D
35		3589AF49
36	1	36F30552
37		242027BC
38		F4A0F351
39		918407E9
40	0	4928D987
41		50580061
42		549CB361
43		1DC70D38

Table 3-32: Bit Sequence for 1-lane Configurations that Includes RS(198, 194) FEC Parity Bytes before Pre-coding[a] (Continued)

Symbol #	Lane 0	
	CDI	Data
44	0	9C47712E
45		A99049F4
46		2D7A6B9A
47		539D17F2
48	1	5F61D7A7
49		3A0A2768
50		AEF63BCB
51		85051E5C
52	1	455EC932
53		37112F42
54		EB39AC61
55		E00C90E3
56	0	99D5A8F9
57		2D76F6AF
58		5996EAEF
59		6664B8D1
60	0	262F1F6D
61		006858C4
62		C825EEDA
63		72F80488
64	1	BFBC59DE
65		1EDE0011
66		B7EB6C38
67		F698EB92
68	1	D4697E73
69		229A0B48
70		6A5413B0
71		C2753941
72	0	0DCA705B
73		27ACDD8C
74		B6F7BAFF
75		56FB2F6E

Table 3-32: Bit Sequence for 1-lane Configurations that Includes RS(198, 194) FEC Parity Bytes before Pre-coding[a] (Continued)

Symbol #	Lane 0	
	CDI	Data
76	0	1A8EBC3D
77		E0026E4D
78		4156F8D5
79		925F5D1A
80	1	FB1385EC
81		9E027AD7
82		82C0F8DB
83		A031493F
84	1	8523ADAA
85		0A32FECC
86		6D46B31B
87		D62635D5
88	0	56FAEC73
89		43E65CFB
90		79F81AA3
91		45DAFD23
92	0	C5D002D4
93		58AFFA68
94		7EFE32EB
95		AE79371E
Pad		33
	FEC_ENC_PE3 = 85	
	FEC_ENC_PO3 = BD	
	FEC_ENC_PE2 = 8D	
	FEC_ENC_PO2 = 7C	
	FEC_ENC_PE1 = D2	
	FEC_ENC_PO1 = AB	
	FEC_ENC_PE0 = 7D	
	FEC_ENC_PO0 = 92	

a. 1st RS block, starting with 1st 1-bit CDI field immediately following Link Training completion.
All symbols are data link symbols with raw data of all 0s, scrambled.
1-bit CDIs are all 0s, but XOR'd with 333h before RS(198, 194) FEC encoding.
All values listed are in hex.

3.5.2.17.2.2 Lane 0 of 1-lane Main-Link Bit Sequence List #1

```
CDI     8b_0,    8b_1,    8b_2,    8b_3
3  0  7      0,7      0,7      0,7      0
1100  11001100,11001100,11001100,00110011; CDI = Ch, LT_SCRAMBLER_RESET Symbol, 8b_3 ~ 8b_0 = 33CCCCCCh
      01101100,10111101,10010100,10011000; 8b_3 ~ 8b_0 = 9894BD6Ch
      01010011,11000110,11011000,11001110; 8b_3 ~ 8b_0 = CED8C653h
      01010000,01101010,01110101,11000001; 8b_3 ~ 8b_0 = C1756A50h
0011  00000100,01001111,11000011,00000111; CDI = 3h, 8b_3 ~ 8b_0 = 07C34F04h
      01110101,00100110,11000110,00000110; 8b_3 ~ 8b_0 = 06C62675h
      10100011,10110000,10110100,10101011; 8b_3 ~ 8b_0 = ABB4B0A3h
      00000101,00010001,11001100,01010111; 8b_3 ~ 8b_0 = 57CC1105h
```

3.5.2.17.2.3 Lane 0 of 1-lane Main-Link Bit Sequence List #2

```
CDI     8b_0,    8b_1,    8b_2,    8b_3
3  0  7      0,7      0,7      0,7      0
0011  11100010,11111111,10001001,10010111; CDI = 3h, 8b_3 ~ 8b_0 = 9789FFE2h
      11100010,10111010,01011001,00001110; 8b_3 ~ 8b_0 = 0E59BAE2h
      00001011,11101100,01110010,10110010; 8b_3 ~ 8b_0 = B272EC0Bh
      00101010,10011010,10110011,01110110; 8b_3 ~ 8b_0 = 76B39A2Ah
1100  00111100,00111100,00111100,00110011; CDI = Ch, PHY_SYNC_ONLY Symbol, 8b_3 ~ 8b_0 = 333C3C3Ch
      11001010,01010100,01000010,10100001; 8b_3 ~ 8b_0 = A14254CAh
      11010010,00001110,10100000,10111001; 8b_3 ~ 8b_0 = B9A00ED2h
      10101000,10101000,10110111,10110110; 8b_3 ~ 8b_0 = B6B7A8A8h
```

3.5.2.17.2.4 Lane 0 of 1-lane Main-Link Bit Sequence List #3

```
CDI     8b_0,    8b_1,    8b_2,    8b_3
3  0  7      0,7      0,7      0,7      0
0011  11011011,10011111,00000000,01011110; CDI = 3h, 8b_3 ~ 8b_0 = 5E009FDBh
      10110000,11101001,01000010,10101100; 8b_3 ~ 8b_0 = AC42E9B0h
      00111011,11101111,01110100,10000010; 8b_3 ~ 8b_0 = 8274EF3Bh
      01000000,01111001,10010110,11111000; 8b_3 ~ 8b_0 = F8967940h
1100  11110000,11110000,11110000,00110011; CDI = Ch, POST_LT_SCRAMBLER_RESET Symbol, 8b_3 ~ 8b_0 = 33F0F0F0h
      01101100,10111101,10010100,10011000; 8b_3 ~ 8b_0 = 9894BD6Ch
      01010011,11000110,11011000,11001110; 8b_3 ~ 8b_0 = CED8C653h
      01010000,01101010,01110101,11000001; 8b_3 ~ 8b_0 = C1756A50h
   1  00000011,11000101,10111110,00000010; CDI = 1, 8b_3 ~ 8b_0 = 02BEC503h
      11010011,00011101,01000010,00000010; 8b_3 ~ 8b_0 = 02421DD3h
      01100001,10010000,10010011,01100110; 8b_3 ~ 8b_0 = 66939061h
      00000011,00001111,01000100,11001101; 8b_3 ~ 8b_0 = CD440F03h

Starting from the first 1-bit CDI field on, all bits are pre-coded prior to transmission
(e.g., CDI field value 0 is pre-coded to 1).
```

3.5.2.17.2.5 Lane 0 of 1-lane Main-Link Bit Sequence List #4

```
CDI     8b_0,    8b_1,    8b_2,    8b_3
3  0  7      0,7      0,7      0,7      0
   1  10110011,00000001,10110000,10111100; CDI = 1, 8b_3 ~ 8b_0 = BCB001B3h
      00100111,01010110,01100101,11001000; 8b_3 ~ 8b_0 = C8655627h
      10100110,00010001,10101010,11010101; 8b_3 ~ 8b_0 = D5AA11A6h
      11110101,00010010,11010111,01100101; 8b_3 ~ 8b_0 = 65D712F5h
      00010001                           ; Pre-coded eight padded bits = 11h
      10000011,10010100,10000100,00101011; Pre-coded RS Parity Symbol,
                                         ; 8b_0 = PE3 = 83h, 8b_1 = PO3 = 94h, 8b_2 = PE2 = 84h, 8b_3 = PO2 = 2Bh
      01001110,10011001,11010100,01110001; Pre-coded RS Parity Symbol,
                                         ; 8b_0 = PE1 = 4Eh, 8b_1 = PO1 = 99h, 8b_2 = PE0 = D4h, 8b_3 = PO0 = 71h
   1  10101111,11110101,11110110,10001110; CDI = 1, 8b_3 ~ 8b_0 = 8EF6F5AFh
      10010101,10000101,00100010,11011001; 8b_3 ~ 8b_0 = D9228595h
      00011110,11011010,00001001,11101001; 8b_3 ~ 8b_0 = E909DA1Eh
      10101010,00001010,00111010,01011010; 8b_3 ~ 8b_0 = 5A3A0AAAh
```

3.5.2.18 Total Data Bandwidth Efficiency (Informative)

Table 3-33 lists the calculations that are used for determining the total data bandwidth efficiency.

Table 3-33: Total Data Bandwidth Efficiency (Informative)

Parameter	Efficiency	Calculations
PHY Logical Channel Coding Efficiency	96.72%	Total number of bits transmitted per PHY Logical Frame per lane is as follows: (12 of 129-bit codes + 4 padded bits + 32 bits of RS parity symbol) / RS block × 8 RS blocks/PHY Logical Frame = 12672 bits/PHY Logical Frame/lane Total number of link symbol bits transmitted per PHY Logical Frame per lane is as follows: (12 × 128-bit super symbol) / RS blocks × 8 RS blocks/PHY Logical Frame – 32-bit PHY sync symbol/PHY Logical Frame = 12256 bits Thus, PHY Logical Channel Coding Efficiency is calculated as follows: 12256 bits / 12672 bits = 96.72%
Link Layer Overhead	0.0061%	The Link Layer adds the overhead of a 4-Symbol LLCP for every 1024 MTPs –or– 65536 symbols, thus Link Layer Overhead is calculated as follows: 4 / (4 + 65536) = 0.0061%
Total Data Bandwidth Efficiency	96.71%	Total Data Bandwidth Efficiency is calculated as follows: PHY Logical Channel Coding Efficiency × (1 – Link Layer Overhead) = 96.71%

3.5.2.19 Link Layer Frame and PHY Logical Frame Boundaries (Informative)

The Link Layer Frame is composed of four link symbols for the LLCP, and 1024 MTPs.

- Total number of link symbols, 65540, is divisible by 4

The PHY Logical Frame is composed of one PHY sync symbol and 383 link symbols

- Total number of link symbols, 383, is **not** divisible by 4
- Link Layer's total number of link symbols, 65540, is **not** divisible by 383

Therefore:

- Phase of the 4-link symbol sequence of LLCPs relative to the super symbol boundary changes every PHY Logical Frame
- LLCP phase relative to PHY sync symbol changes at every Link Layer Frame
  - LLCP 4-link symbol sequence is likely to straddle the PHY sync symbol

3.5.3 Main-Link PHY Logical Sublayer FEC- and PHY Test-related Registers

3.5.3.1 DPCD Registers Used for FEC

Table 3-34 lists the DPCD registers that are used for FEC support. (For complete register descriptions, see Table 2-183 through Table 2-185.)

Table 3-34: DPCD Registers Used for FEC

DPCD Address	Register
00090h	FEC_CAPABILITY_0
00091h	FEC_CAPABILITY_1
00120h	FEC_CONFIGURATION
00280h	FEC_STATUS
00281h and 00282h	FEC_ERROR_COUNT

FEC-related policy needs are discussed in the following sections:

- **Accounting for FEC overhead in SST mode** – Section 2.2
- **Accounting for FEC overhead in MST mode** – Section 2.6
- **Accounting for FEC overhead in DSC bitstream transport, both in SST and MST modes** – Section 2.6.1.1
- FEC support – Section 5
  - **Devices supporting DSC (compression and/or decompression)** – Shall be supported
  - **MST Branch device** – Should be supported
  - **PHY Repeater** – Does **not** need to be supported

3.5.3.2 DPCD Registers Used for FEC for LT-tunable Bit-level PHY Repeaters

Updated in *DP v2.0*.

FEC decoding and re-encoding by an LT-tunable Bit-level PHY Repeater may be supported. Table 3-35 lists the DPCD registers that are used for FEC support for LT-tunable Bit-level PHY Repeaters. (For complete register descriptions, see Table 2-198 and Table 2-199.)

Table 3-35: DPCD Registers Used for FEC for LT-tunable Bit-level PHY Repeaters

DPCD Address	Register
F0000h	LT_TUNABLE_PHY_REPEATER_FIELD_DATA_STRUCTURE_REV
F0290h	FEC_STATUS_PHY_REPEATER1
F0291h and F0292h	FEC_ERROR_COUNT_PHY_REPEATER1
F0294h	FEC_CAPABILITY_0_PHY_REPEATER1
F0295h	FEC_CAPABILITY_1_PHY_REPEATER1
F0298h	FEC_STATUS_PHY_REPEATER2
F0299h and F029Ah	FEC_ERROR_COUNT_PHY_REPEATER2
F029Ch	FEC_CAPABILITY_0_PHY_REPEATER2
F029Dh	FEC_CAPABILITY_1_PHY_REPEATER2
F02A0h	FEC_STATUS_PHY_REPEATER3
F02A1h and F02A2h	FEC_ERROR_COUNT_PHY_REPEATER3
F02A4h	FEC_CAPABILITY_0_PHY_REPEATER3
F02A5h	FEC_CAPABILITY_1_PHY_REPEATER3
F02A8h	FEC_STATUS_PHY_REPEATER4
F02A9h and F02AAh	FEC_ERROR_COUNT_PHY_REPEATER4
F02ACh	FEC_CAPABILITY_0_PHY_REPEATER4
F02ADh	FEC_CAPABILITY_1_PHY_REPEATER4
F02B0h	FEC_STATUS_PHY_REPEATER5
F02B1h and F02B2h	FEC_ERROR_COUNT_PHY_REPEATER5
F02B4h	FEC_CAPABILITY_0_PHY_REPEATER5
F02B5h	FEC_CAPABILITY_1_PHY_REPEATER5

Table 3-35: DPCD Registers Used for FEC for LT-tunable Bit-level PHY Repeaters (Continued)

DPCD Address	Register
F02B8h	FEC_STATUS_PHY_REPEATER6
F02B9h and F02BAh	FEC_ERROR_COUNT_PHY_REPEATER6
F02BCh	FEC_CAPABILITY_0_PHY_REPEATER6
F02BDh	FEC_CAPABILITY_1_PHY_REPEATER6
F02C0h	FEC_STATUS_PHY_REPEATER7
F02C1h and F02C2h	FEC_ERROR_COUNT_PHY_REPEATER7
F02C4h	FEC_CAPABILITY_0_PHY_REPEATER7
F02C5h	FEC_CAPABILITY_1_PHY_REPEATER7
F02C8h	FEC_STATUS_PHY_REPEATER8
F02C9h and F02CAh	FEC_ERROR_COUNT_PHY_REPEATER8
F02CCh	FEC_CAPABILITY_0_PHY_REPEATER8
F02CDh	FEC_CAPABILITY_1_PHY_REPEATER8

3.5.3.3 FEC Error Counters

Note: *Symbol size of Reed Solomon (RS) FEC is dependent on the type of channel coding used:*

- ***8b/10b channel coding*** *– For RS(254, 250) FEC, the symbol size is set to 10 bits.*
- ***128b/132b channel coding*** *– For RS(198, 194) FEC, the symbol size is 8 bits. Four 8-bit parity symbols (referred to as "four parity bytes") are mapped to one 32-bit RS parity symbol, as defined in Section 3.5.2.4 and Section 3.5.2.11.*

New to *DP v1.4a*. Updated in *DP v2.0*.

Table 3-36 defines the five internal error counters that an FEC-capable DPRX shall use to count FEC block and bit errors.

Table 3-36: FEC Error Counters

Counter	Description[a]
UNCORRECTED_BLOCK_ERROR_COUNT	Counts RS data symbol uncorrected FEC block errors.
CORRECTED_BLOCK_ERROR_COUNT	Counts RS data symbol corrected FEC block errors.
CORRECTED_BIT_ERROR_COUNT	Counts RS data symbol corrected FEC bit errors.
PARITY_BLOCK_ERROR_COUNT	Counts RS parity symbol corrected FEC block errors.
PARITY_BIT_ERROR_COUNT	Counts RS parity symbol corrected FEC bit errors.

a. Counter capability is enabled by setting its associated bit in the FEC_CAPABILITY_0 register (DPCD Address 00090h, bits 1:5, respectively).

The FEC-capable DPRX shall maintain each of the five internal error counters, per lane:

- Twenty internal error counters in a 4-lane configuration
- Ten internal error counters in a 2-lane configuration
- Five internal error counters in a 1-lane configuration

All error counters shall be 15 bits wide, and saturate at the maximum value ($2^{15} - 1$). Therefore, an FEC-capable DPRX shall set all five FEC Error Counter Capability declaration bits and FEC_ERROR_REPORTING_POLICY_SUPPORTED bit in the FEC_CAPABILITY_0 register (DPCD Address 00090h, bits 5:1 and bit 7, respectively) to all 1s. These six capability/policy bits are included so that an upstream DPTX can identify FEC-capable DPRX implementations that precede the FEC_ERROR_COUNT register (DPCD Addresses 00281h and 00282h) specification update.

All internal counters shall be cleared whenever the FEC_ERROR_COUNT_SEL field in the FEC_CONFIGURATION register (DPCD Address 00120h, bits 3:1) is cleared to 000b to indicate FEC_ERROR_COUNT_DIS. When the FEC_ERROR_COUNT_SEL field is programmed to any other value, all internal counters shall be continuously updated based on the errors detected by the FEC decoders. A single error can cause the update of more than one internal counter. Similarly, all internal counters shall be continuously updated based on errors that are detected by the FEC decoders, regardless of the register's LANE_DEC_SELECT field (bits 5:4) value.

To access one of the internal error counters, the following FEC_CONFIGURATION register fields shall be programmed to select a specific internal counter:

- FEC_ERROR_COUNT_SEL field (bits 3:1) and
- LANE_DEC_SELECT field (bits 5:4) –or– AGGREGATED_ENABLED_LANES_ERRORS bit (bit 6)

Based on these configuration bits, the selected internal counter's value (or aggregated value from several internal counters) can be read from the FEC_ERROR_COUNT register.

To read from the counter selected by the FEC_ERROR_COUNT_SEL and LANE_DEC_SELECT fields, the DPTX shall read the two bytes of the FEC_ERROR_COUNT register (DPCD Addresses 00281h and 00282h) with a single AUX burst read transaction. The two bytes read from the FEC_ERROR_COUNT register shall represent the selected internal counter's value at the time of the read from the lower byte (DPCD Address 00281h). In other words, when the byte at DPCD Address 00281h is read, the DPRX shall return the lower bits of the selected internal counter and concurrently make the upper bits of the same counter available for the subsequent byte read from DPCD Address 00282h (which will be the next access in the burst read).

The register's FEC_ERROR_COUNT_VALID bit value returned by a read from the upper byte (DPCD Address 00282h, bit 7) shall be 1 whenever the internal count value is valid. This shall be the case as long as both of the following conditions exist in the FEC_CONFIGURATION register (DPCD Address 00120h):

- FEC_READY bit (bit 0) is set to 1 (8b/10b channel coding only)
- FEC_ERROR_COUNT_SEL field, and LANE_DEC_SELECT field –or– AGGREGATED_ENABLED_LANES_ERRORS bit, select a valid internal counter

Each internal counter (20, 10, or 5 in a 4-, 2-, or 1-lane configuration, respectively) is updated, based on error conditions that are detected by the RS decoders, either RS(254, 250) for 8b/10b channel coding or RS(198, 194) for 128b/132b channel coding. Some errors can be attributed to a particular DP Main-Link lane, while others cannot due to interleaving in the RS decoders. Therefore, some error types are attributed to the Main-Link lane, whereas others are attributed to the RS decoder.

In 4- and 2-lane configurations, each RS decoder is assigned a number. The decoder number corresponds to the Main-Link lane to which it is associated. Specifically, the RS decoder assigned the number *i* is the decoder that shall process the even-numbered RS data symbols that are carried over Main-Link *i*.

In a 1-lane configuration, regardless of the physical implementation, there is assumed to be only one RS decoder. Therefore, all errors attributed to the RS decoder shall be attributed to Decoder 0. However, in a 1-lane configuration, two RS blocks are carried in a single FEC block. Block-based error conditions shall be counted per RS block, and **not** per FEC block.

The mechanism that is used for counting the different error types is described in the sections that follow.

3.5.3.3.1 Uncorrectable FEC Block Errors

In 4- and 2-lane configurations, if an RS decoder detects an uncorrectable FEC block, it shall increment the associated internal UNCORRECTED_BLOCK_ERROR_COUNT counter by one.

In a 1-lane configuration, an RS decoder can detect an uncorrectable FEC block in one or both of the two RS FEC blocks that are contained within one FEC block. Each uncorrectable RS FEC block shall cause the UNCORRECTED_BLOCK_ERROR_COUNT counter associated with Decoder 0 to increment once, thus allowing the counter to increment up to two times for the uncorrectable FEC block errors found in one FEC block.

In 4- and 2-lane configurations, each RS decoder processes an RS FEC block that contains interleaved symbols from two different DP Main-Link lanes. When an uncorrectable RS FEC block is detected, it is impossible to determine which symbols within the block are corrupt, and thus the corruptions may have come from any of the Main-Link lanes. As a result, an uncorrectable FEC block error shall be attributed to an RS decoder, not a Main-Link lane, and the associated internal UNCORRECTED_BLOCK_ERROR_COUNT counter shall be incremented.

Note: *It is impossible to detect all possible combinations of uncorrectable FEC blocks. The RS code is capable of correcting up to two errored symbols within each RS FEC block. Due to inherent limitations within the RS code, when the number of symbol errors within an RS FEC block is more than two, the RS decoder may do one of the following:*

- *Determine that the FEC block is uncorrectable (and is therefore counted here)*
- *Conclude that the FEC block contains only one or two errored symbols, which may be different than the actual errored symbols in the RS FEC block*
  - *Corresponding CORRECTED_BLOCK_ERROR_COUNT, CORRECTED_BIT_ERROR_COUNT, PARITY_BLOCK_ERROR_COUNT, and/or PARITY_BIT_ERROR_COUNT counters will be incremented instead*
  - *This will result in additional symbols being corrupted*
- *Conclude that the FEC block contains no errors*
  - *This condition would occur only rarely*
  - *Under this condition, no error counters are incremented*

The associated internal UNCORRECTED_BLOCK_ERROR_COUNT counter shall be readable from the FEC_ERROR_COUNT register (DPCD Addresses 00281h and 00282h) when the FEC_ERROR_COUNT_SEL field in the FEC_CONFIGURATION register is programmed to UNCORRECTED_BLOCK_ERROR_COUNT (DPCD Address 00120h, bits 3:1, are programmed to 001b).

3.5.3.3.2 Corrected FEC Block Errors

For RS FEC interleaving, either RS(254, 250) for 8b/10b channel coding or RS(198, 194) for 128b/132b channel coding, 4- and 2-lane configurations and 1-lane configuration are handled differently, as defined in the sections that follow.

3.5.3.3.2.1 Corrected FEC Block Errors – 4- and 2-lane Configurations

In 4- and 2-lane configurations, each RS decoder is capable of detecting and correcting up to two symbols within the RS FEC block. When performing correction, the RS decoder can determine which symbol(s) contains errors.

The DPRX shall implement three internal bit error counters per lane/decoder:

- UNCORRECTED_BLOCK_ERROR_COUNT
- CORRECTED_BLOCK_ERROR_COUNT
- PARITY_BLOCK_ERROR_COUNT

The RS FEC block consists of the following:

- RS data symbols (10 bits in size for RS(254, 250) and 8 bits in size for RS(198, 194), which are formed from the even/odd interleaving of the RS symbols from a pair of lanes
- Four RS parity symbols (10 bits in size for RS(254, 250) and 8 bits in size for RS(198, 194) containing parity information in any of the lanes

Due to the simple even/odd interleaving of RS data symbols, when an error is detected in an RS data symbol, it is easy to determine over which Main-Link lane the error occurred. Conversely, errors detected in the RS parity symbols may be caused by corruption within any of the Main-Link lanes. As a result, a DPRX shall maintain two internal counters per lane/decoder for counting corrected FEC blocks – CORRECTED_BLOCK_ERROR_COUNT and PARITY_BLOCK_ERROR_COUNT.

The CORRECTED_BLOCK_ERROR_COUNT counter shall count the FEC blocks that had at least one RS data symbol corrected, as follows:

- If Decoder 2i corrects at least one even-numbered RS data symbol, this counts as a corrected FEC block for Lane 2i
- If Decoder 2i corrects at least one odd-numbered RS data symbol, this counts as a corrected FEC block for Lane 2i + 1.
- If Decoder 2i + 1 corrects an even-numbered RS data symbol, this counts as a corrected FEC block for Lane 2i + 1
- If Decoder 2i + 1 corrects an odd-numbered RS data symbol, this counts as a corrected FEC block for Lane 2i

Although there can be up to four corrected RS data symbols on a Main-Link lane within a given FEC block period (i.e., two even-numbered RS data symbols in one decoder and two odd-numbered RS data symbols in the other decoder), each CORRECTED_BLOCK_ERROR_COUNT counter can increment only once during an FEC block period.

The appropriate internal CORRECTED_BLOCK_ERROR_COUNT counter shall be readable from the FEC_ERROR_COUNT register (DPCD Addresses 00281h and 00282h) when the FEC_ERROR_COUNT_SEL field in the FEC_CONFIGURATION register (DPCD Address 00120h, bits 3:1) is programmed to 010b.

The PARITY_BLOCK_ERROR_COUNT counter shall count the FEC blocks in which at least one RS parity symbol was corrected. RS parity symbol FEC block errors are counted per each RS decoder; if Decoder *i* corrects an error in an RS parity symbol, the internal PARITY_BLOCK_ERROR_COUNT counter for Decoder *i* shall be incremented. Although the RS decoder can correct errors in up to two RS parity symbols, each PARITY_BLOCK_ERROR_COUNT counter can increment only once during an FEC block period.

The appropriate internal PARITY_BLOCK_ERROR_COUNT counter shall be readable from the FEC_ERROR_COUNT register when the FEC_ERROR_COUNT_SEL field is programmed to 100b.

If RS data symbol and RS parity symbol FEC errors are corrected, the appropriate lane's CORRECTED_BLOCK_ERROR_COUNT counter and appropriate decoder's PARITY_BLOCK_ERROR_COUNT counter shall both be incremented.

3.5.3.3.2.2 Corrected FEC Block Errors – 1-lane Configuration

In a 1-lane configuration, a corrected FEC block can be detected in one or both of the two RS FEC blocks contained within one FEC block, in RS data symbols and/or RS parity symbols. The internal CORRECTED_BLOCK_ERROR_COUNT counter for Lane 0 shall be incremented once for each RS FEC block that contains at least one corrected RS data symbol. Similarly, the PARITY_BLOCK_ERROR_COUNT counter for Decoder 0 shall be incremented once for each RS FEC block that contains at least one corrected RS parity symbol.

3.5.3.3.3 Corrected FEC Bit Errors

When the RS decoder corrects an errored symbol, the number of corrected FEC bits can be determined by comparing the errored and corrected symbol. In a similar manner to the FEC block error counters defined in Section 3.5.3.3.2.1, RS data symbol errors shall be attributed to DP Main-Link lanes, whereas RS parity symbol errors shall be attributed to decoders. The DPRX shall implement two internal FEC bit error counters per lane/decoder:

- CORRECTED_BIT_ERROR_COUNT
- PARITY_BIT_ERROR_COUNT

In 4- and 2-lane configurations, when RS data symbol FEC bit errors are detected, the internal CORRECTED_BIT_ERROR_COUNT counter for the appropriate lane shall be incremented by the number of flipped bits in the RS code. Similar to the FEC block error counters defined in Section 3.5.3.3.2.1, FEC bit errors shall be attributed to a decoder, as follows:

- Even-numbered RS data symbols of Decoder 2*i* shall be attributed to Lane 2*i*
- Odd-numbered RS data symbols of Decoder 2*i* shall be attributed to Lane 2*i* + 1
- Even-numbered RS data symbols of Decoder 2*i* + 1 shall be attributed to Lane 2*i* + 1
- Odd-numbered RS data symbols of Decoder 2*i* + 1 shall be attributed to Lane 2*i*

In a 1-lane configuration, the internal CORRECTED_BIT_ERROR_COUNT counter for Lane 0 shall be incremented by the number of flipped bits in the RS code, regardless of which decoder detected the errors.

The appropriate internal CORRECTED_BIT_ERROR_COUNT counter shall be readable from the FEC_ERROR_COUNT register (DPCD Addresses 00281h and 00282h) when the FEC_ERROR_COUNT_SEL field in the FEC_CONFIGURATION register (DPCD Address 00120h, bits 3:1) is programmed to 011b.

In 4- and 2-lane configurations, when Decoder *i* detects RS parity symbol FEC bit errors, the number of flipped bits shall be added to the internal PARITY_BIT_ERROR_COUNT counter for Decoder *i*.

In a 1-lane configuration, the internal PARITY_BIT_ERROR_COUNT counter Decoder 0 shall be incremented by the number of flipped bits in the RS code, regardless of which decoder detected the errors.

Note: ***8b/10b channel coding only*** *– Due to 8b/10b parity-code decoding in a DPRX, the number of bits that are flipped in the RS parity symbols may not be the same as the number of bits that are flipped on the Main-Link lane.*

The appropriate internal PARITY_BIT_ERROR_COUNT counter shall be readable from the FEC_ERROR_COUNT register when the FEC_ERROR_COUNT_SEL field is programmed to 101b.

3.5.3.4 DPCD Registers Used for PHY Test Modes

Table 3-37 lists the DPCD registers that are used for PHY test modes. Although the same registers used for 8b/10b channel coding are also used for 128b/132b channel coding, the registers function differently, depending on the channel coding type. (For complete register descriptions, see Table 2-184.)

Table 3-37: DPCD Registers Used for PHY Test Modes

DPCD Address	Register
00102h	TRAINING_PATTERN_SET
0010Bh	LINK_QUAL_LANE0_SET
0010Ch	LINK_QUAL_LANE1_SET
0010Dh	LINK_QUAL_LANE2_SET
0010Eh	LINK_QUAL_LANE3_SET
00120h	FEC_CONFIGURATION

3.5.4 8b/10b Main-Link Electrical Sub-block

Entire section updated in *DP v1.4a*.

The electrical sub-block of a DP Main-Link consists of up to four differential pairs. The DPTX drives doubly terminated, AC-coupled differential pairs, as illustrated in Figure 3-52, in a manner that is compliant with the Main-Link Transmitter electrical specification.

Note: *The 50Ω termination resistors may be integrated on the chip. The DPRX receives incoming differential signals and extracts data with its link clock and data recovery (CDR) circuits.*

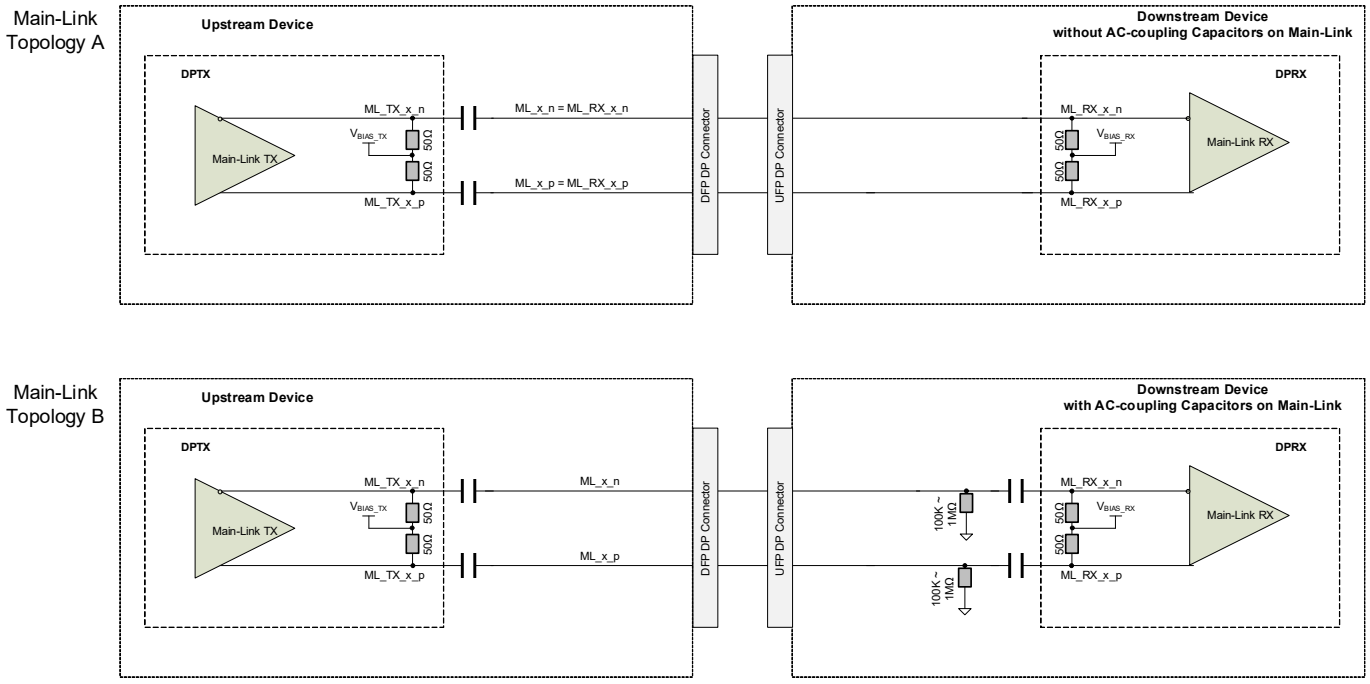


Figure 3-52: Main-Link Differential Pair

Table 3-38 through Table 3-42 define the Main-Link transmitter electrical parameters. Table 3-43 through Table 3-46 define the Main-Link receiver electrical parameters. (Table 3-39, Table 3-41, and Table 3-45 are new to *DP v1.4a*. Table 3-42 was replaced in *DP v1.4a*.)

Table 3-38: DP Main-Link Transmitter System Parameters

Symbol	Parameter	Min	Nom	Max	Units	Comments
System Parameters						
f_{HBR3}	Frequency for high bit rate 3	8.05707	8.1	8.10243	Gbps	Frequency high limit = +300ppm Frequency low limit = -5300ppm
f_{HBR2}	Frequency for high bit rate 2	5.37138	5.4	5.40162	Gbps	
f_{HBR}	Frequency for high bit rate	2.68569	2.7	2.70081	Gbps	
f_{RBR}	Frequency for reduced bit rate	1.611414	1.62	1.620486	Gbps	
UI_HBR3	Unit Interval for high bit rate 3 (8.1Gbps/lane)		123		ps	Informative (approximate values)
UI_HBR2	Unit Interval for high bit rate 2 (5.4Gbps/lane)		185		ps	
UI_HBR	Unit Interval for high bit rate (2.7Gbps/lane)		370		ps	
UI_RBR	Unit Interval for reduced bit rate (1.62Gbps/lane)		617		ps	
Down_Spread _Amplitude	Link clock down spreading	0		0.5	%	Range: 0 to 0.5% when down spread is enabled
Down_Spread _Frequency	Link clock down-spreading frequency	30		33	kHz	Range: 30 to 33kHz when down spread is enabled
C_{TX}	AC-coupling Capacitor	75		265	nF	All DP Main-Link lanes as well as AUX_CH shall be AC-coupled. AC-coupling capacitors shall be placed on the transmitter side. AC-coupling capacitors may also be placed on the receiver side.

Table 3-39: HBR3/HBR2 DP Main-Link Transmitter TP2 Parameters

Symbol	Parameter	Min	Nom	Max	Units	Comments
TP2 (TX External Connector – Normative)[a]						
$V_{TX\_OUTPUT\_LEVEL0\_RATIO\_HBR2\_HBR3}$	Ratio of Voltage Swing VSL[1] / VSL[0]	1.6		4.5	dB	• Calculated using measured value of 1st harmonic of FFT at TX_EQL[0] • VSL[3] mandatory
	Ratio of Voltage Swing VSL[2] / VSL[0]	3.2		7.0	dB	
	Ratio of Voltage Swing VSL[3] / VSL[0]	4.8		10.5	dB	
$V_{TX\_OUTPUT\_RATIO\_HBR2\_HBR3}$	Ratio of Voltage Swing VSL[1] / VSL[0]	1.6			dB	• Calculated using measured value of 1st harmonic of FFT at TX_EQL[0] • VSL[3] mandatory
	Ratio of Voltage Swing VSL[2] / VSL[1]	1.1			dB	
	Ratio of Voltage Swing VSL[3] / VSL[2]	1.1			dB	
$V_{TX\_MEQ\_LEVEL0\_DELTA\_HBR2\_HBR3}$	Delta of TX Emphasis TX_EQL[1] / TX_EQL[0]	1.3		4.0	dB	• Applies to all valid VSLs • Calculated using measured value of 1st and 5th harmonics of FFT • For a given VSL[*M*]: TX_EQL[*N*] / TX_EQL[0] = (5th – 1st)[*N*] – (5th – 1st)[0] • TX_EQL[3] mandatory
	Delta of TX Emphasis TX_EQL[2] / TX_EQL[0]	2.4		6.0	dB	
	Delta of TX Emphasis TX_EQL[3] / TX_EQL[0]	3.5		8.0	dB	
$V_{TX\_MEQ\_DELTA\_HBR2\_HBR3}$	Delta of TX Emphasis TX_EQL[1] / TX_EQL[0]	1.3			dB	• Applies to all valid VSLs • Calculated using measured value of 1st and 5th harmonics of FFT • For a given VSL[*M*]: TX_EQL[*N*] / TX_EQL[*N* – 1] = (5th – 1st)[*N*] – (5th – 1st)[*N* – 1] • TX_EQL[3] mandatory
	Delta of TX Emphasis TX_EQL[2] / TX_EQL[1]	0.7			dB	
	Delta of TX Emphasis TX_EQL[3] / TX_EQL[2]	0.7			dB	

Table 3-39: HBR3/HBR2 DP Main-Link Transmitter TP2 Parameters (Continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
TP2 (TX External Connector – Normative)[a]						
$V_{TX\_PE\_RATIO\_HBR2\_HBR3}$	Ratio of PE[*N*] / TX_MEQ[*N*]	2/3				• Applies to all valid VSL and TX_EQL combinations • PE[*N*] = 5^{th}[*N*] – 5^{th}[0] • Pass/fail based on PE vs. TX_MEQ specification (see Figure 3-53)
$V_{TX\_TRANSITION\_BIT\_OUTPUT\_RATIO\_PEL[N]/PEL[N-1]\_HBR2\_HBR3}$	Transition Bit Amplitude Ratio between TX_EQL[*N*] and TX_EQL[*N* – 1] for a Given VSL[*M*]	0			dB	• TX_EQL[*N*] transition bit amplitude shall be greater than or equal to that of TX_EQL[*N* – 1] • 5^{th} (*N*) – 5^{th} (*N* – 1)
$V_{TX\_DIFFpp\_MAX}$	Maximum Differential Output Voltage Swing			1.38	V_diff_pp	• For all VSL and TX_EQL combinations

a. All parameters to be tested with PLTPAT, and with SSC disabled. SSC is disabled when the SPREAD_AMP bit in the DOWNSPREAD_CTRL register (DPCD Address 00107h, bit 4) is cleared to 0.

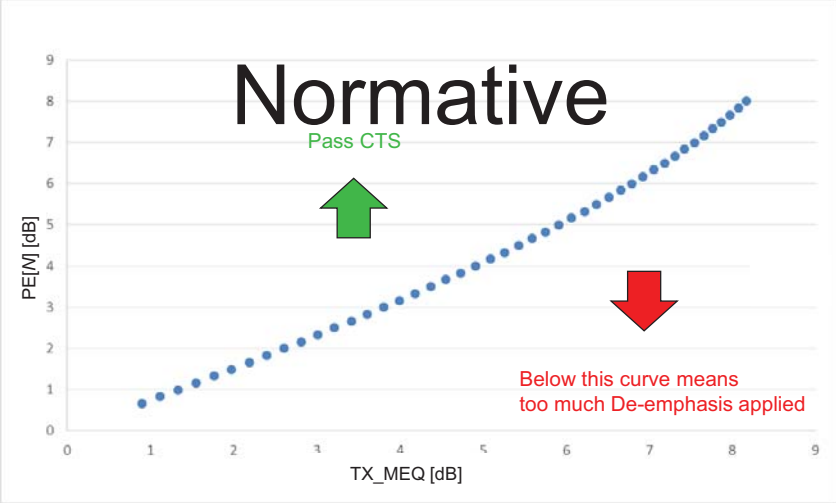


Figure 3-53: PE vs. TX_MEQ Specification (Normative)

Notes: *TX_MEQ = (Gain at 5^{th} Harmonic[N] – Gain at 1^{st} Harmonic[N]) – (Gain at 5^{th} Harmonic[0] – Gain at 1^{st} Harmonic[0]) in dB PE[N] = 5^{th}[N] – 5^{th}[0] in dB.*

TX_MEQ is influenced by not only the 5^{th} harmonic, but also by the 1^{st} harmonic, which is non-linear to TX_AEQ.

Table 3-40: HBR/RBR DP Main-Link Transmitter TP2 Parameters

Symbol	Parameter	Min	Nom	Max	Units	Comments
TP2 (TX External Connector – Normative)						
$V_{TX\text{-}OUTPUT\text{-}RATIO\_RBR\_HBR}$[a]	Ratio of Output Voltage Level 1/Level 0	0.8		6.0	dB	Measured on non-transition bits at Pre-emphasis Level 0 setting. Voltage Level 3 may be supported.
	Ratio of Output Voltage Level 2/Level 1	0.1		5.1	dB	
	Ratio of Output Voltage Level 3/Level 2	0.8		6.0	dB	
$V_{TX\text{-}PREEMP\text{-}OFF}$	Maximum Pre-emphasis when disabled			0.25	dB	Pre-emphasis Level 0 setting shall not show any pre-emphasis at TP2 to prevent link training issues.
$V_{TX\text{-}PREEMP\text{-}DELTA}$	Delta of Pre-emphasis Level 1 vs. Level 0	2			dB	Applies to all valid voltage settings. Pre-emphasis Level 3 may be supported.
	Delta of Pre-emphasis Level 2 vs. Level 1	1.6			dB	
	Delta of Pre-emphasis Level 3 vs. Level 2	1.6			dB	
$V_{TX\text{-}DIFF\_REDUCTION}$	Non-transition reduction Output Voltage Level 2			3	dB	V_{TX_DIFF} at each non-zero nominal pre-emphasis level shall not be lower than the specified amount less than V_{TX_DIFF} at the zero nominal pre-emphasis level.
	Non-transition reduction Output Voltage Level 1			3	dB	
	Non-transition reduction Output Voltage Level 0			1.4	dB	
$V_{TX\text{-}DIFFp\text{-}p\text{-}MAX}$	Maximum Output Voltage Level			1.38	V	For all Output Level and Pre-emphasis combinations.
$t_{TX\text{-}SKEW\text{-}INTER\_PAIR}$	Lane-to-Lane Output Skew			1250	ps	Applies to transmitters capable of 2- and 4-lane operation. Applies to all pairwise combinations of supported lanes for all data rates.
$t_{TX\text{-}SKEW\text{-}INTRA\_PAIR}$	Lane Intra-pair Output Skew			30	ps	Applies to all supported lanes.

a. Earlier versions of this Standard had the Main-Link DPTX output voltage ratios to ensure that the DPTX supports the specified range of output voltage levels. For HBR2 and higher, the Voltage Swing and Pre-emphasis level checks are defined using the spectral method, as defined in Table 3-39.

Table 3-41: HBR3 DP Main-Link Transmitter TP2_CTLE and TP3_CTLE Parameters

Parameter	HBR3 DP Source Device TX Limits[a]		Unit	Comments
Test Point	TP2_CTLE (Informative)	TP3_CTLE		
Training Pattern	TPS4			
Drive Setting	Any Voltage Swing and Pre-emphasis level combination may be used; however, that same combination shall be used for both		mV_diff_pp	
RJ_{rms}	Bound by TJ and Non-ISI jitter limit		mUI	
SJ_{SWEEP}	N/A		mUI	
SJ_{FIXED}	N/A		mUI	
A_dc	≥ -8		dB	
Residual ISI	TJ minus Non-ISI Jitter		mUI	
Non-ISI	≤ 230		mUI	
TJ	≤ 330	≤ 470	mUI	SSC is enabled if supported.[b]
EH	≥ 65	≥ 65	mV_diff_pp	
BER	$1E^{-6}$		UI	

a. TP2_CTLE values are intended to test a no/short channel usage. TP3_CTLE values are intended for a long channel (cabled) usage.

b. SSC is supported when the MAX_DOWNSPREAD bit in the MAX_DOWNSPREAD register(s) (DPCD Address(es) 00003h and 02203h, bit 0) is set to 1. SSC is enabled or disabled when the SPREAD_AMP bit in the DOWNSPREAD_CTRL register (DPCD Address 00107h, bit 4) is set to 1 or cleared to 0, respectively.

Table 3-42: HBR2 DP Main-Link Transmitter TP2 and TP3_EQ Parameters

Parameter	HBR2 DP Source Device TX Limits		Unit	Comments
Test Point	TP2 (Informative)	TP3_EQ		
Training Pattern	CP2520			
Drive Setting	Any Voltage Swing and Pre-emphasis level combination may be used; however, that same combination shall be used for both		mV_diff_pp	
RJ_{rms}	0.13		UI	
Non-ISI[a]	≤ 380	≤ 360	mUI	
TJ[a]	≤ 600	≤ 580	mUI	SSC is enabled if supported.[b]
EH	≥ 40	≥ 90	mV_diff_pp	
BER	$1E^{-9}$		UI	

a. TP2 Non-ISI and TJ include a de-rating of 0.02UI to account for only mated connector crosstalk (NEXT). TP3_EQ Non-ISI and TJ include a de-rating of 0.04UI to account for cable crosstalk effect.

b. SSC is supported when the MAX_DOWNSPREAD bit in the MAX_DOWNSPREAD register(s) (DPCD Address(es) 00003h and 02203h, bit 0) is set to 1. SSC is enabled or disabled when the SPREAD_AMP bit in the DOWNSPREAD_CTRL register (DPCD Address 00107h, bit 4) is set to 1 or cleared to 0, respectively.

Table 3-43: DP Main-Link Receiver System Parameters

Symbol	Parameter	Min	Nom	Max	Units	Comments
System Parameters						
f_{HBR3}	Frequency for high bit rate 3	8.05707	8.1	8.10243	Gbps	Frequency high limit = +300ppm
f_{HBR2}	Frequency for high bit rate 2	5.37138	5.4	5.40162	Gbps	Frequency low limit = -5300ppm
f_{HBR}	Frequency for high bit rate	2.68569	2.7	2.70081	Gbps	DP link RX does not require local crystal for link clock generation.
f_{RBR}	Frequency for reduced bit rate	1.611414	1.62	1.620486	Gbps	
UI_HBR3	Unit Interval for high bit rate 3 (8.1Gbps/lane)		123		ps	Informative (approximate values)
UI_HBR2	Unit Interval for high bit rate 2 (5.4Gbps/lane)		185		ps	
UI_HBR	Unit Interval for high bit rate (2.7Gbps/lane)		370		ps	
UI_RBR	Unit Interval for reduced bit rate (1.62Gbps/lane)		617		ps	
Down_Spread _Amplitude	Link clock down spreading	0		0.5	%	Up to 0.5% down spread shall be supported. Modulation frequency range of 30 to 33kHz shall be supported.

Table 3-44: DP Main-Link Receiver TP3 Parameters

Symbol	Parameter	Min	Nom	Max	Units	Comments
TP3 (RX External Connector – Normative)						
t_{RX-EYE_CONN}	Minimum Receiver EYE Width at RX-side connector pins	0.25			UI	For Reduced Bit Rate (1 - T_{RX-EYE_CONN}) specifies the allowable TJ.
$t_{RX-SKEW-INTRA\_PAIR\ HBR3}$	Lane Intra-pair Skew Tolerance			50	ps	For HBR3. Represents the skew (between D+ and D- of the same lane) contribution from the cable in addition to the stressed EYE at TP3_EQ.
$t_{RX-SKEW-INTRA\_PAIR\ HBR2}$	Lane Intra-pair Skew Tolerance			50	ps	For HBR2. Represents the skew (between D+ and D- of the same lane) contribution from the cable in addition to the stressed EYE at TP3_EQ.
$t_{RX-SKEW-INTRA\_PAIR\ High-Bit-Rate}$	Lane Intra-pair Skew Tolerance			60	ps	Represents the skew (between D+ and D- of the same lane) contribution from the cable in addition to the stressed EYE at TP3.
$t_{RX-SKEW-INTRA\_PAIR\ Reduced-Bit-Rate}$				260	ps	
$f_{RX-TRACKING-BW\_HBR3}$	Jitter Closed-Loop Tracking Bandwidth	15			MHz	Minimum CDR closed-loop tracking bandwidth at the receiver when the input is an 8b/10b pattern, such as a TPS4.
$f_{RX-TRACKING-BW\_HBR2}$		10			MHz	
$f_{RX-TRACKING-BW\_HBR}$		10			MHz	
$f_{RX-TRACKING-BW\_RBR}$		5.4			MHz	

Table 3-45: HBR3 DP Main-Link Receiver TP3_CTLE Parameters

Symbol	Parameter	Min	Nom	Max	Units	Comments
RX TP3_CTLE (RX External Connector after Reference Receiver Equalizer – Normative[a])						
$t_{RX-TJ\_TPS4\_HBR3}$	Minimum Receiver EYE Width	0.38			UI	Measured at $1E^{-6}$ BER using TPS4.[b]
$V_{RX-DIFFp-p\_HBR3}$	RX Differential Peak-to-Peak EYE Voltage	40			mV	
$t_{RX-NonISI\_TPS4\_HBR3}$	Minimum Receiver Non-ISI Jitter			0.38	UI	Measured at $1E^{-6}$ BER.[b]
$t_{TX-RJ\_TPS4\_HBR3}$	Random Jitter Contribution from TX			0.123	UI	Without crosstalk. Measured at $1E^{-6}$ BER.[b]
$t_{RX-DIFFp-p\_RANGE\_HBR3}$	RX Differential Peak-to-Peak EYE Voltage Measurement Range	0.375		0.625	UI	Uses 0.5 CDF of the jitter distribution as the 0UI reference point. RX Differential Peak-to-Peak EYE Voltage mandate can be met anywhere within this UI range.

a. An 80-bit custom pattern is requested for PHY test automation by programming the LINK_QUAL_PATTERN_SELECT register at DPCD Address 00248h to 04h when 8b/10b channel coding is enabled. The TEST_80BIT_CUSTOM_PATTERN register (DPCD Addresses 00250h through 00259h) is used for programming the 80-bit custom pattern. The test mode enables the user to further impair the incoming stressed EYE with the continuous presence of a near-end crosstalk (NEXT) aggressor. The AUX_CH signal differential voltage swing is a downstream device implementation-specific choice. The lower the voltage swing set by the downstream device, the lower the effect of NEXT aggression to the incoming Main-Link signal.

b. Defining the jitter budget at $1E^{-6}$ BER does not mean that the BER target has been modified from $1E^{-9}$ to $1E^{-6}$. Rather, the purpose is to eliminate the impact of TE post-processing RJ estimation error from compliance testing.

Table 3-46: HBR2 DP Main-Link Receiver TP3_EQ Parameters

Symbol	Parameter	Min	Nom	Max	Units	Comments
RX TP3_EQ (RX External Connector after Reference Receiver Equalizer – Normative[a])						
$t_{RX-TJ\_CP2520\_HBR2}$	Minimum Receiver EYE Width	0.38			UI	Measured at $1E^{-9}$ BER using the CP2520 PHY Layer Compliance EYE pattern.
$V_{RX-DIFFp-p\_HBR2}$	RX Differential Peak-to-Peak EYE Voltage	70			mV	
$t_{RX-DIFFp-p\_RANGE\_HBR2}$	RX Differential Peak-to-Peak EYE Voltage Measurement Range	0.375		0.625	UI	Uses 0.5 CDF of the jitter distribution as the 0UI reference point. RX Differential Peak-to-Peak EYE Voltage mandate can be met anywhere within this UI range.

a. *An 80-bit custom pattern is requested for PHY test automation by programming the LINK_QUAL_PATTERN_SELECT register at DPCD Address 00248h to 04h when 8b/10b channel coding is enabled. The TEST_80BIT_CUSTOM_PATTERN register (DPCD Addresses 00250h through 00259h) is used for programming the 80-bit custom pattern. The test mode enables the user to further impair the incoming stressed EYE with the continuous presence of a near-end crosstalk (NEXT) aggressor. The AUX_CH signal differential voltage swing is a downstream device implementation-specific choice. The lower the voltage swing set by the downstream device, the lower the effect of NEXT aggression to the incoming Main-Link signal.*

3.5.4.1 AC-coupling

Each lane of a DP link shall be AC-coupled. The minimum and maximum values for the capacitance are specified in Table 3-38. The mandate for including AC-coupling capacitors is specified at the DPTX.

3.5.4.2 Termination

Care should be taken to minimize emissions and crosstalk from unused lanes. Unused lanes should be parked at an implementation-specific fixed voltage and any active termination be enabled.

3.5.4.3 DC Common Mode Voltage

For the DP Main-Link, transmitter DC common mode voltage shall be held at the same value during transmission. A downstream device shall keep the common mode voltage at the UFP connector pins within the range of 0 to 2.0V while the DPRX is in the ACTIVE or STANDBY power state. (See Section 5.2.5 for downstream device power states.) If the downstream device has AC-coupling capacitors on the Main-Link lanes as illustrated in Main-Link Topology B of Figure 3-52, the downstream device shall pull the Main-Link's UFP connector pins to ground (using 100kΩ to 1MΩ pull-down resistors) to prevent those pins from floating.

The DPTX shall pre-charge the bus to a common mode voltage for 10us or longer before starting the Link Training sequence.

3.5.4.4 Short Circuit Mandates

The driver and receiver circuits of the Main-Link block shall survive the worst-case short-circuit current of 50mA (2.0V over 40Ω).

3.5.4.5 Bandwidth of Transmitter/Receiver PLLs

It is not necessary to forward a reference clock over the DP link. An accurate local time reference (e.g., a local crystal), however, may be used for a downstream (receiving) device. The Training Sequence shall be used to establish the proper clock recovery by the DPRX.

The downstream device clock-recovery PLL shall have a closed-loop bandwidth, as listed in Table 3-47. Compliance to the upstream device jitter specification described in Section 3.5.4.7 is measured at the upstream device connector pins. The measurement shall be done by way of a signal analyzer that has a second-order clock recovery function with a closed-loop tracking bandwidth, as listed in Table 3-47.

Table 3-47: Receiver PLL Clock Recovery Technique

Bit Rate	Downstream Device[a]	Upstream Device[a]	
	Clock-recovery PLL Closed-loop Tracking Bandwidth (MHz)	2nd Order Clock-recovery PLL Closed-loop Tracking Bandwidth (MHz)	Damping Factor
HBR3	> 15	15	1.00
HBR2	> 10	10	1.00
HBR	> 10	10	1.51
RBR	> 5.4	5.4	1.51

a. With respect to the PRBS7 pattern.

3.5.4.6 Down Spreading of Link Clock

Downstream devices shall support down spreading of the link clock. The down-spread amplitude shall either be disabled (0.0%) or up to 0.5%, as written by the upstream device to the DOWNSPREAD_CTRL register (DPCD Address 00107h). The modulation frequency range shall be 30 to 33kHz.

3.5.4.7 DisplayPort Jitter Specifications

This section describes the jitter budget for upstream and downstream devices. For HBR3 and HBR2, jitter specification compliance is measured at the downstream device connector pins after the Reference Receiver Equalizer (TP3_EQ), as described in Section 3.5.4.9. For HBR and RBR, jitter specification compliance is measured at the upstream device connector pins (TP2) and downstream device connector pins (TP3).

Jitter specifications at the transmitter and receiver IC package pins are informative.

The PHY compliance test method is to be defined in a separate PHY compliance test specification.

3.5.4.7.1 Receiver Jitter Tolerance

The DP spectral jitter used for receiver compliance testing shall comply with the mandates described in this section.

3.5.4.7.1.1 HBR3 Receiver Jitter Tolerance

The HBR3 jitter tolerance equations apply after application of the Reference Receiver Equalizer for HBR3 described in Section 3.5.4.9 and with a response not exceeding the response curve illustrated in Figure 3-54.

The HBR3 jitter tolerance is calculated using the following equations:

$$s(f) = 2 \cdot \pi \cdot f \cdot j \qquad \zeta = 1 \qquad BW = 2 \cdot \pi \cdot 1.5 \cdot 10^7$$

$$\omega_n = \frac{BW}{\sqrt{1 + 2\zeta^2 + \sqrt{(1 + 2\zeta^2)^2 + 1}}}$$

$$JTF(f) = \frac{s(f)^2}{s(f)^2 + 2 \cdot s(f) \cdot \zeta \cdot \omega_n + {\omega_n}^2}$$

$$JTHBR3(f) = \frac{SJ_{SWEEP}}{|JTF(f)|} + SJ_{FIXED} + ISI + RJ$$

$$SJ_{SWEEP}(f) = \frac{SJ_{SWEEP}}{|JTF(f)|}$$

where the following values should be used:

- SJ_{SWEEP} = 0.1UI
- SJ_{FIXED} = 0.15UI
- ISI = 0.24UI
- RJ = 0.16UI

The HBR3 TJ is divided into SJ, ISI, and RJ terms. SJ is composed of a fixed tone SJ_{FIXED} placed at 297MHz and a swept tone SJ_{SWEEP} placed between 2 to 100MHz. The relative trade-off between SJ_{SWEEP}, SJ_{FIXED}, ISI, and RJ is determined by the corresponding test within *PHY CTS*, rather than by this Standard.

Note: *Budgeting of the SJ/ISI/RJ terms was determined empirically and not the result of rigorous analysis or derivation.*

Figure 3-54 provides an example of the JTHBR3 curve used for testing the Jitter tolerance at HBR3 of a downstream device (receiver).

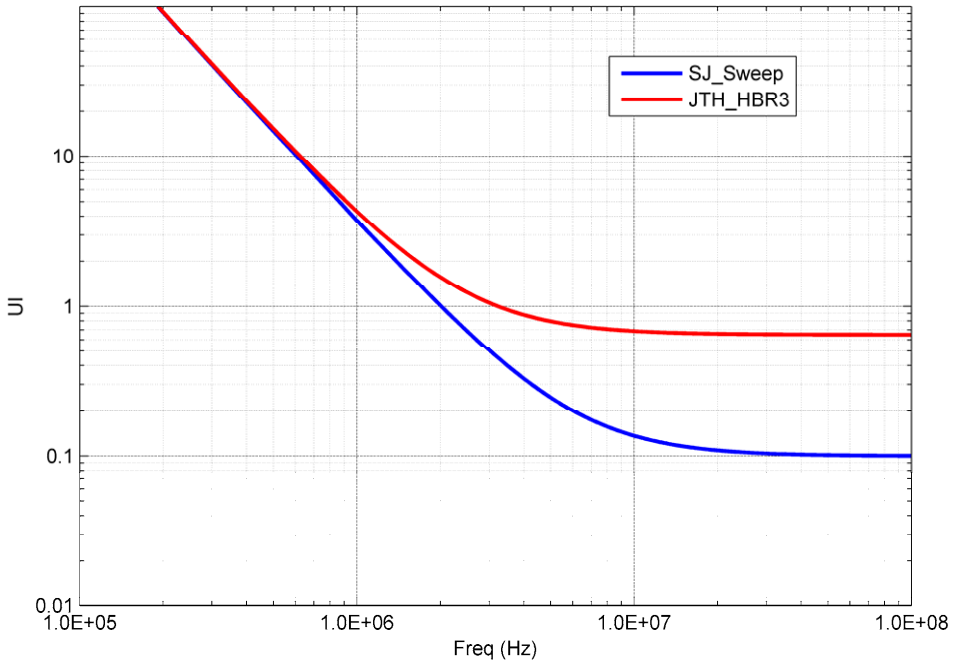


Figure 3-54: HBR3 Receiver Jitter Output/Input Tolerance Mask

3.5.4.7.1.2 HBR2 Receiver Jitter Tolerance

The HBR2 jitter tolerance equations apply after the application of the Reference Receiver Equalizer for HBR2 described in Section 3.5.4.9 and with a response not exceeding the response curve illustrated in Figure 3-63.

The HBR2 jitter tolerance is calculated using the following equations:

$$s(f) = 2 \cdot \pi \cdot f \cdot j \qquad \zeta = 1 \qquad BW = 2 \cdot \pi \cdot 10^7$$

$$\omega_n = \frac{BW}{\sqrt{1 + 2\zeta^2 + \sqrt{\left(1 + 2\zeta^2\right)^2 + 1}}}$$

$$JTF(f) = \frac{s(f)^2}{s(f)^2 + 2 \cdot s(f) \cdot \zeta \cdot \omega_n + \omega_n^2}$$

$$JTHBR2(f) = \frac{SJ_{SWEEP}}{|JTF(f)|} + SJ_{FIXED} + ISI + RJ$$

$$SJ_{SWEEP}(f) = \frac{SJ_{SWEEP}}{|JTF(f)|}$$

where the following values should be used:

- SJ_{SWEEP} = 0.1UI
- SJ_{FIXED} = 0.1UI
- ISI = 0.22UI
- RJ = 12.3 × 16.3mUI

The HBR2 TJ is divided into SJ, ISI, and RJ terms. SJ is composed of a fixed tone SJ_{FIXED} placed above 100MHz and a swept tone SJ_{SWEEP} placed between 0.1 to 100MHz. The relative trade-off between SJ_{SWEEP}, SJ_{FIXED}, ISI, and RJ is determined by the corresponding test within *PHY CTS*, rather than by this Standard.

Note: *Budgeting of the SJ/ISI/RJ terms was determined empirically and not the result of rigorous analysis or derivation.*

Figure 3-55 gives an example of the JTHBR2 curve used for testing the Jitter tolerance at HBR2 of a downstream device (receiver).

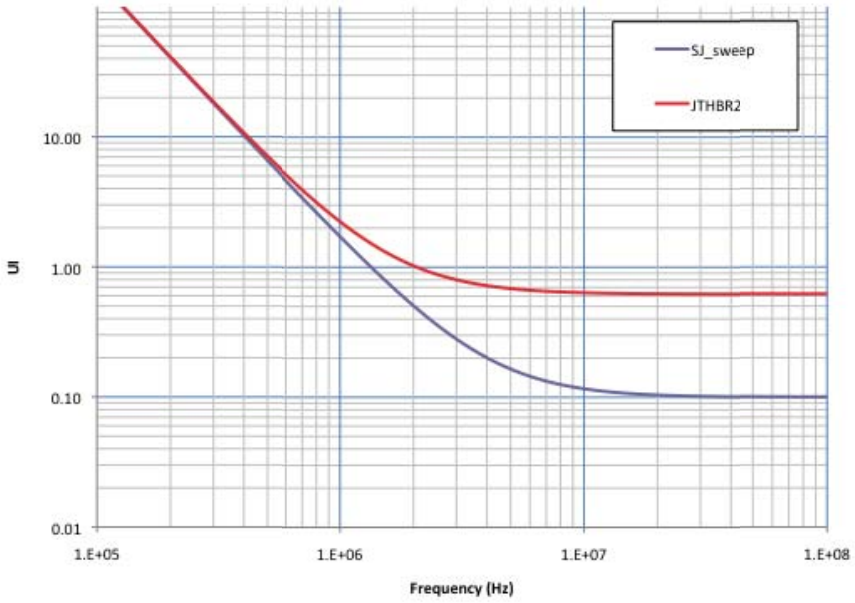


Figure 3-55: HBR2 Receiver Jitter Output/Input Tolerance Mask

3.5.4.7.1.3 HBR Receiver Jitter Tolerance

The HBR mask applies after the application of the Reference Receiver Equalizer for HBR described in Section 3.5.4.9, and with a response not exceeding the response curve illustrated in Figure 3-64. The HBR jitter tolerance mask is calculated as follows:

$$s(f) = 2 \cdot \pi \cdot f \cdot j \qquad \tau_z = 1.656 \cdot 10^{-7} \qquad \tau_{p2} = 6.596 \cdot 10^{-10} \qquad G = 3.421 \cdot 10^{14}$$

$$G_o(f) = \frac{G}{s(f)^2} \cdot \frac{(s(f) \cdot \tau_z + 1)}{(s(f) \cdot \tau_{p2} + 1)} \qquad Hs(f) = \frac{G_o(f)}{1 + G_0(f)}$$

$$JTHBR(f) = \left(\left| \frac{0.2}{1 - Hs(f)} \right| - 0.2 \right) + ISI\_HBR + non\_ISI\_HBR$$

where:

- *ISI_HBR* = 0.161
- *non_ISI_HBR* = 0.330

The ISI_HBR is equal to (TJ – non-ISI). The non-ISI is divided into a frequency-independent term represented by non_ISI_HBR and a frequency-dependent term that reaches an invariant value of 0 at frequencies much greater than the closed-loop bandwidth of the CDR (i.e., frequencies approximately 1.35GHz and greater for HBR).

Note: *Budgeting of the non-ISI was determined empirically and is not the result of a rigorous analysis or derivation.*

At HBR, a compliant downstream device (receiver) jitter tolerance shall be at or above the JTHBR curve illustrated in Figure 3-56.

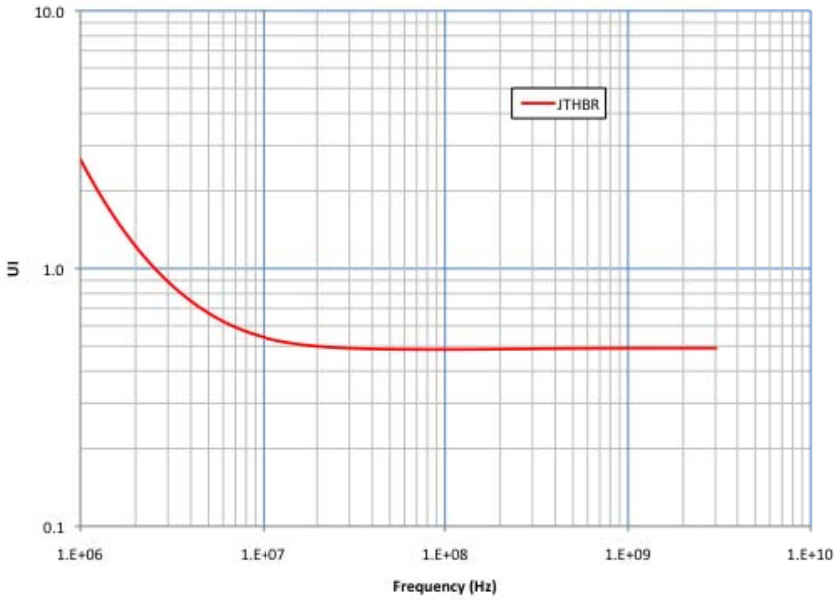


Figure 3-56: HBR Jitter Output/Input Tolerance Mask

3.5.4.7.1.4 RBR Receiver Jitter Tolerance

The Reduced Bit Rate (RBR) jitter tolerance mask is calculated as follows:

$$s(f) = 2 \cdot \pi \cdot f \cdot j \qquad \tau_z = 1.656 \cdot 10^{-7} \qquad \tau_{p2} = 6.596 \cdot 10^{-10} \qquad G = 1.673 \cdot 10^{14}$$

$$G_o(f) = \frac{G}{s(f)^2} \cdot \frac{(s(f) \cdot \tau_z + 1)}{(s(f) \cdot \tau_{p2} + 1)} \qquad Hs(f) = \frac{G_o(f)}{1 + G_0(f)}$$

$$JTRBR(f) = \left| \frac{ISI\_RBR + non\_ISI\_RBR}{1 - Hs(f)} \right|$$

where:

- $ISI\_RBR = 0.570$
- $non\_ISI\_RBR = 0.180$

The ISI_RBR is equal to (TJ – non-ISI). The non-ISI is divided into a frequency-independent term represented by non_ISI_RBR and a frequency-dependent term that reaches an invariant value of 0 at frequencies much greater than the closed-loop bandwidth of the CDR (i.e., frequencies of approximately 810MHz and greater for RBR).

Note: *Budgeting of the non-ISI was determined empirically and is not the result of a rigorous analysis or derivation.*

At RBR, a compliant downstream device (receiver) jitter tolerance shall be at or above the JTRBR curve illustrated in Figure 3-57.

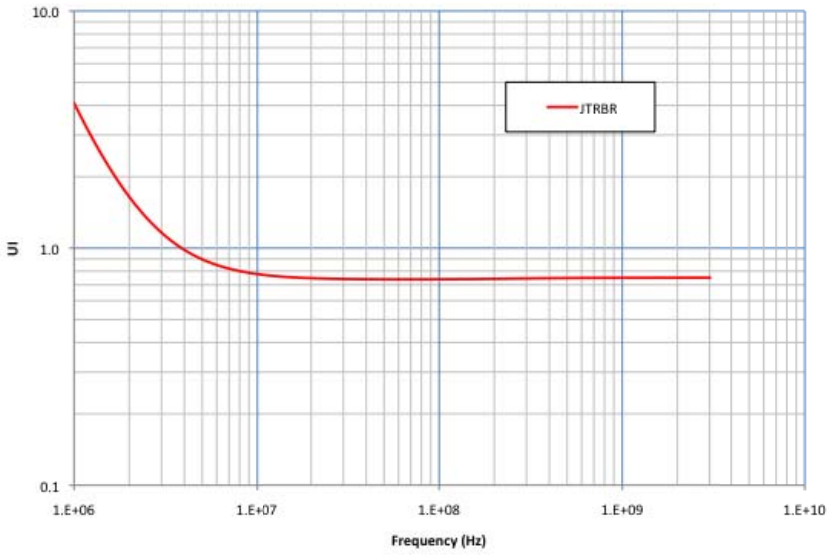


Figure 3-57: RBR Jitter Output/Input Tolerance Mask

3.5.4.7.2 Differential Noise Budget

Jitter specifications relate to the phase relationship between an idealized reference clock and the data. Any phase error that results in the sample being improperly read (i.e., prior bit or following bit sampled) shall result in a bit error. The error components are as follows:

- **HBR3** – Non-ISI jitter and TJ
- **HBR2** – DJ and TJ
- **HBR and RBR** – ISI and non-ISI jitter

The TJ (total jitter) is the total peak-to-peak phase variation in the 0-V differential crossing point of the data stream for a given BER, and is defined as:

$$DJ + (RJ \times \text{scale factor})$$

where the scale factor is determined by the BER and data transition edge density. For HBR3 at 10^{-6} BER, the scale factor is 9.507.

DP interface jitter characteristics shall comply with *PHY CTS* jitter budget allocations.

3.5.4.8 Differential Voltage/Timing (EYE) Diagram

An EYE diagram is used to measure compliance of upstream devices and to calibrate the stressed signal for jitter tolerance testing of downstream devices.

3.5.4.8.1 HBR3/HBR2 EYE Diagrams

HBR3 and HBR2 EYE diagram masks are defined with a variable EYE height placement. The EYE height is measured at the optimal location within a 0.25UI window located at EYE center, 0.375 to 0.625UI, as illustrated in Figure 3-58. The upstream device can select any supported Voltage Swing and Pre-emphasis level combination to achieve an EYE that complies with the following mask limits:

1 EYE diagram width is established at any passing location along 0mV.

2 EYE diagram height (symmetric around 0mV) is established at any passing location between 0.375 to 0.625UI.

Note: *0.5 of the jitter histogram CDF is used as the 0UI reference point.*

3 Perimeter formed around EYE diagram width/height vertices established in steps 1 and 2 to check for violations.

4 Steps 1 through 4 are repeated, as necessary, until a passing configuration is found.

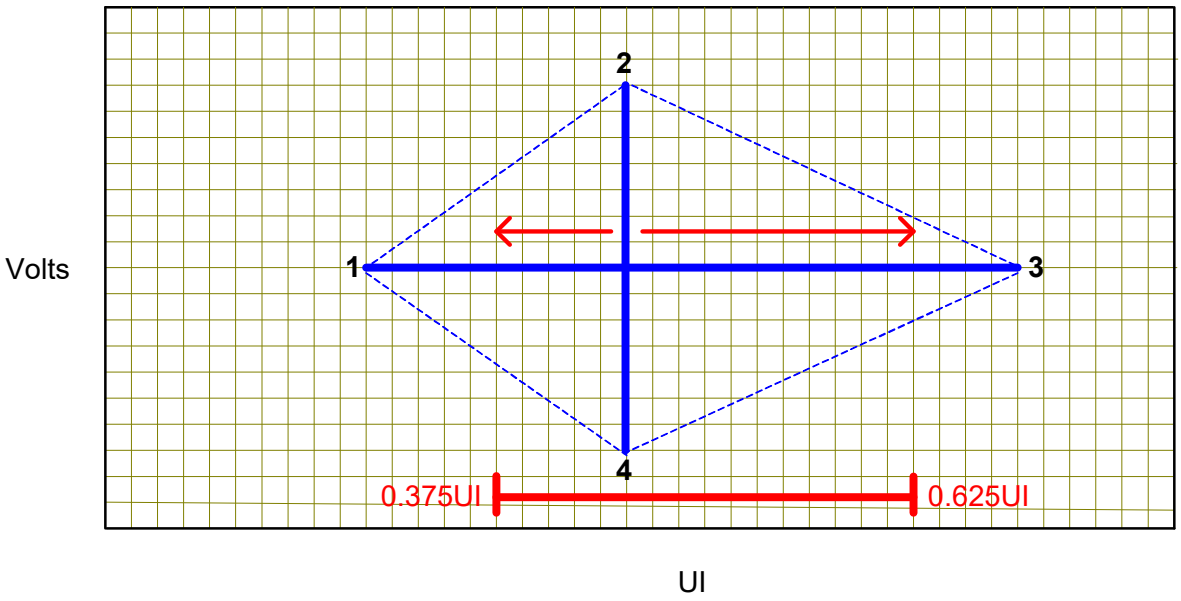


Figure 3-58: HBR3/HBR2 Variable EYE Height Placement

Table 3-41 and Table 3-42 define the HBR3 and HBR2 EYE mask limits, respectively. The measured EYE shall be greater than or equal to the appropriate EYE mask.

The EYE diagram shall be measured at TP3_CTLE for HBR3 and TP3_EQ for HBR2 (with a Compliance Test Load), using a signal analyzer whose Link CDR emulation function:

- Meets the mandates specified in Section 3.5.4.5
- Matches the DPRX Jitter Output/Input Tolerance Mask specifications defined in Section 3.5.4.7.1.1 (HBR3) and Section 3.5.4.7.1.2 (HBR2), within ±10% accuracy

All Main-Link lanes shall be on and driving TPS4 for HBR3 and CP2520 for HBR2 with a two-symbol (20UI) skew between each lane and adjacent lane(s). At least one combination of differential voltage swing and pre-emphasis shall result in an EYE that meets the TP3_EQ EYE mask specification. This measurement is to be performed using HBR3 CTLE (normative) and DFE (informative) for the upstream device EYE opening test at HBR3 and HBR2 CTLE at HBR2. The same differential voltage swing and pre-emphasis shall be used for all Main-Link lanes, unless per-lane settings (**optional**) are supported.

Those upstream devices that support down spreading of the link clock shall produce a compliant EYE, both with and without down spread enabled.

This EYE Mask is used for testing the jitter tolerance of downstream device. A test pattern generator, while transmitting TPS4 for HBR3 and CP2520 for HBR2, shall be adjusted to achieve the minimum EYE, after traveling through the appropriate (TP1-TP3) channel and application of the appropriate Reference Receiver Equalizer, as defined in Section 3.5.4.9.

After the test pattern generator (or the stressed signal generator) is adjusted, the bitstream shall be transmitted to the downstream device's TP3 connector pins. With this input, the downstream device shall achieve the target BER or better.

For a downstream device with a permanently tethered cable, the test pattern generator is adjusted to provide a signal equal to the required EYE mask without passing through a compliance test cable model. *PHY CTS* details the calibration process for all bit rates.

3.5.4.8.2 HBR/RBR EYE Diagrams

HBR and RBR use pre-defined polygons for the EYE diagram. The polygon in Figure 3-59 represents the upstream device EYE mask at the upstream device connector pins (TP2) for HBR and RBR. Table 3-48 and Table 3-49 define the values to be used for the upstream device mask's HBR and RBR vertices, respectively.

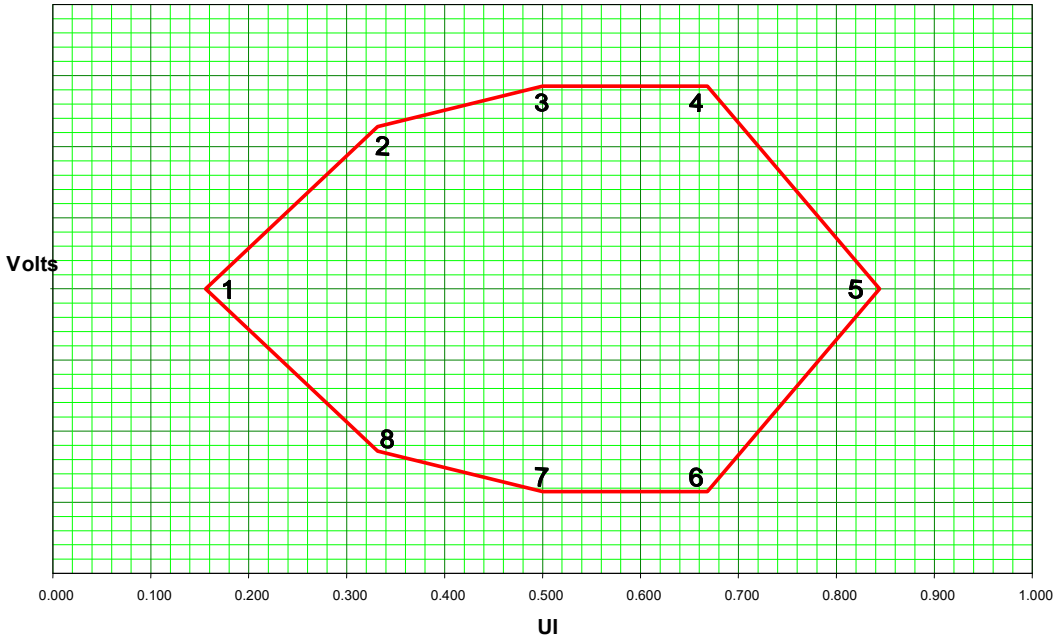


Figure 3-59: HBR/RBR EYE Mask at Upstream Device DFP Connector Pins

Table 3-48: HBR Upstream Device DFP Time and Voltage Values at TP2 EYE Mask Vertices

Point	Time (UI)	Voltage (V)
1	0.210	0.000
2	0.355	0.140
3	0.500	0.175
4	0.645	0.175
5	0.790	0.000
6	0.645	-0.175
7	0.500	-0.175
8	0.355	-0.140

Table 3-49: RBR Upstream Device DFP Time and Voltage Values at TP2 EYE Mask Vertices

Point	Time (UI)	Voltage (V)
1	0.127	0.000
2	0.291	0.160
3	0.500	0.200
4	0.709	0.200
5	0.873	0.000
6	0.709	-0.200
7	0.500	-0.200
8	0.291	-0.160

The measured EYE shall be greater than or equal to the appropriate EYE mask.

The EYE diagram shall be measured at TP2 for HBR and RBR, using a signal analyzer whose Link CDR emulation function:

- Meets the mandates specified in Section 3.5.4.5
- Matches the DPRX Jitter Output/Input Tolerance Mask specifications defined in Section 3.5.4.7.1.3 (HBR) and Section 3.5.4.7.1.4 (RBR), within ±10% accuracy

All Main-Link lanes shall be on and driving the PRBS7 test pattern with a two-symbol (20UI) skew between each lane and adjacent lane(s). The differential Voltage Swing shall be programmed to Level 2 and Pre-emphasis programmed to Level 0 to meet the TP2 EYE mask specification. This measurement is to be performed using a signal analyzer that embeds a worst-case (TP2-TP3) HBR cable model with the insertion loss profile defined in Section 4.1.5.1.1.

Upstream devices that support down spreading of the link clock shall produce a compliant EYE, both with and without down spread enabled.

The polygon in Figure 3-60 represents the minimum entry UFP EYE mask into the downstream device at TP3_EQ for HBR and at TP3 for RBR. Table 3-50 and Table 3-51 define the values to be used for the vertices of the downstream device UFP EYE mask for HBR and RBR, respectively.

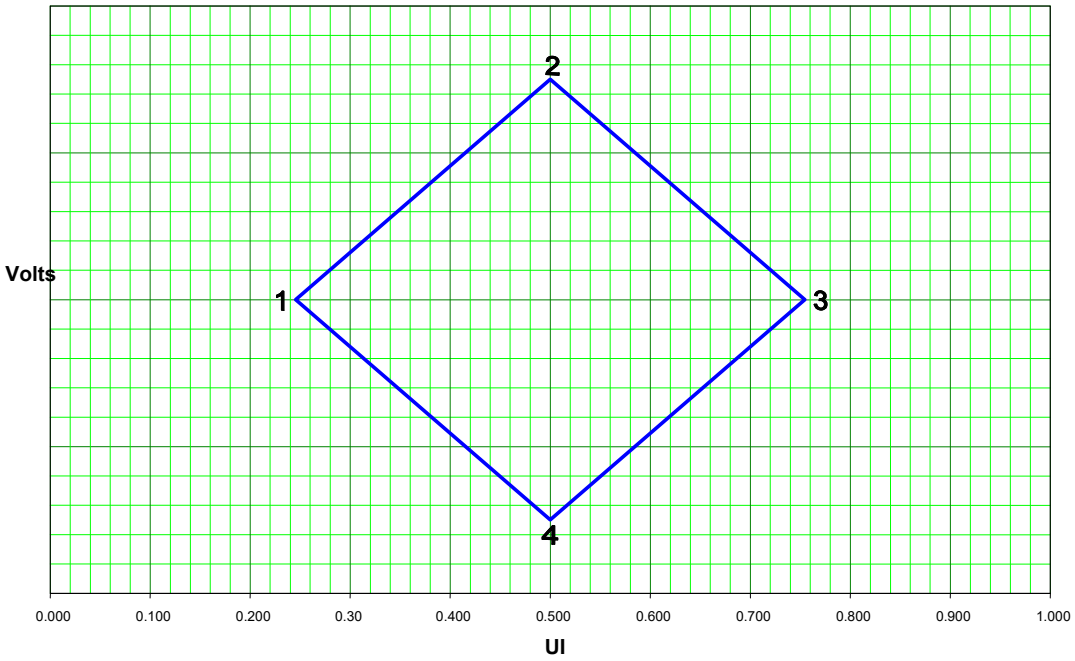


Figure 3-60: Downstream Device UFP EYE Mask at TP3_EQ (HBR) or TP3 (RBR)

Table 3-50: HBR Downstream Device UFP Time and Voltage Values at TP3_EQ EYE Mask Vertices

Point	Time (UI)	Voltage (V)
1	0.246	0.000
2	0.500	0.075
3	0.755	0.000
4	0.500	-0.075

Table 3-51: RBR Downstream Device UFP Time and Voltage Values at TP3 EYE Mask Vertices

Point	Time (UI)	Voltage (V)
1	0.375	0.000
2	0.500	0.023
3	0.625	0.000
4	0.500	-0.023

This EYE Mask is used for testing the jitter tolerance of downstream device. A test pattern generator, while transmitting the PRBS7 bitstream, shall be adjusted to achieve the minimum EYE, after traveling through the appropriate (TP1-TP3) channel and application of the appropriate Reference Receiver Equalizer for , as defined in Section 3.5.4.9.

After the test pattern generator (or the stressed signal generator) is adjusted, the bitstream shall be transmitted to the downstream device's TP3 connector pins. With this input, the downstream device shall achieve a BER of $1E^{-9}$ or better.

For a downstream device with a permanently tethered cable, the BER specification shall be met with an input EYE to the plug connector that is equal to the TP2 EYE mask for RBR. For HBR, the test pattern generator is adjusted to provide a signal equal to the TP3_EQ EYE mask after passing through a compliance test cable model based on the electrical parameters for cable Type E1. The permanently tethered HBR downstream device is then tested by removing the compliance test cable model from the calibrated test setup and replacing it with the tethered downstream device.

3.5.4.9 Reference Receiver Equalizers

The HBR3, HBR2, and HBR EYE diagrams are defined after application of a corresponding Reference Receiver Equalizer with a response curve, as defined below. The Reference Receiver Equalizer's primary function is to open the EYE for compliance measurements and does not define the Downstream Device Reference Receiver Equalizer implementation. A downstream device that implements RX EQ similar to the Reference Receiver Equalizer is not guaranteed to pass downstream device compliance tests.

Note: *The application of an equalizer with a response curve at the receiver may degrade the receive EYE in some configurations. An equalizer should be designed to adapt to the received signal during link training with a maximum response granularity of 2dB at data rate frequencies.*

3.5.4.9.1 Reference Receiver Equalizer for HBR3

The Reference Receiver Equalizer for HBR3 is modeled as a first-order Reference Receiver Continuous Time Linear Equalizer (Reference Receiver CTLE) that is cascaded with a one-tap Reference Receiver Decision Feedback Equalizer (Reference Receiver DFE).

The Reference Receiver Equalizer's primary function is to open the EYE for compliance measurements, and does **not** define the Downstream Device Reference Receiver Equalizer implementation. A downstream device that implements RX EQ similar to the Reference Receiver Equalizer is **not** guaranteed to pass Downstream Device Compliance tests.

The Reference Receiver CTLE for HBR3 uses the following equation:

$$H(s) = A_{ac} \times \omega_{p2} \times [s + (A_{dc} / A_{ac}) \times \omega_{p1}] / (s + \omega_{p1}) \times (s + \omega_{p2})$$

where:

- A_{ac} = 3.5dB
- A_{dc} = Integer within the range of 0 through -9dB, inclusive
- ω_{p1} = 3.03GHz
- ω_{p2} = 5.60GHz

Figure 3-61 illustrates the Reference Receiver CTLE for HBR3 curves.

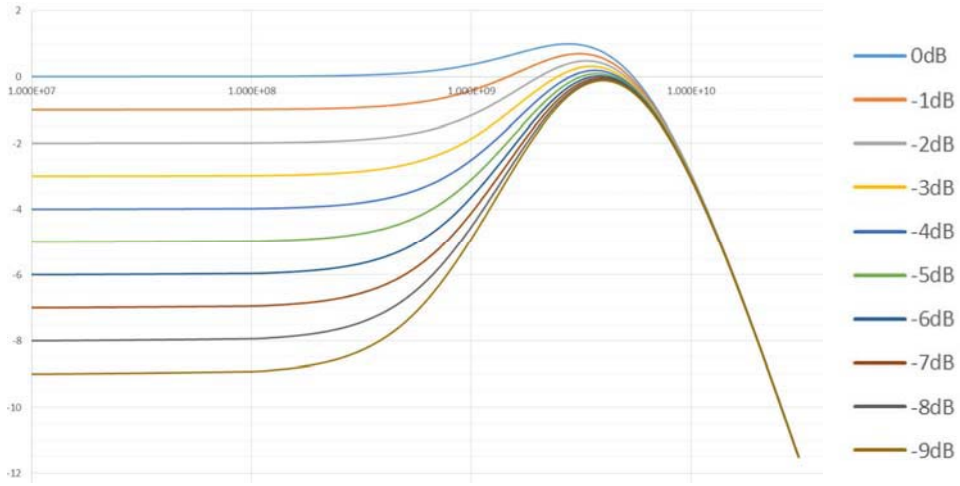


Figure 3-61: Reference Receiver CTLE for TP3_CTLE and TP2_CTLE Test Point for HBR3 Curves

3.5.4.9.2 Reference Receiver DFE for HBR3

The Reference Receiver Equalizer for HBR3 includes a Reference Receiver CTLE cascaded with a one-tap adaptive Reference Receiver DFE with a feedback coefficient limited to < 50mV. The Reference Receiver DFE behavior is described below.

$$y_k = x_k - d1\ sgn\ (y_{k-1})$$

where:

- y_k = Reference Receiver DFE differential output voltage.
- y_k^* = Decision function output voltage.
- x_k = Differential input voltage after Reference Receiver CTLE.
- $d1$ = Feedback coefficient.
- k = UI sample.

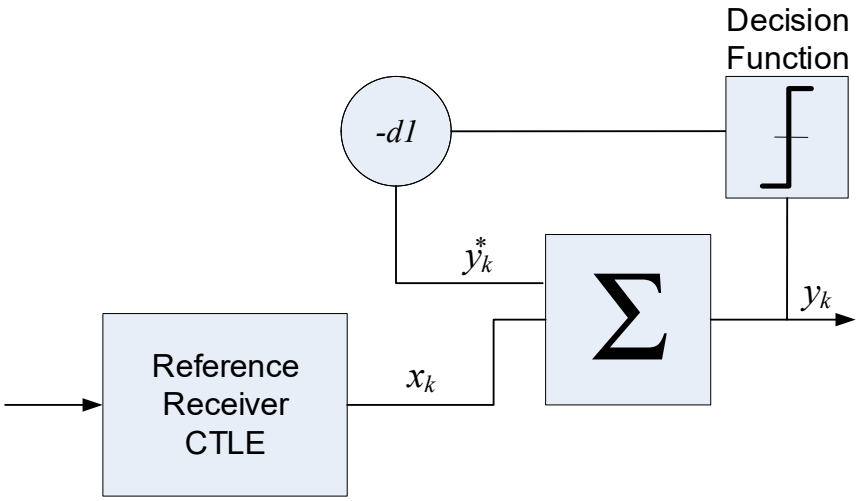


Figure 3-62: Reference Receiver Equalizer for HBR3 with Reference Receiver DFE

3.5.4.9.3 Reference Receiver Equalizer for HBR2

The Reference Receiver Equalizer for HBR2 is modeled as a Reference Receiver CTLE with a 0 at 640MHz and poles at 2.7GHz, 4.5GHz, and 13.5GHz, as illustrated in Figure 3-63.

The Reference Receiver Equalizer's primary function is to open the EYE for compliance measurements and does not define the Downstream Device Reference Receiver Equalizer implementation. A downstream device that implements RX EQ similar to the Reference Receiver Equalizer is not guaranteed to pass Downstream Device Compliance tests.

The Reference Receiver Equalizer for HBR2 transfer function is given by:

$$H(s) = \frac{\omega_{p1}\omega_{p2}\omega_{p3}}{\omega_z} \cdot \frac{s+\omega_z}{(s+\omega_{p1})(s+\omega_{p2})(s+\omega_{p3})}$$

which has magnitude given by:

$$|H(j\omega)| = \frac{\omega_{p1}\omega_{p2}\omega_{p3}}{\omega_z} \cdot \frac{\sqrt{\omega^2+\omega_z^2}}{\sqrt{\omega^2+\omega_{p1}^2} \cdot \sqrt{\omega^2+\omega_{p2}^2} \cdot \sqrt{\omega^2+\omega_{p3}^2}}$$

where:

- $\omega_z = 2\pi\ (0.64 \times 10^9)$ for upstream device compliance
- $\omega_{p1} = 2\pi\ (2.7 \times 10^9)$
- $\omega_{p2} = 2\pi\ (4.5 \times 10^9)$
- $\omega_{p3} = 2\pi\ (13.5 \times 10^9)$

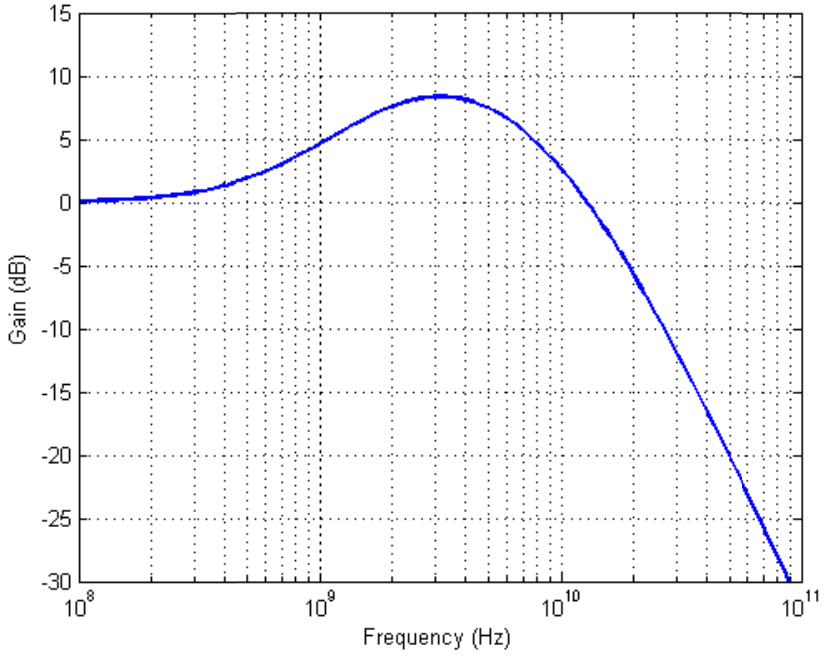


Figure 3-63: Reference Receiver Equalizer for HBR2 Transfer Function

3.5.4.9.4 Reference Receiver Equalizer for HBR

The Reference Receiver Equalizer for HBR is modeled as a Reference Receiver CTLE with a 0 at 725MHz and poles at 1.35GHz and 2.5GHz, as illustrated in Figure 3-64.

The Reference Receiver Equalizer for HBR transfer function is given by:

$$H(s) = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{s + \omega_z}{(s + \omega_{p1})(s + \omega_{p2})}$$

which has magnitude given by:

$$|H(j\omega)| = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{\sqrt{\omega^2 + \omega_z^2}}{\sqrt{\omega^2 + \omega_{p1}^2} \cdot \sqrt{\omega^2 + \omega_{p2}^2}}$$

where:

- $\omega_z = 2\pi\ (0.725 \times 10^9)$
- $\omega_{p1} = 2\pi\ (1.35 \times 10^9)$
- $\omega_{p2} = 2\pi\ (2.5 \times 10^9)$

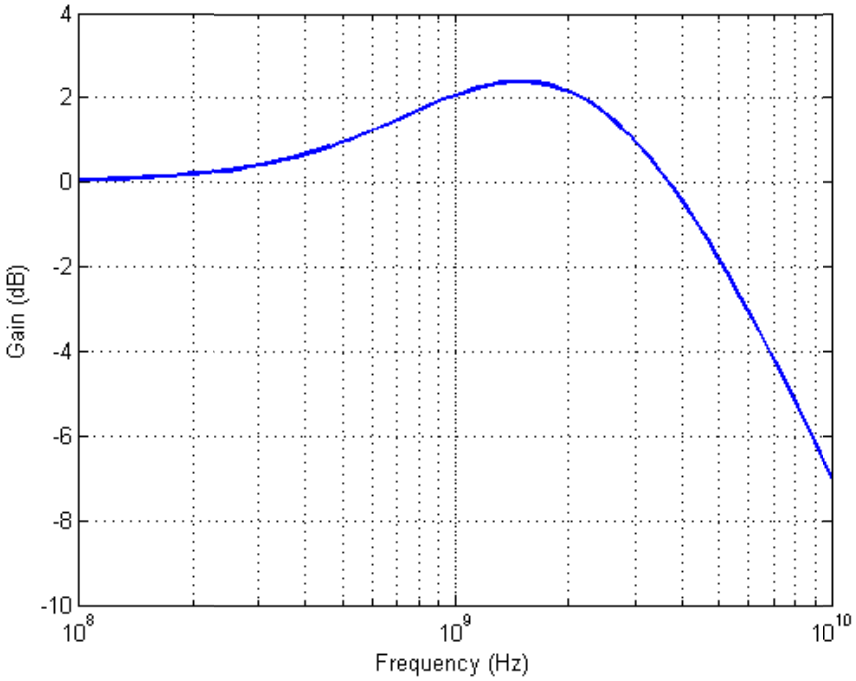


Figure 3-64: Reference Receiver Equalizer for HBR Transfer Function

3.5.4.9.5 Enhanced Reference Receiver Equalizer for HBR

The insertion loss of the HBR cable specification at the Nyquist frequency of HBR (= 1.35GHz) is approximately 70% of that of HBR2 (= 2.7GHz). Given this, it makes a logical sense to have an Reference Receiver CTLE for HBR whose peak gain at 1.35GHz is 6dB, which is approximately 70% of the HBR2 CTLE peak gain at 2.7GHz, instead of 2.4dB as defined in Section 3.5.4.9.4. This section defines the Enhanced Reference Receiver CTLE for HBR that is proportional to that of HBR2.

For new DPRX designs, the Enhanced Reference Receiver CTLE for HBR should be used.

The Enhanced Reference Receiver CTLE for HBR transfer function is given by:

$$H(s) = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \times \frac{s + \omega_z}{(s + \omega_{p1})(s + \omega_{p2})}$$

which has magnitude given by:

$$|H(j\omega)| = \frac{\omega_{p1}\omega_{p2}}{\omega} \times \frac{\sqrt{\omega^2 + \omega_z^2}}{\sqrt{\omega^2 + \omega_{p1}^2}\sqrt{\omega^2 + \omega_{p2}^2}}$$

where:

- $\omega_z = 2\pi\ (0.38 \times 10^9)$
- $\omega_{p1} = 2\pi\ (1.15 \times 10^9)$
- $\omega_{p2} = 2\pi\ (2.0 \times 10^9)$

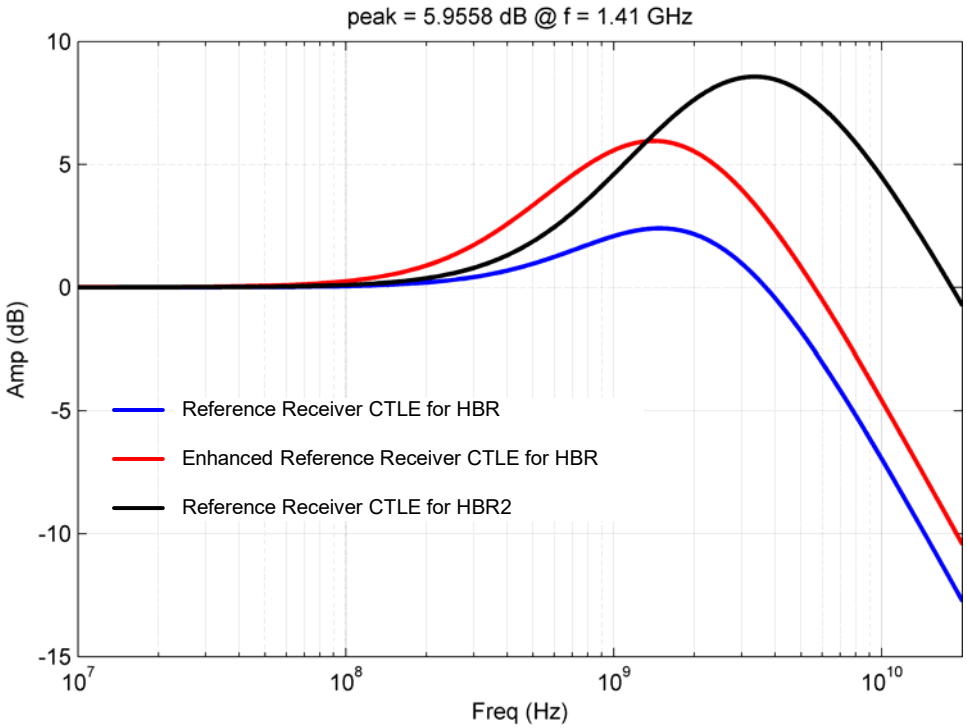


Figure 3-65: Enhanced Reference Receiver CTLE for HBR Relative to Reference Receiver CTLE for HBR and HBR2

3.5.4.10 Embedded Connection (Informative)

See *eDP Standard*, *Section 4*, for applicable electrical specifications. While there is no required formal industry compliance test for the eDP connection compliance to the electrical performance described in *eDP Standard* helps ensure embedded Source and Sink devices shall interoperate.

3.5.5 128b/132b Main-Link PHY Electrical Sub-block

New to *DP v2.0*.

This section introduces three new data rates – Ultra-high Bit Rate (UHBR) at 10, 13.5, and 20Gbps/lane (UHBR10, UHBR13.5, and UHBR20, respectively). Migration to bit rates that are higher than HBR3 required several key innovations:

- System-related loss must be more tightly controlled
- Additional equalization is necessary to overcome remaining system-related losses
- Certain rates or systems may require active cabling

This section breaks out the notable changes, in detail.

3.5.5.1 UHBR Connectivity

The UHBR10 PHY Electrical Specification is defined so that UHBR10-capable devices interoperate when connected using a detachable DP8K cable or USB SuperSpeed Gen 1-only Type-C cable (see Figure 3-66), as well as a DPRX with a tethered USB Type-C plug cable (see Figure 3-67). UHBR10-capable devices may use DP, mDP, or USB Type-C connectors.

UHBR13.5- and UHBR20-capable devices are currently specified to use only a DPRX with a tethered USB Type-C plug cable (see Figure 3-67).

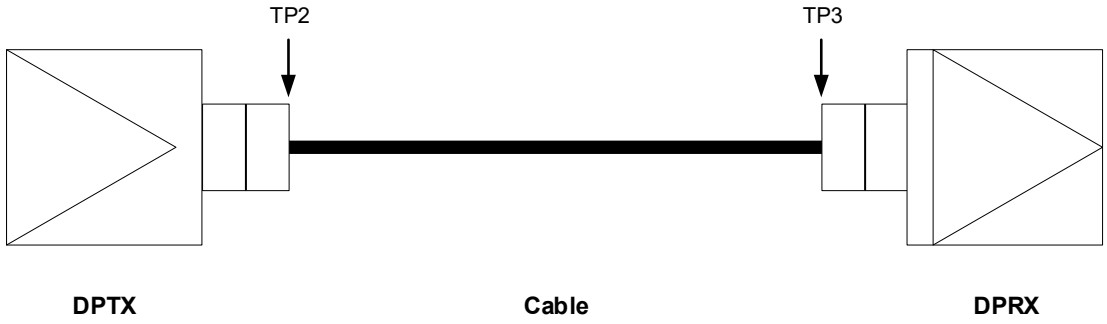


Figure 3-66: DPTX and DPRX Connected by way of a Detachable Cable

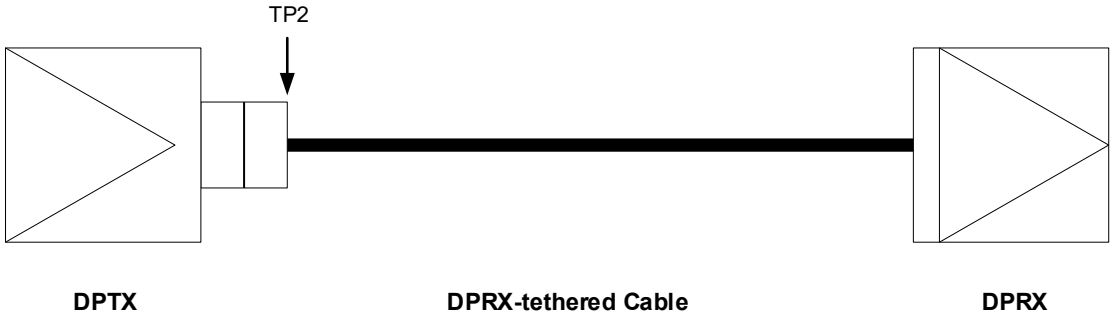


Figure 3-67: DPRX with a Tethered USB Type-C Plug Cable

3.5.5.2 DP Main-Link UHBR System Parameters

Table 3-52 defines the UHBR-related system parameters that are common to DPTXs and DPRXs.

Table 3-52: Common DP Main-Link UHBR Electrical System Parameters

Symbol	Parameter	Min	Nom	Max	Units	Conditions
B_{UHBR10}	UHBR10 Bit Rate	9.94700	10	10.00300	Gbps	Frequency high limit = +300ppm. Frequency low limit = -5300ppm.
$B_{UHBR13.5}$	UHBR13.5 Bit Rate	13.42845	13.5	13.50405	Gbps	
B_{UHBR20}	UHBR20 Bit Rate	19.89400	20	20.00600	Gbps	
UI_UHBR10	UHBR10 Unit Interval		100		ps	Informative (approximate values).
UI_UHBR13.5	UHBR13.5 Unit Interval		74		ps	
UI_UHBR20	UHBR20 Unit Interval		50		ps	
SSC_DOWN_SPREAD_RANGE	SSC Dynamic Range Down Spreading during Steady State	0.4		0.5	%	See Note 1 and Figure 3-68.
SSC_DOWN_SPREAD_RATE	SSC Down Spreading Modulation Rate during Steady State	30		33	KHz	See Figure 3-68.
SSC_PHASE_DEVIATION	Phase Jitter Associated with the SSC modulation during Steady State	2.5		22	ns pp	See Note 2 and Figure 3-68.
SSC_SLEW_RATE	SSC Frequency Slew Rate (df/dt) during Steady State			1250	ppm/us	See Note 3 and Figure 3-68.

Notes:

1 *SSC_DOWN_SPREAD_RANGE specifies the mandated SSC modulation depth, represented by the difference of the minimum and maximum modulated frequencies, referenced to the link speed.*

2 *SSC phase deviation shall be extracted from the transmitted signal. During this test, the transmitter shall be configured to send the PRBS31 pattern. The SSC phase deviation shall be measured after applying a 2^{nd} order low-pass filter with 3-dB point at 5MHz.*

3 *The SSC slew rate shall be extracted from the transmitted signal over measurement intervals of 0.5us. The SSC slew rate shall be extracted from the signal phase after applying a 2^{nd} order low-pass filter with 3-dB point at 5MHz.*

4 *See Table 3-28 for the inter-lane skew normative specification.*

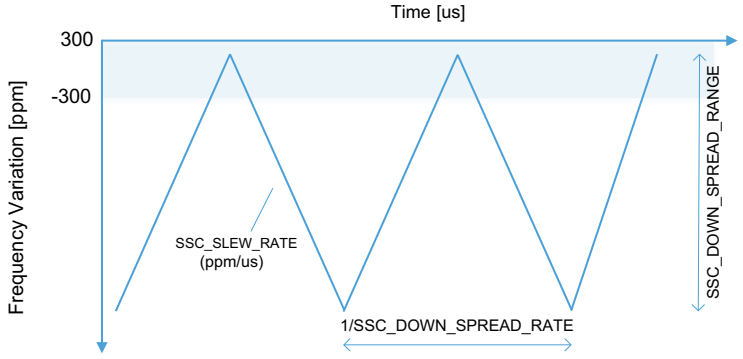


Figure 3-68: UHBR SSC Parameters

3.5.5.3 Transmitter Equalization and Presets

This section describes transmitter equalization presets that are common to all three UHBR bit rates.

A UHBR-capable DPTX shall implement a 3-tap equalization. The DPTX applies transmitter coefficients, as illustrated in Figure 3-69. Individual coefficients may be positive or negative values. C_0 may be $0 < C_0 < 1$. C_{-1} and C_{+1} shall be 0 or a negative value.

A DPTX that is capable of up to HBR3 (or lower bit rates) may implement a 2-tap Feed Forward Equalization (FFE) implementation. Table 3-53 defines the equalization values. The DPTX may implement a 3-tap equalization as is used for UHBR bit rates; however, if doing so the coefficient C_{-1} value shall be 0. Implementers that use a 3-tap equalization should note that the coefficients, as specified, create de-emphasis and the voltage swing level would need to be increased to be equivalent to the pre-emphasis defined in Section 3.5.4.

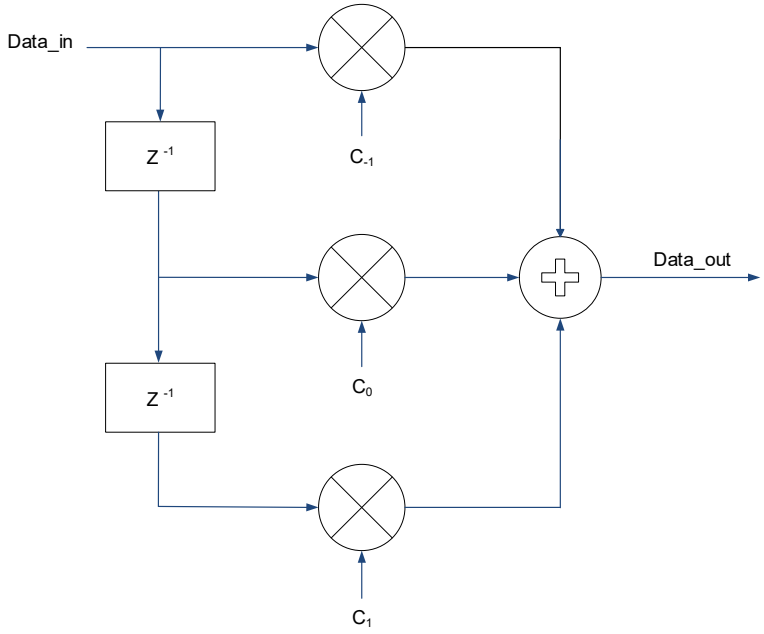


Figure 3-69: 3-tap FFE Example

where:

- Z^{-1} = Delay element, 1-unit interval
- C_i = Transmitter FFE (FIR) equalization coefficients; index *i* is the location relative to the main cursor (preshoot, cursor, or post cursor)

$$Preshoot = 20 \times log_{10} \times \frac{-C_{-1} + C_0 + C_1}{C_{-1} + C_0 + C_1}$$

$$De\text{-}emphasis = 20 \times log_{10} \times \frac{C_{-1} + C_0 + C_1}{C_{-1} + C_0 - C_1}$$

Figure 3-70: FFE Coefficients

Table 3-53: Preset FFE Coefficients[a] [b]

Preset #	Pre-shoot (dB)	De-emphasis (dB)	Informative Filter Coefficients		
			C_{-1}	C_0	C_{+1}
0	0	0	0	1	0
1	0	-1.9	0	0.90	-0.10
2	0	-3.6	0	0.83	-0.17
3	0	-5.0	0	0.78	-0.22
4	0	-8.4	0	0.69	-0.31
5	0.9	0	-0.05	0.95	0
6	1.1	-1.9	-0.05	0.86	-0.09
7	1.4	-3.8	-0.05	0.79	-0.16
8	1.7	-5.8	-0.05	0.73	-0.22
9	2.1	-8.0	-0.05	0.68	-0.27
10	1.7	0	-0.09	0.91	0
11	2.2	-2.2	-0.09	0.82	-0.09
12	2.5	-3.6	-0.09	0.77	-0.14
13	3.4	-6.7	-0.09	0.69	-0.22
14	3.8	-3.8	-0.13	0.74	-0.13
15	1.7	-1.7	-0.05	0.55	-0.05

a. The coefficients are normalized such that $|C_{-1}| + C_0 + |C_1|$ corresponds to full output swing that is 800mV_diff_pp nominal. Preset configuration 15 represents operation mode that has a lower transmitter swing.

b. See Figure 3-70 for how preshoot and de-emphasis are calculated.

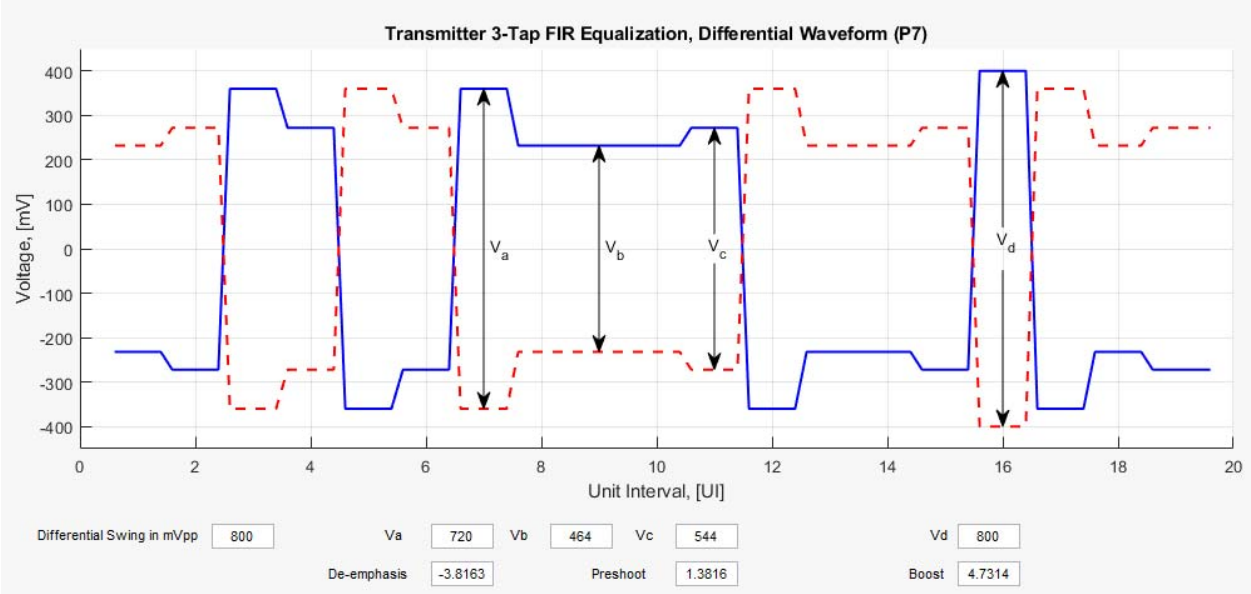


Figure 3-71: 3-tap FFE Example Waveform (for Preset #7 of Table 3-53)

where:

- $V_a = -C_{-1} + C_0 + C_1$
- $V_b = C_{-1} + C_0 + C_1$
- $V_c = C_{-1} + C_0 - C_1$
- $V_d = -C_{-1} + C_0 - C_1 = 1$ by definition

3.5.5.4 Reference Receiver CDR

All measurements are performed after the effects of a Reference Receiver CDR. The CDR can be modeled by a 2nd order PLL response that derives the following jitter transfer function, described in the Laplace domain, as follows:

$$H_{jitter}(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

where:

- s = Frequency in the Laplace domain
- ζ = Damping factor, 0.94
- ω_n = System's natural frequency, 2.2E7rad/sec

The observed jitter transfer function (OJTF) shall be as illustrated in Figure 3-72.

Note: *In contrast to the OJTF for UHBRx Reference Receiver CDRs, which is a high-pass filter, the Reference Receiver CDRs for bit rates up to HBR3 are defined as jitter tracking function (JTF), which is a low-pass filter.*

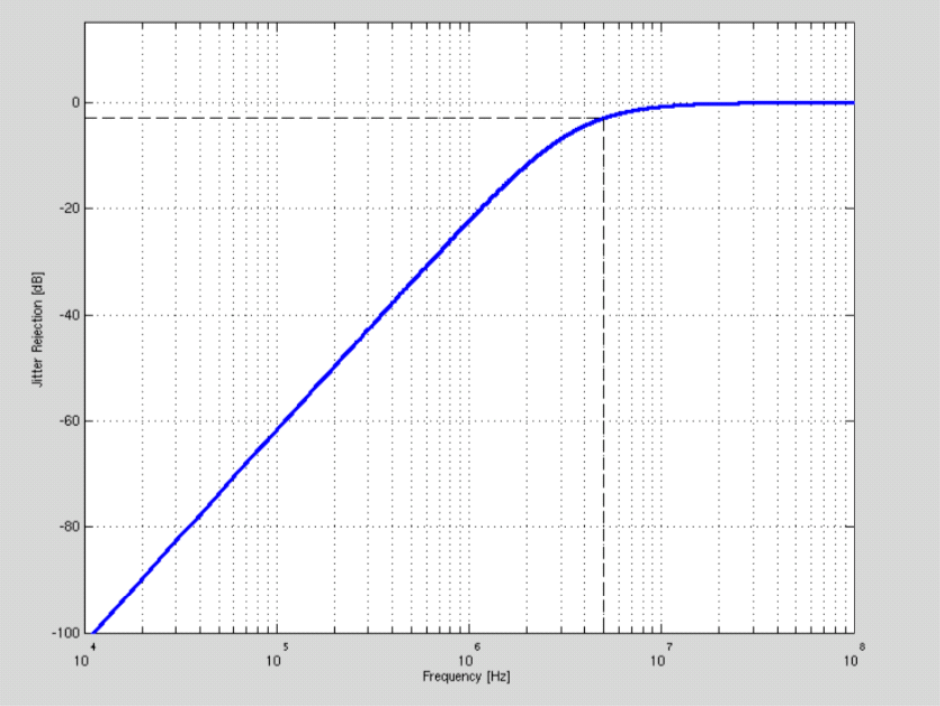


Figure 3-72: UHBR*x* Reference Receiver CDR OJTF

3.5.5.5 RL Specification

This section defines the Return Loss (RL) specifications for UHBR-capable DPTXs and DPRXs.

3.5.5.5.1 RL for DPTXs and DPRXs with a USB Type-C Connector (Normative)

A UHBR-capable DPTX or DPRX with a USB Type-C connector shall meet the RL specifications listed below. RL specifications are defined with mated connectors, namely, TP2 on the DPTX and TP3' on the DPRX.

Differential RL

$$\text{SDD11}(f) \begin{cases} -8.5 & 0.05 < f_{GHz} \leq 3 \\ -3.5 + 8.3 \times \log_{10}\left(\frac{f_{GHz}}{12}\right) & 3 < f_{GHz} \leq 12 \end{cases}$$

Common Mode RL

$$\text{SCC11}(f) \begin{cases} -6 & 0.05 < f_{GHz} \leq 2.5 \\ -3 & 2.5 < f_{GHz} \leq 12 \end{cases}$$

3.5.5.5.2 RL for DPTXs and DPRXs with a DP Connector (Informative)

A UHBR-capable DPTX or DPRX with a DP connector shall meet the RL specifications listed below.

Differential RL

$$\text{SDD11}(f) \begin{cases} -6.5 & 0.05 < f_{GHz} \leq 3 \\ -1.5 + 8.3 \times \log_{10}\left(\frac{f_{GHz}}{12}\right) & 3 < f_{GHz} \leq 12 \end{cases}$$

Common Mode RL

$$\text{SCC11}(f) \begin{cases} -6 & 0.05 < f_{GHz} \leq 2.5 \\ -3 & 2.5 < f_{GHz} \leq 12 \end{cases}$$

3.5.5.6 UHBR10

This section covers assumptions that are related to UHBR10 loss budget, cable interoperability matrix, Reference Receiver CTLE + Reference Receiver DFE, and EYE masks that are used for PHY Layer compliance testing. All UHBR-capable devices shall support the UHBR10 bit rate.

3.5.5.6.1 UHBR10 Topology

UHBR10 is expected to function over existing DP and USB Type-C infrastructure. As such, additional losses that are incurred by operating at higher bit rates shall be absorbed or overcome by the remaining system components. Currently, it is expected that connections made by way of USB Type-C connectors and cables will have lower overall system-related loss than DP8K cables.

Table 3-54 defines the UHBR10 bit rate insertion loss budgets.

Table 3-54: UHBR10 Cable Interoperability Matrix (Informative)

Cable Type	Connector		DPTX IL to TP2[a]	Cable[a]	DPRX IL to TP3[a]	Units
	DPTX End	DPRX End				
DP8K[b]	DP	DP	-7.2	-13.3	-4.5	dB
	DP	USB Type-C	-7.2	-13.3	-4.5	dB
	USB Type-C	DP	-5.5	-13.3	-4.5	dB
USB Type-C Gen 1-only[c]	USB Type-C	USB Type-C	-5.5	-12	-4.5	dB
USB Type-C Gen 2[d]	USB Type-C	USB Type-C	-5.5	-6	-4.5	dB

a. Loss values specified are ILFit at 5GHz.
b. DP8K cables are available with both standard DP connectors as well as USB Type-C connectors. Both cables have similar electrical performance, regardless of connector type.
c. USB Type-C Gen 1 cables are capable of supporting USB SuperSpeed Gen 1 at 5Gbps (see USB Type-C Specification).
d. USB Type-C Gen 1 cables are capable of supporting USB SuperSpeed Gen 1 at 10Gbps (see USB Type-C Specification).

3.5.5.6.2 Reference Receiver CTLE + Reference Receiver DFE for UHBR10 (Normative)

Designers may choose to implement a second-order CTLE and/or additional peak if it is deemed more effective than the Reference Receiver CTLE for UHBR10.

The Reference Receiver CTLE for UHBR10 is defined by the following equation.

$$H(s) = 1.496 \times \omega_{p2} \times \frac{\left(s + \frac{A_{DC}}{1.496} \times \omega_{p1}\right)}{(s + \omega_{p1}) \times (s + \omega_{p2})}$$

Note: *Equation is subject to change, pending analysis.*

where:

- $A_{AC} = 3.5\text{dB}$
- $A_{DC} = \left\{10^{\frac{-x}{20}}: x = 0, 1, 2, , , 9[dB]\right\}$
- $\omega_{p1} = 2\pi \times 1E9 \frac{rad}{sec}$
- $\omega_{p2} = 2\pi \times 8E9 \frac{rad}{sec}$

Figure 3-73 illustrates the normative Reference Receiver CTLE for UHBR10 curves.

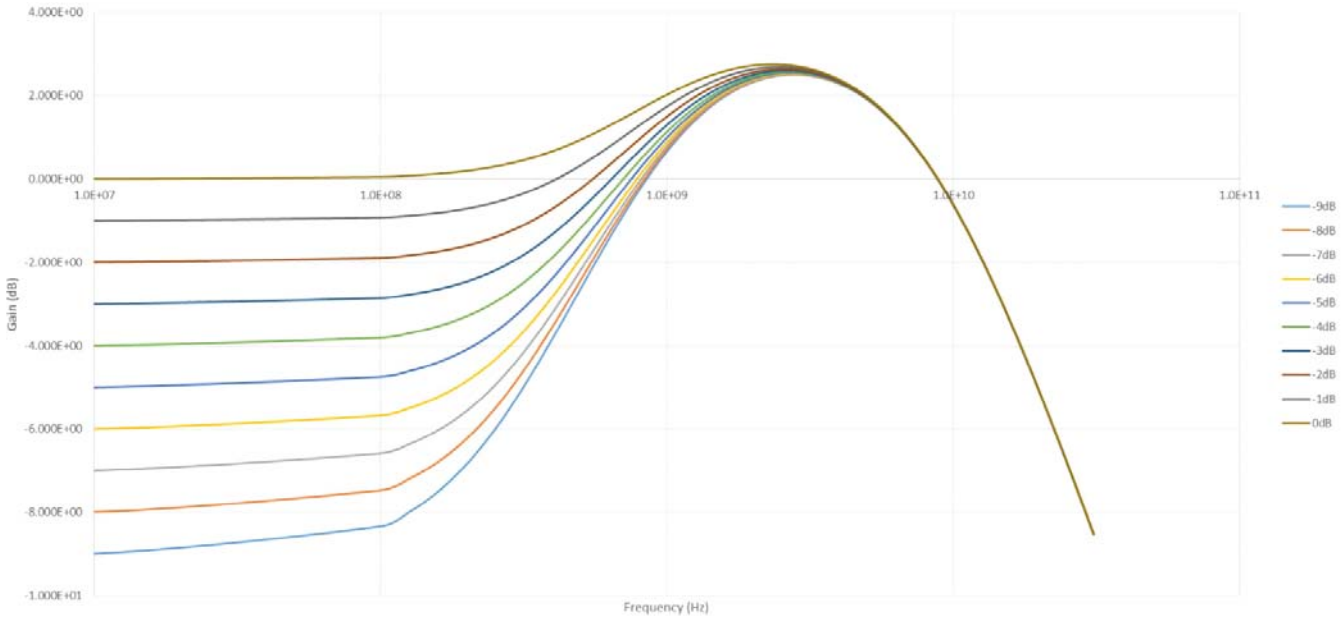


Figure 3-73: Reference Receiver CTLE for UHBR10 Curves (Normative)

For UHBR10, a Reference Receiver DFE is necessary to equalize channel loss. For UHBR10, a 1-tap Reference Receiver DFE, such as the one illustrated in Figure 3-74, is mandatory.

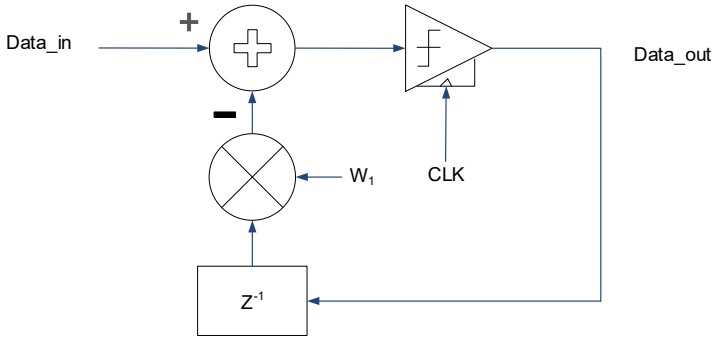


Figure 3-74: UHBR10 1-tap Reference Receiver DFE Example

where:

- Z^{-1} = Delay element, 1-unit interval.
- W = Tap weight or coefficient applied to the feedback sum relative to the delay. Up to 50mV for a 1-tap DFE.

3.5.5.6.3 UHBR10 DPTX EYE Opening Specification at TP3_EQ and TP2 (Normative), and TPRX_EQ (Informative)

The minimum required operation of UHBR-capable systems is 10Gbps. A UHBR-capable transmitter shall meet the mandates defined in Table 3-55 and Table 3-56 for TP3_EQ and TP2, respectively. The Table 3-55 and Table 3-57 parameters are with TX FFE and the Reference Receiver Equalizer both adapted. The Table 3-56 parameters are TX FFE adapted without the Reference Receiver Equalizer. A UHBR-capable transmitter may also meet the specifications defined in Table 3-57 for TPRX_EQ. These tables do not include eye closure due to crosstalk. See Figure 3-75 for the EYE-opening definition.

Note: *See Appendix O for the EYE mask methodology that is used for UHBRx bit rates and how it contrasts with the methodology used for HBR3 and HBR2.*

Table 3-55: UHBR10 DPTX TP3_EQ Metrics System Parameters (Normative)

Symbol	Parameter	Min	Nom	Max	Units	Comments
TJ_{UHBR10}	Total Jitter			475	mUI	Peak-to-peak at $1E^{-9}$ BER.[a]
UJ_{UHBR10}	Sum of Uncorrelated Deterministic Jitter (UDJ) and Random Jitter (RJ) Components[b]			260	mUI	Peak-to-peak at $1E^{-9}$ BER.[a]
DDJ_{UHBR10}	Data-dependent Jitter[c]			215	mUI	
UDJ_{UHBR10}	Deterministic Jitter that Is Uncorrelated to the Transmitted Data[d]			170	mUI	
RJ_{UHBR10}	Random Jitter			120	mUI	Peak-to-peak at $1E^{-9}$ BER.[a]
$X1_{UHBR10}$	EYE Mask Horizontal Deviation			187	mUI	Measured at $1E^{-6}$ BER.[e] [f]
$Y1_{UHBR10}$	EYE Mask Inner Height[g]	55			mV	Measured at $1E^{-6}$ BER.[e] [f]
$Y2_{UHBR10}$	EYE Outer Height[g]			500	mV	Measured at $1E^{-6}$ BER.[e] [f]

a. Crest factor of 12.
b. All jitter components except for Data-dependent jitter (DDJ). The sum of UDJ and RJ shall not exceed the maximum UJ_{UHBR10} jitter. A DPTX that exhibits the maximum-allowed RJ_{UHBR10} shall limit DDJ_{UHBR10} below the mandate to meet UJ_{UHBR10}. A DPTX that exhibits the maximum-allowed DDJ_{UHBR10} shall limit RJ_{UHBR10} below the mandate to meet UJ_{UHBR10}.
c. Also referred to as "Residual ISI."
d. Also referred to as "Non-ISI DJ."
e. Measured without RJ/DJ decomposition, using 1-M UI capture.
f. See Appendix O for further details.
g. One-sided voltage opening of the differential signal.

Table 3-56: UHBR10 DPTX TP2 Metrics System Parameters (Normative)

Symbol	Parameter	Min	Nom	Max	Units	Comments
TJ_{UHBR10}	Total Jitter			380	mUI	Peak-to-peak at $1E^{-9}$ BER.[a]
UJ_{UHBR10}	Sum of Uncorrelated Deterministic Jitter (UDJ) and Random Jitter (RJ) Components[b]			260	mUI	Peak-to-peak at $1E^{-9}$ BER.[a]
DDJ_{UHBR10}	Data-dependent Jitter[c]			110	mUI	
UDJ_{UHBR10}	Deterministic Jitter that Is Uncorrelated to the Transmitted Data[d]			170	mUI	
RJ_{UHBR10}	Random Jitter			120	mUI	Peak-to-peak at $1E^{-9}$ BER.[a]
$X1_{UHBR10}$	EYE Mask Horizontal Deviation			150	mUI	Measured at $1E^{-6}$ BER.[e] [f]
$Y1_{UHBR10}$	EYE Mask Inner Height[g]	162			mV	Measured at $1E^{-6}$ BER.[e] [f]
$Y2_{UHBR10}$	EYE Outer Height[g]			500	mV	Measured at $1E^{-6}$ BER.[e] [f]

a. Crest factor of 12.
b. All jitter components except for Data-dependent jitter (DDJ). The sum of UDJ and RJ shall not exceed the maximum UJ_{UHBR10} jitter. A DPTX that exhibits the maximum-allowed RJ_{UHBR10} shall limit DDJ_{UHBR10} below the mandate to meet UJ_{UHBR10}. A DPTX that exhibits the maximum-allowed DDJ_{UHBR10} shall limit RJ_{UHBR10} below the mandate to meet UJ_{UHBR10}.
c. Also referred to as "Residual ISI."
d. Also referred to as "Non-ISI DJ."
e. Measured without RJ/DJ decomposition, using 1-M UI capture.
f. See Appendix O for further details.
g. One-sided voltage opening of the differential signal.

Table 3-57: UHBR10 DPTX TPRX_EQ Metrics System Parameters (Informative)

Symbol	Parameter	Min	Nom	Max	Units	Comments
TJ_{UHBR10}	Total Jitter			560	mUI	Peak-to-peak at $1E^{-9}$ BER.[a]
UJ_{UHBR10}	Sum of Uncorrelated Deterministic Jitter (UDJ) and Random Jitter (RJ) Components[b]			260	mUI	Peak-to-peak at $1E^{-9}$ BER.[a]
DDJ_{UHBR10}	Data-dependent Jitter[c]			300	mUI	
UDJ_{UHBR10}	Deterministic Jitter that Is Uncorrelated to the Transmitted Data[d]			170	mUI	
RJ_{UHBR10}	Random Jitter (rms)			120	mUI	Peak-to-peak at $1E^{-9}$ BER.[a]
$X1_{UHBR10}$	EYE Mask Horizontal Deviation			222	mUI	Measured at $1E^{-6}$ BER.[e] [f]
$Y1_{UHBR10}$	EYE Mask Inner Height[g]	27			mV	Measured at $1E^{-6}$ BER.[e] [f]
$Y2_{UHBR10}$	EYE Outer Height[g]			500	mV	Measured at $1E^{-6}$ BER.[e] [f]

a. Crest factor of 12.
b. All jitter components except for Data-dependent jitter (DDJ). The sum of UDJ and RJ shall not exceed the maximum UJ_{UHBR10} jitter. A DPTX that exhibits the maximum-allowed RJ_{UHBR10} shall limit DDJ_{UHBR10} below the mandate to meet UJ_{UHBR10}. A DPTX that exhibits the maximum-allowed DDJ_{UHBR10} shall limit RJ_{UHBR10} below the mandate to meet UJ_{UHBR10}.
c. Also referred to as "Residual ISI."
d. Also referred to as "Non-ISI DJ."
e. Measured without RJ/DJ decomposition, using 1-M UI capture.
f. See Appendix O for further details.
g. One-sided voltage opening of the differential signal.

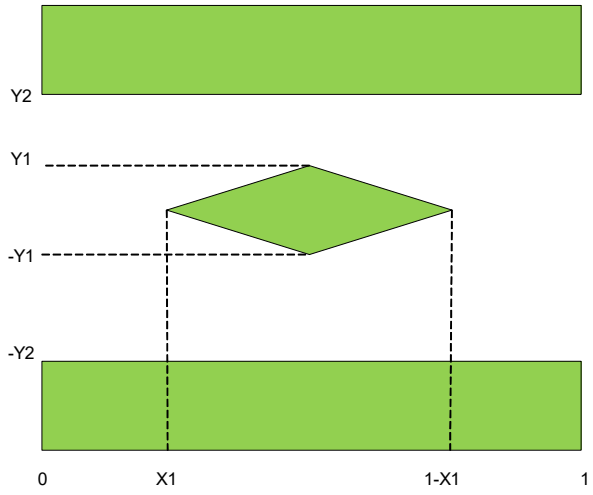


Figure 3-75: UHBR*x* EYE Opening Definitions

Note: *See Section O.2 for X/Y definitions.*

3.5.5.6.4 UHBR10 DPRX Jitter Tolerance Specification at TP3_EQ (Normative)

Table 3-58 describes the normative stressed signal EYE mask specifications used for UHBR10 DPRX jitter tolerance testing at TP3_EQ. Crosstalk is comprehended with PJ_{UHBR10}.

Table 3-58: UHBR10 DPRX TP3_EQ Metrics System Parameters at $1E^{-6}$ BER (Informative)[a]

Symbol	Parameter	Value	Units	Comments
DDJ_{UHBR10}	Data-dependent Jitter[b]	190	mUI	
RJ_{UHBR10}	Random Jitter	120	mUI	See footnote [c].
PJ_{UHBR10}	Periodic Jitter[d]	180	mUI	In RX JTOL PHY Compliance testing, SJ_{FIXED} and SJ_{SWEEP} components are used to constitute PJ_{UHBR10}. SJ_{FIXED} is adjusted to match the EW_{UHBR10} specification.
EW_{UHBR10}	EYE Width	548		
EH_{UHBR10}	EYE Inner Height[e]	98		In RX JTOL PHY Compliance testing, the Stressed Signal Generator (SSG) voltage swing is adjusted to match the EH_{UHBR10} specification.

a. All parameters are measured are at the cable output, with Reference Receiver CDR.
b. Also referred to as "Residual ISI."
c. Crest factor of 9.5.
d. Sum of SJ_{FIXED} and SJ_{SWEEP}.
e. Peak-to-peak voltage opening of the differential signal.

3.5.5.7 UHBR13.5

This section covers UHBR13.5 link parameters. Normative specifications are defined at TP2' without Reference Receiver CTLE + Reference Receiver DFE because UHBR13.5 is targeted for tethered USB Type-C cable usage only.

3.5.5.7.1 UHBR13.5 Topology

UHBR13.5 is designed to work with tethered DPRXs. DPTXs shall be designed with insertion losses that allow the DPTX to meet the TP2' EYE metrics defined in Table 3-59. See Figure 3-75 for the EYE mask definition.

Note: *See Appendix O for the EYE mask methodology that is used for UHBRx bit rates and how it contrasts with the methodology used for HBR3 and HBR2.*

3.5.5.7.2 UHBR13.5 DPTX EYE Opening at TP2' (Normative)

Table 3-59: UHBR13.5 DPTX TP2' Metrics System Parameters (Normative)[a]

Symbol	Parameter	Min	Nom	Max	Units	Comments
$TJ_{UHBR13.5}$	Total Jitter			450	mUI	Peak-to-peak at $1E^{-9}$ BER.
$UDJ_{UHBR13.5}$	Deterministic Jitter that Is Uncorrelated to the Transmitted Data[b]			170	mUI	
$RJ_{UHBR13.5}$	Random Jitter			120	mUI	Peak-to-peak at $1E^{-9}$ BER.
$X1_{UHBR13.5}$	EYE Mask Horizontal Deviation			200	mUI	Measured at $1E^{-6}$ BER.[c] [d]
$Y1_{UHBR13.5}$	EYE Mask Inner Height[e]	125			mV	Measured at $1E^{-6}$ BER.[c] [d]
$Y2_{UHBR13.5}$	EYE Outer Height[e]			500	mV	Measured at $1E^{-6}$ BER.[c] [d]

a. All parameters are measured at the cable input (TP2') without Reference Receiver CTLE + Reference Receiver DFE applied, but with the optimal FFE preset value.
b. Also referred to as "Non-ISI DJ."
c. Measured without RJ/DJ decomposition, using 1-M UI capture.
d. See.Appendix O for further details.
e. One-sided voltage opening of the differential signal.

3.5.5.7.3 UHBR13.5 Loss Budget Assumption and TP3_EQ EYE Masks (Informative)

3.5.5.7.3.1 UHBR13.5 Loss Budget Assumption (Informative)

UHBR13.5 is developed as a tethered cable system. Table 3-60 lists the losses assumed used in the development of this specification. Cables of 6.6dB of loss are expected to work with DPRXs. DPTX and DPRX systems that have 7.5dB of loss at Nyquist.

Table 3-60: UHBR13.5 Cable Interoperability Matrix (Informative)[a]

Cable Type	DPTX	Cable	DPRX	Units
USB Type-C Tethered	-7.5	-6.6	-7.5	dB

a. Loss budget values are specified at 6.75GHz.

3.5.5.7.3.2 Reference Receiver CTLE + Reference Receiver DFE for UHBR13.5 (Informative)

Designers may choose to implement a second-order CTLE and/or additional peak if it is deemed more effective than the Reference Receiver CTLE for UHBR13.5.

The informative Reference Receiver CTLE for UHBR13.5 is defined by the following equation.

$$H(s) = 1.41 \times \omega_{p2} \times \frac{\left(s + \frac{A_{DC}}{1.41} \times \omega_{p1}\right)}{(s + \omega_{p1}) \times (s + \omega_{p2})}$$

Note: *Equation is subject to change, pending analysis.*

where:

- $A_{AC} = 3.0\text{dB}$

  $A_{DC} = \left\{10^{\frac{-x}{20}}: x = 0, 1, 2, , , 9[dB]\right\}$

- $\omega_{p1} = 2\pi \times 5\text{E}9 \frac{rad}{sec}$

- $\omega_{p2} = 2\pi \times 10\text{E}9 \frac{rad}{sec}$

Figure 3-76 illustrates the informative Reference Receiver CTLE for UHBR13.5 curves.

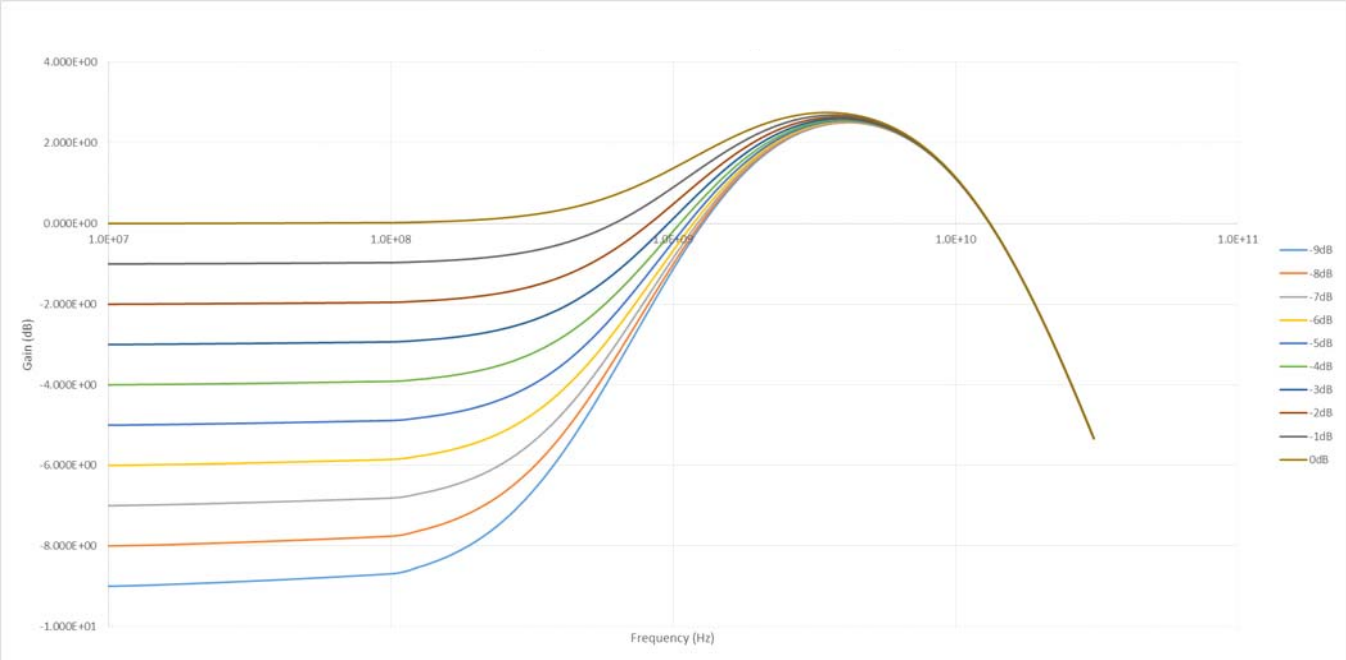


Figure 3-76: Reference Receiver CTLE for UHBR13.5 Curves (Informative)

The UHBR13.5 PHY Layer Electrical specification development used a 1-tap Reference Receiver DFE with a 50-mV tap weight (W_1) to equalize channel loss in system modeling. In practice, implementers may choose to implement a higher-order DFE, such as the one illustrated in Figure 3-77.

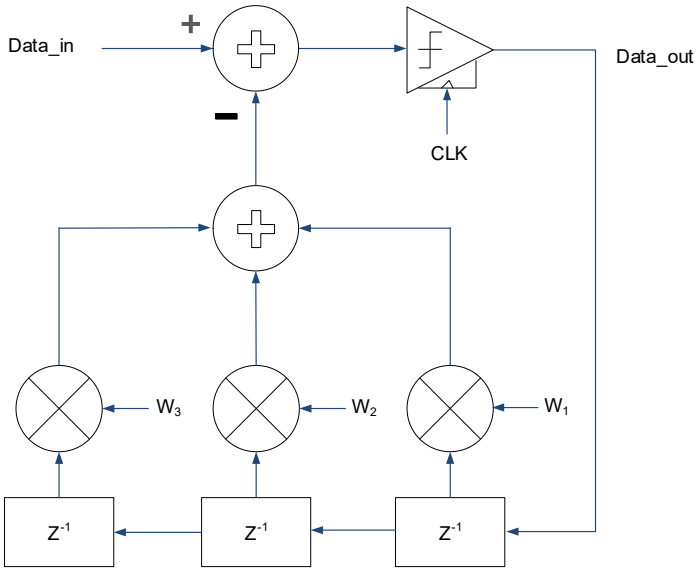


Figure 3-77: 3-tap Reference Receiver DFE Example

where:

- Z^{-1} = Delay element, 1-unit interval.
- W = Weight or coefficient applied to the feedback sum relative to the delay. Up to 50mV is the current cursor weight for a 3-tap DFE.

3.5.5.7.3.3 UHBR13.5 EYE Opening at TP3_EQ (Informative)

Table 3-61 lists the informative UHBR13.5 TP3_EQ EYE metrics system parameters at the end of the cable with Reference Receiver CTLE + Reference Receiver DFE for UHBR13.5 applied. See Figure 3-75 for the EYE mask definition.

Table 3-61: UHBR13.5 TP3_EQ Metrics System Parameters (Informative)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$TJ_{UHBR13.5}$	Total Jitter			500	mUI	Peak-to-peak $1E^{-9}$ BER.[a]
$UDJ_{UHBR13.5}$	Deterministic Jitter that Is Uncorrelated to the Transmitted Data[b]			170	mUI	
$RJ_{UHBR13.5}$	Random Jitter			120	mUI	Peak-to-peak $1E^{-9}$ BER.[a]
$X1_{UHBR13.5}$	EYE Mask Horizontal Deviation			220	mUI	Measured at $1E^{-6}$ BER.[c] [d]
$Y1_{UHBR13.5}$	EYE Mask Inner Height[e]	50			mV	Measured at $1E^{-6}$ BER.[c] [d]
$Y2_{UHBR13.5}$	EYE Outer Height[e]			500	mV	Measured at $1E^{-6}$ BER.[c] [d]

a. Crest factor of 12.
b. Also referred to as "Non-ISI DJ."
c. Measured without RJ/DJ decomposition, using 1-M UI capture.
d. See Appendix O for further details.
e. One-sided voltage opening of the differential signal.

3.5.5.8 UHBR20

This section covers UHBR20 link parameters. Normative specifications are defined at TP2' without Reference Receiver CTLE + Reference Receiver DFE because UHBR20 is targeted for tethered USB Type-C cable usage only.

3.5.5.8.1 UHBR20 Topology

UHBR20 is designed to work with tethered DPRXs. DPTXs shall be designed with insertion losses that allow the DPTX to meet the TP2' EYE metrics defined in Table 3-62. See Figure 3-75 for the EYE mask definition.

Note: *See Appendix O for the EYE mask methodology that is used for UHBRx bit rates and how it contrasts with the methodology used for HBR3 and HBR2.*

3.5.5.8.2 UHBR20 DPTX EYE Opening at TP2' (Normative)

Table 3-62: UHBR20 DPTX TP2' Metrics System Parameters (Normative)[a] [b]

Symbol	Parameter	Min	Nom	Max	Units	Comments
TJ_{UHBR20}	Total Jitter			450	mUI	Peak-to-peak $1E^{-9}$ BER.
UDJ_{UHBR20}	Deterministic Jitter that Is Uncorrelated to the Transmitted Data[c]			170	mUI	
RJ_{UHBR20}	Random Jitter			120	mUI	Peak-to-peak $1E^{-9}$ BER.
$X1_{UHBR20}$	EYE Mask Horizontal Deviation			200	mUI	Measured at $1E^{-6}$ BER.[d] [e]
$Y1_{UHBR20}$	EYE Mask Inner Height[f]	125			mV	Measured at $1E^{-6}$ BER.[d] [e]
$Y2_{UHBR20}$	EYE Outer Height[f]			500	mV	Measured at $1E^{-6}$ BER.[c] [d]

a. All parameters are measured at the DPTX receptacle, with CDR applied, and without CTLE and DFE.
b. FFE preset optimized for measurement point.
c. Also referred to as "Non-ISI DJ."
d. Measured without RJ/DJ decomposition, using 1-M UI capture.
e. See.Appendix O for further details.
f. One-sided voltage opening of the differential signal.

3.5.5.8.3 UHBR20 Loss Budget Assumption and TP3_EQ EYE Masks (Informative)

3.5.5.8.3.1 UHBR20 Loss Budget Assumption (Informative)

UHBR20 is developed as a tethered cable system. It is possible that other cables may lead to system interoperability. Table 3-63 lists the losses that are assumed to be used in the development of this specification. Cables with 9.0dB of loss are expected to work with DPTX and DPRX systems that have 7.5dB of loss at Nyquist.

Table 3-63: UHBR20 Cable Interoperability Matrix (Informative)[a]

Cable Type	DPTX	Cable	DPRX	Units
USB Type-C Tethered	-7.5	-9.0	-7.5	dB

a. Loss budget values are specified at 10GHz.

3.5.5.8.3.2 Reference Receiver CTLE + Reference Receiver DFE for UHBR20 (Informative)

Designers may choose to implement a second-order CTLE and/or additional peak if it is deemed more effective than the Reference Receiver CTLE for UHBR20.

The informative Reference Receiver CTLE for UHBR20 is defined by the following equation.

$$H(s) = 1.41 \times \omega_{p2} \times \frac{\left(s + \frac{A_{DC}}{1.41} \times \omega_{p1}\right)}{(s + \omega_{p1}) \times (s + \omega_{p2})}$$

Note: *Equation is subject to change, pending analysis.*

where:

- $A_{AC} = 3.0\text{dB}$

  $A_{DC} = \left\{10^{\frac{-x}{20}}: x = 0, 1, 2, , , 9[dB]\right\}$

- $\omega_{p1} = 2\pi \times 5E9 \frac{rad}{sec}$

- $\omega_{p2} = 2\pi \times 10E9 \frac{rad}{sec}$

Figure 3-78 illustrates the informative Reference Receiver CTLE for UHBR20 curves.

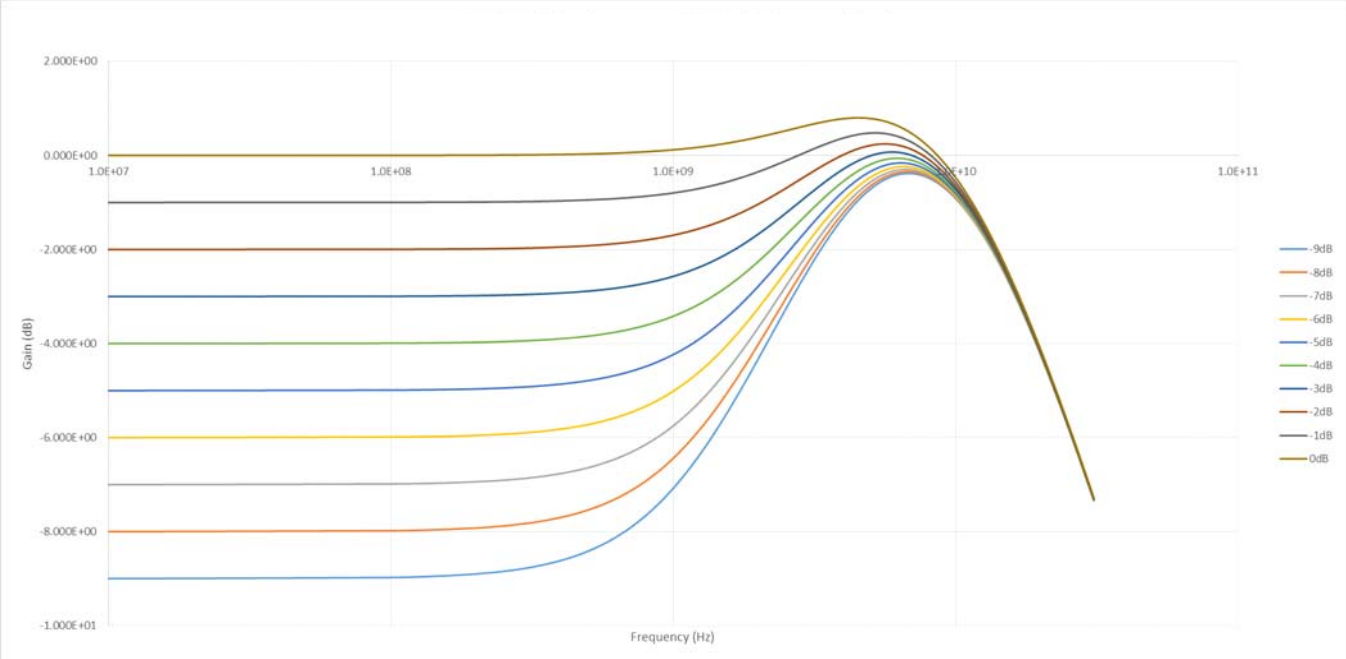


Figure 3-78: Reference Receiver CTLE for UHBR20 Curves (Informative)

The UHBR20 PHY Layer Electrical specification development used a 1-tap Reference Receiver DFE with a 50-mV tap weight (W_1) to equalize channel loss in system modeling. In practice, implementers may choose to implement a higher-order DFE, such as the one illustrated in Figure 3-79.

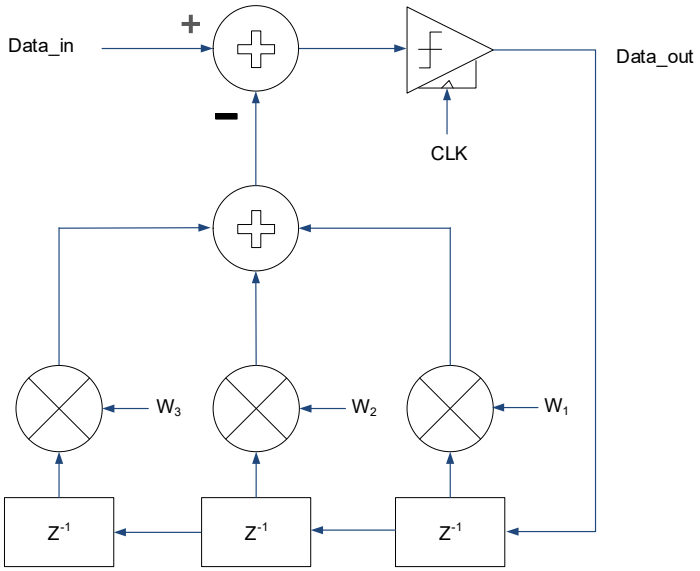


Figure 3-79: 3-tap Reference Receiver DFE Example

where:

- Z^{-1} = Delay element, 1-unit interval.
- W = Weight or coefficient applied to the feedback sum relative to the delay. Up to 50mV is the current cursor weight for a 3-tap DFE.

3.5.5.8.3.3 UHBR20 EYE Opening at TP3_EQ (Informative)

Table 3-64 lists the informative UHBR20 TP3_EQ EYE metrics system parameters at the end of the cable with Reference Receiver CTLE + Reference Receiver DFE for UHBR20 applied. See Figure 3-75 for the EYE mask definition.

Table 3-64: UHB20 TP3_EQ Metrics System Parameters (Informative)

Symbol	Parameter	Min	Nom	Max	Units	Comments
TJ_{UHBR20}	Total Jitter			500	mUI	Peak-to-peak $1E^{-9}$ BER.
UDJ_{UHBR20}	Deterministic Jitter that Is Uncorrelated to the Transmitted Data[a]			170	mUI	
RJ_{UHBR20}	Random Jitter			120	mUI	Peak-to-peak $1E^{-9}$ BER.
$X1_{UHBR20}$	EYE Mask Horizontal Deviation			220	mUI	Measured at $1E^{-6}$ BER.[b] [c]
$Y1_{UHBR20}$	EYE Mask Inner Height[d]	50			mV	Measured at $1E^{-6}$ BER.[b] [c]
$Y2_{UHBR20}$	EYE Outer Height[d]			500	mV	Measured at $1E^{-6}$ BER.[b] [c]

a. Also referred to as "Non-ISI DJ."
b. Measured without RJ/DJ decomposition, using 1-M UI capture.
c. See Appendix O for further details.
d. One-sided voltage opening of the differential signal.

3.5.6 ESD and EOS Protection

All signal and power pins of associated DP components (transmitter IC, receiver IC, and associated I/O circuitry) shall withstand at least *ANSI/ESDA/JEDEC JS-001* Class 2 (2000 to < 4000V) strikes.

DP devices implementing this specification may swing the I/O lines as high as ±0.3V single-ended with respect to the common mode bias reference level. The designer shall carefully select clamping devices and clamping rail voltages, such that ESD devices shall not cause clipping of normal signals.

3.6 LTTPRs

DP Source devices should support LTTPRs, including LTTPR recognition, capability discovery, link configuration, and link training.

A DPTX operating with 8b/10b Link Layer (MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 01h) may configure LTTPRs to either Transparent (default) or Non-transparent mode by programming the PHY_REPEATER_MODE register (DPCD Address F0003h) to 55h or AAh, respectively.

A DPTX that establishes the DP link with 128b/132b channel coding shall write 02h to the MAIN_LINK_CHANNEL_CODING_SET register and configure LTTPRs to Non-transparent mode by programming the PHY_REPEATER_MODE register to AAh.

3.6.1 Introduction

A device containing only the PHY Layer circuit of the DPRX and DPTX (i.e., DPRX_PHY and DPTX_PHY, respectively) is referred to as a "PHY Repeater." A PHY Repeater is placed between a DPTX and DPRX, both of which have PHY and Link Layer blocks with Link Policy Maker. Multiple LTTPRs can be placed between a DPTX and DPRX.

This section defines relevant terminologies and numbering rules and describes the means of discovery and support for tuning of up to eight LTTPRs between a DPTX and DPRX.

Note: *Non-LTTPRs are beyond the scope of this Standard.*

3.6.1.1 Data Path Types

There are two data path types:

- Redriver data path
  - Serial bitstream into the DPRX_PHY is optionally equalized and transmitted directly to the DPTX_PHY for retransmission with optional voltage swing/pre-emphasis adjustment
  - PHY Repeater with only a redriver data path is referred to as a "redriver"
- Retimer data path
  - Serial bitstream into the DPRX_PHY is optionally equalized, transmitted to a clock and data recovery (CDR) block for retiming, and then transmitted to the DPTX_PHY for retransmission with optional voltage swing/pre-emphasis adjustment
  - PHY Repeater with a retimer data path is referred to as a "retimer"
  - Properly implemented retimer is better equipped to output less jittery serial bitstream than a redriver

3.6.1.2 Capability Types

Orthogonal to data path types, a PHY Repeater has two capability types:

- LT-tunable
  - Provides for means for a DPTX aware of an LTTPR to tune the PHY parameters (i.e., RX EQ and DPTX drive setting) during Link Training (LT) procedure
- Non-LT-tunable
  - Does not provide means for a DPTX to tune the PHY parameters

Note: *Non-LTTPRs are beyond the scope of this Standard.*

3.6.1.3 Operating Modes

LTTPRs have two operating modes:

- Non-transparent mode
  - LTTPR replies to AUX request transactions from the DPTX to the DPCD LTTPR field while passing through other AUX request transactions.
- Transparent mode
  - When the upstream DPTX is unaware of the LTTPR, the upstream DPTX never generates AUX request transactions to the LTTPR, thereby resulting in the LTTPR's passing through all AUX transactions (while snooping AUX transactions to certain Link Configuration registers). This operating condition is referred to as "Transparent mode."
  - LTTPR transitions from Transparent to Non-transparent mode when the DPTX issues an AUX transaction to the PHY_REPEATER_MODE register (DPCD Address F0003h) to program the register's value to AAh.
  - When an LTTPR is in Transparent mode, AUX reply transactions to LTTPR DPCD registers at and above DPCD Address F0010h are invalid and shall be ignored by the DPTX.

Note: *Non-LTTPRs are considered to always be in Transparent mode. Non-LTTPRs are beyond the scope of this Standard.*

A DPTX operating with 8b/10b Link Layer may configure LTTPRs to either Transparent (default) or Non-transparent mode. A DPTX operating with 128b/132b Link Layer shall configure LTTPRs to Non-transparent mode.

3.6.1.4 LTTPR Numbering for Multiple LTTPRs between a DPTX and DPRX

When multiple LTTPRs are placed between a DPTX and DPRX, the one nearest to the DPRX is annotated as LTTPR1 and the next up as LTTPR2, as shown in the example topology illustrated in Figure 3-80.

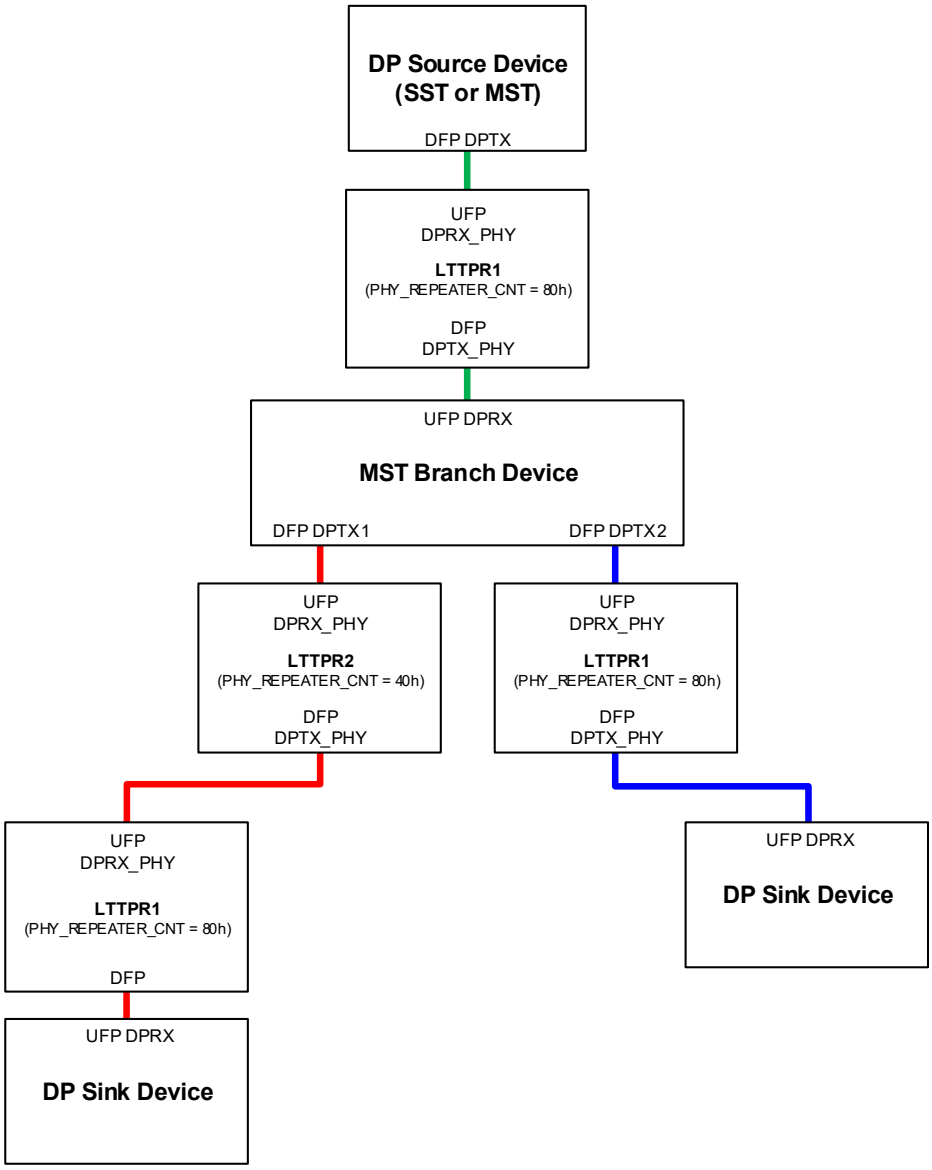


Figure 3-80: DP Topology Example with LTTPRs

3.6.2 Signal Routing Mandates

An LTTPR shall have its DP Main-Link lanes and AUX_CH signal lines routed through, as illustrated in Figure 3-81. The HPD signal could be snooped by the LTTPR or pass-through. If the HPD is pass-through, the LTTPR shall meet the delay mandates defined in Section 3.6.6.2.

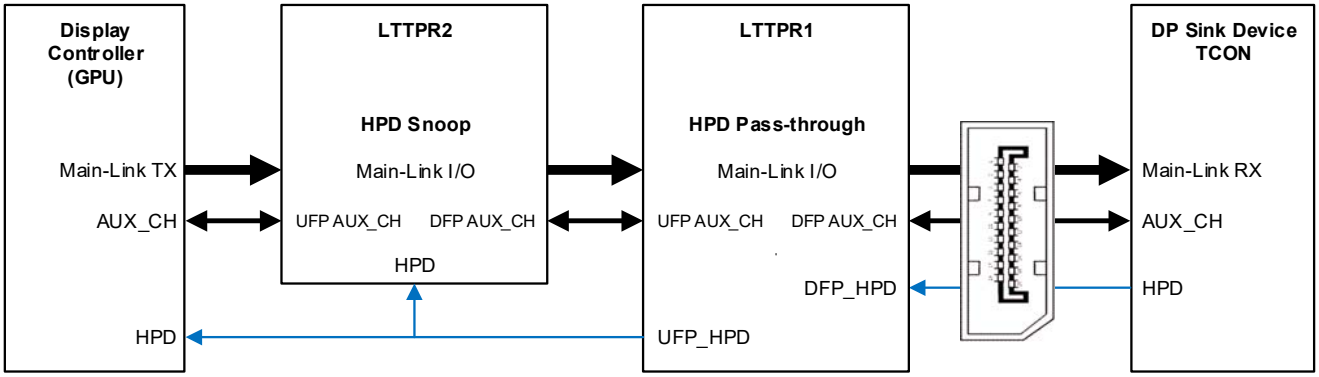


Figure 3-81: Signal Routing Mandates

3.6.3 LTTPR DPCD Address Mapping

Figure 3-82 illustrates how the DPCD LTTPR field is partitioned for multiple LTTPRs between a DPTX and DPRX.

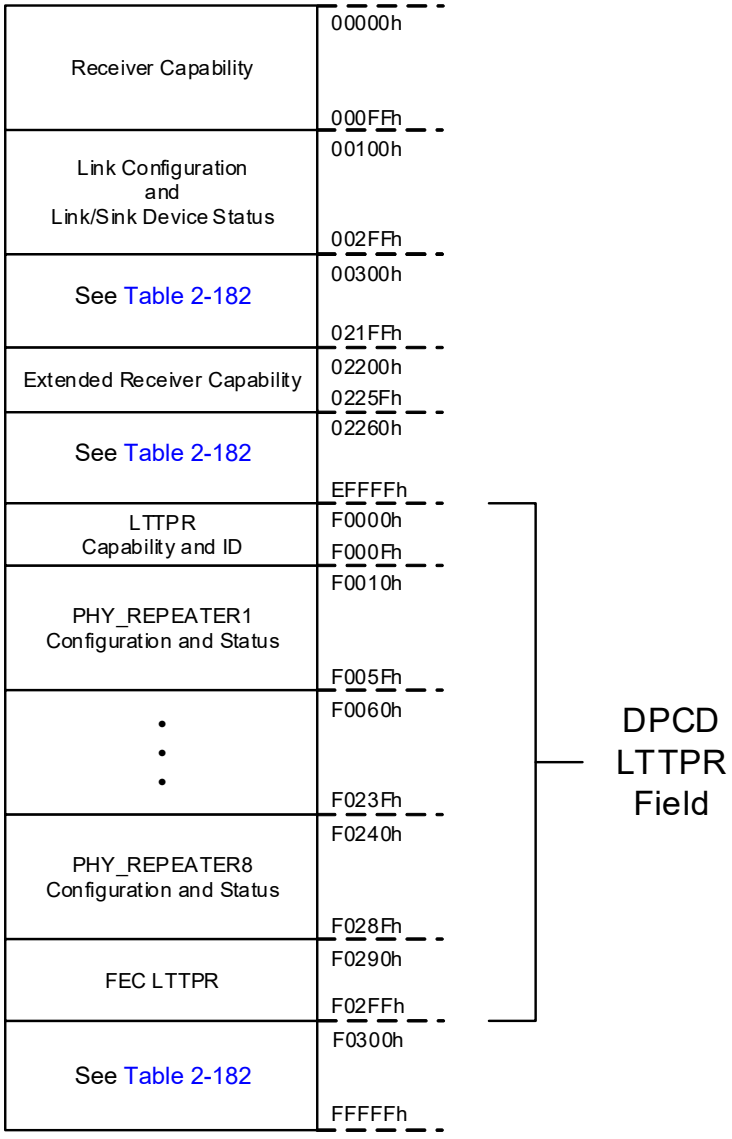


Figure 3-82: Partitioning within the DPCD LTTPR Field

Upon discovering its location between the DPTX and DPRX, the LTTPR replies to AUX request transactions to its DPCD address range within the LTTPR field. The LTTPR passes through all other AUX request transactions with one exception – an LTTPR shall snoop AUX request transactions to those DPCD Addresses listed in Table 3-65 and take necessary actions as specified in the table. (For complete register descriptions, see Table 2-184.)

Table 3-65: DPCD Addresses Snooped by LTTPR

DPCD Address	Definition
00100h	LINK_BW_SET LTTPR in Non-transparent or Transparent mode shall snoop this register.
00101h	LANE_COUNT_SET LTTPR in Non-transparent or Transparent mode shall snoop this register.
00102h	TRAINING_PATTERN_SET All LTTPRs shall snoop this register's 8b/10b_TRAINING_PATTERN_SELECT field (bits 3:0) to know when link training is complete.
00103h 00104h 00105h 00106h	TRAINING_LANE0_SET TRAINING_LANE1_SET TRAINING_LANE2_SET TRAINING_LANE3_SET LTTPRs in Transparent mode shall snoop these register(s) and update the voltage swing and pre-emphasis levels, as specified. LTTPR1 in Non-transparent mode shall snoop these register(s) and update the voltage swing and pre-emphasis levels, as specified.
00108h	MAIN_LINK_CHANNEL_CODING_SET 01h = 8b/10b Link Layer (default value when a power-on reset or upstream device disconnect occurs). 02h = 128b/132b Link Layer.
0010Bh 0010Ch 0010Dh 0010Eh	LINK_QUAL_LANE0_SET LINK_QUAL_LANE1_SET LINK_QUAL_LANE2_SET LINK_QUAL_LANE3_SET LTTPRs in Non-transparent or Transparent mode shall snoop these register(s) to avoid indication of LANE*x*_SYMBOL_LOCKED status loss if an upstream DPTX transmits a pattern that does **not** contain K28.5/K28.1 characters.
00600h	SET_POWER & SET_DP_PWR_VOLTAGE LTTPRs in Non-transparent or Transparent mode shall snoop this field to detect entering a power-saving state, as described in Section 3.6.10.

3.6.4 LTTPR DPCD Registers

LTTPRs transition to Non-transparent mode only when the DPTX programs the PHY_REPEATER_MODE register (DPCD Address F0003h) value to AAh.

3.6.4.1 LTTPR DPCD Capability and ID Field

Table 3-66 lists the registers that are shared by all LTTPRs between a DPTX and DPRX. Therefore, all LTTPRs shall reply to AUX read request transactions to these registers. (For complete register descriptions, see Table 2-198.)

Table 3-66: LTTPR DPCD Capability and ID Field

DPCD Address	Register
F0000h	LT_TUNABLE_PHY_REPEATER_FIELD_DATA_STRUCTURE_REV
F0001h	8b/10b_MAX_LINK_RATE_PHY_REPEATER
F0002h	PHY_REPEATER_CNT
F0003h	PHY_REPEATER_MODE
F0004h	MAX_LANE_COUNT_PHY_REPEATER
F0005h	PHY_REPEATER_EXTENDED_WAKE_TIMEOUT
F0006h	MAIN_LINK_CHANNEL_CODING_PHY_REPEATER
F0007h	PHY_REPEATER_128b/132b_RATES

The DPRX shall reply to the above AUX request transactions with an AUX_ACK followed by a 00h value. The DPRX's failure to respond with 0s can result in undefined system behavior.

An LTTPR that receives an all-zero data reply from its downstream device (i.e., the one nearest to the DPRX) shall replace the received data with its own data. An LTTPR that receives a non-zero data reply shall update the received data based on the specified behavior for each DPCD register.

3.6.4.2 LTTPR DPCD Link Configuration and Status Field(s)

Table 3-67 lists the DPCD LTTPR CONFIGURATION AND STATUS fields for up to eight LTTPRs (LTTPR[8:1]). Only the LTTPR that matches the AUX request address shall modify the reply from the downstream device. (For complete register descriptions, see Table 2-198.)

Table 3-67: LTTPR DPCD Link Configuration and Status Field(s)

DPCD Address	Register
F0010h through F005Fh	PHY_REPEATER1 CONFIGURATION AND STATUS FIELD
F0060h through F00AFh	PHY_REPEATER2 CONFIGURATION AND STATUS FIELD
F00B0h through F00FFh	PHY_REPEATER3 CONFIGURATION AND STATUS FIELD
F0100h through F014Fh	PHY_REPEATER4 CONFIGURATION AND STATUS FIELD
F0150h through F019Fh	PHY_REPEATER5 CONFIGURATION AND STATUS FIELD
F01A0h through F01EFh	PHY_REPEATER6 CONFIGURATION AND STATUS FIELD
F01F0h through F023Fh	PHY_REPEATER7 CONFIGURATION AND STATUS FIELD
F0240h through F028Fh	PHY_REPEATER8 CONFIGURATION AND STATUS FIELD

3.6.5 AUX Transaction Handling Mandates

Entire section rewritten for *DP v1.4a*.

This section details the AUX transaction handling of the DPTX, DPRX, and LTTPRs. All DPTXs shall support LTTPRs. These devices shall meet the AUX transaction handling mandates defined in Section 2.11 unless stated otherwise within the following sub-sections.

3.6.5.1 DPTX

The DPTX shall function as defined in Section 2.11. The AUX Reply Timeout timer period is defined in Section 2.11.2.

The DPTX shall not target an AUX transaction to more than one LTTPR at a time, with the exception of accessing the LTTPR DPCD Capability and ID Field, as defined in Section 3.6.4.1.

3.6.5.2 DPRX

The DPRX shall function as defined in Section 2.11. The timeout remains the same at 300us.

3.6.5.3 LTTPR

An LTTPR shall pass all AUX request transactions (read or write) received on its UFP to its DFP, and have one of the following behaviors for the transaction's reply.

Reply to AUX read request:

- Passes unmodified LTTPR reply to its UFP if the AUX read request did **not** target the LTTPR.
- If the AUX read request targeted the LTTPR DPCD Capability and ID Field (see Table 3-66), the LTTPR replaces the DPRX's DPCD data with its own DPCD data.
- If the AUX read request targeted the LTTPR's DPCD register and not the LTTPR DPCD Capability and ID Field, the LTTPR can replace the DPRX's DPCD data with its own DPCD data, –or– if the data is not ready, the LTTPR can respond accordingly as specified in Section 2.11.

Reply to AUX write request:

- Passes unmodified LTTPR reply to its UFP if the AUX write request did **not** target the LTTPR.
- If the AUX write request targeted the LTTPR DPCD Capability and ID Field:
  - Changes the DPRX's AUX_NACK with $M = 0$ reply with AUX_ACK,
  - Changes the DPRX's AUX_DEFER reply with AUX_ACK,
  - Passes along the DPRX's AUX_ACK reply.
- If the AUX write request targeted the LTTPR's DPCD register and **not** the LTTPR DPCD Capability and ID Field:
  - Changes the DPRX's AUX_NAK with $M = 0$, AUX_DEFER or AUX_ACK reply with AUX_ACK, –or– if the access operation is not complete, the LTTPR can respond accordingly, as specified in Section 2.11.

The LTTPR shall maintain the specified number of pre-charge and SYNC pulses as defined in this Standard because AUX transactions traverse through the LTTPR in either the upstream or downstream direction.

For any LTTPR, the combination of the LTTPR AUX request and response delays shall **not** be greater than 350us:

- **LTTPR AUX request delay** – Time measured from the end of the AUX_SYNC END pattern being received on the LTTPR UFP AUX port to the end of the AUX_SYNC END pattern being re-transmitted from the LTTPR DFP AUX_CH transceiver
- **LTTPR AUX response delay** – Time measured from the end of the AUX_SYNC END pattern being received on the LTTPR DFP AUX port to the end of the AUX_SYNC END pattern being re-transmitted from the LTTPR's UFP AUX_CH transceiver

When operating in Transparent mode, the LTTPR should minimize its impact to AUX transaction time. This is to avoid having the AUX Reply Timeout timer time out (see Section 2.11.2) when the LTTPR is used with a DPTX that is **not** LTTPR-aware.

3.6.5.3.1 AUX Error Conditions

- No reply to an AUX request targeting the LTTPR field:
  - This shall result in the DPTX's AUX Reply Timeout timer timing out. If the DPTX decides to issue another AUX request, the LTTPR shall discard the previous transaction and act on the new request.
- DPRX replies with non-zero data to an AUX read request to its reserved space:
  - This non-compliant DPRX behavior might result in undefined system behavior.
- DPRX replies with an AUX_ACK to an AUX write request to its reserved space:
  - LTTPR shall pass the AUX_ACK upstream.
- Corrupted AUX request transaction:
  - Pass-through to a DFP is implementation-specific.
  - If pass-through, shall **not** fix the cause of corruption.
  - Shall result in the DPTX's AUX Reply Timeout timer timing out.
- Corrupted AUX reply:
  - Pass-through to a UFP is implementation-specific.
  - If pass-through, shall **not** fix the cause of corruption.
  - Shall result in the DPTX's AUX Reply Timeout timer timing out.

3.6.5.3.2 LTTPR AUX UFP (Informative)

The DPTX is likely to periodically issue AUX request transactions. An LTTPR's UFP shall continuously monitor the address of the AUX request transaction to determine whether the request targets the LTTPR. When the request address matches the LTTPR's address, the LTTPR shall set an internal AUX_PEND flag. The AUX_PEND flag shall remain set until the LTTPR updates or modifies the DPRX's reply –or– a new AUX request transaction is received on the LTTPR's UFP.

An AUX Write transaction to a RESERVED address within the DPCD LTTPR field should **not** be considered a match and the internal AUX_PEND flag should **not** be set.

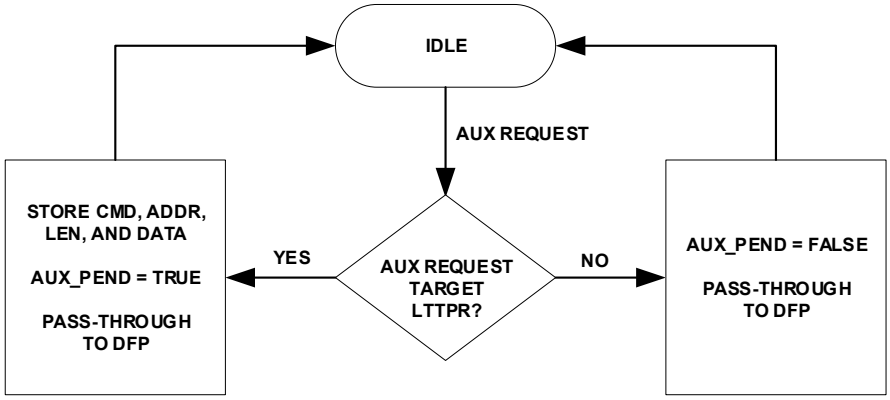
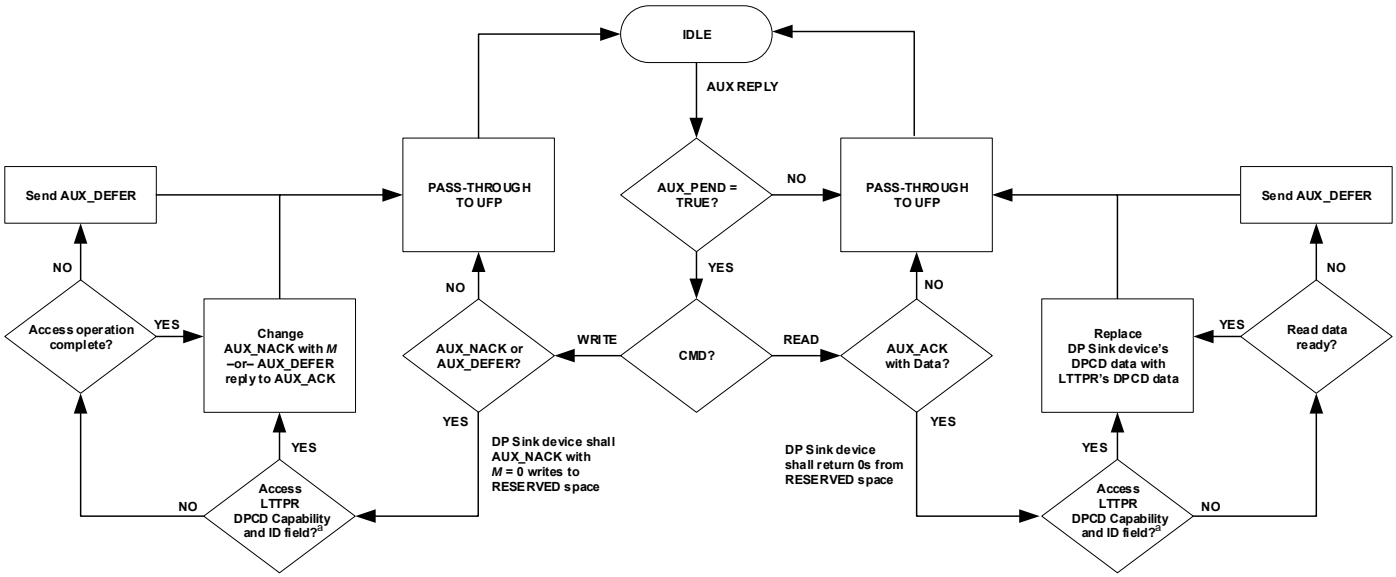


Figure 3-83: LTTPR AUX UFP State Machine (Informative)

3.6.5.3.3 LTTPR AUX DFP (Informative)

An LTTPR's DFP shall typically pass all AUX replies, unmodified, to its UFP. When the internal AUX_PEND flag is set, the LTTPR shall wait until the DPRX replies to an AUX request transaction. When replying to an AUX read request, the LTTPR shall either replace or modify the DPRX data with its own DPCD data in case the AUX read request transaction addresses the LTTPR DPCD Capability and ID Field (see Table 3-66). When replying to an AUX write request, the LTTPR shall modify the AUX reply acknowledge type (AUX_NACK *M* = 0 or AUX_DEFER) to an AUX_ACK in case the AUX write request transaction addresses the LTTPR DPCD Capability and ID Field. When the AUX transaction targets only one LTTPR, that LTTPR's DFP shall reply as defined in Section 2.11. The internal AUX_PEND flag shall be cleared after the reply is transmitted on the LTTPR's UFP.



a. See Table 3-66.

Figure 3-84: LTTPR AUX DFP State Machine (Informative)

3.6.5.3.4 AUX Read Examples

Figure 3-85 illustrates an example of LTTPR behavior when an AUX read request does not target the LTTPR. In this example, the DPRX's DPCD data 11h and 22h is passed, unmodified, through the LTTPR to the DPTX.

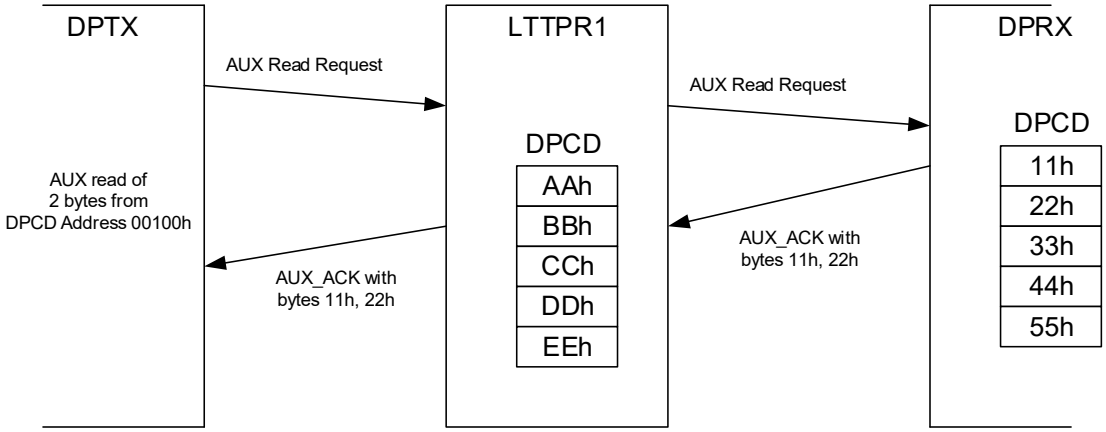


Figure 3-85: AUX Read that Does Not Target an LTTPR

Figure 3-86 illustrates an example of LTTPR behavior when an AUX read request targets an LTTPR's DPCD register. The DPRX responds with 0s to the AUX read request that is targeting its RESERVED space. The LTTPR changes the DPRX's data with its own data (AAh and BBh), and then transmits that data to the DPTX.

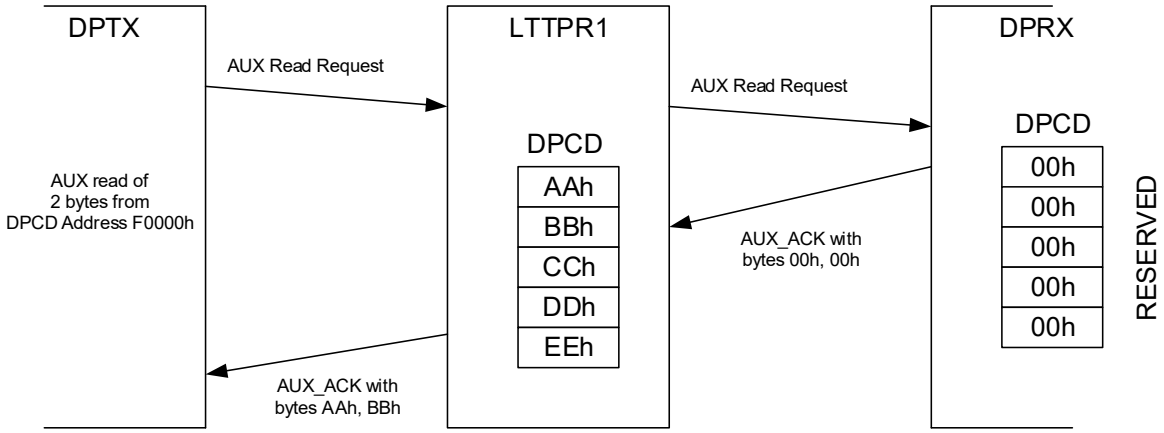


Figure 3-86: AUX Read that Targets Only an LTTPR

3.6.5.3.5 AUX Write Examples

The reply to an AUX write request transaction that does not target the LTTPR is always passed, unmodified, through the LTTPR. In Figure 3-87, the LTTPR forwards the AUX_ACK from the DPRX to the DPTX.

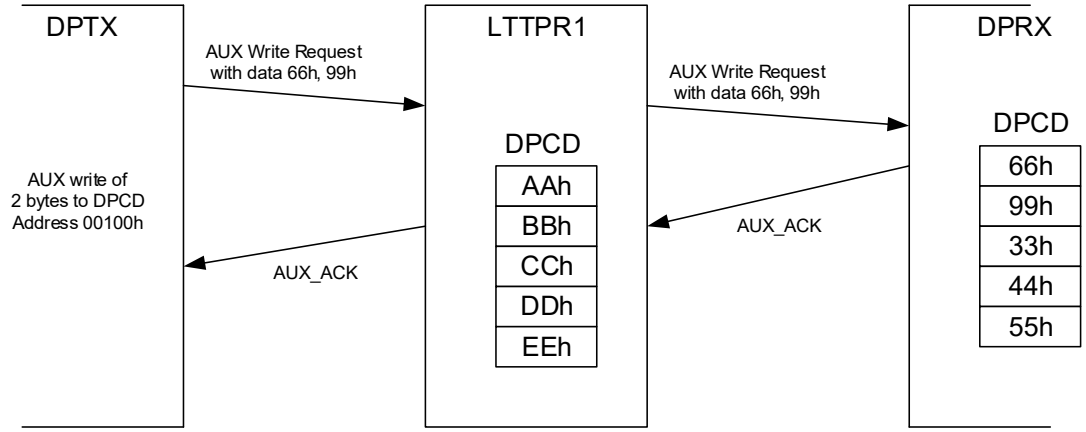


Figure 3-87: AUX Write that Does Not Target an LTTPR

Figure 3-88 illustrates an AUX write request transaction that targets the LTTPR. Because the LTTPR's DPCD registers are RESERVED in the DPRX, the DPRX shall reply to the AUX write request transaction with an AUX_NACK *M* = 0 –or– AUX_DEFER. The LTTPR shall change the DPRX's reply to an AUX_ACK, which is then transmitted to the DPTX.

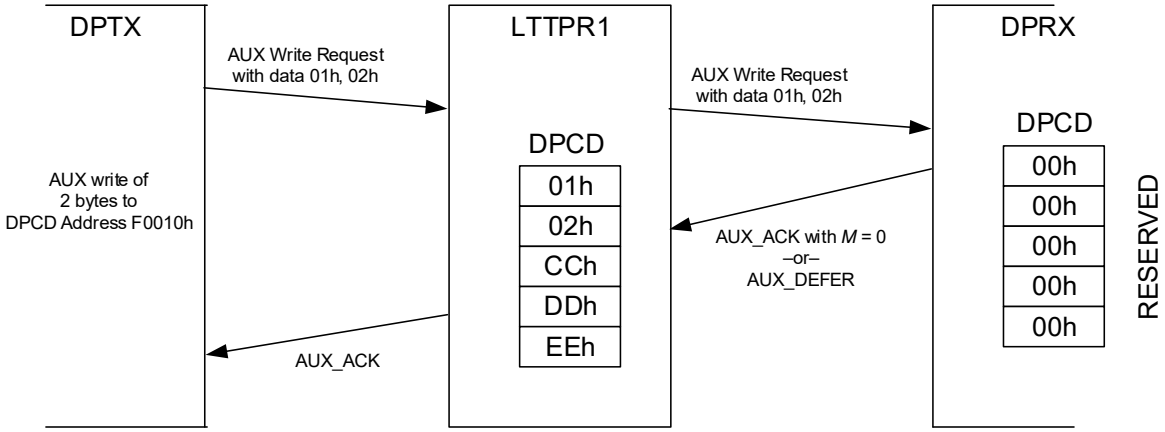


Figure 3-88: AUX Write that Targets an LTTPR

3.6.6 Link Training

3.6.6.1 8b/10b Link Layer DPTX Link Training Mandates

Updated in *DP v1.4a*.

This section describes the link training mandates for a DPTX operating in 8b/10b Link Layer that supports LTTPRs. DP upstream devices that do not enable the Non-transparent mode of LTTPRs shall program the PHY_REPEATER_MODE register (DPCD Address F0003h) to 55h (default) prior to link training, and do **not** need to meet the remaining mandates indicated within this section. If the PHY_REPEATER_CNT register (DPCD Address F0002h) reports a value other than 80h, 40h, 20h, 10h, 08h, 04h, 02h, or 01h, the DPTX shall **neither** program the PHY_REPEATER_MODE register to AAh **nor** follow the link training mandates indicated within this section.

- DPTX shall always provide a training pattern (TPS1, TPS2, TPS3, or TPS4).
- DPTX shall change its Main-Link voltage swing and pre-emphasis levels only when communicating with the most immediate downstream LTTPR. For example, if the PHY_REPEATER_CNT register is programmed to 08h, the DPTX shall change its Main-Link levels based on values returned from the ADJUST_REQUEST_LANE0_1_PHY_REPEATER5 and ADJUST_REQUEST_LANE2_3_PHY_REPEATER5 DPCD registers.
- Before performing link training with LTTPR(s), the DPTX may place the LTTPR(s) in Non-transparent mode by first writing 55h to the PHY_REPEATER_MODE register, and then writing AAh. This operation does **not** need to be performed on subsequent link training actions unless a downstream device unplug event is detected.
- DPTX shall write the DPRX's LINK_BW_SET and LANE_COUNT_SET registers (DPCD Addresses 00100h and 00101h, respectively) with the appropriate link rate and lane count, respectively.
- DPTX shall fully train one link at a time, starting from the link nearest to the DPTX and ending at the link nearest to the DPRX.
  - Achieve LANE*x*_CR_DONE, LANE*x*_SYMBOL_LOCKED, LANE*x*_CHANNEL_EQ_DONE, and INTERLANE_ALIGN_DONE for each link before training the next downstream link
- DPTX shall **not** write to the DPRX's TRAINING_PATTERN_SET register (DPCD Address 00102h) unless the LTTPR nearest to the DPRX has achieved LANE*x*_CR_DONE, LANE*x*_SYMBOL_LOCKED, LANE*x*_CHANNEL_EQ_DONE, and INTERLANE_ALIGN_DONE.
- DPTX shall drive the training patterns, as follows:
  - TPS1 for all LANE*x*_CR_DONE sequences
  - TPS4 for the LTTPR Sink device's LANE*x*_CHANNEL_EQ_DONE sequence
  - TPS2/TPS3/TPS4 for DPRX's LANE*x*_CHANNEL_EQ_DONE sequence, according to the DPRX's capability reported at the TPS3_SUPPORTED bit in the MAX_LANE_COUNT register and TPS4_SUPPORTED bit in the MAX_DOWNSPREAD register (DPCD Address 00002h, bit 6, and DPCD Address 00003h, bit 7, respectively)

- DPTX shall read the TRANSMITTER_CAPABILITY_PHY_REPEATER*x* register (e.g., DPCD Address F0021h for LTTPR1) corresponding to the LTTPR being used as a transmitter. The DPTX shall then use the register's VOLTAGE_SWING_LEVEL_3_SUPPORTED and PRE_EMPHASIS_LEVEL_3_SUPPORTED bits (bits 0 and 1, respectively) to determine whether the MAX_SWING_REACHED and MAX_PRE-EMPHASIS_REACHED bits in the TRAINING_LANE*x*_SET register (DPCD Addresses 00103h through 00106h, bits 2 and 5, respectively) should be set.
- DPTX shall terminate link training by writing 0h to the 8b/10b_TRAINING_PATTERN_SELECT field in the TRAINING_PATTERN_SET register (DPCD Address 00102h, bits 3:0) to notify the LTTPRs and DPRX that link training is complete.
- LTTPRs include a register that programs the Link Status/Adjust Request read interval in the TRAINING_AUX_RD_INTERVAL_PHY_REPEATER*x* field in the TRAINING_AUX_RD_INTERVAL_PHY_REPEATER*x* register(s) (e.g., DPCD Address F0020h for LTTPR1, bits 6:0). The DPTX shall read the field value that corresponds to the LTTPR being trained, and then use the read interval requested in that register for Main-Link training. This mandate does **not** impact communication with the DPRX. The TRAINING_AUX_RD_INTERVAL field in the 8b/10b_TRAINING_AUX_RD_INTERVAL register (DPCD Address 0220Eh, bits 6:0) read interval reported by the DPRX shall then be used when communicating with the DPRX.

3.6.6.2 8b/10b Link Layer LTTPR Link Training Mandates

- LTTPR shall be ready for link training immediately after the AUX transaction that is used to program the PHY_REPEATER_MODE register (DPCD Address F0003h) to 55h or AAh successfully completes.
- LTTPR shall support either two or four DP Main-Link lanes.
- LTTPR shall support all required voltage swing and pre-emphasis combinations defined in Table 3-2. The LTTPR shall reflect its support of optional Voltage Swing Level 3 and Pre-emphasis Level 3 in the VOLTAGE_SWING_LEVEL_3_SUPPORTED and VOLTAGE_SWING_LEVEL_3_SUPPORTED bits, respectively, in the TRANSMITTER_CAPABILITY_PHY_REPEATER*x* register(s) (e.g., DPCD Address F0021h for LTTPR1, bits 0 and 1, respectively).
- LTTPR shall support TPS4.
- If the DPTX sets the voltage swing or pre-emphasis to a level that the LTTPR does not support, the LTTPR shall set its transmitter levels as close as possible to those requested by the DPTX. Although the LTTPR's level choosing is implementation-specific, the levels chosen shall comply with Section 3.5.4.
- LTTPR does not create training patterns. The LTTPR shall pass training patterns that are received on its UFP to its DFP.
- IRQ_HPD received on the LTTPR's DFP shall be passed through to the LTTPR's UFP. The delay from "received on DFP" to "output on UFP" shall be no greater than 200us.
- HPD unplug event on the LTTPR's DFP shall be passed through to the LTTPR's UFP. The delay from "received on DFP" to "output on UFP" shall be no greater than 200us.

- Upstream device disconnect event on the LTTPR's UFP shall be passed through to the LTTPR's DFP. The delay from "received on UFP" to "output on DFP" shall be no greater than 200us.
- LTTPR's Main-Link output shall remain in an electrical idle state until LANE*x*_CR_DONE is achieved on its UFP.
- All LTTPRs shall snoop AUX write transactions to a DPRX's LINK_BW_SET and LANE_COUNT_SET registers (DPCD Addresses 00100h and 00101h, respectively). LTTPRs shall use the information written to these two registers to enable the specified link rate and number of lanes, respectively.
- LTTPR shall adjust its voltage swing and pre-emphasis levels based on an AUX write request transaction to the TRAINING_LANE*x*_SET_PHY_REPEATER*y* register(s) (e.g., DPCD Address F0011h for LTTPR1, Lane 0), where $x = 0, 1, 2,$ or 3 and y = the PHY_REPEATER_CNT register's (DPCD Address F0002h) count of its immediate downstream device. For example, LTTPR3 shall adjust its output levels based on AUX write transactions to LTTPR2.
- LTTPR1 with the PHY_REPEATER_CNT register programmed to 80h shall adjust its voltage swing and pre-emphasis levels based on AUX write transactions to the DPTX TRAINING_LANE*x*_SET register(s), where $x = 0, 1, 2,$ and/or 3 (DPCD Addresses 00103h through 00106h, respectively). Similarly, LTTPR[*N*] with the corresponding PHY_REPEATER_CNT register value shall adjust its output levels based on AUX write transactions to the TRAINING_LANE*x*_SET_PHY_REPEATER[$N - 1$] register(s).
- LTTPR shall consider link training of its Sink device to be complete when its TRAINING_PATTERN_SELECT field in the TRAINING_PATTERN_SET_PHY_REPEATER*x* register (e.g., DPCD Address F0010h for LTTPR1) transitions from non-zero to 00h.
- After an LTTPR UFP's link training is complete, the LTTPR shall forward all symbols and patterns that respect the 8b/10b encodings from its UFP to its DFP, including TPS1. The LTTPR that receives TPS1 shall maintain LANE*x*_SYMBOL_LOCKED and INTERLANE_ALIGN_DONE on its UFP.

3.6.6.3 128b/132b Link Layer DPTX Link Training Mandates

New to *DP v2.0*.

This section describes the Link Training mandates for a DPTX that supports 128b/132b Link Layer. If the PHY_REPEATER_CNT register (DPCD Address F0002h) reports a value of 80h, 40h, 20h, 10h, 08h, 04h, 02h, or 01h, the DPTX shall program the PHY_REPEATER_MODE register (DPCD Address F0003h) as Non-transparent mode with a value of AAh.

- DPTX shall always provide a training pattern (128b/132b_TPS1 or 128b/132b_TPS2).
- DPTX shall change its TX_FFE_PRESET_VALUE field (e.g., TRAINING_LANE0_SET_PHY_REPEATER1 register, DPCD Address F0011h, bits 3:0) value only when communicating with the most immediate downstream LTTPR. For example, if the PHY_REPEATER_CNT register is programmed to 08h, the DPTX shall change its TX_FFE_PRESET_VALUE field value based on values returned from the TX_FFE_PRESET_VALUE_LANE*x* fields in the ADJUST_REQUEST_LANE0_1_PHY_REPEATER5 and ADJUST_REQUEST_LANE2_3_PHY_REPEATER5 DPCD registers.
- Before performing link training with LTTPR(s), the DPTX may place the LTTPR(s) in Non-transparent mode by writing AAh to the PHY_REPEATER_MODE register. This operation does **not** need to be performed on subsequent link training actions unless a downstream device unplug event is detected.
- DPTX shall write the DPRX's the MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h), and then write the DPRX's LINK_BW_SET and LANE_COUNT_SET registers (DPCD Addresses 00100h and 00101h, respectively) with the appropriate link rate and lane count, respectively.
- DPTX shall fully train one link at a time, starting from the link nearest to the DPTX and ending at the link nearest to the DPRX.
  - Achieve LANE*x*_CR_DONE, LANE*x*_SYMBOL_LOCKED, LANE*x*_CHANNEL_EQ_DONE, and INTERLANE_ALIGN_DONE for each link before training the next downstream link
- DPTX shall **not** write to the DPRX's TRAINING_PATTERN_SET register (DPCD Address 00102h) unless the LTTPR nearest to the DPRX has achieved LANE*x*_CR_DONE, LANE*x*_SYMBOL_LOCKED, LANE*x*_CHANNEL_EQ_DONE, and INTERLANE_ALIGN_DONE.
- DPTX training at 128b/132b shall drive the training patterns for all downstream LTTPRs and the DPRX, as follows:
  - Program the MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) to 02h
  - 128b/132b_TPS1 for all LANE*x*_CR_DONE sequences
  - 128b/132b_TPS2 for the LTTPR Sink device's LANE*x*_CHANNEL_EQ_DONE sequence
- DPTX shall terminate link training by writing 0h to the 8b/10b_TRAINING_PATTERN_SELECT field in the TRAINING_PATTERN_SET register (DPCD Address 00102h, bits 3:0) to notify the LTTPRs and DPRX that link training is complete.

- LTTPRs include a register that programs the Link Status/Adjust Request read interval in the 128b/132b_TRAINING_AUX_RD_INTERVAL_PHY_REPEATER*x* field in the 128b/132b_TRAINING_AUX_RD_INTERVAL_PHY_REPEATER*x* register(s) (e.g., DPCD Address F0022h for LTTPR1, bits 6:0). The DPTX shall read the field value that corresponds to the LTTPR being trained, and then use the read interval requested in that register for Main-Link training. This mandate does **not** impact communication with the DPRX. The 128b/132b_TRAINING_AUX_RD_INTERVAL field in the 128b/132b_TRAINING_AUX_RD_INTERVAL register (DPCD Address 02216h, bits 6:0) read interval reported by the DPRX shall then be used when communicating with the DPRX.

3.6.6.4 128b/132b Link Layer LTTPR Link Training Mandates

New to *DP v2.0*.

- LTTPR shall be ready for link training immediately after the AUX transaction that is used to program the PHY_REPEATER_MODE register (DPCD Address F0003h) to AAh successfully completes.
- LTTPR shall support either two or four DP Main-Link lanes.
- LTTPR shall support all mandated FFE levels (see Section 3.5.5.3 for details).
- LTTPR does not create training patterns. The LTTPR shall pass training patterns that are received on its UFP to its DFP.
- All LTTPRs shall snoop AUX write transactions to the MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) and a DPRX's LINK_BW_SET and LANE_COUNT_SET registers (DPCD Addresses 00100h and 00101h, respectively). LTTPRs shall use the information written to the LINK_BW_SET and LANE_COUNT_SET registers to enable the specified link rate and number of lanes, respectively.
- LTTPR shall adjust its output FFE level, based on an AUX write request transaction to the TRAINING_LANE*x*_SET_PHY_REPEATER*y* registers (e.g., DPCD Address F0011h for LTTPR1, Lane 0), where $x = 0, 1, 2,$ or 3 and $y =$ the PHY_REPEATER_CNT register's (DPCD Address F0002h) count of its immediate downstream device. For example, LTTPR3 shall adjust its output levels based on AUX write transactions to LTTPR2.
- LTTPR1 with the PHY_REPEATER_CNT register programmed to 80h shall adjust its output FFE level based on AUX write transactions to the DPTX TRAINING_LANE*x*_SET register(s), where $x = 0, 1, 2,$ and/or 3 (DPCD Addresses 00103h through 00106h, respectively). Similarly, LTTPR[*N*] with the corresponding PHY_REPEATER_CNT register value shall adjust its output levels based on AUX write transactions to the TRAINING_LANE*x*_SET_PHY_REPEATER[$N - 1$] register(s).
- LTTPR shall consider link training of its immediate downstream RX (i.e., UFP of the next LTTPR) to be complete when its TRAINING_PATTERN_SELECT field in the TRAINING_PATTERN_SET_PHY_REPEATER*x* register (e.g., DPCD Address F0010h for LTTPR1) transitions from non-zero to 00h.

- After an LTTPR UFP's link training is complete, the LTTPR shall forward all 128b/132b Link Layer symbols and patterns that are transmitted from the LTTPR's UFP to the LTTPR's DFP, including 128b/132b_TPS1 or 128b/132b_TPS2. The LTTPR that receives 128b/132b_TPS1 shall maintain LANE*x*_SYMBOL_LOCKED and INTERLANE_ALIGN_DONE on its UFP.

3.6.6.5 Link Training Error Cases

- Errors that occur during the LANE*x*_CR_DONE sequence should follow Figure 3-12 on page 745
- Errors that occur during the LANE*x*_CHANNEL_EQ_DONE sequence should follow Figure 3-13 on page 750
- If the DPTX needs to change the link bandwidth and number of Main-Link lanes, the DPTX shall abort and then re-initiate training, writing new values to DPRX's LINK_BW_SET register and LANE_COUNT_SET field in the LANE_COUNT_SET register (DPCD Address 00100h, and DPCD Address 00101h, bits 4:0, respectively)

3.6.6.6 8b/10b Example Use Case

Figure 3-89 illustrates an LTTPR in both a laptop and docking station. This section steps through what the DPTX (GPU), LTTPR1, LTTPR2, and DPRX (DP Sink device) behavior shall be during link training. This example assumes that the following conditions exist:

- DPTX supports an 8.1Gbps/lane link rate (HBR3)
- LTTPR2 has only two lanes available
- DPRX supports up to a 5.4Gbps/lane link rate (HBR2)

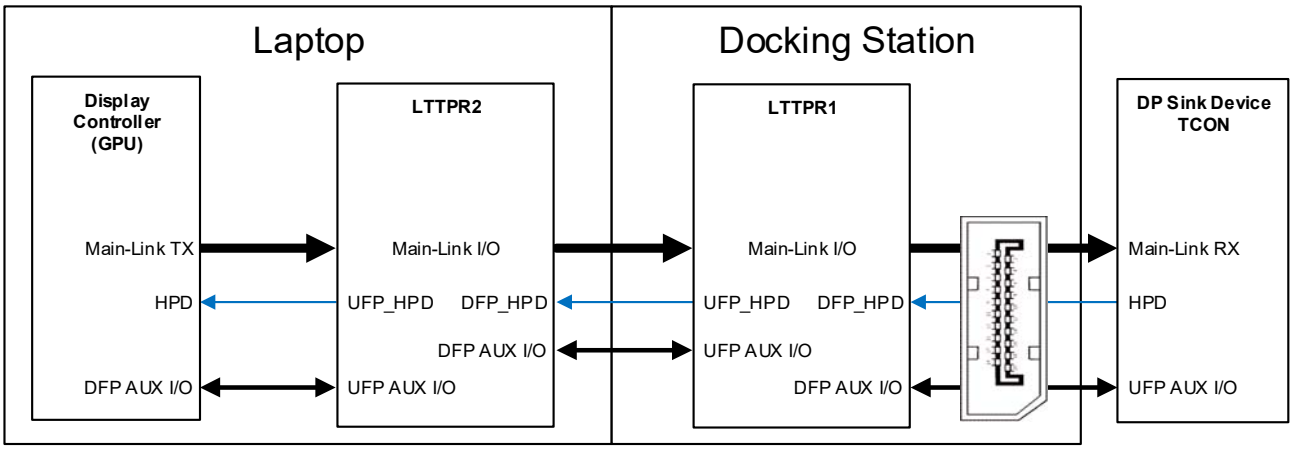


Figure 3-89: Laptop and Docking Station Example

3.6.6.6.1 LTTPR Recognition

Section entirely rewritten for *DP v1.4a*.

When the DPRX is inserted into a docking station, the DPRX shall assert HPD upon DPTX detection. Because both LTTPRs in the Example Use Case implement HPD Pass-through, they shall pass the HPD assertion from their DFP to their UFP, as illustrated in Figure 3-90.

After HPD is propagated from the DPRX to the DPTX, a DP Source device with a DPTX shall read specific registers within the LTTPR field (DPCD Addresses F0000h through F0004h; see Table 2-198) to determine whether any LTTPR(s) are present and if so, how many. This read shall be in the form of a 5-byte native AUX Read transaction. If one or more LTTPRs are present in the link (as indicated by the DPTX receiving a response with a value of 80h, 40h, 20h, 10h, 08h, 04h, 02h, or 01h for the PHY_REPEATER_CNT register (DPCD Address F0002h)), the LTTPR-aware DPTX may place the LTTPR(s) in Non-transparent mode. If there are no LTTPRs present in the link, the DP Source device may reduce its AUX Reply Timeout timer period. (See Section 2.11.2.)

After LTTPR recognition, a DP Source device with a DPTX shall read the DP Sink device with a DPRX's capability by reading DisplayID or legacy EDID and the DPRX's Receiver Capability field (DPCD Addresses 00000h through 000FFh; see Table 2-183). (DisplayID or legacy EDID is **not** mapped to DPCD address space.)

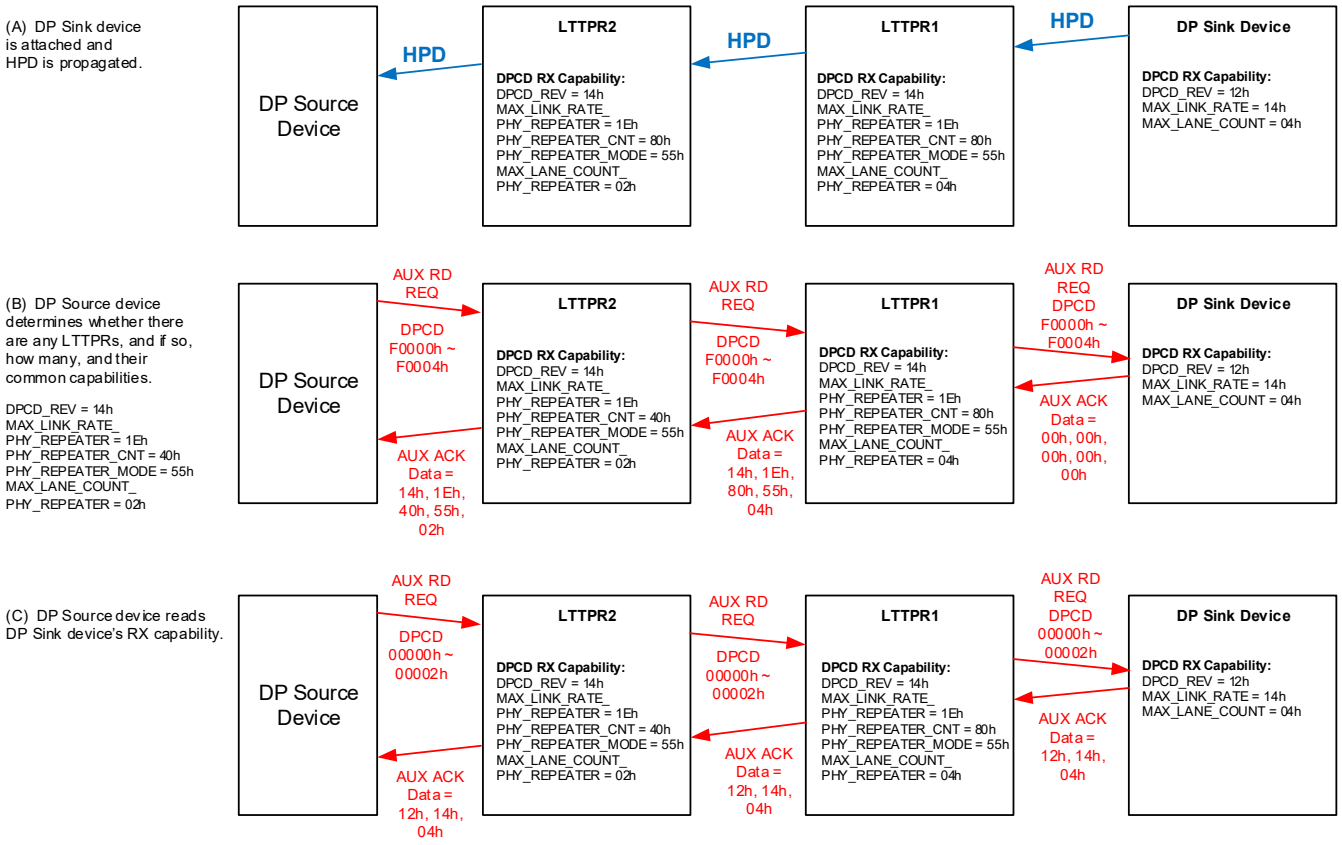


Figure 3-90: LTTPR Recognition

Because the PHY_REPEATER_CNT register is programmed to 40h, the DPTX knows that there are two LTTPRs between itself and the DPRX. The LTTPR with the smallest PHY_REPEATER_CNT value is nearest to the DPTX. The LTTPR with largest PHY_REPEATER_CNT value is furthest from the DPTX but nearest to the DPRX.

The DPTX shall use the link rate returned by the 8b/10b_MAX_LINK_RATE_PHY_REPEATER register and the DPRX's 8b/10b_MAX_LINK_RATE register (DPCD Addresses F0001h and 00001h, respectively) to determine the supported link rates. The DPTX shall use the lane count returned by the MAX_LANE_COUNT_PHY_REPEATER register and the DPRX's MAX_LANE_COUNT register (DPCD Addresses F0004h and 00002h, respectively) to determine the supported lane counts. The DPTX shall then enable Non-transparent mode in all LTTPRs by changing the PHY_REPEATER_MODE register (DPCD Address F0003h).

3.6.6.6.2 Link Training High-level Sequence

New to *DP v1.4a*.

The DPTX shall fully train each link, starting from the link nearest to the DPTX and ending at the link nearest to DPRX. All training patterns are driven by the DPTX. After an LTTPR's UFP completes link training, the training pattern is forwarded to the LTTPR's DFP. Figure 3-91 illustrates the link training high-level sequence and the training-pattern propagation for this Example Use Case.

Figure 3-91 also illustrates that each LANE*x*_CHANNEL_EQ_DONE sequence can be performed with a different training pattern. The DPTX shall use TPS4 to train an LTTPR's UFPs, if the DPTX supports TPS4, and a different training pattern to train the DPRX, based on the DPRX's support. In this Example Use Case, the DPTX uses TPS3 (**bolded** in the figure) to train the DPRX.

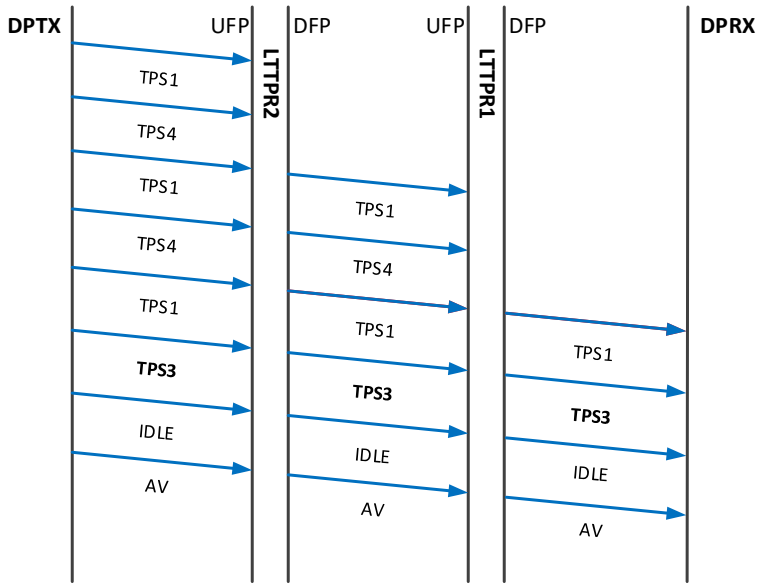


Figure 3-91: Link Training High-level Sequence

3.6.6.6.3 Start of Link Training

New to *DP v1.4a*.

To start link training, the DPTX shall write the DPRX's LINK_BW_SET register and LANE_COUNT_SET field in the LANE_COUNT_SET register (DPCD Address 00100h, and DPCD Address 00101h, bits 4:0, respectively) within the range of the supported parameters (up to HBR2 and two lanes in the Example Use Case). The LTTPRs snoop the DPCD write, as described in Section 3.6.3, which makes the LTTPRs aware of the link parameters that will be established. Discovery and recognition of the supported parameters is described in Section 3.6.6.6.1.

The DPTX shall read the relevant capabilities of each LTTPR before it starts training each link. The DPTX shall read the following registers for an LTTPR's UFP and DFP capabilities:

- **UFP capabilities** – TRAINING_AUX_RD_INTERVAL_PHY_REPEATER*x* register (e.g., DPCD Address F0020h for LTTPR1)
- **DFP capabilities** – TRANSMITTER_CAPABILITY_PHY_REPEATER*x* register (e.g., DPCD Address F0021h for LTTPR1, 8b/10b Link Layer only), as described in Section 3.6.6.1

3.6.6.6.4 LANE*x*_CR_DONE Sequence with LTTPR2

Section entirely rewritten for *DP v1.4a*.

The DPTX shall start the link training LANE*x*_CR_DONE sequence with LTTPR2 by transmitting TPS1 and programming LTTPR2's TRAINING_PATTERN_SET, TRAINING_LANE0_SET, and TRAINING_LANE1_SET registers (DPCD Addresses F0060h, F0061h, and F0062h, respectively).

Typically, the DPTX starts signaling at Voltage Swing Level 0 and Pre-emphasis Level 0. The DPTX may start with non-minimum differential voltage swing and/or non-zero pre-emphasis if the optimal setting is already known.

If the DPTX started signaling with Voltage Swing Level 0 and Pre-emphasis Level 0, program the following LTTPR2 register bits, as follows:

- TRAINING_PATTERN_SET_PHY_REPEATER2 = 01h
- TRAINING_LANE0_SET_PHY_REPEATER2 = 00h
- TRAINING_LANE1_SET_PHY_REPEATER2 = 00h

In Figure 3-92, LTTPR1 passes the AUX reply from the DPRX, unmodified, because the AUX write request targeted LTTPR2 registers instead of LTTPR1 registers. It is LTTPR2's responsibility to modify the DPRX's reply.

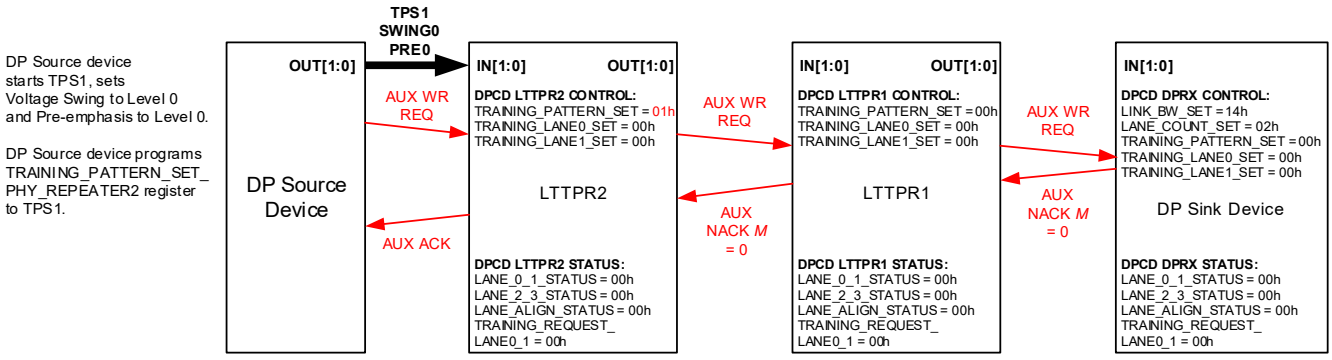


Figure 3-92: Start of LANE*x*_CR_DONE Sequence with LTTPR2

Figure 3-93 illustrates that LTTPR2 has not achieved LANE*x*_CR_DONE for either Lane 0 or 1, and thus requested a change in voltage swing and pre-emphasis levels from the DPTX.
Figure 3-94 illustrates the DPTX adjusting the voltage swing and pre-emphasis levels accordingly.
Figure 3-95 illustrates LTTPR2 achieving LANE*x*_CR_DONE on Lanes 0 and 1.

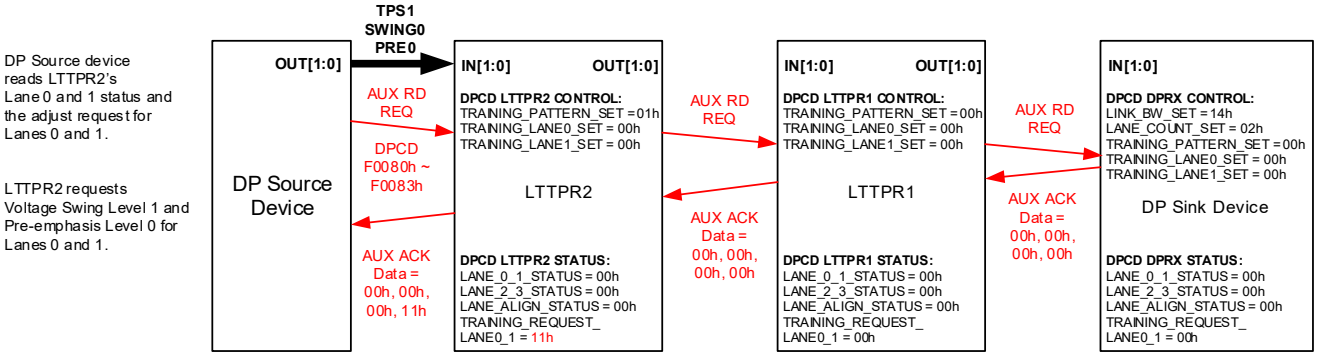


Figure 3-93: Read Status of LTTPR2 Lanes 0 and 1

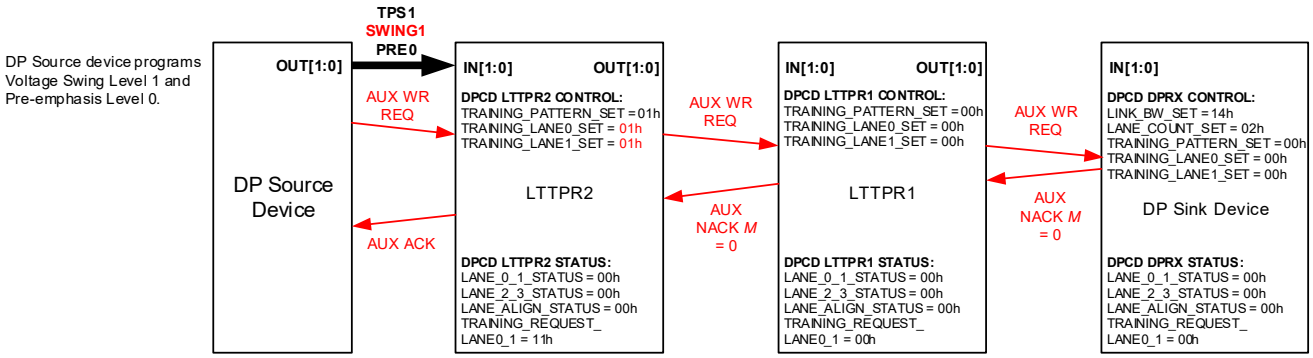


Figure 3-94: DPTX Adjusts Output Voltage Swing and Pre-emphasis

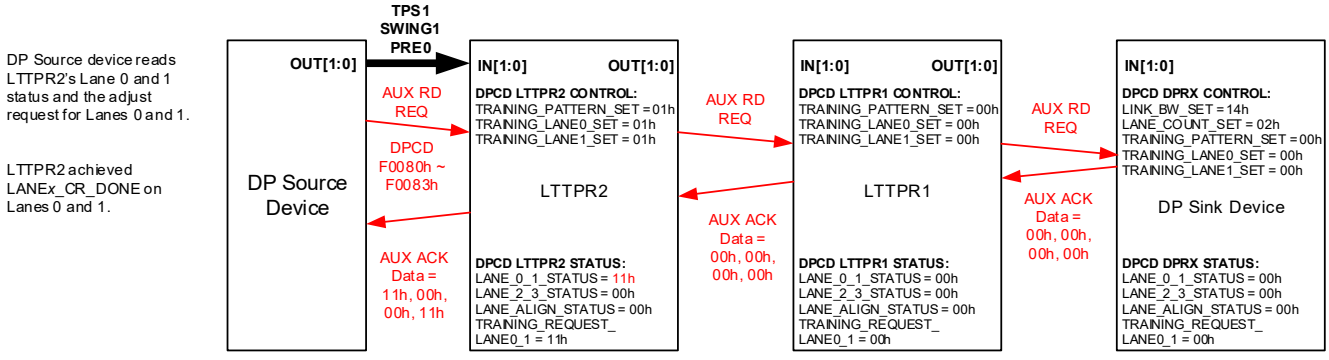


Figure 3-95: LTTPR2 Achieved LANE*x*_CR_DONE

3.6.6.6.5 LANE*x*_CHANNEL_EQ_DONE Sequence with LTTPR2

Section entirely rewritten for *DP v1.4a*.

A DPTX shall transition from the LANE*x*_CR_DONE sequence to the LANE*x*_CHANNEL_EQ_DONE sequence of LTTPR2's link training by changing the training pattern to TPS3 (or TPS4 if supported by the DPTX), and then writing to LTTPR2's TRAINING_PATTERN_SET, TRAINING_LANE0_SET, and TRAINING_LANE1_SET registers (DPCD Addresses F0060h, F0061h, and F0062h, respectively), as illustrated in Figure 3-96.

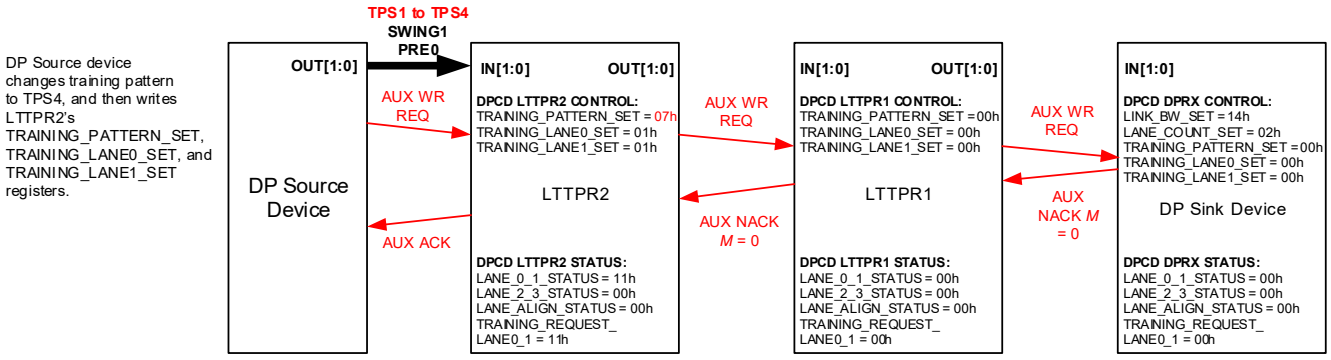


Figure 3-96: DPTX Initiates LANE*x*_CHANNEL_EQ_DONE Sequence with LTTPR2

Figure 3-97 illustrates that LTTPR2 has achieved LANE*x*_CR_DONE, LANE*x*_SYMBOL_LOCKED, LANE*x*_CHANNEL_EQ_DONE, and INTERLANE_ALIGN_DONE.

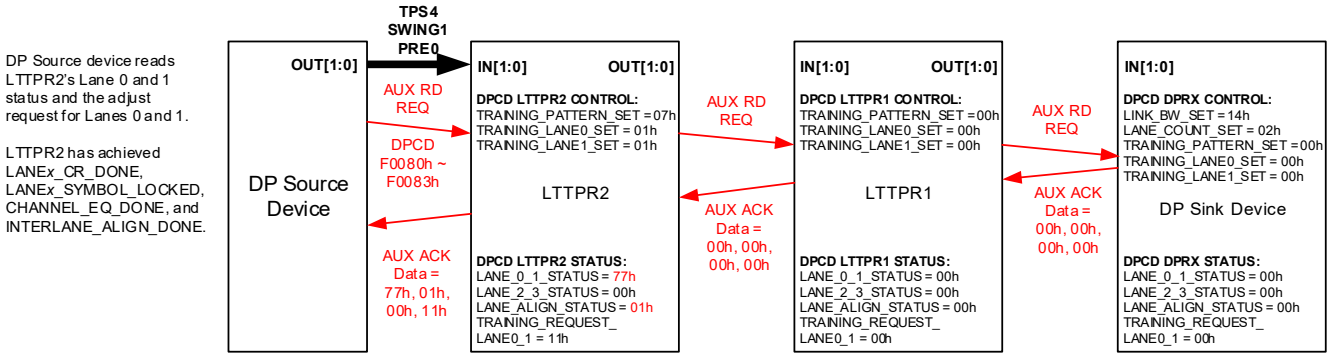


Figure 3-97: LTTPR2 Achieved LANE*x*_CHANNEL_EQ_DONE Sequence

The DPTX shall then end link training to LTTPR2 and start link training to LTTPR1. Figure 3-98 illustrates that the DPTX ends link training by writing 00h to the TRAINING_PATTERN_SET_PHY_REPEATER2 register (DPCD Addresses F0060h). LTTPR2 shall then forward the high-speed training patterns from its UFP to its DFP as a result of ending link training.

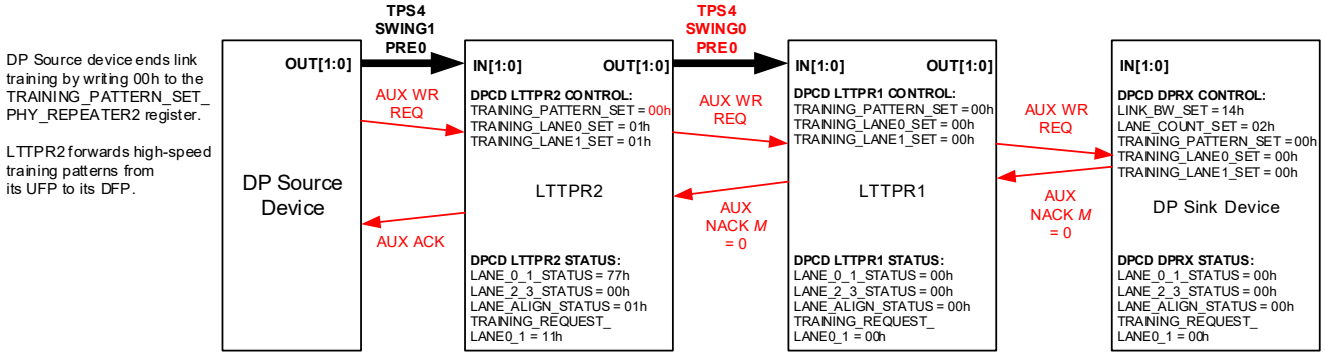


Figure 3-98: DPTX Ends LTTPR2 Link Training

3.6.6.6.6 LANE*x*_CR_DONE Sequence with LTTPR1

Section entirely rewritten for *DP v1.4a*.

The DPTX shall start the link training LANE*x*_CR_DONE sequence with LTTPR1 by transmitting TPS1 and programming the following LTTPR1 registers:

- TRAINING_PATTERN_SET_PHY_REPEATER1 register (DPCD Address F0010h) = 01h
- TRAINING_LANE0_SET_PHY_REPEATER1 register (DPCD Address F0011h) = 00h
- TRAINING_LANE1_SET_PHY_REPEATER1 register (DPCD Address F0012h) = 00h

In the example above, the DPTX started signaling with Voltage Swing Level 0 and Pre-emphasis Level 0.

In Figure 3-99, LTTPR1 modifies the DPRX's reply to an AUX_ACK, while LTTPR2 passes the AUX reply to the DPTX, unmodified.

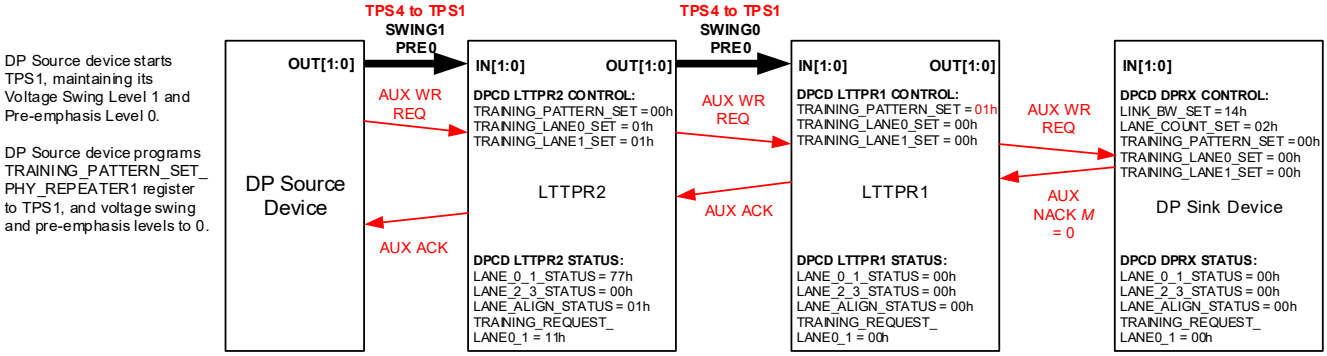


Figure 3-99: Start of LANE*x*_CR_DONE Sequence with LTTPR1

In Figure 3-100, the LTTPR1 LANE*x*_CR_DONE status flags are **not** set and the ADJUST_REQUEST_LANE0_1_PHY_REPEATER1 register (DPCD Address F0033h) indicates that LTTPR1 is requesting Voltage Swing Level 2 and Pre-emphasis Level 0.

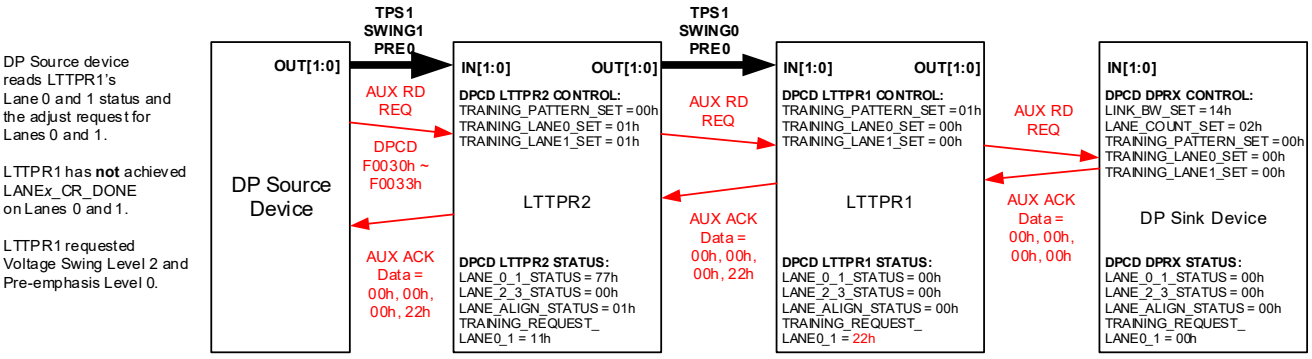


Figure 3-100: Determine LTTPR1's LANE*x*_CR_DONE Status

The DPTX shall write Voltage Swing Level 2 and Pre-emphasis Level 0 to the TRAINING_LANE0_SET_PHY_REPEATER1 and TRAINING_LANE1_SET_PHY_REPEATER1 registers, as illustrated in Figure 3-101. LTTPR2 shall snoop this write and adjust its output levels to Voltage Swing Level 2 and Pre-emphasis Level 0.

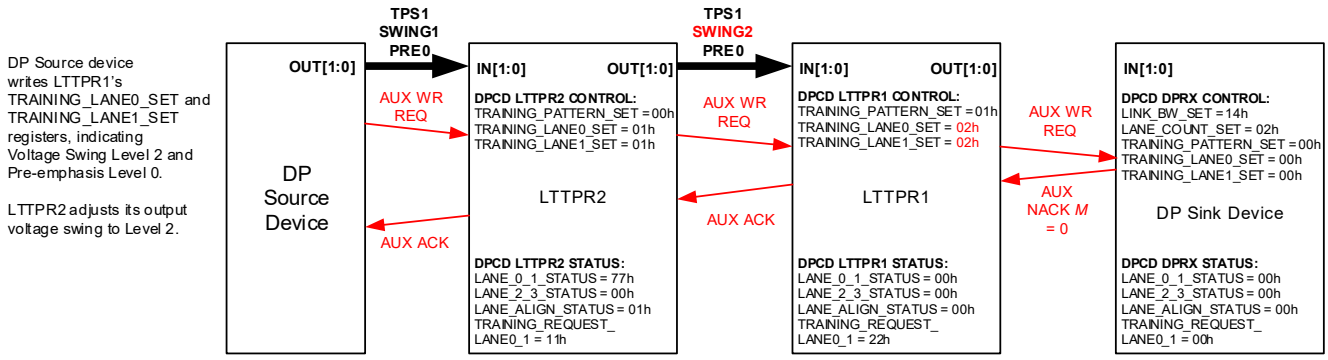


Figure 3-101: LTTPR2 Adjusts Output Voltage Swing and Pre-emphasis

The DPTX voltage swing and pre-emphasis levels always remain fixed. Only LTTPR2 shall adjust its voltage swing and pre-emphasis output levels.

After receiving the acknowledge to the AUX Write request, the DPTX shall then check to determine whether LTTPR1 has achieved LANE*x*_CR_DONE on Lanes 0 and 1. If LTTPR1 achieved LANE*x*_CR_DONE on both lanes, the DPTX shall move to the LANE*x*_CHANNEL_EQ_DONE sequence with LTTPR1.

The DPTX shall transition from TPS1 to TPS4 on a symbol boundary to ensure that LTTPR2's UFP can maintain its LANE*x*_SYMBOL_LOCKED and INTERLANE_ALIGN_DONE.

It is possible that LTTPR1 never achieves LANE*x*_CR_DONE on Lanes 0 and/or 1. This could happen for various reasons, as described in Section 3.5.1.2.2. If LTTPR1 never achieves LANE*x*_CR_DONE on Lanes 0 and/or 1, the DPTX shall follow the LANE*x*_CR_DONE sequence as illustrated in Figure 3-12 on page 745, changing the link rate and/or lane count, and then starting the LANE*x*_CR_DONE sequence again, but with LTTPR2. All LTTPRs shall snoop AUX writes to the LINK_BW_SET register and LANE_COUNT_SET field in the LANE_COUNT_SET register (DPCD Address 00100h, and DPCD Address 00101h, bits 4:0, respectively), and then prepare for a new link-training process.

3.6.6.6.7 LANE*x*_CHANNEL_EQ_DONE Sequence with LTTPR1

Section entirely rewritten for *DP v1.4a*.

The DPTX shall perform LTTPR1's LANE*x*_CHANNEL_EQ_DONE sequence similar to LTTPR2's LANE*x*_CHANNEL_EQ_DONE sequence, as described in Section 3.6.6.6.5. Figure 3-102 illustrates that LTTPR1 has achieved LANE*x*_CR_DONE, LANE*x*_SYMBOL_LOCKED, LANE*x*_CHANNEL_EQ_DONE, and INTERLANE_ALIGN_DONE.

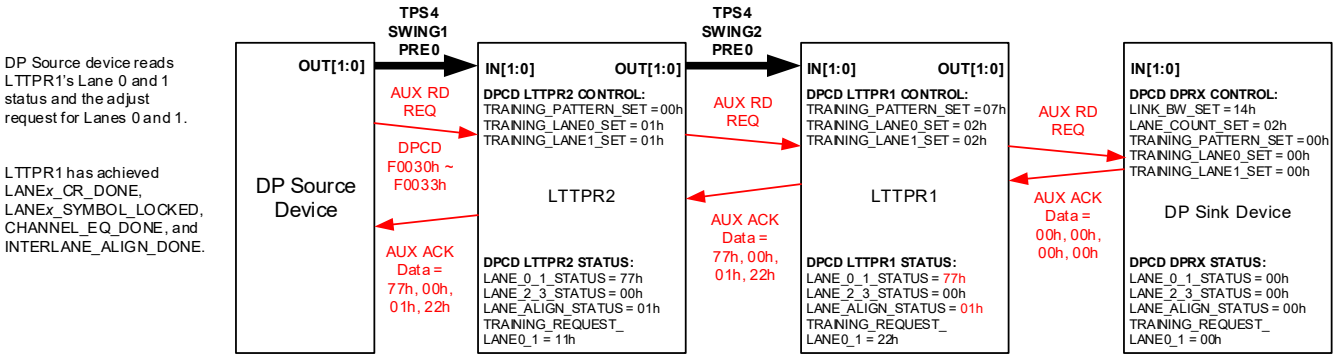


Figure 3-102: LTTPR1 Achieved LANE*x*_CHANNEL_EQ_DONE Sequence

Figure 3-103 illustrates that the DPTX ends link training by writing 00h to the TRAINING_PATTERN_SET_PHY_REPEATER1 register (DPCD Address F0010h).

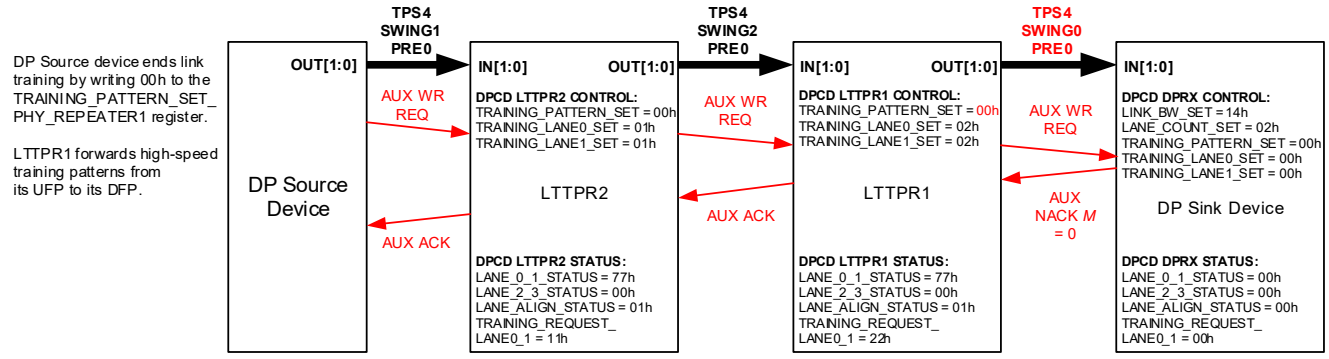


Figure 3-103: End LTTPR1 Link Training

It is possible that LTTPR1 never completes the LANE*x*_CHANNEL_EQ_DONE sequence. This could happen for various reasons, as described in Section 3.5.1.2.3. If LTTPR1 never completes the LANE*x*_CHANNEL_EQ_DONE sequence, the DPTX shall follow the LANE*x*_CHANNEL_EQ_DONE sequence as illustrated in Figure 3-13 on page 750, changing the link rate and/or lane count, and then starting the LANE*x*_CR_DONE sequence, but with LTTPR2. All LTTPRs shall snoop AUX writes to the LINK_BW_SET register and LANE_COUNT_SET field in the LANE_COUNT_SET register (DPCD Address 00100h, and DPCD Address 00101h, bits 4:0, respectively), and then prepare for a new link-training process.

3.6.6.6.8 LANE*x*_CR_DONE Sequence with DPRX

Updated in *DP v1.4a*.

The DPTX shall write to the DPRX's TRAINING_PATTERN_SET, TRAINING_LANE0_SET, and TRAINING_LANE1_SET registers (DPCD Addresses 00102h through 00104h, respectively) to notify the DPRX that the link training LANE*x*_CR_DONE sequence has started. The LTTPR nearest to the DPRX (i.e., LTTPR1) shall snoop writes to the DPRX's link training-related DPCD registers. LTTPR1 shall adjust its output based on an AUX write request to the DPRX's TRAINING_LANE0_SET, and TRAINING_LANE1_SET. In the example illustrated in Figure 3-104, the DPTX began with a Voltage Swing Level 0 and Pre-emphasis Level 0.

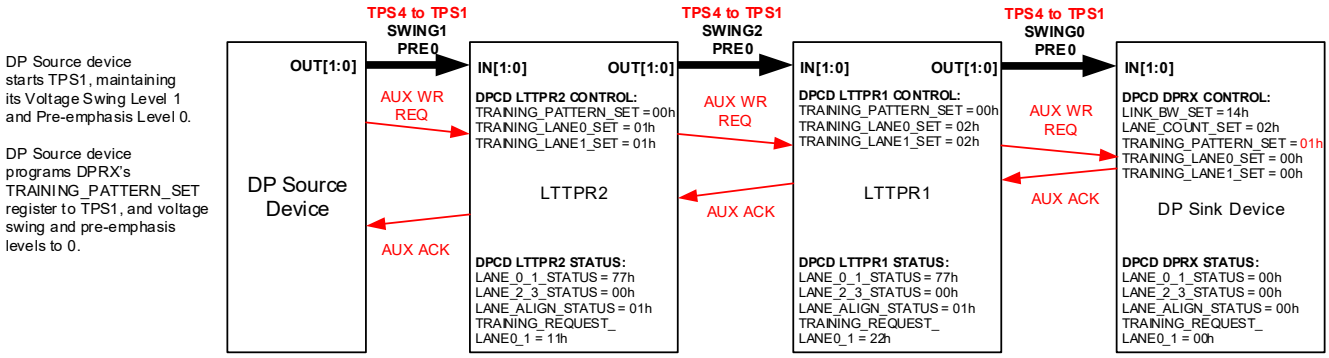


Figure 3-104: Start of LANE*x*_CR_DONE Sequence with DPRX

In Figure 3-105, the DPTX determines that the DPRX has achieved LANE*x*_CR_DONE. After the DPRX achieves LANE*x*_CR_DONE, the DPTX shall begin the DPRX's link training LANE*x*_CHANNEL_EQ_DONE sequence.

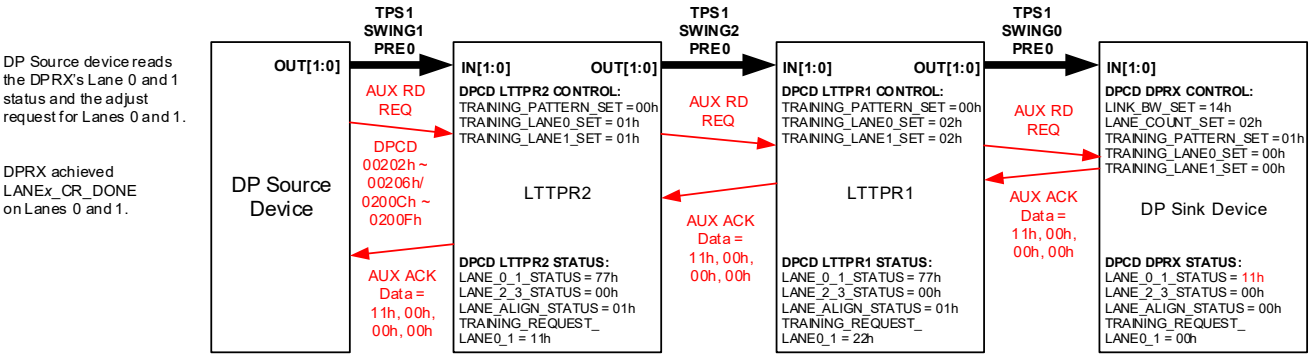


Figure 3-105: DPRX Achieved LANE*x*_CR_DONE

3.6.6.6.9 LANE*x*_CHANNEL_EQ_DONE Sequence with DPRX

Section entirely rewritten for *DP v1.4a*.

The DPTX shall write to the DPRX's TRAINING_PATTERN_SET, TRAINING_LANE0_SET, and TRAINING_LANE1_SET registers (DPCD Addresses 00102h through 00104h, respectively) to notify the DPRX of the start of the link training LANE*x*_CHANNEL_EQ_DONE sequence, as illustrated in Figure 3-106.

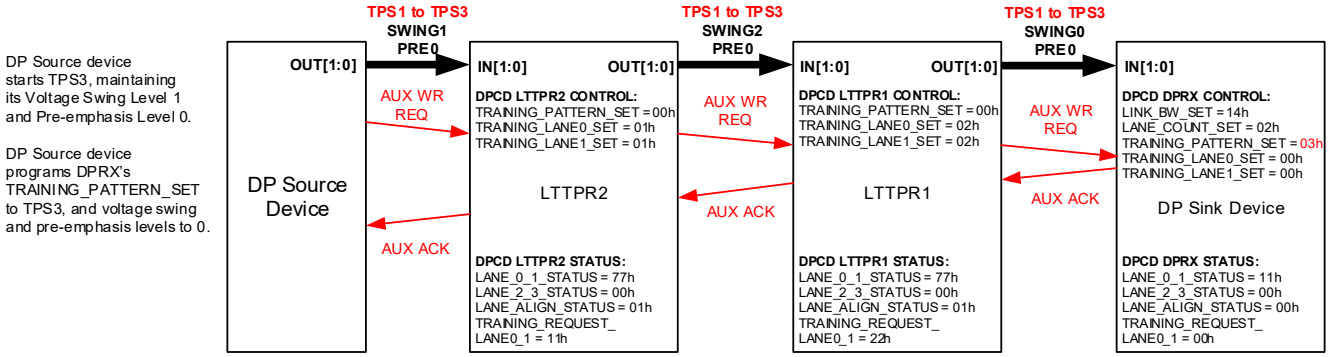


Figure 3-106: Start of LANE*x*_CHANNEL_EQ_DONE Sequence with DPRX

In Figure 3-107, the DPTX reads the DPRX's lane status and adjust request DPCD registers (DPCD Addresses 00202h through 00206h, and DPCD Addresses 0200Ch through 0200Fh (there is not a 0200*x*h register that is identical to 00206h)).

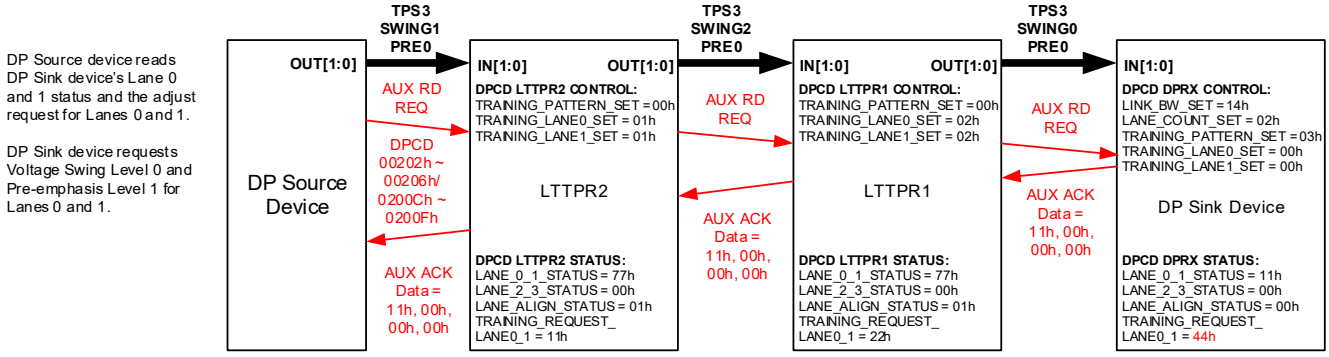


Figure 3-107: Determine DPRX's LANE*x*_CHANNEL_EQ_DONE Sequence Status

The DPTX writes 01b to the VOLTAGE_SWING_SET field in the DPRX's TRAINING_LANE*x*_SET registers for Lanes 0 and 1 (DPCD Addresses 00103h and 00104h, bits 1:0, respectively) to indicate an increase to Pre-emphasis Level 1. LTTPR1 monitors this write and increases the pre-emphasis level.

Figure 3-108 illustrates that the DPRX has achieved LANE*x*_CR_DONE, LANE*x*_SYMBOL_LOCKED, LANE*x*_CHANNEL_EQ_DONE, and INTERLANE_ALIGN_DONE. The DPTX can now end link training and start transmitting an Idle Pattern.

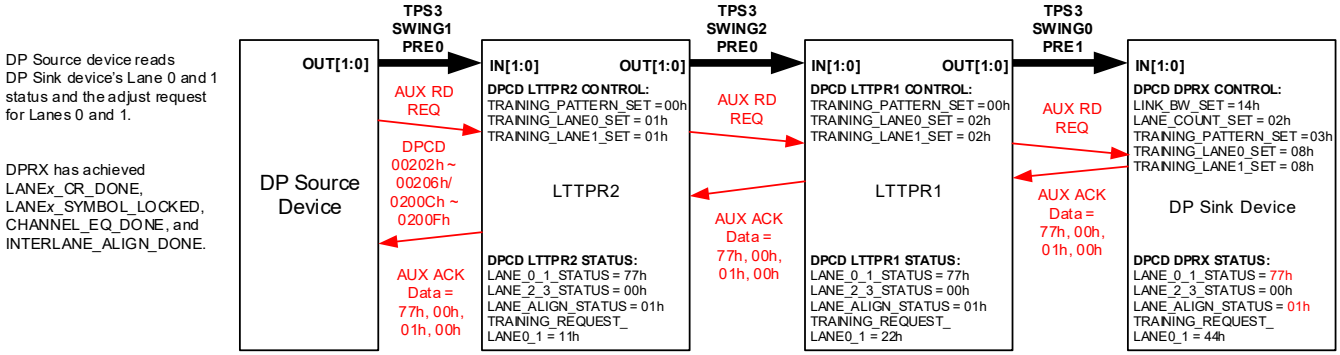


Figure 3-108: DPRX Achieved LANE*x*_CHANNEL_EQ_DONE Sequence

3.6.6.6.10 End of Link Training

Section entirely rewritten for *DP v1.4a*.

Figure 3-109 illustrates the end of the link training processes. The DPTX ends link training by writing 00h to the DPRX's TRAINING_PATTERN_SET register (DPCD Address 00102h). All the LTTPRs continuously monitor writes to this register. Whenever the 8b/10b_TRAINING_PATTERN_SELECT field in the TRAINING_PATTERN_SET register (DPCD Address 00102h, bits 3:0) transitions to a 0h value, the LTTPRs know that link training is complete. The DPTX changes the training pattern to the Idle Pattern.

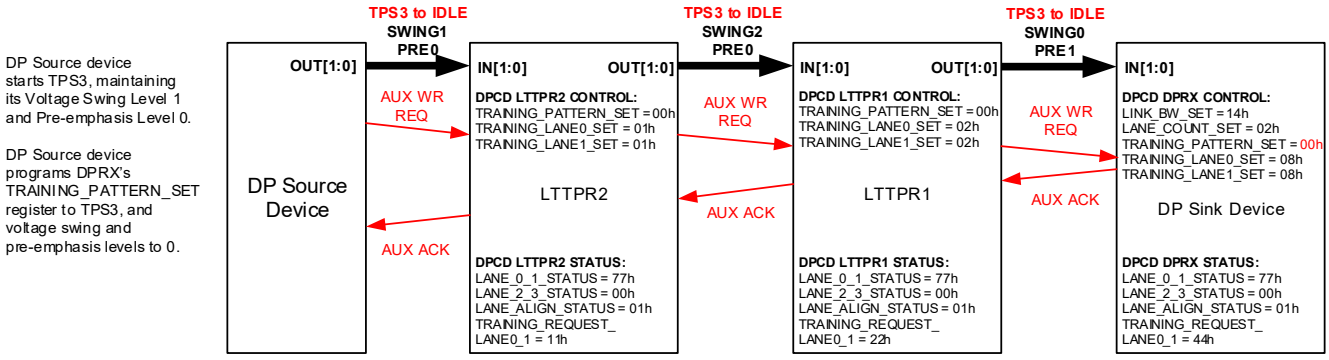


Figure 3-109: End Link Training

3.6.6.6.11 POST_LT_ADJ_REQ Sequence with DPRX

New to *DP v1.4a*.

The POST_LT_ADJ_REQ sequence, as described in Section 3.5.1.2.5, may be initiated between the DPTX, DPRX, and LTTPRs after link training is complete. The LTTPR nearest to the DPRX (i.e., LTTPR1) shall snoop writes to the DPRX's TRAINING_LANE*x*_SET register(s) (DPCD Addresses 00103h through 00106h), and then adjust its transmitter's voltage swing and pre-emphasis levels accordingly.

3.6.7 Transition to Transparent Mode

New to *DP v1.4a*.

An LTTPR shall reset its internal state and configure itself to Transparent mode when any of the following conditions exist:

- Power is cycling
- Disconnection of an upstream device is detected
  - An LTTPR shall implement the detection of both an upstream device connection and a powered upstream device connection
- PHY_REPEATER_MODE register (DPCD Address F0003h) transitions from Non-transparent mode to Transparent mode (value of AAh to 55h, respectively)
  - If a DP Source device programs the PHY_REPEATER_MODE register to Transparent mode (value of 55h), the DP Source device shall perform link training before transmitting active video

3.6.8 Dual Mode Mandates

Dual Mode adapters may be supported. However, if the LTTPR supports Dual Mode adapters being connected to their DFP, the LTTPR shall meet the mandates outlined in this section.

1 CONFIG1 shall be connected to each LTTPR between the Dual Mode adapter and DPTX.

   a LTTPR shall use CONFIG1 to know if downstream traffic is standard DP or DP++ (TMDS over DisplayPort).

2 DDC communication (whether in the form of I^2C-over-AUX transaction syntax or in 3.3V I^2C) between a DPTX and Dual Mode adapter shall not be negatively impacted.

3 LTTPR output electrical levels shall comply with *Dual-Mode Standard* for a Dual Mode DPTX.

4 LTTPR shall be able to accept a 25 to 300MHz TMDS clock as per *Dual-Mode Standard* and pass-through to its DFP.

5 LTTPR shall not implement the Dual Mode Adapter ID unless it implements the AC-coupling to DC-coupling level shift on its output port.

3.6.9 LTTPR Electrical Specification Mandates

3.6.9.1 LTTPR DPTX_PHY Electrical Compliance

An LTTPR that is connected to a DP connector shall meet the electrical mandates defined in Section 3.5.4.

Before any TX electrical testing can be performed, the link between a DPTX and DPRX (in this case, a piece of test equipment), including all LTTPRs within the path, shall be trained as defined in this Standard. After the link is trained to a specific link rate, the DPTX can change the LTTPR's output levels (TX voltage swing and pre-emphasis) by writing to the DPRX's TRAINING_LANE*x*_SET register(s) (DPCD Addresses 00103h through 00106h). The link between the DPTX and DPRX shall be retrained when the TEST_LANE_COUNT or TEST_LINK_RATE register (DPCD Address 00220h or 00219h, respectively) value changes.

Any test pattern that is requested by test equipment through the LINK_QUAL_PATTERN_SEL field in the LINK_QUAL_PATTERN_SELECT register (DPCD Address 00248h, bits 6:0) for compliance test shall be generated by the DPTX. The DPTX shall declare the test pattern by writing to the Lane's LINK_QUAL_PATTERN_SET field in the LINK_QUAL_LANE*x*_SET register(s) (DPCD Address(es) 0010Bh through 0010Eh, bits 6:0).

3.6.9.2 LTTPR DPRX_PHY Electrical Compliance

An LTTPR that is connected to a DP connector shall meet the electrical mandates defined in Section 3.5.4.

3.6.10 LTTPR Power-saving State

New to *DP v1.4a*.

This section describes the LTTPR Main-Link and AUX_CH behavior in a power-saving state.

3.6.10.1 Entering a Power-saving State

After snooping an LTTPR's AUX_ACK for a write of 010b or 101b to the SET_POWER_STATE field in the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h, bits 2:0), the LTTPR may enter a power-saving state. In a power-saving state, the LTTPR may disable Main-Link receivers of their UFPs and Main-Link transmitters of their DFPs.

3.6.10.2 Exiting a Power-saving State

A DP Source device initiates exit from the SLEEP power state by writing 001b to the SET_POWER_STATE field in a DP Sink device's SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h, bits 2:0), as described in Section 5.1.5 and Section 5.2.5.
An LTTPR's UFP shall monitor the presence of a differential signal on the AUX_CH. If the LTTPR detects AUX_CH activity, the LTTPR shall immediately exit the power-saving state, thereby ensuring that no AUX transactions are lost. Immediately after this AUX write transaction occurs, the LTTPR shall be ready for the DP Source device to initiate link training.

3.6.10.3 Extended Wake Timeout from a Power-saving State

Updated in *DP v2.0*.

An LTTPR can request an extended timeout for waking from a power-saving state. The LTTPR shall immediately wakeup, as described in Section 3.6.10.2, when either of the following conditions exist:

- DP Source device does **not** grant the extended timeout request
- Entrance to a power-saving state resulted from writing 101b to the SET_POWER_STATE field in the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h, bits 2:0)

When an LTTPR is in Transparent mode, the extended timeout request is achieved through the EXTENDED_DPRX_SLEEP_WAKE_TIMEOUT_REQUEST register (DPCD Address 02211h). When a DPTX issues an AUX read transaction to this address, the LTTPR may replace the AUX reply transaction data with the value that corresponds to its own wake timeout if the value is greater than the downstream DPRX's reply. The extended timeout grant is achieved by the DPTX writing 1 to the DPRX_SLEEP_WAKE_TIMEOUT_PERIOD_GRANTED bit in the EXTENDED_DPRX_SLEEP_WAKE_TIMEOUT_GRANT register (DPCD Address 00119h, bit 0).

When an LTTPR is in Non-transparent mode, the extended timeout request is achieved by reading the PHY_REPEATER_EXTENDED_WAKE_TIMEOUT register (DPCD Address F0005h), where each LTTPR may request extended wake, in 10-ms increments, in the register's EXTENDED_WAKE_TIMEOUT_REQUEST field (bits 6:0). Each LTTPR may request up to 50ms for extended wake timeout. The extended timeout grant is achieved by writing 1 to the register's EXTENDED_WAKE_TIMEOUT_GRANT bit (bit 7).

Because there are multiple devices to wake from a power-saving state and the SLEEP power state, a DP Source device shall constantly retry the AUX transaction, up to the extended timeout being requested and granted for the LTTPRs and DP Sink device.

4 Mechanical Specifications

This section describes the mechanical specifications of a DP link. Cable assembly specification for external connection and connector specification are covered in this section. Applications requiring a larger or longer box-to-box application space than supported by a passive cable assembly as defined in this section may be supported by the use of an active Hybrid device or any other such device as provided for under Section 2.1.4. The interfaces of these devices shall meet the interface requirements of a Source and Sink device.

4.1 Cable-Connector Assembly Specifications (for Box-to-box)

The cable assembly specification is divided into two categories that reflect the high bit rates (10, 8.1, 5.4, and 2.7Gbps/lane (UHBR10, HBR3, HBR2, and HBR, respectively) and low bit rate (1.62Gbps/lane; RBR):

- High bit rate specification generally has higher performance electrical requirements and is usually represented by one or more of the following – shorter lengths, larger wire gauges, and/or lower dielectric loss insulation materials
- Low bit rate specification generally has lower performance electrical requirements and is usually represented by one or more of the following – longer lengths, smaller wire gauges, and/or higher dielectric loss insulation materials

Among the cable-connector assembly parameters, insertion loss (IL), return loss (RL), skew (both intra- and inter-pair), and Near-End Noise (NEN) differ between the high and low bit rate specifications. The power sum equal level far-end noise (PSELFEN) parameter applies to the high bit rate cable assembly specification only.

Both categories represent the box-to-box application space sometimes referred to as external/ desktop and consumer electronics (CE).

The embedded cable application space, which is characterized by its inaccessibility to the user and is sometimes referred to as internal/mobile, is not explicitly specified here. Instead, the system integrator shall meet the EYE mask requirements at the receiver pins by making appropriate trade-offs between circuit trace performance and cabling performance.

In general the high bit rate and low bit rate electrical specification presented below still apply to the internal/mobile cable assemblies given the same PCB traces at both ends of the channel except that the physical dimensions are much smaller.

The cable-connector assembly is tested with test fixtures that have receptacle connectors, as described in *PHY CTS*.

4.1.1 Cable-Connector Assembly Definition

A DP Cable Assembly is composed of two plug-type connectors terminating both ends of a bulk cable.

The plug on either end may be a full-size DP plug or an mDP plug.

Table 4-1 lists the supported cable assembly types.

Table 4-1: Supported Cable Assembly Types

Type	Description	Illustrated In
C1	Cable Assembly with a full-size DP plug on each end.	Figure 4-1
C2	Cable Assembly with an mDP plug on one end and a full-size DP plug on the other end.	Figure 4-2
C3	Cable Assembly with an mDP plug on each end.	Figure 4-3

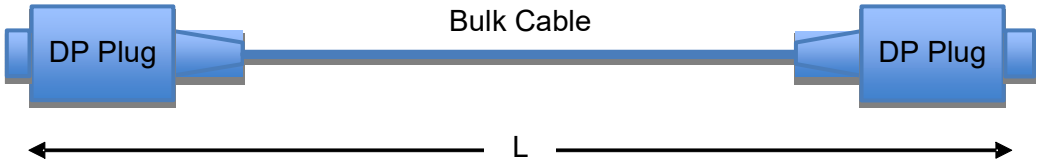


Figure 4-1: Type C1 Cable Assembly

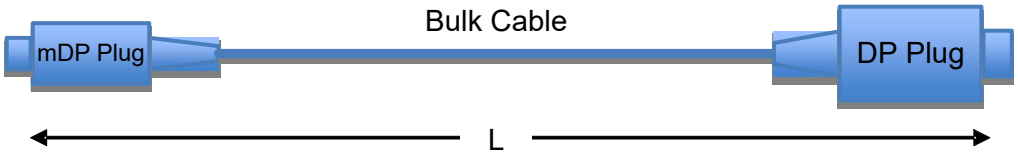


Figure 4-2: Type C2 Cable Assembly

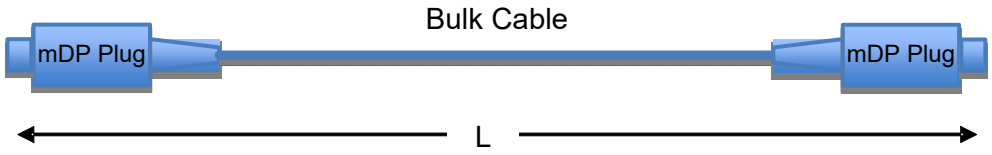


Figure 4-3: Type C3 Cable Assembly

A DP Connector resizing adapter is composed of a plug-type connector terminating one end of a bulk cable and a receptacle type connector terminating the other end of the same cable.

Table 4-2 lists the supported resizing adapter assembly types.

Table 4-2: Supported Resizing Adapter Types

Type	Description	Illustrated In
A1	Resizing adapter with an mDP plug on one end and a full-size DP receptacle on the other end.	Figure 4-4
A2	Resizing adapter with a full-size DP plug on one end and an mDP receptacle on the other end.	Figure 4-5

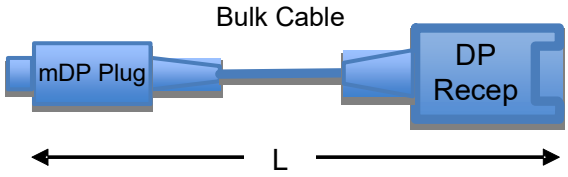


Figure 4-4: Type A1 Resizing Adapter

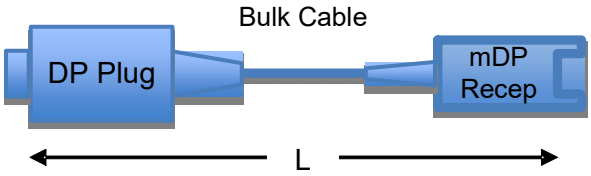


Figure 4-5: Type A2 Resizing Adapter

In addition, a Sink device may have a permanently attached cable with a full-size DP plug or a permanently attached cable with an mDP plug.

A DP extension cable is designed specifically to be used in conjunction with displays (or adapters) with a permanently attached cable with an mDP plug.

Table 4-3 lists the supported extension cable type.

Table 4-3: Supported Extension Cable Type

Type	Description	Illustrated In
E1	Cable assembly with an mDP plug on one end and an mDP receptacle on the other end.	Figure 4-6

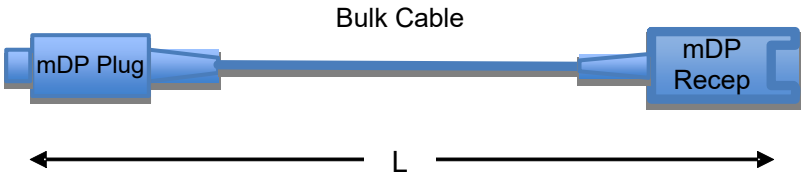


Figure 4-6: Type E1 Extension Cable

The following cable assembly and resizing adapter configurations are supported for all bit rates:

- Upstream Device (TP2) → Cable Assembly Type C1 → Downstream Device (TP3)
- Upstream Device (TP2) → Cable Assembly Type C2 → Downstream Device (TP3)
- Upstream Device (TP2) → Cable Assembly Type C3 → Downstream Device (TP3)
- Upstream Device (TP2) → Full-size DP plug permanently attached to Downstream Device
- Upstream Device (TP2) → mDP plug permanently attached to Downstream Device
- Upstream Device (TP2) → Resizing Adapter Type A1 → Full-size DisplayPort plug permanently attached to Downstream Device
- Upstream Device (TP2) → Resizing Adapter Type A2 → mDP plug permanently attached to Downstream Device
- Upstream Device (TP2) → Extension Cable Type E1 → mDP plug permanently attached to Downstream Device

The following configurations of cable assemblies and resizing adapters are supported for HBR and RBR only:

- Upstream Device (TP2) → Resizing Adapter Type A1 → Cable Assembly Type C1 → Downstream Device (TP3)
- Upstream Device (TP2) → Resizing Adapter Type A2 → Cable Assembly Type C3 → Downstream Device (TP3)

In addition to the above cable assembly types, active versions of Types C1, C2, C3, and Type E1 cable assemblies are supported, indicated as C1A, C2A, C3A, and E1A, respectively. See Section 5.13.3 for active cable assembly details.

4.1.1.1 Cable Construction Guideline for EMI Reduction (Informative)

The following recommendations for the construction of DP cable assemblies should be followed to prevent EMI issues:

- Intra-pair skew for differential pairs in the cable assembly should be made as small as possible and should meet the defined limits defined by the cable assembly electrical specification.
- Termination of the cable shielding to the connector shield should cover a full 360^{o} around the cable and be of low impedance.
- Shielding between the device chassis, DP receptacle shield, DP plug shield, and cable shielding should form a unified low impedance link to maximize the efficiency of the shielding and minimize EMI. To facilitate this, multiple grounding points and contact points should be used between shield parts.
- As a general rule, unnecessary apertures in the shields may cause leakage. Gaps between shielding components should be eliminated. The shell should cover as much of the connector as possible to yield the maximum EMI protection of the signal pins.
- Bulk cable's shielding construction should follow general high-speed practices of including both foil and braid shielding materials in its construction. The foil layer should be an Aluminum/Mylar foil wrap (spiral or longitudinal) with a minimum 20% overlap, and the conductive braid should have a minimum 75% coverage over the inner foil layer to ensure effective EMI shielding.

4.1.2 Bulk Cable Type

The bulk cable shall be chosen to meet or exceed all the electrical and mechanical requirements described below. A reference construction is depicted in Figure 4-7.

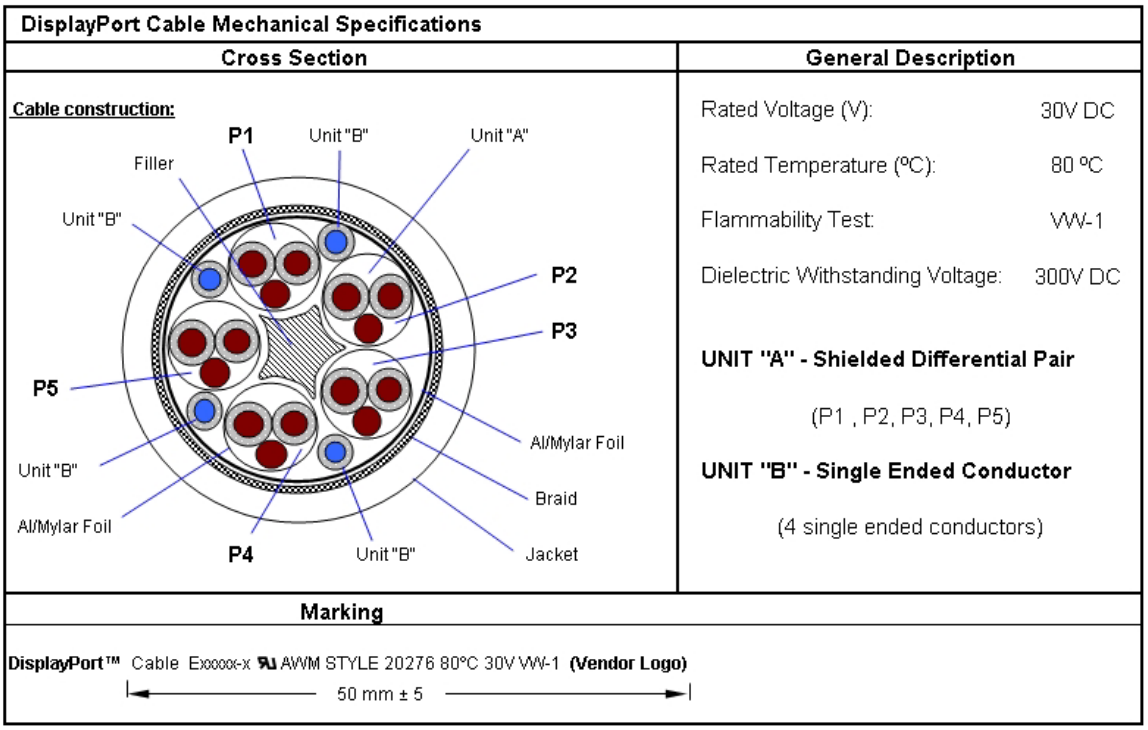


Figure 4-7: Bulk Cable Construction (Informative – for Reference Only)

The following is the description of the reference bulk cable construction. This description is for reference only.

- Overall shielded (braid) structure coated with jacket above;
- **Unit "A"** – P1-P5 'STP' or 'Twinax' #30 AWG insulated stranded conductors, with #30 AWG drain conductor for use in Cable Assembly Type C1 and displays with permanently attached cables with full-size DisplayPort connectors, and #36 or #38 AWG insulated stranded conductors, with #36 or #38 AWG drain conductor for use in all other Cable Assemblies, Resizing Adapters and Extension Cables (for use for Main-Link and AUX connections);
- **Unit "B"** – Unshielded, #30 AWG single insulated stranded conductors (for GND). #30 - #8 AWG single insulated stranded conductor (for use for CONFIG1, CONFIG2 and HPD connections).

Examples of differences:

- Wire gauge selection is implementation-specific, provided that all appropriate electrical cable specification conditions exist.
- A cable permanently attached to a DP device may have fewer than four Main-Link Lanes.
- Downstream devices with permanently attached cables may have an extra #24 to #28 AWG single insulated stranded conductor for power.
- Resizing adapters shall have a #30 to #36 AWG single insulated stranded conductor for power.
- Extension cables shall carry all four lanes and include a #24 AWG single insulated stranded conductor for power.

4.1.3 Impedance Profile

The impedance profile is intended to provide confidence in the system and connector design. The return loss specification described later in this section provides the limit on the electrical performance resulting from impedance excursions and mismatches.

The impedance specification is defined in the time domain. The impedance profile shall be measured using a controlled impedance fixture and TDR with a differential sampling head. The fixture rise time shall be 50ps (20 to 80%) or faster while the readout of measurement shall be filtered to tr = 130ps (20 to 80%). Two impedance profiles are defined:

- One for when the impedance is measured through a full-size DP connector
- One for when the impedance is measured through an mDP Connector

Impedance values attributed in part or in whole to the connector on the Cable Assembly under test shall conform to those listed in Table 4-4 or Table 4-5, as appropriate. Figure 4-8 and Figure 4-9 illustrate examples of measured data.

The Impedance Profile as it applies to the test fixture is Informative. The test fixture requirements are defined in *PHY CTS*.

4.1.3.1 Impedance Profile through a DP Connector

Table 4-4: Impedance Profile Values for Cable Assembly with DP Connector

Segment	Differential Impedance Value	Maximum Tolerance	Comment
Fixture	100Ω	±10%	Fixture should have trace lengths of no more than 50mm (2 inches)
Connector		±10%	
Wire Management		±10%	Transition from ±10% to ±5% shall have a slope of 5Ω / 80ps
Cable		±5%	

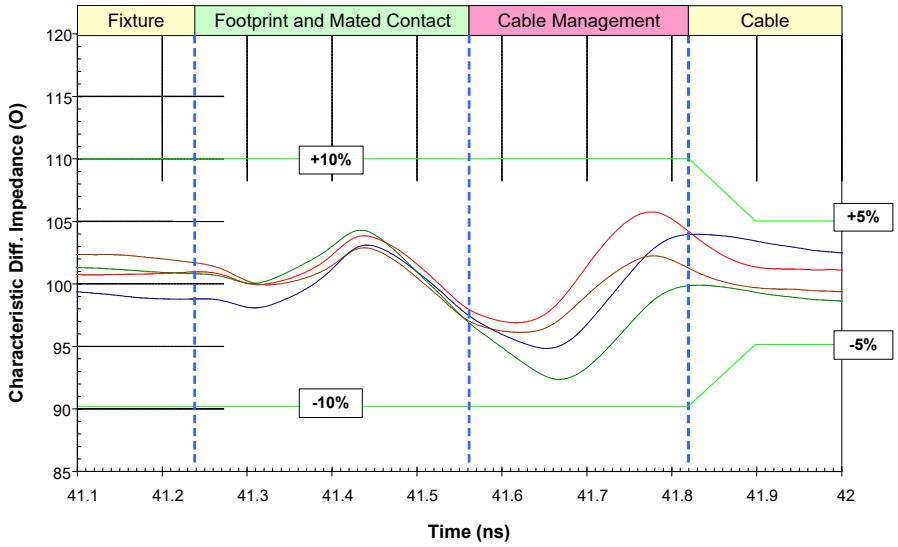


Figure 4-8: DP Connector Differential Impedance Profile Measurement Data Example

4.1.3.2 Impedance Profile through an mDP Connector

Table 4-5: Impedance Profile Values for Cable Assembly with mDP Connector

Segment	Differential Impedance Value	Maximum Tolerance	Comment
Fixture	100Ω	±10%	Fixture should have traces lengths of no more than 50mm (2 inches)
Connector	100Ω	±15%	Exception window peak duration of 200ps, Transition from ±15% to ±5% shall have a slope of 10Ω / 200ps
Wire Management	100Ω	±10%	
Cable	100Ω	±5%	

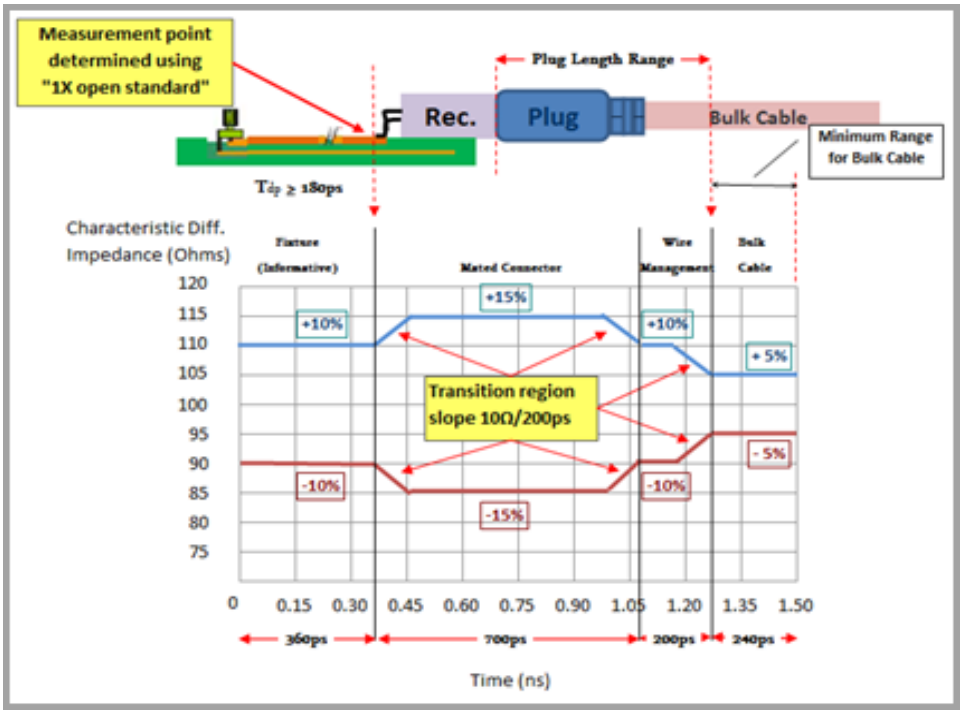


Figure 4-9: mDP Connector Differential Impedance Profile Measurement Data Example

4.1.4 Insertion Loss and Return Loss

Insertion Loss and Return Loss specified in this section are the mixed mode S-parameters known as SDD21 and SDD11, respectively. Unlike Single-Ended case, SDDij refers to differential stimulus and differential response, as illustrated in Table 4-6 by the matrix of all mixed modes in differential case.

Table 4-6: Mixed Mode Differential/Common Relations of S-parameters

Response	Stimulus			
	Differential		Common	
Differential	SDD11	SDD12	SDC11	SDC12
	SDD21	SDD22	SDC21	SDC22
Common	SCD11	SCD12	SCC11	SCC12
	SCD21	SCD22	SCC21	SCC22

4.1.5 High Bit Rate Cable-Connector Assembly Specification

4.1.5.1 Insertion Loss and Return Loss

The following equations represent the reference lines that limit the Insertion Loss and Return Loss measured results. Insertion loss limits are provided for Cable Assembly types C1, C2, and C3, for Resizing Adapters and for Extension cables. Return loss limits are provided for cable assemblies and resizing adapters when measured through the full-size DP connector and when measured through the mDP connector.

4.1.5.1.1 Insertion Loss – Lower Limit for High Bit Rate Cable Assembly Types C1, C2, and C3

$$IL_{\min.}[dB] = \begin{cases} -8.7 \times \sqrt{\frac{f}{f_0}} - 0.072; & 0.1 < f \le \frac{f_0}{3} \\ 5.68\sqrt{f} - 5.3 * f - 6.52; & \frac{f_0}{3} < f \le 8.1 \end{cases}$$

where:

- f is given in GHz
- $f_0 = 1.35GHz$

The chart presented in Figure 4-10 illustrates the above equation's Insertion Loss, and shall be referenced as the lower limit. The cable assembly measured results shall comply with this limit.

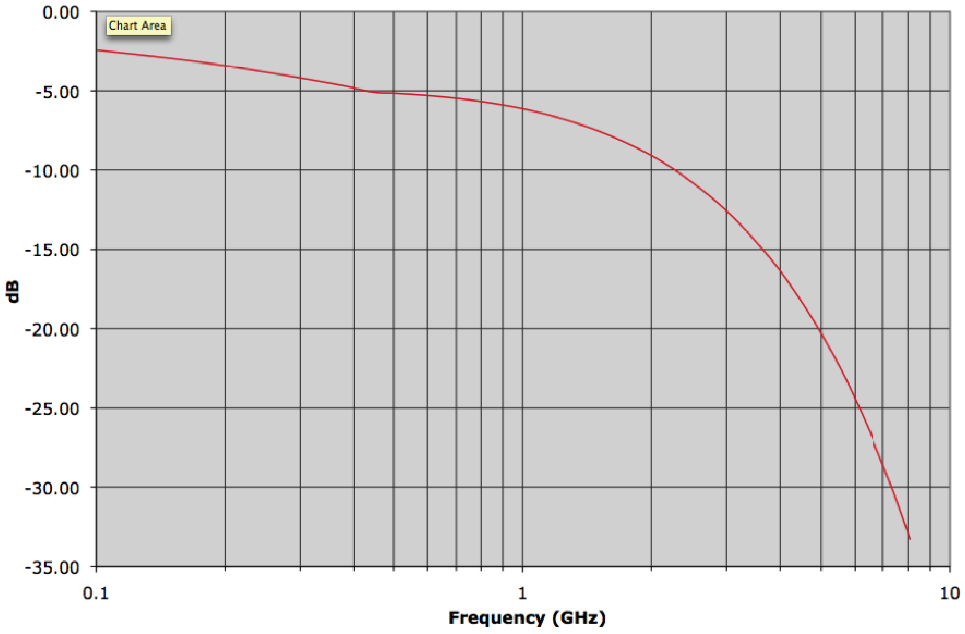


Figure 4-10: Mixed Mode Differential Insertion Loss for HBR Cable Assembly Types C1, C2, and C3

4.1.5.1.2 Insertion Loss – Lower Limit for High Bit Rate Resizing Adapters

$$IL_{\min.}[dB] = \begin{cases} -1.6 \times \sqrt{\frac{f}{f_0}}; & 0.1 < f \le \frac{f_0}{3} \\ 1.75\sqrt{f} - 1.65 * f - 1.31; & \frac{f_0}{3} < f \le 8.1 \end{cases}$$

where:

- f is given in GHz
- $f_0 = 1.35 GHz$

The chart presented in Figure 4-11 illustrates the above equation's Insertion Loss, and shall be referenced as the lower limit. The resizing adapter measured results shall comply with this limit.

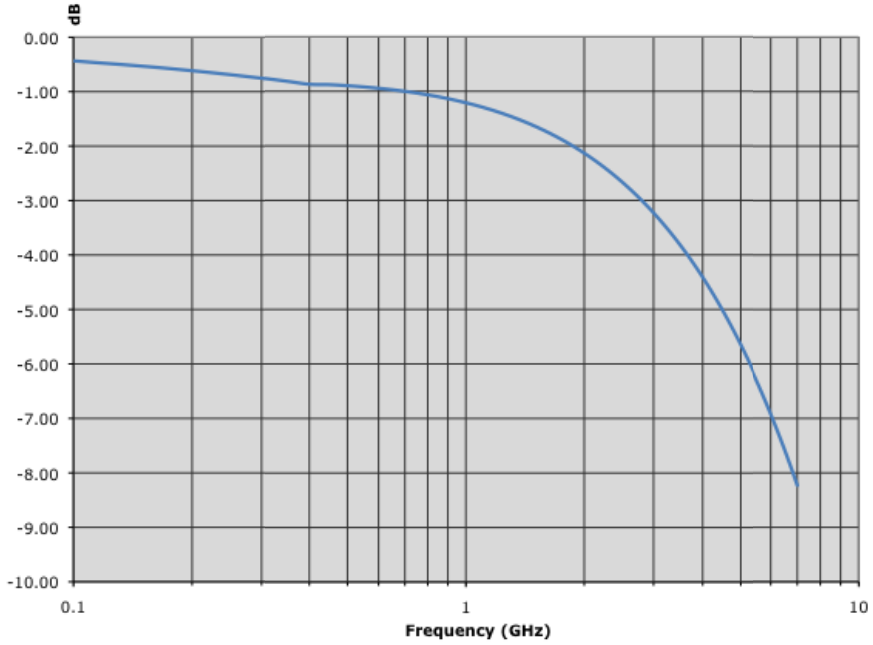


Figure 4-11: Mixed Mode Differential Insertion Loss for HBR Resizing Adapter

4.1.5.1.3 Insertion Loss – Lower Limit for Extension Cables

$$IL_{\min.}[dB] = \begin{cases} -5.22 \times \sqrt{\frac{f}{f_0}} - 0.043\,; & 0.1 < f \le \frac{f_0}{3} \\ 3.41\sqrt{f} - 3.18 * f - 3.91; & \frac{f_0}{3} < f \le 8.1 \end{cases}$$

where:

- f is given in GHz
- $f_0 = 1.35 GHz$

The chart presented in Figure 4-12 illustrates the above equation's Insertion Loss, and shall be referenced as the lower limit. The Extension Cable measured results shall comply with this limit.

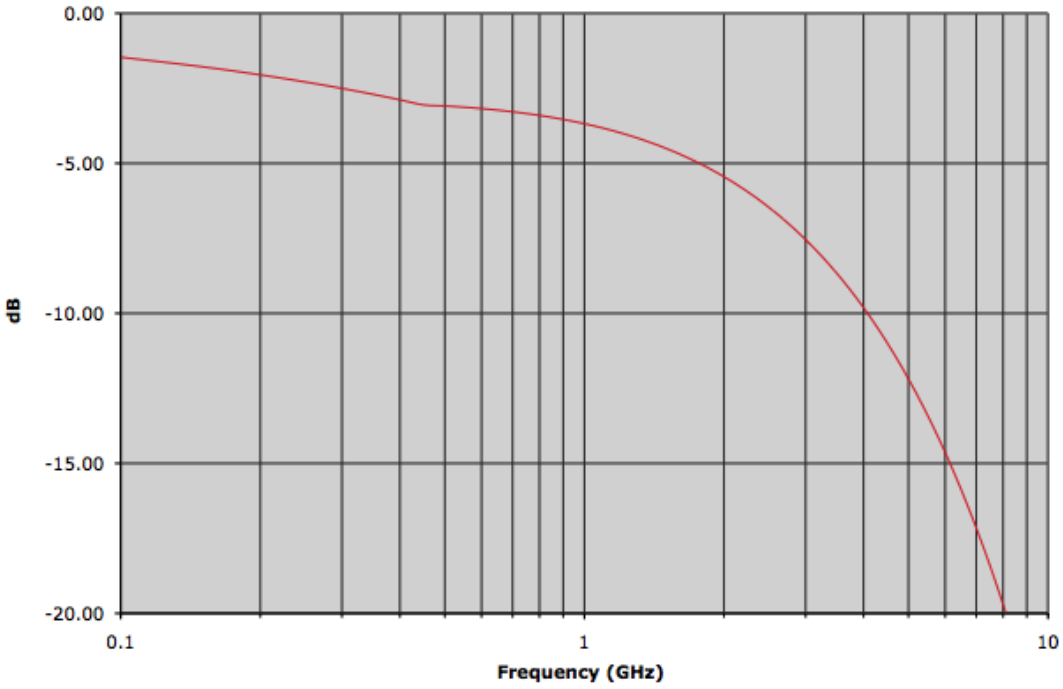


Figure 4-12: Mixed Mode Differential Insertion Loss for Extension Cable

4.1.5.1.4 Return Loss – Upper Limit for HBR Cable Assembly/Adapter (Full-sized DP Connector)

The return loss for a HBR cable assembly or resizing adapter measured through a full-sized DP connector is given by:

$$RL_{\max.}[dB] = \begin{cases} -15; & 0.1 < f \le \dfrac{f_0}{2} \\ -15 + 12.3\ Log_{10}\left(\dfrac{2f}{f_0}\right); & \dfrac{f_0}{2} < f \le 8.1 \end{cases}$$

where:

- f is given in GHz
- $f_0 = 1.35 GHz$

The chart presented in Figure 4-13 illustrates the above Return Loss equation and shall be referenced as the upper limit for Return Loss.

The measured cable assembly results shall comply with this limit.

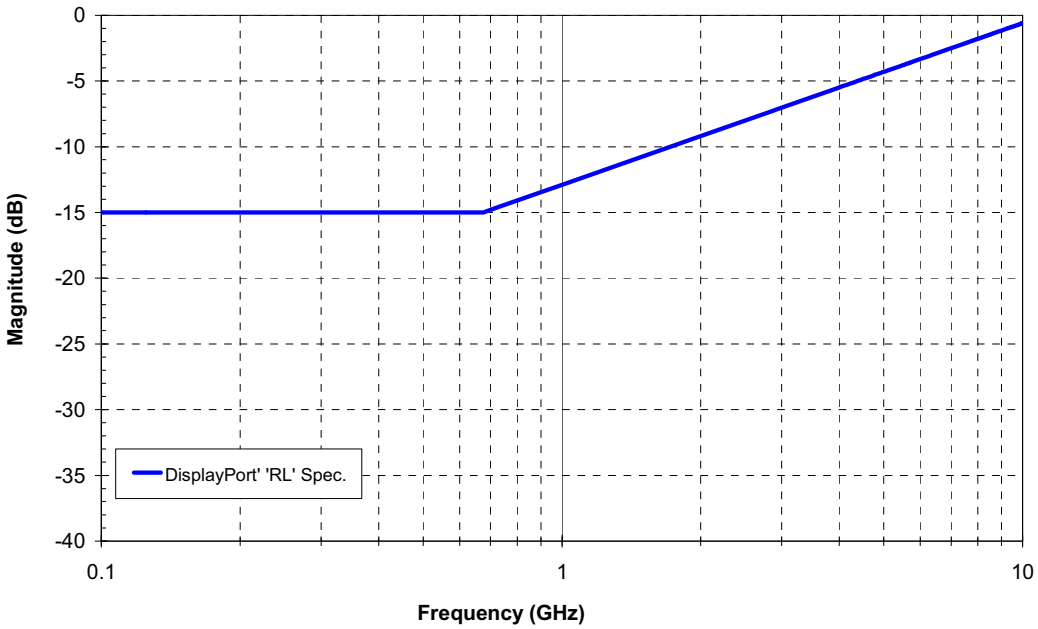


Figure 4-13: Mixed Mode Differential RL for HBR Cable Assembly/Adapter (DP Connector)

4.1.5.1.5 Return Loss – Upper Limit for HBR Cable Assembly/Adapter/Extension Cable

The return loss for a HBR cable assembly, resizing adapter or extension cable measured through an mDP connector is given by:

$$RL_{\max.}[dB] = \begin{cases} -15; & 0.1 < f \le \dfrac{f_0}{2} \\ -15 + 12.3\ Log_{10}\left(\dfrac{2f}{f_0}\right); & \dfrac{f_0}{2} < f \le 8.1 \end{cases}$$

where:

- f is given in GHz
- $f_0 = 1.35GHz$

The chart presented in Figure 4-14 illustrates the above Return Loss equation and shall be referenced as the upper limit for Return Loss.

The measured cable assembly results shall comply with this limit.

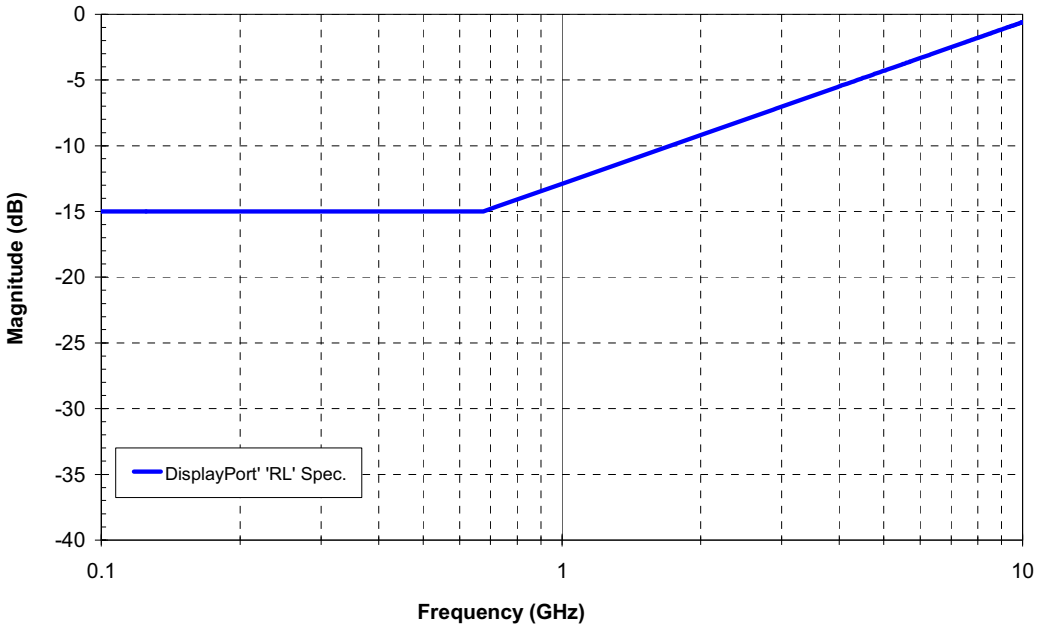


Figure 4-14: Mixed Mode Differential RL for HBR Cable Assembly/Adapter (mDP Connector)

4.1.5.2 Near-End Noise

The Near-End Noise (NEN) specification applies to all cable assembly types. It is defined in the frequency domain and covers the bandwidth up to 7GHz. The NEN shall be lower than the upper limit in the Isolation equation and depicted in Figure 4-15.

4.1.5.2.1 Near-End Noise – Upper Limit for High Bit Rate Cable Assembly

$$Isolation_{\max.}[dB] = \begin{cases} -26 & ; \quad 0.1 < f \le f_0 \\ -26 + 15\,Log_{10}\left(\frac{f}{f_0}\right) & ; \quad f_0 < f \le 8.1 \end{cases}$$

where:

- f is given in GHz
- $f_0 = 1.35 GHz$

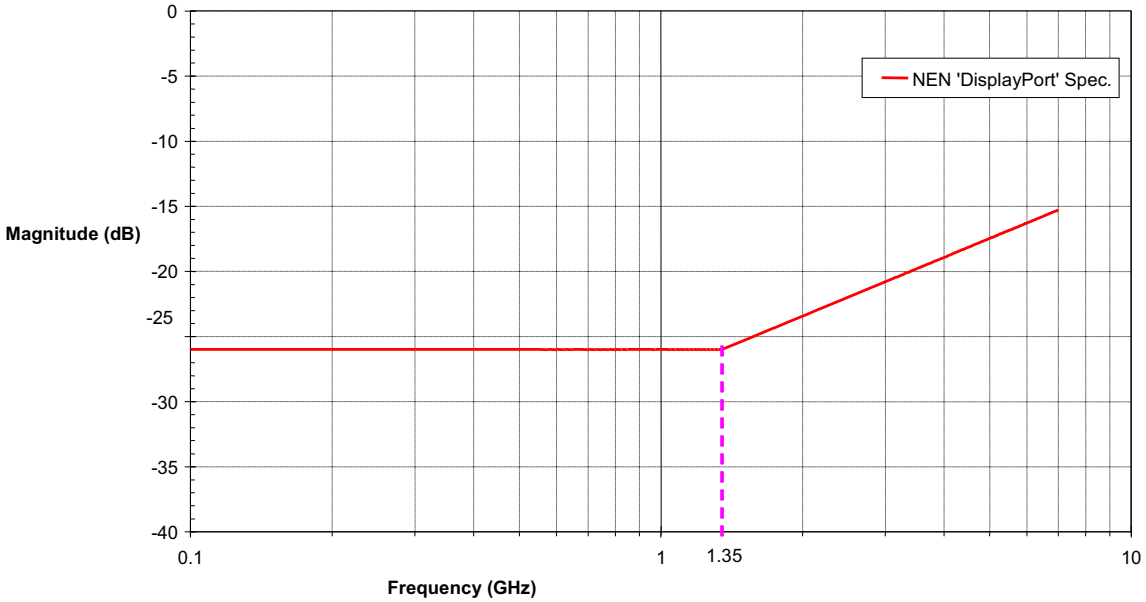


Figure 4-15: Near-End Total Noise (peak) for HBR Cable Assembly

4.1.5.3 Power Sum Equal Level Far-End Noise

The Power Sum Equal Level Far-End Noise (PSELFEN) specification applies to all cable assembly types. The PSELFEN represents the difference between cable insertion loss and the total power sum far-end noise from aggressor cable lanes.

$$PSFEN(f) = 10 \times \log \sum_{1}^{n} 10^{\left(\frac{FENn(f)}{10}\right)}$$

$$PSELFEN(f) = PSFEN(f) - IL(f)$$

where:

- *FENn(f)* is the far-end noise in dB
- *IL(f)* is the victim lane insertion loss in dB

The Power Sum Equal Level Far-End Noise shall be lower than the upper limit depicted in Figure 4-16.

4.1.5.3.1 Power Sum Equal Level Far-End Noise – Upper Limit for High Bit Rate Cable Assembly

$$PSELFEN_{\max.}[dB] = \begin{cases} -22 + 6Log_{10}\left(\frac{f}{f_0}\right); & 0.1 < f \le f_0 \\ -22 + 40Log_{10}\left(\frac{f}{f_0}\right); & f_0 < f \le 8.1 \end{cases}$$

where:

- f is given in GHz
- $f_0 = 2.7GHz$

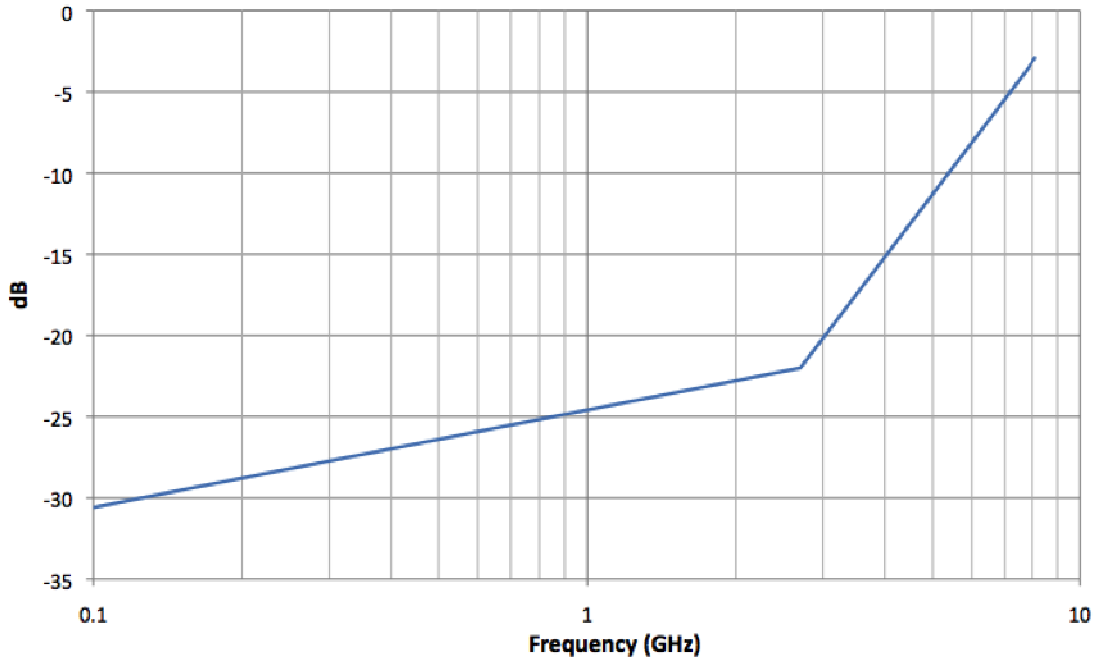


Figure 4-16: Power Sum Equal Level Far-End Total Noise (peak) for HBR Cable Assembly

4.1.5.4 Intra- and Inter-pair Skew

Both intra-pair and inter-pair skew are measured in the time domain with Differential TDR at the fixture rise/fall time, i.e., 50ps measured (20 to 80%).

4.1.5.4.1 Intra-pair Skew

Table 4-7 lists the intra-pair skew limits, when measured as illustrated in Figure 4-17.

Table 4-7: Intra-pair Skew Limits

Component Type	Limit
Cable Types C1, C2, and C3	≤ 50ps
Resizing Adapter Types A1 and A2	≤ 10ps
Extension Cables Type E1	≤ 35ps

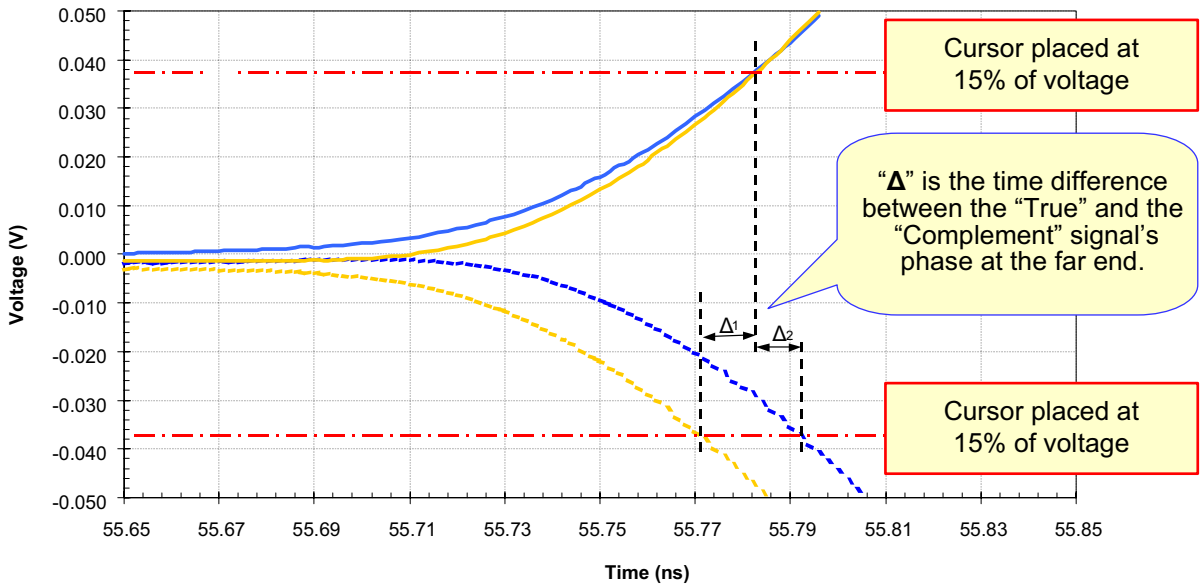


Figure 4-17: Intra-pair Skew Measurement Method

4.1.5.4.2 Inter-pair Skew

Table 4-8 lists the inter-pair skew limits, when measured as illustrated in Figure 4-18.

Table 4-8: Inter-pair Skew Limits

Component Type	Limit
Cable Types C1, C2, and C3	≤ 2UI at HBR
Resizing Adapter Types A1 and A2	≤ 2UI at HBR
Extension Cables Type E1	≤ 1UI at HBR

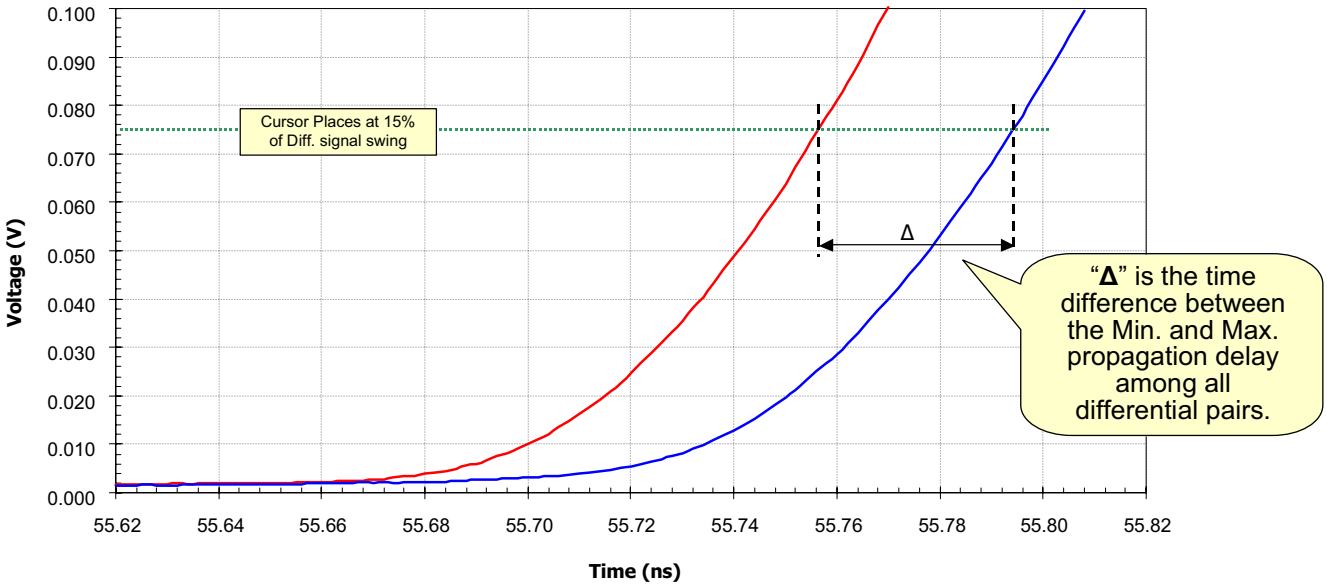


Figure 4-18: Inter-pair Skew Measurement Method

4.1.6 Reduced Bit Rate Cable-Connector Assembly Specification

4.1.6.1 Insertion Loss and Return Loss

The following equations represents the reference line that limits the Insertion Loss and Return Loss measured results.

4.1.6.1.1 Insertion Loss – Lower Limit for Reduced Bit Rate Cable Assembly

$$IL_{\min.}[dB] = \begin{cases} -1 - 13.5 \times \sqrt{\frac{f}{f_0}} & ; \quad 0.01 < f \le \frac{f_0}{3} \\ -2.1 - [12(f - \frac{f_0}{3}) + 6.8] & ; \quad \frac{f_0}{3} < f \le 4 \end{cases}$$

where:

- f is given in GHz
- $f_0 = 0.825 GHz$

The chart presented in Figure 4-19 illustrates the above Insertion Loss equation and shall be referenced as the lower limit. The measured cable assembly results shall comply with this limit.

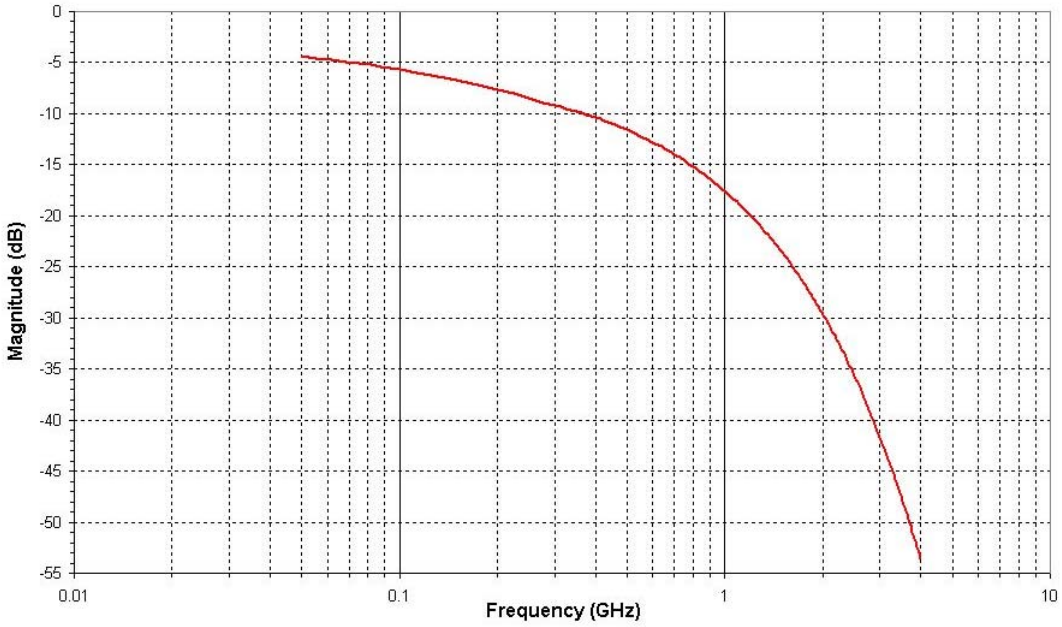


Figure 4-19: Mixed Mode Differential Insertion Loss (SDD21) Mask of RBR Cable

4.1.6.1.2 Return Loss – Upper Limit for Reduced Bit Rate Cable Assembly

$$RL_{\max.}[dB] = \begin{cases} -15 & ; \quad 0.1 < f \le \dfrac{f_0}{2} \\ -15 + 12\ Log_{10}\left(2x\dfrac{f}{f_0}\right) & ; \quad \dfrac{f_0}{2} < f \le 4 \end{cases}$$

where:

- f is given in GHz
- $f_0 = 0.8GHz$

The chart presented in Figure 4-20 illustrates the above Return Loss equation and shall be referenced as the upper limit.

The cable assembly measured results shall comply with these limits.

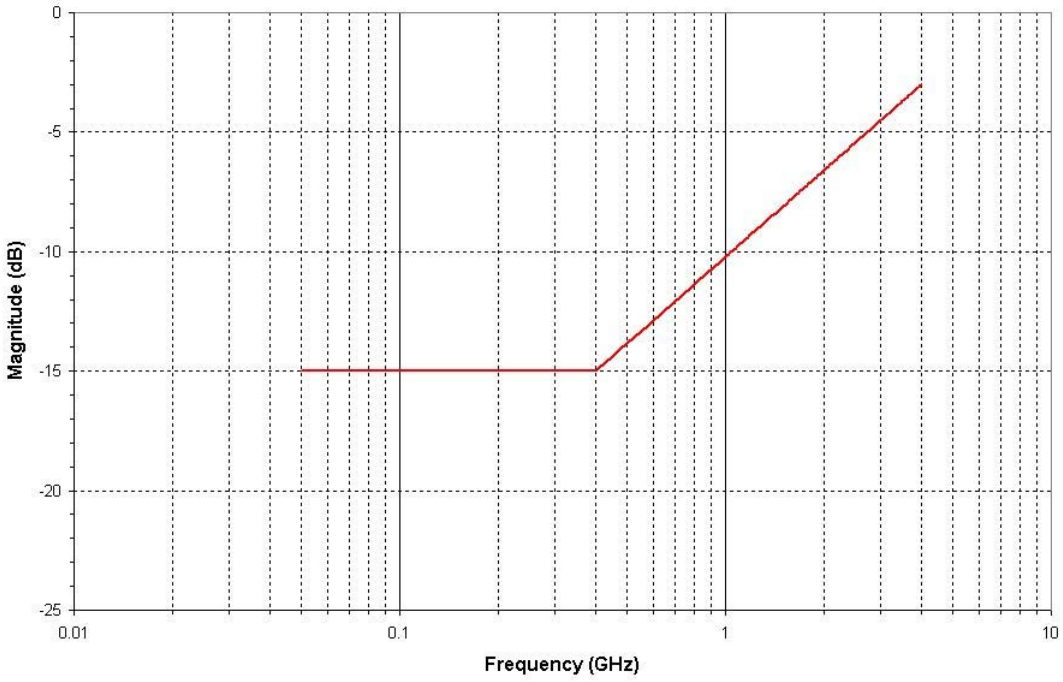


Figure 4-20: Mixed Mode Differential Return Loss (SDD11) of RBR Cable

4.1.6.2 Near-End Noise

Near-End Noise (NEN) shall be lower than the upper limit in the Isolation equation and illustrated in Figure 4-21.

4.1.6.2.1 Near-End Noise – Upper Limit for Reduced Bit Rate Cable Assembly

$$Isolation_{\max.}[dB] = \begin{cases} -26 & ; \quad 0.1 < f \le f_0 \\ -26 + 15\, Log_{10}\left(\frac{f}{f_0}\right) & ; \quad f_0 < f \le 4 \end{cases}$$

where:

- f is given in GHz
- $f_0 = 0.8GHz$

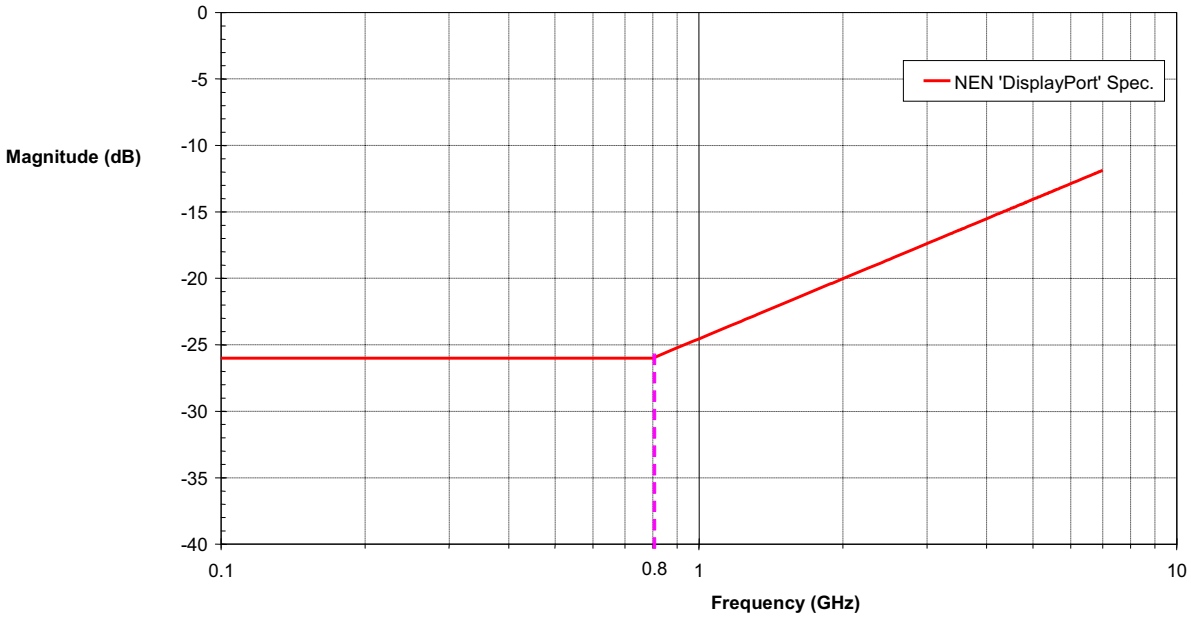


Figure 4-21: Near-End Total Noise (peak) for RBR Cable Assembly

4.1.6.3 Far-End Noise

Far-End Noise (FEN) shall be lower than the upper limit illustrated in Figure 4-22.

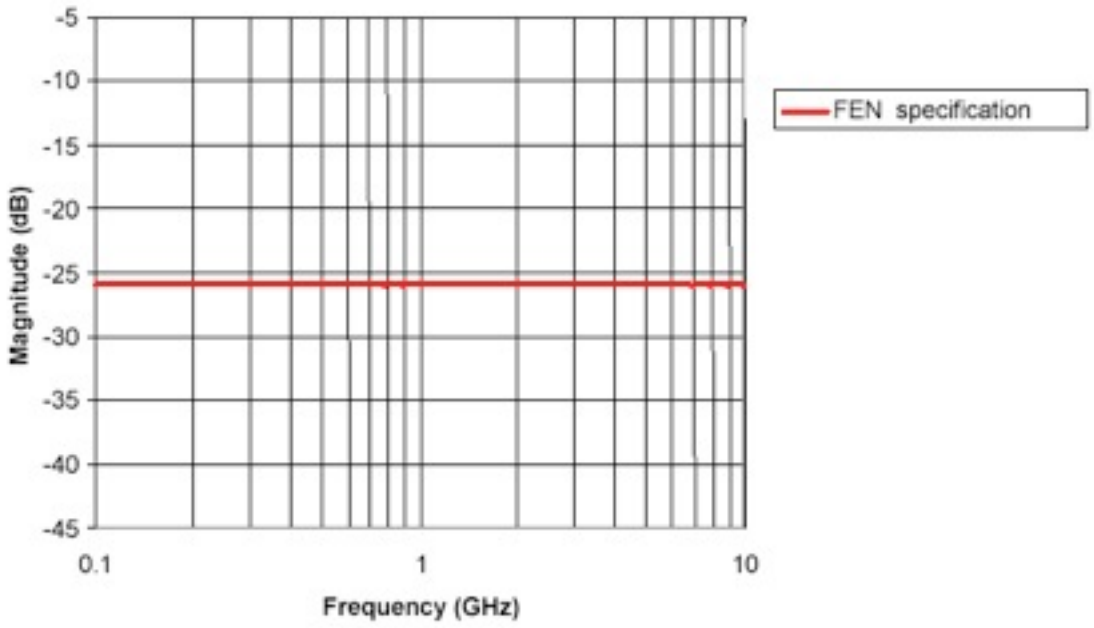


Figure 4-22: Far-End Total Noise (peak) for RBR Cable Assembly

4.1.6.4 Intra- and Inter-pair Skew

Both intra- and inter-pair skew are measured in the time domain with Differential TDR at fixture rise/fall time (i.e., 50ps measured (20 to 80%)).

4.1.6.4.1 Intra-pair Skew

Intra-pair skew shall be no more than 250ps. See Figure 4-17 for the measurement method.

4.1.6.4.2 Inter-pair Skew

Inter-pair skew shall be no more than 2UI at RBR for Cable Types C1, C2, and C3. See Figure 4-18 for the measurement method.

4.1.7 DP8K Cable Specification

New to *DP v1.4a*.

4.1.7.1 HBR3 DP-to-DP Cable Electrical Properties

The cable assembly's electrical specification is based on the specification methodology for USB Type-C-to-DP passive cable assemblies (see *DisplayPort Alt Mode Standard*, *Section 4.2.3*). Insertion loss and Return loss are to be tested relative to a 100-Ω differential environment at the DP connectors. The IntePar-DP test tool will adjust reference impedance to 90Ω. The appropriate parameters in the referenced methodology are to be adjusted accordingly. With respect to *fmax* and T_b, the values to be used shall be *fmax* = 12.15GHz and T_b = 123.4ps.

4.1.7.2 Intra-pair Skew (Normative)

Intra-pair skew is the skew between true and complement signals of a differential pair. Intra-pair skew shall be limited to 30ps. This is designed to support 2-m cables at 30-ps maximum skew.

4.1.7.3 Insertion Loss Fit at Nyquist Frequencies

Updated in *DP v2.0*.

Table 4-9 lists the Nyquist frequencies for UHBR10, HBR3, HBR2, and HBR and their Insertion Loss Fit at Nyquist Frequency (ILFitAtNq) requirements.

Table 4-9: Nyquist Frequencies and their ILFitAtNq Requirements

Bit Rate	Nyquist Frequency (GHz)	ILFitAtNq Requirement (dB)
UHBR10	5	≥ -13.3
HBR3	4.05	≥ -11.0
HBR2	2.7	≥ -8.5
HBR	1.35	≥ -5.5

Figure 4-23 through Figure 4-26 illustrate the Insertion Loss and Insertion Loss Fit curves for an example cable assembly at UHBR10 and HBR3, HBR2, and HBR, respectively. Each graph identifies the Insertion Loss and Insertion Loss Fit for the Nyquist frequency corresponding to one of the three DP high-bit transmission rates, also providing the ILFitAtNq limit in each case.

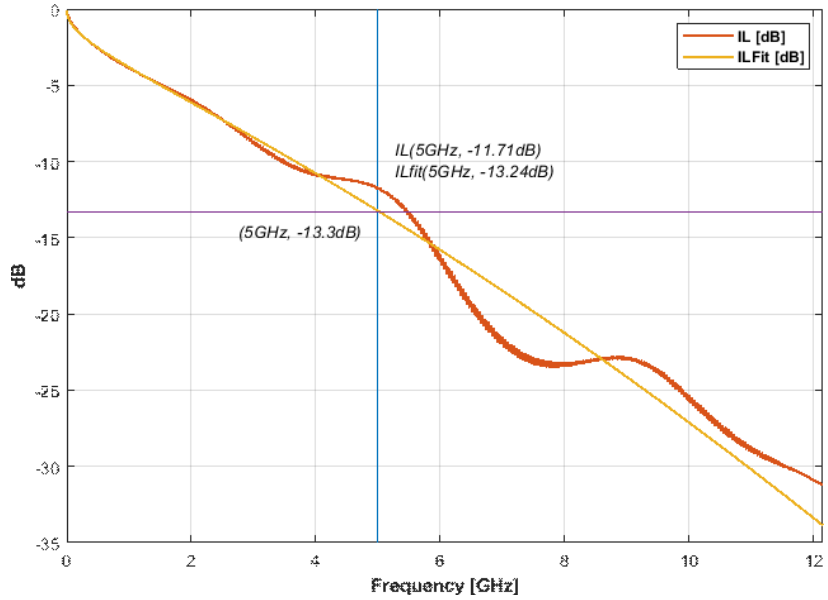


Figure 4-23: UHBR10 Insertion Loss Fit at Nyquist

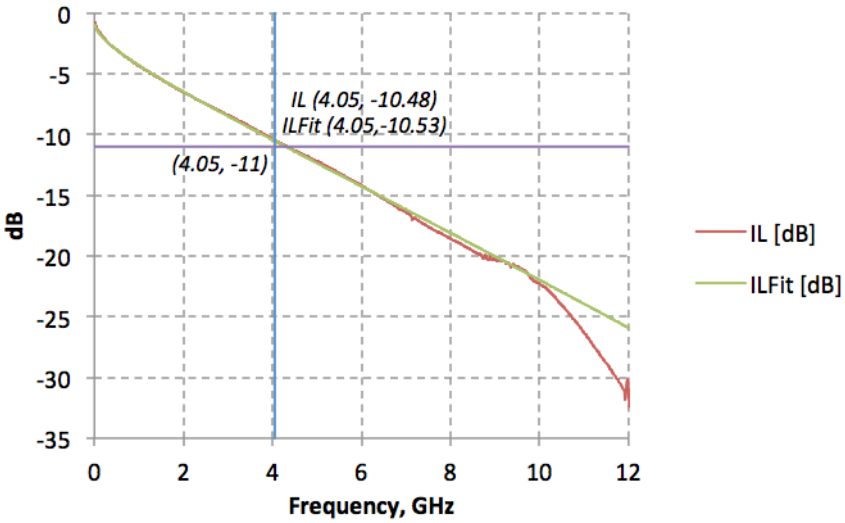


Figure 4-24: HBR3 Insertion Loss Fit at Nyquist

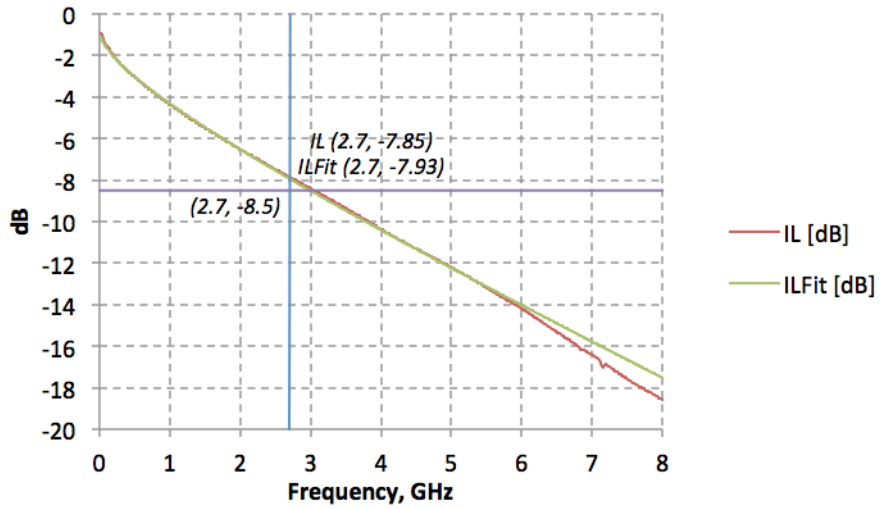


Figure 4-25: HBR2 Insertion Loss Fit at Nyquist

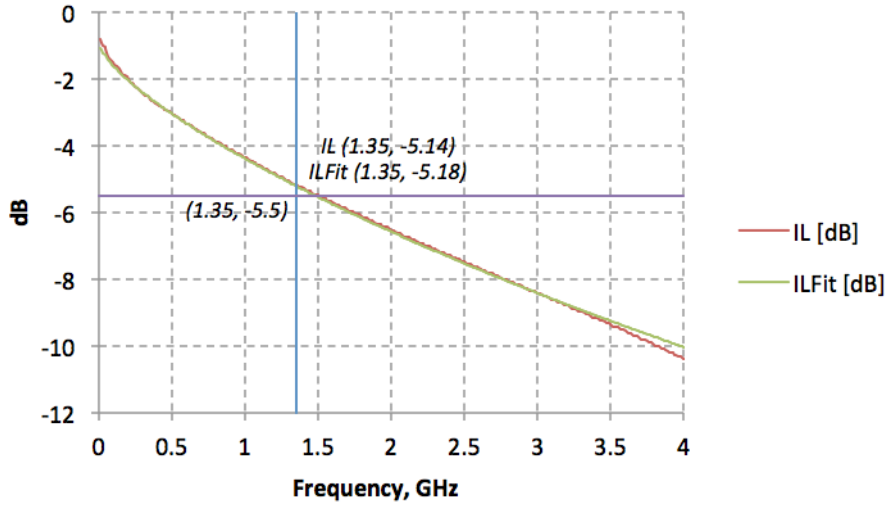


Figure 4-26: HBR Insertion Loss Fit at Nyquist

4.1.7.4 Integrated Multi-reflection

For the Input Pulse Spectrum (used in the calculation of integrated multi-reflection (IMR)), the DP HBR3, HBR2, and HBR bit rates correspond to UIs of 123.4, 185.2, and 370.4ps, respectively. The rise time is 0.4UI. With respect to *fmax* and T_b, the values to be used shall be *fmax* = 12.15GHz and T_b = 123.4ps.

IMR has dependency on ILFitAtNq. More IMR may be tolerated when ILFitAtNq decreases.

The IMR limit is specified as a function of ILFitAtNq:

$$IMR \leq 0.0579 \times ILFitAtNq^2 + 1.64 \times ILFitAtNq - 23.23$$

Figure 4-27 illustrates IMR's compensation curve as a function of ILFitAtNq at HBR3.

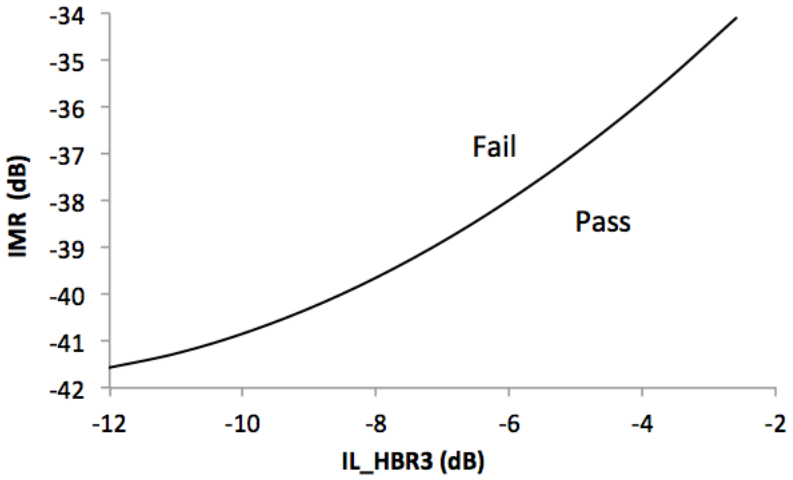


Figure 4-27: HBR3 IMR as a Function of ILFitAtNq

4.1.7.5 Integrated Crosstalk between DP Lanes

The power sum limits for integrated crosstalk between the DP lanes shall comply with the following limits:

- IFEXT ≤ -35dB (up to 12GHz)
- INEXT ≤ -23dB (up to 12GHz) when measured through the DP connector

4.1.7.6 Integrated Return Loss

IRL has a strong dependency on ILFitAtNq, and its limit is specified as a function of ILFitAtNq:

$$IRL \leq 0.0336 \times ILFitAtNq^2 + 1.28 \times ILFitAtNq - 8.87$$

Figure 4-28 illustrates the compensation curve of IRL as a function of ILFitAtNq at HBR3.

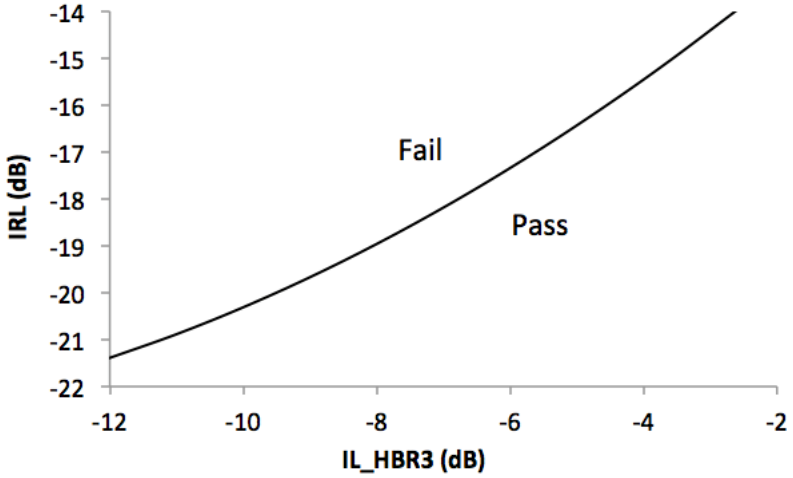


Figure 4-28: HBR3 IRL as a Function of ILFitAtNq

4.1.7.7 Differential-to-Common Mode Conversion

SCD12/SCD21 shall be less than or equal to -17dB from 100MHz to 8.1GHz.

4.1.8 Bulk Cable and Connector Impedance (Normative)

The Bulk Cable impedance and Connector Impedance shall meet the limits specified for HBR cable assemblies.

4.2 Connector Specification

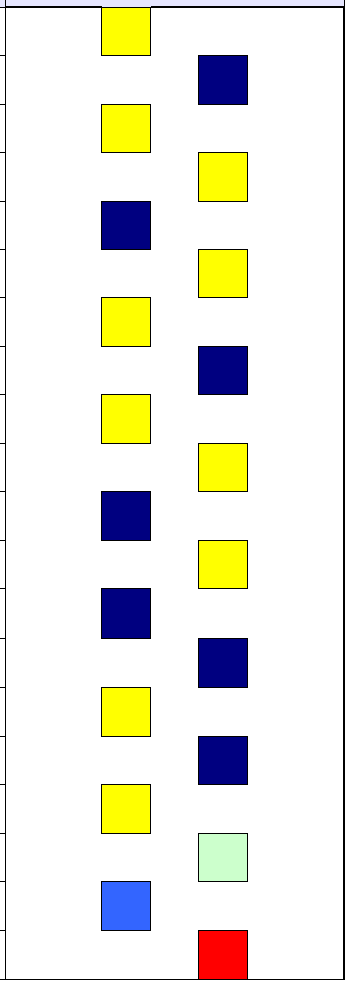
This section describes the specifications of the external and internal DP connectors.

4.2.1 External Full-size Connector

4.2.1.1 Connector Pin Assignment

Table 4-10 defines the pin assignments of the DP external connector on a downstream-facing port (DFP) on an upstream device. Table 4-11 defines the pin assignments of the DP external connector on an upstream-facing port (UFP) on an downstream device.

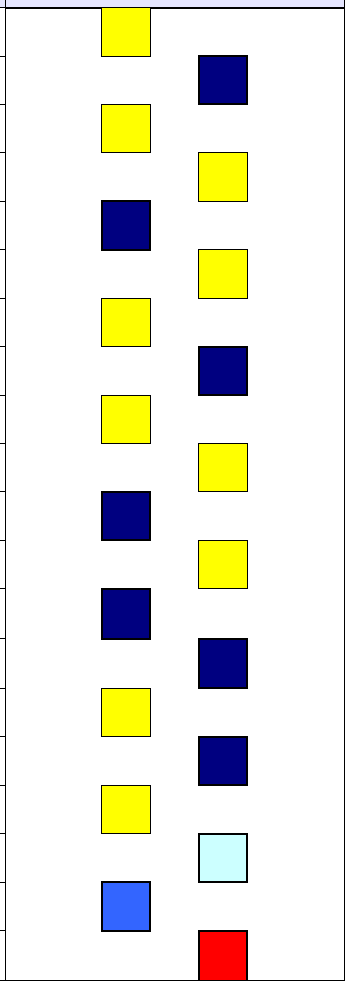
Table 4-10: DFP Connector Pin Assignment

Pin Number	Signal Type	Pin Name	Mating Row Contact Location	Vertically Opposed Connector's Front View
1	Out	ML_Lane_0_P	Top	
2	GND	**GND**	Bottom	
3	Out	ML_Lane_0_N	Top	
4	Out	ML_Lane_1_P	Bottom	
5	GND	GND	Top	
6	Out	ML_Lane_1_N	Bottom	
7	Out	ML_Lane_2_P	Top	
8	GND	**GND**	Bottom	
9	Out	ML_Lane_2_N	Top	
10	Out	ML_Lane_3_P	Bottom	
11	GND	**GND**	Top	
12	Out	ML_Lane_3_N	Bottom	
13	CONFIG[a]	**CONFIG1**	Top	
14	CONFIG[a]	**CONFIG2**	Bottom	
15	I/O	AUX_CH_P	Top	
16	GND	**GND**	Bottom	
17	I/O	AUX_CH_N	Top	
18	In	Hot Plug Detect	Bottom	
19	RTN	Return	Top	
20	PWR Out[b]	DP_PWR	Bottom	

a. Pins 13 and 14 shall be connected to ground through a pull-down device. External devices and cable assemblies shall be designed to not rely on a low-impedance ground path from these pins.

b. Pin 20, PWR Out, shall provide +3.3V ±10% with a maximum current of 500mA and minimum power capability of 1.5W.

Table 4-11: UFP Connector Pin Assignment

Pin Number	Signal Type	Pin Name	Mating Row Contact Location	Vertically Opposed Connector's Front View
1	In	ML_Lane_3_N	Top	
2	GND	**GND**	Bottom	
3	In	ML_Lane_3_P	Top	
4	In	ML_Lane_2_N	Bottom	
5	GND	**GND**	Top	
6	In	ML_Lane_2_P	Bottom	
7	In	ML_Lane_1_N	Top	
8	GND	**GND**	Bottom	
9	In	ML_Lane_1_P	Top	
10	In	ML_Lane_0_N	Bottom	
11	GND	**GND**	Top	
12	In	ML_Lane_0_P	Bottom	
13	CONFIG[a]	**CONFIG1**	Top	
14	CONFIG[a]	**CONFIG2**	Bottom	
15	I/O	AUX_CH_P	Top	
16	GND	**GND**	Bottom	
17	I/O	AUX_CH_N	Top	
18	Out	Hot Plug Detect	Bottom	
19	RTN	Return	Top	
20	PWR Out[b]	DP_PWR	Bottom	

a. Pins 13 and 14 shall be connected to ground through a pull-down device. External devices and cable assemblies shall be designed to not rely on a low-impedance ground path from these pins.

b. Pin 20, PWR Out, shall provide +3.3V ±10% with a maximum current of 500mA and minimum power capability of 1.5W.

Figure 4-29 illustrates an external cable connector assembly's wiring. The standard external cable connector assembly shall **not** have a wire on pin 20, DP_PWR.

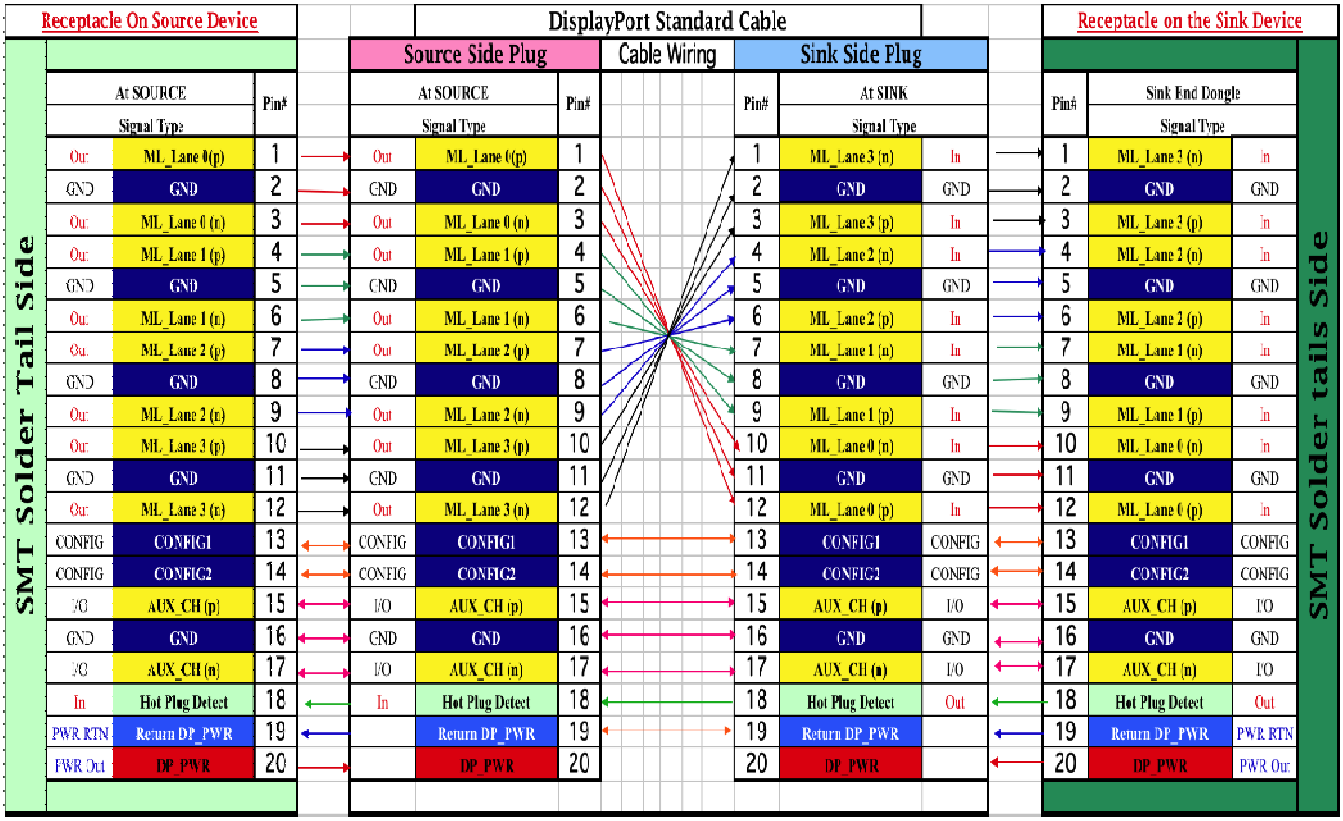


Figure 4-29: External Cable Connector Assembly Wiring

4.2.1.2 Mating Sequence

Table 4-12 presents the legend for signal name/type mating level.

Table 4-12: Mating Sequence Levels

Signal Type			Level
Connector Shell			First Mate
DP_PWR	Return	GND	Second Mate
AUX_CH_P, AUX_CH_N	ML_Lane_0_P, ML_Lane_0_N, ML_Lane_1_P, ML_Lane_1_N, ML_Lane_2_P, ML_Lane_2_N, ML_Lane_3_P, ML_Lane_3_N	Hot Plug Detect. CONFIG1. CONFIG2	Third Mate

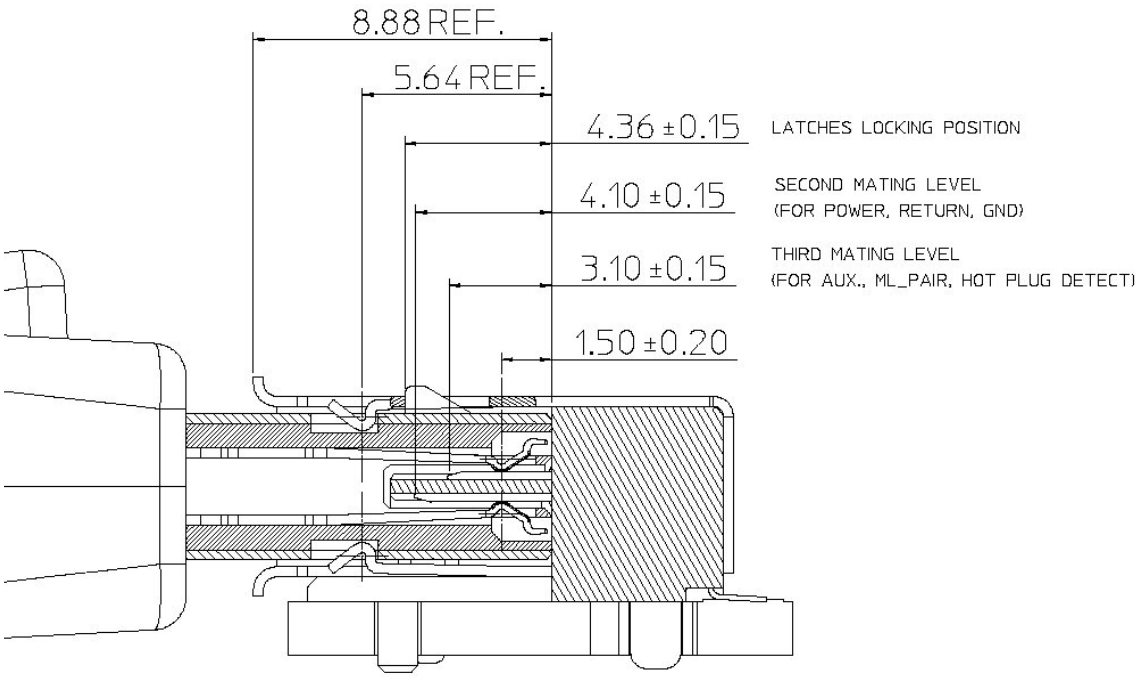


Figure 4-30: Connector Mating Levels

4.2.1.3 Connector Mechanical Performance

Table 4-13 defines the mechanical performance requirements for a DP external connector.

Table 4-13: DP External Connector Mechanical Performance

Item	Test Condition	Requirement	
Vibration	Amplitude: 1.52mm P-P or 147m/s^2 {15G} Sweep time: 50-2000-50Hz in 20 minutes. Duration: 12 times in each of X, Y, Z axes (Total of 36 times) Electrical load: DC 100mA current shall be conducted during the test. (*EIA-364-28* Condition III, Method 5A)	Appearance	No Damage
		Contact Resistance	Contact: Change from initial value = 30mΩ maximum Shell Part: Change from initial value = 50mΩ maximum
		Discontinuity	1us maximum
Durability	Measure contact and shell resistance after the following. Automatic cycling: 10,000 cycles at 100 ±50 cycles/hr. (*EIA-364-09*)	Contact Resistance	Contact: Change from initial value = 30mΩ maximum Shell Part: Change from initial value = 50mΩ maximum
Insertion/ Withdrawal Force (no latches)	Insertion and withdrawal speed: 25mm/minute. (*EIA-364-13*)	Withdrawal force	9.8N {1.0kgf} minimum 39.2N {4.0kgf} maximum
		Insertion force	44.1N {4.5kgf} maximum
Latch Strength	Mate connectors, apply axial pull-out force at a rate of 13mm/minute until the latch is disengaged or damaged. (*EIA-364-98*)	Appearance	No damage on either part of connector
		Pull force	49.0N {5.0kgf} minimum
Cable Flex	100 cycles in each of 2 planes. Dimension: $X = 3.7 \times$ Cable Diameter. (*EIA-364-41*, Condition I)	Discontinuity	1us maximum
		Dielectric Withstanding Voltage and Insulation Resistance.	Conform to item of dielectric withstanding voltage and insulation resistance

4.2.1.4 Connector Electrical Performance

Table 4-14 defines the electrical performance requirements for a DP external connector.

Table 4-14: DP External Connector Electrical Performance

Item	Test Condition	Requirement
Low Level Contact Resistance	Mated connectors Contact: measured by dry circuit, 20mV maximum, and 10mA. Shell: measured by open circuit, 5V maximum, 100mA. (*EIA-364-23*)	Contact: Change from initial value = 30mΩ maximum Shell: Change from initial value = 50mΩ maximum
Dielectric Strength	Unmated connectors, apply 500Vrms between adjacent terminal and ground. (*EIA-364-20*, Method 301) Mated connector, apply 300Vrms between adjacent terminal and ground.	No Breakdown
Insulation Resistance	Unmated connectors, apply 500V_{DC} between adjacent terminal and ground. (*EIA-364-21*, Method 302)	Unmated: 100MΩ minimum
	Mated connectors, apply 150V_{DC} between adjacent terminal and ground.	Mated: 10MΩ minimum
Contact Current Rating	55°C, maximum ambient 85°C, maximum temperature change (*EIA-364-70*)	0.5A minimum
Applied Voltage Rating	40-Vrms continuous maximum, on any signal pin with respect to the shield.	No Breakdown
Electrostatic Discharge	Test unmated connectors from 1 to 8kV, in 1-kV steps, using 8-mm ball probe. (*IEC 61000-4-2*)	No evidence of discharge to contacts at 8kV

4.2.1.5 Connector Environment Performance

Table 4-15 defines the environment performance requirements for a DP external connector.

Table 4-15: DP External Connector Environment Performance

Item	Test Condition	Requirement	
Thermal Shock	10 cycles of: • -55°C for 30 minutes • +85°C for 30 minutes (*EIA-364-32*, Condition I)	Appearance	No Damage
		Contact Resistance	Contact: Change from initial value = 30mΩ maximum Shell Part: Change from initial value = 50mΩ maximum
Humidity	A) Mate connectors together and perform the test as follows: • Temperature: +25 to +85°C • Relative Humidity: 80 to 95% • Duration: Four cycles (96 hours) Upon completion of the test, specimens shall be conditioned at ambient room conditions for 24 hours, after which the specified measurements shall be performed. (*EIA-364-31*)	Appearance	No Damage
		Contact Resistance	Contact: Change from initial value = 30mΩ maximum Shell Part: Change from initial value = 50mΩ maximum
	B) Unmate connectors and perform the test as follows: • Temperature: +25 to +85°C • Relative Humidity: 80 to 95% • Duration: Four cycles (96 hours) Upon completion of the test, specimens shall be conditioned at ambient room conditions for 24 hours, after which the specified measurements shall be performed. (*EIA-364-31*)	Appearance	No Damage
		Dielectric Withstanding Voltage and Insulation Resistance	Conform to item of Dielectric Withstanding Voltage and Insulation Resistance
Thermal Aging	Mate connectors and expose to (+105 ±2)°C for 250 hours. Upon completion of the exposure period, the test specimens shall be conditioned at ambient room conditions for one to two hours after which the specified measurements shall be performed. (*EIA-364-17*, Condition 4, Method A)	Appearance	No Damage
		Contact Resistance	Contact: Change from initial value = 30mΩ maximum Shell Part: Change from initial value = 50mΩ maximum

4.2.1.6 Connector Performance Test Sequence

To evaluate the connector performance, the test sequence shall follow Test Groups 1, 2, 3, and 7 in *EIA-364-1000.01*.

4.2.1.7 Connector Drawings

Figure 4-31 illustrates the DP external connector. All dimensions are in mm.

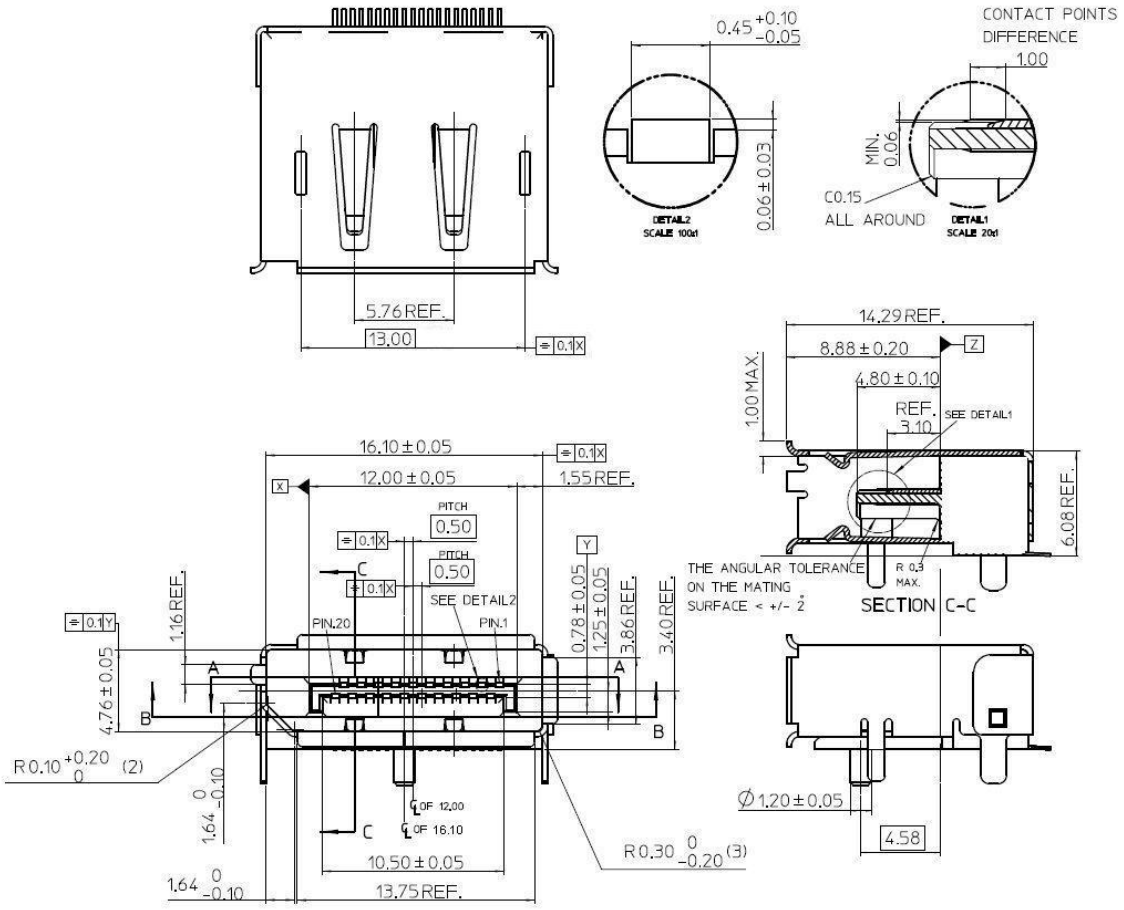


Figure 4-31: DisplayPort External Connector Drawings

4.2.1.8 Cable Connector Drawings

Figure 4-32 illustrates the DP external cable-connector assembly.

Recommendations for plug connector construction:

- Locate the thumb button on the opposite side to the interface chamfer corner.
- Provide the thumb button on the plug's top cover, regardless of whether the latches are fitted. This shall provide the user with a good indicator of plug orientation.
- A plug without latches may have an alternate feature providing the same orientation indicator as the thumb button of the standard plug.

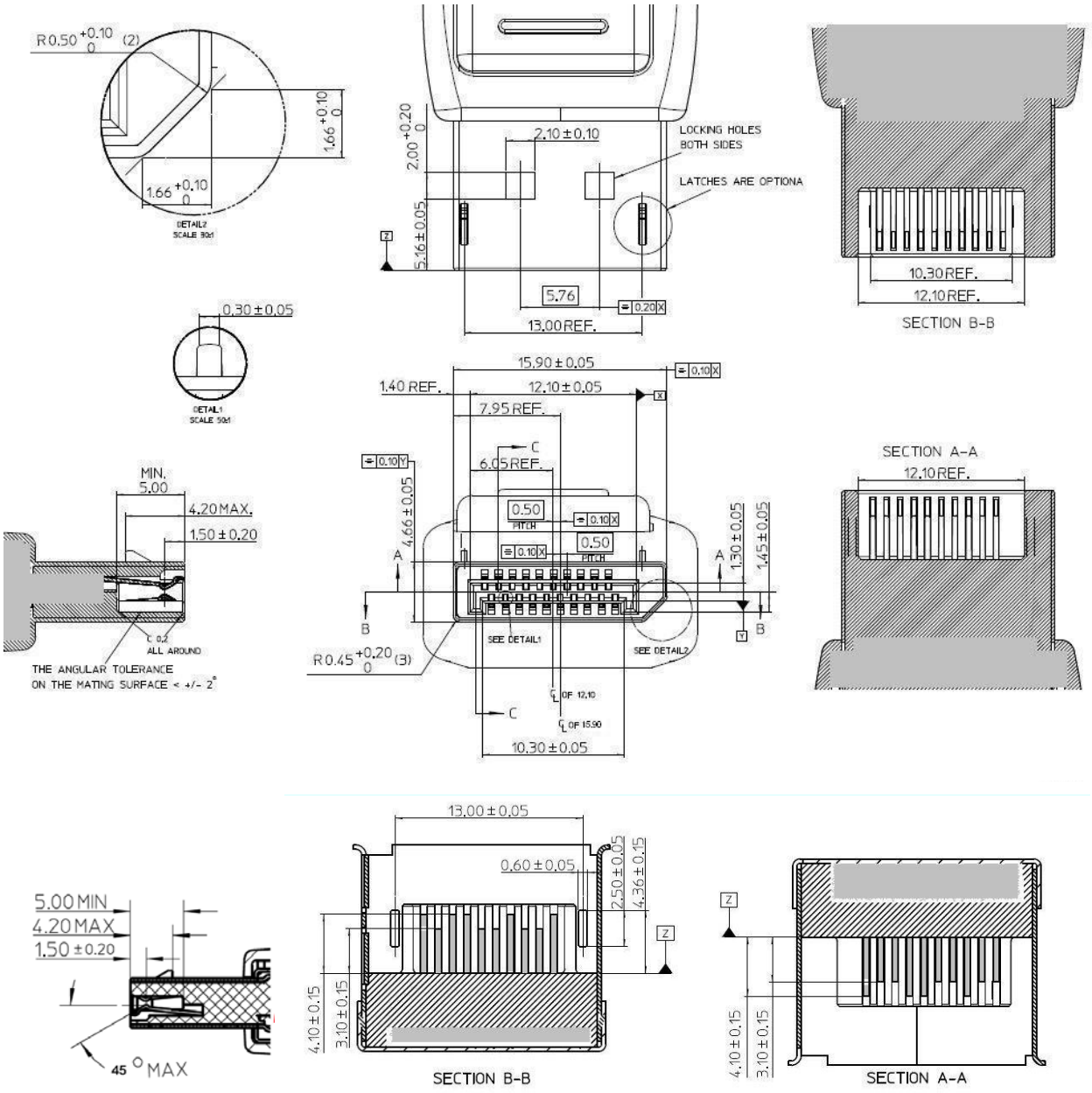


Figure 4-32: DisplayPort External Cable-Connector Assembly Drawings

The external connector should use the orientations illustrated in Figure 4-33.

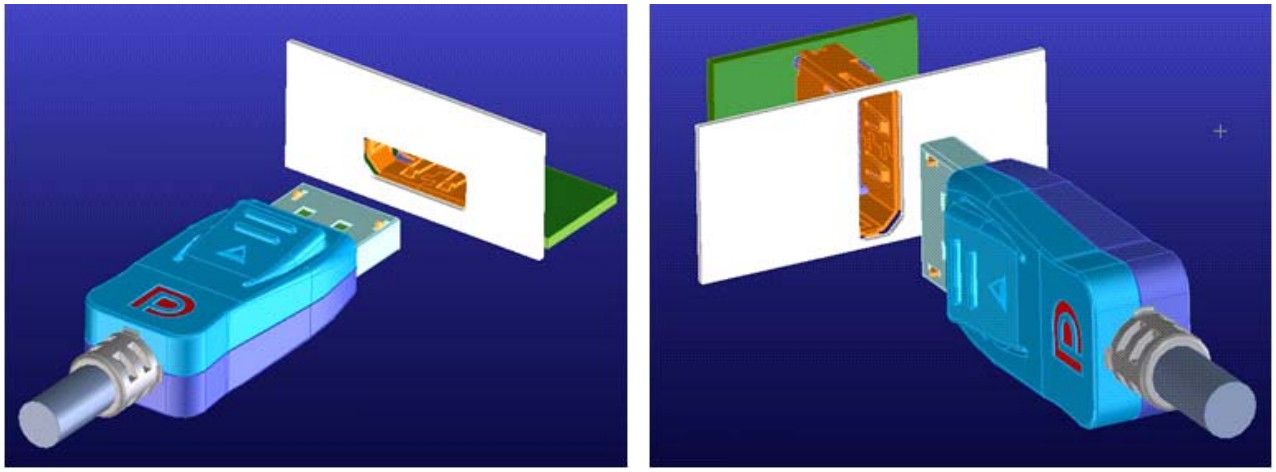
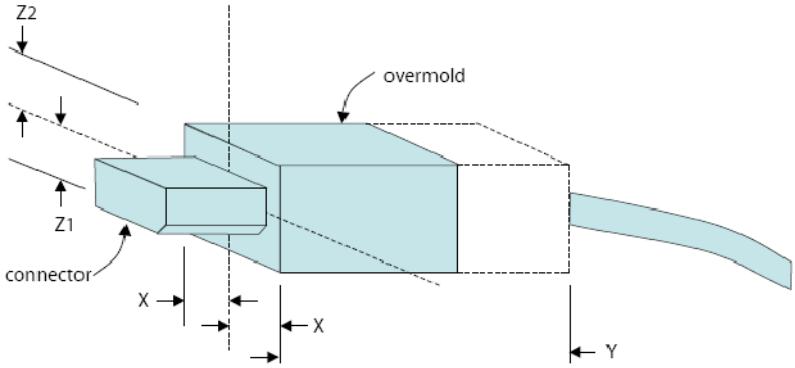


Figure 4-33: Recommended External Connector Orientations

4.2.1.9 Plug Overmold Dimensions for Non-Latch Plug Connector

For non-latching plug connectors, the following overmold dimension parameters in Figure 4-34 shall be met.



X: max 10mm from connector centerline
Z1: max 5mm from connector centerline
Z2: max 5mm from connector centerline for Y from overmold face
Y: X and Z2 apply for 25mm from overmold face or depth of plug (if less);
Designs intended for use on portable systems are encouraged to use smaller dimensions for Z1 and Z2 wherever practical

Figure 4-34: Plug Overmold Dimensions for Non-Latch Plug Connector

4.2.1.10 Plug Connector and Board Connector Fully Mated Condition

Figure 4-35 illustrates the fully mated condition of the plug and board connectors.

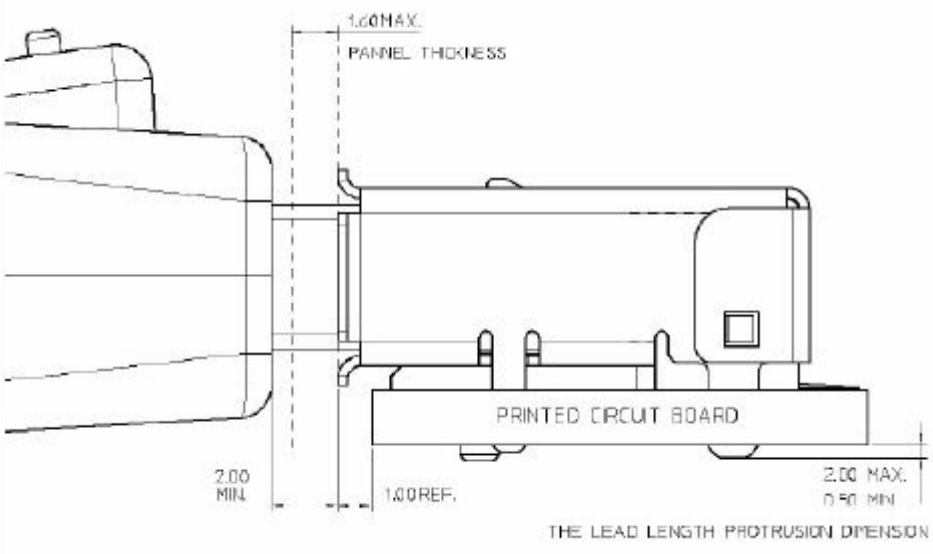


Figure 4-35: Fully Mated Condition for DP External Connectors

4.2.1.11 Recommended PCB Layout for DP External Cable-Connector Assembly

Figure 4-36 illustrates the DP external cable-connector assembly that should be used in a PCB layout.

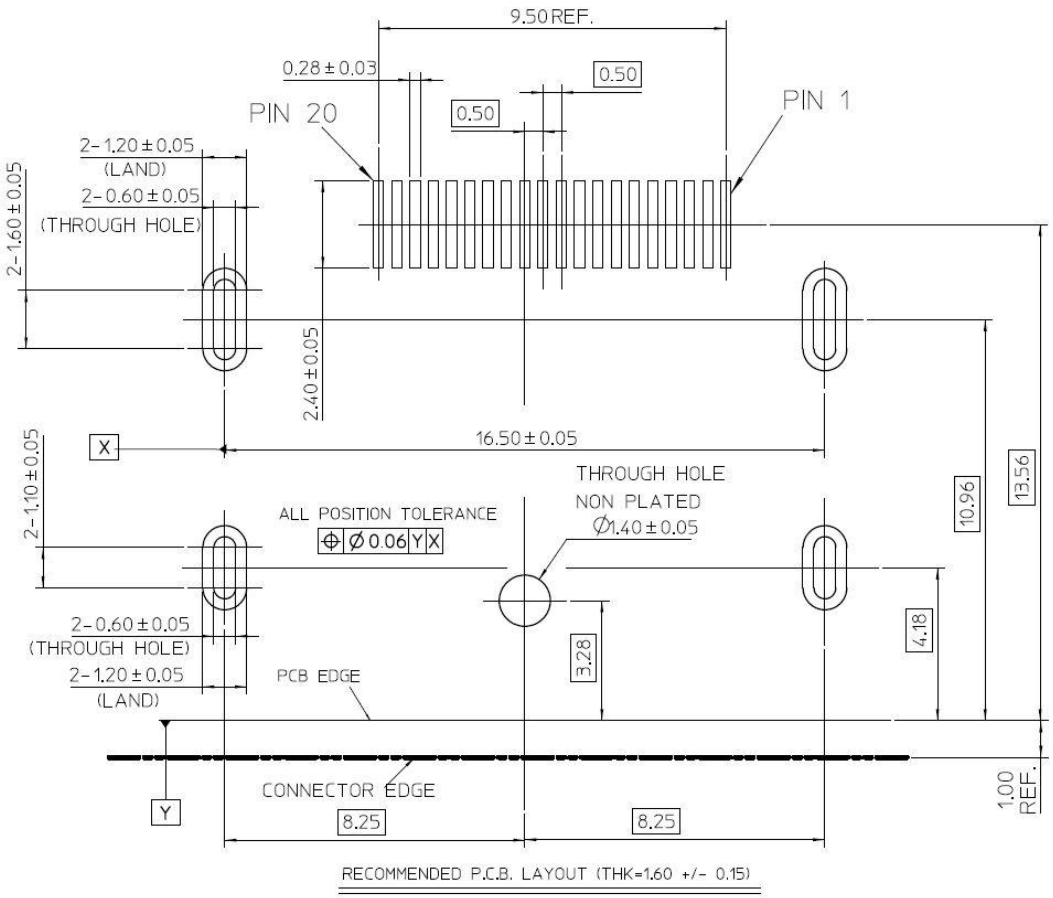


Figure 4-36: Recommended PCB Layout for DP External Cable-Connector Assembly

4.2.1.12 Reference Design for Four DP External Connectors on a PCI Card

Figure 4-37 illustrates a reference application design for four external connectors on a standard PCI card. Figure 4-38 illustrates the panel cut-out reference dimensions.

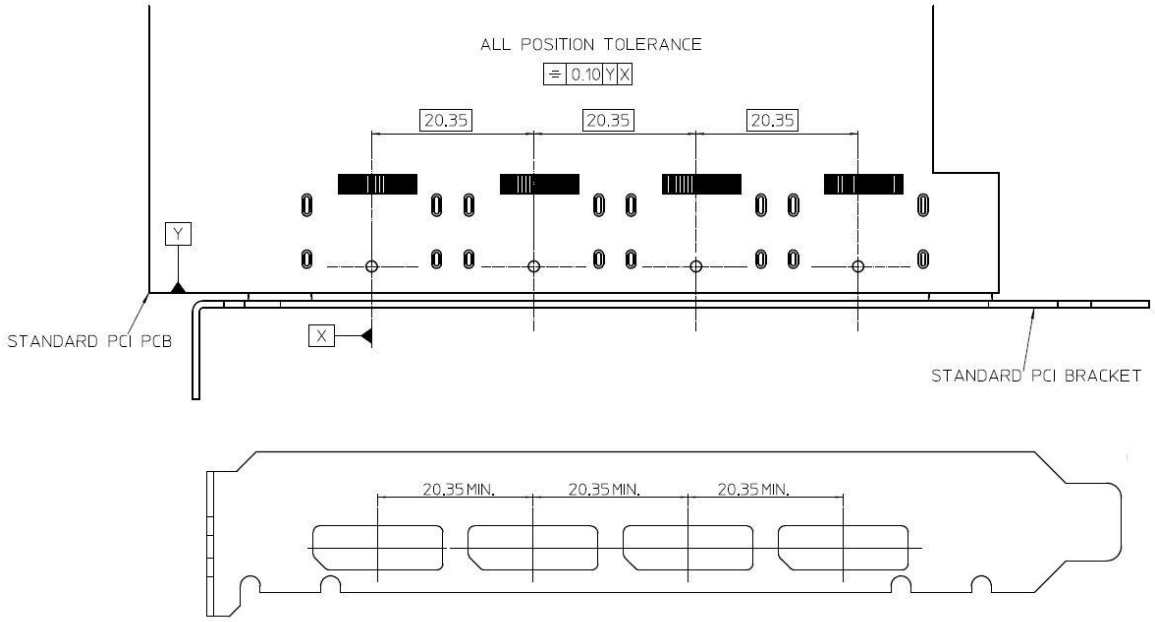


Figure 4-37: Reference Design for Four DP External Connectors on a PCI Card

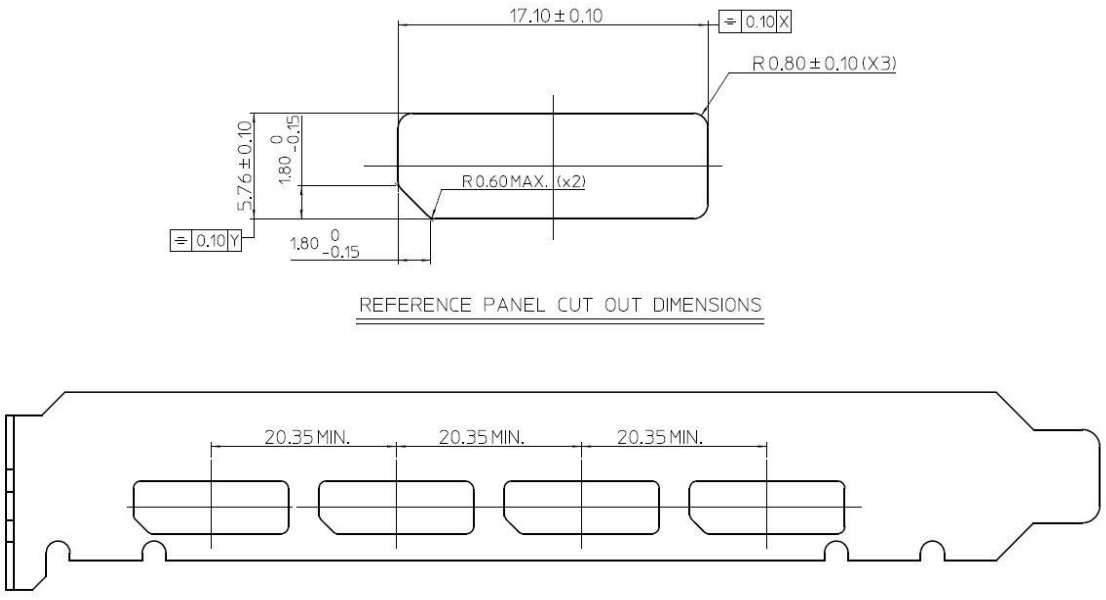


Figure 4-38: Panel Cut Out Reference Dimensions

4.2.2 mDP External Connector

The mDP connector is intended for use as an external connector on Source devices where a small form factor connector is advantageous.

4.2.2.1 mDP Connector Pin Assignment

Table 4-16 defines the pin assignments of the mDP external connector on a DFP on an upstream device.

Table 4-16: DFP mDP Connector Pin Assignment

Top Row			Bottom Row		
Pin Number	**Signal Type**	**Pin Name**	**Pin Number**	**Signal Type**	**Pin Name**
1	GND	**GND**	2	In	Hot Plug Detect
3	Out	ML_Lane_0_P	4	CONFIG[a]	CONFIG1
5	Out	ML_Lane_0_N	6	CONFIG[a]	CONFIG2
7	GND	**GND**	8	GND	**GND**
9	Out	ML_Lane_1_P	10	Out	ML_Lane_3_P
11	Out	ML_Lane_1_N	12	Out	ML_Lane_3_N
13	GND	**GND**	14	GND	**GND**
15	Out	ML_Lane_2_P	16	I/O	AUX_CH_P
17	Out	ML_Lane_2_N	18	I/O	AUX_CH_N
19	GND	**GND**	20	PWR Out[b]	DP_PWR

a. Pins 4 and 6 shall be connected to ground through a pull-down device. External devices and cable assemblies shall be designed to not rely on a low-impedance ground path from these pins.

b. Pin 20, PWR Out, shall provide +3.3V ±10% with a maximum current of 500mA and minimum power capability of 1.5W.

Downstream devices should use the full-size DP connector on their UFPs. However, if a downstream device implements the mDP connector on a UFP, the connector shall use the pinout defined in Table 4-17.

Table 4-17: UFP mDP Connector Pin Assignment

Top Row			Bottom Row		
Pin Number	**Signal Type**	**Pin Name**	**Pin Number**	**Signal Type**	**Pin Name**
1	GND	**GND**	2	Out	Hot Plug Detect
3	In	ML_Lane_3_N	4	CONFIG[a]	CONFIG1
5	In	ML_Lane_3_P	6	CONFIG[a]	CONFIG2
7	GND	**GND**	8	GND	**GND**
9	In	ML_Lane_2_N	10	In	ML_Lane_0_N
11	In	ML_Lane_2_P	12	In	ML_Lane_0_P
13	GND	**GND**	14	GND	**GND**
15	In	ML_Lane_1_N	16	I/O	AUX_CH_P
17	In	ML_Lane_1_P	18	I/O	AUX_CH_N
19	GND	**GND**	20	PWR Out[b]	DP_PWR

a. Pins 4 and 6 shall be connected to ground through a pull-down device. External devices and cable assemblies shall be designed to not rely on a low-impedance ground path from these pins.

b. Pin 20, PWR Out, shall provide +3.3V ±10% with a maximum current of 500mA and minimum power capability of 1.5W.

A cable assembly may be constructed with an mDP plug at both ends, or an mDP plug at one end and a full-size DP plug at the other end, or a full-size DP plug at both ends. The standard external cable connector assembly shall not have a wire on pin 20, DP_PWR.

Figure 4-39 illustrates an external cable connector assembly's wiring when an mDP plug is used at both ends.

mDP DFP Connector			mDP-to-mDP Cable Assembly			mDP UFP Connector		
Signal Type	Pin Name	Pin	Plug Pin	Direction	Plug Pin	Pin	Pin Name	Signal Type
GND	GND	1	1	⟷	8	8	GND	GND
Out	ML_Lane_0_P	3	3	⟷	12	12	ML_Lane_0_P	In
Out	ML_Lane_0_N	5	5	⟷	10	10	ML_Lane_0_N	In
GND	GND	7	7	⟷	13	13	GND	GND
Out	ML_Lane_1_P	9	9	⟷	17	17	ML_Lane_1_P	In
Out	ML_Lane_1_N	11	11	⟷	15	15	ML_Lane_1_N	In
GND	GND	13	13	⟷	7	7	GND	GND
Out	ML_Lane_2_P	15	15	⟷	11	11	ML_Lane_2_P	In
Out	ML_Lane_2_N	17	17	⟷	9	9	ML_Lane_2_N	In
GND	GND	19	19	⟷	19	19	GND	GND
In	Hot Plug Detect	2	2	⟷	2	2	Hot Plug Detect	Out
CFG	CONFIG1	4	4	⟷	4	4	CONFIG1	CFG
CFG	CONFIG2	6	6	⟷	6	6	CONFIG2	CFG
GND	GND	8	8	⟷	1	1	GND	GND
Out	ML_Lane_3_P	10	10	⟷	5	5	ML_Lane_3_P	In
Out	ML_Lane_3_N	12	12	⟷	3	3	ML_Lane_3_N	In
GND	GND	14	14	⟷	14	14	GND	GND
I/O	AUX_CH_P	16	16	⟷	16	16	AUX_CH_P	I/O
I/O	AUX_CH_N	18	18	⟷	18	18	AUX_CH_N	I/O
PWR Out	DP_PWR	20	20	(no connection)	20	20	DP_PWR	PWR Out

Figure 4-39: mDP Cable Connector Assembly Wiring

Figure 4-40 and Figure 4-41 illustrate an external cable connector assembly's wiring when an mDP plug is used at one end and a full-size DP plug is used at the other end.

mDP DFP Connector			mDP-to-DP Cable Assembly			DP UFP Connector		
Signal Type	Pin Name	Pin	Plug Pin	Direction	Plug Pin	Pin	Pin Name	Signal Type
GND	GND	1	1	⟷	11	11	GND	GND
Out	ML_Lane_0_P	3	3	⟷	12	12	ML_Lane_0_P	In
Out	ML_Lane_0_N	5	5	⟷	10	10	ML_Lane_0_N	In
GND	GND	7	7	⟷	8	8	GND	GND
Out	ML_Lane_1_P	9	9	⟷	9	9	ML_Lane_1_P	In
Out	ML_Lane_1_N	11	11	⟷	7	7	ML_Lane_1_N	In
GND	GND	13	13	⟷	5	5	GND	GND
Out	ML_Lane_2_P	15	15	⟷	6	6	ML_Lane_2_P	In
Out	ML_Lane_2_N	17	17	⟷	4	4	ML_Lane_2_N	In
GND	GND	19	19	⟷	19	19	GND	GND
In	Hot Plug Detect	2	2	⟷	18	18	Hot Plug Detect	Out
CFG	CONFIG1	4	4	⟷	13	13	CONFIG1	CFG
CFG	CONFIG2	6	6	⟷	14	14	CONFIG2	CFG
GND	GND	8	8	⟷	2	2	GND	GND
Out	ML_Lane_3_P	10	10	⟷	3	3	ML_Lane_3_P	In
Out	ML_Lane_3_N	12	12	⟷	1	1	ML_Lane_3_N	In
GND	GND	14	14	⟷	16	16	GND	GND
I/O	AUX_CH_P	16	16	⟷	15	15	AUX_CH_P	I/O
I/O	AUX_CH_N	18	18	⟷	17	17	AUX_CH_N	I/O
PWR Out	DP_PWR	20	20	(no connection)	20	20	DP_PWR	PWR Out

Figure 4-40: mDP-to-DP Cable Connector Assembly Wiring

DP DFP Connector			DP-to-mDP Cable Assembly			mDP UFP Connector		
Signal Type	Pin Name	Pin	Plug Pin	Direction	Plug Pin	Pin	Pin Name	Signal Type
GND	GND	2	2	⟷	8	8	GND	GND
Out	ML_Lane_0_P	1	1	⟷	12	12	ML_Lane_0_P	In
Out	ML_Lane_0_N	3	3	⟷	10	10	ML_Lane_0_N	In
GND	GND	5	5	⟷	13	13	GND	GND
Out	ML_Lane_1_P	4	4	⟷	17	17	ML_Lane_1_P	In
Out	ML_Lane_1_N	6	6	⟷	15	15	ML_Lane_1_N	In
GND	GND	8	8	⟷	7	7	GND	GND
Out	ML_Lane_2_P	7	7	⟷	11	11	ML_Lane_2_P	In
Out	ML_Lane_2_N	9	9	⟷	9	9	ML_Lane_2_N	In
GND	GND	19	19	⟷	19	19	GND	GND
In	Hot Plug Detect	18	18	⟷	2	2	Hot Plug Detect	Out
CFG	CONFIG1	13	13	⟷	4	4	CONFIG1	CFG
CFG	CONFIG2	14	14	⟷	6	6	CONFIG2	CFG
GND	GND	11	11	⟷	1	1	GND	GND
Out	ML_Lane_3_P	10	10	⟷	5	5	ML_Lane_3_P	In
Out	ML_Lane_3_N	12	12	⟷	3	3	ML_Lane_3_N	In
GND	GND	16	16	⟷	14	14	GND	GND
I/O	AUX_CH_P	15	15	⟷	16	16	AUX_CH_P	I/O
I/O	AUX_CH_N	17	17	⟷	18	18	AUX_CH_N	I/O
PWR Out	DP_PWR	20	20	(no connection)	20	20	DP_PWR	PWR Out

Figure 4-41: DP-to-mDP Cable Connector Assembly Wiring

A resizing adapter may be constructed with an mDP plug at one end and a full-size DP connector at the other end. Such an adapter shall carry all 20 signals (including DP_PWR) and shall make the signal connections so that the mDP plug adapts to a full-size DP connector. Figure 4-42 illustrates a passive adapter's wiring with an mDP plug at one end and a full-size DP connector at the other end.

mDP DFP Connector			mDP-to-DP Adapter			DP Cable Plug		
Signal Type	Pin Name	Pin	Plug Pin	Direction	Connector Pin	Pin	Pin Name	Signal Type
GND	GND	1	1	⟷	2	2	GND	GND
Out	ML_Lane_0_P	3	3	⟷	1	1	ML_Lane_0_P	In
Out	ML_Lane_0_N	5	5	⟷	3	3	ML_Lane_0_N	In
GND	GND	7	7	⟷	5	5	GND	GND
Out	ML_Lane_1_P	9	9	⟷	4	4	ML_Lane_1_P	In
Out	ML_Lane_1_N	11	11	⟷	6	6	ML_Lane_1_N	In
GND	GND	13	13	⟷	8	8	GND	GND
Out	ML_Lane_2_P	15	15	⟷	7	7	ML_Lane_2_P	In
Out	ML_Lane_2_N	17	17	⟷	9	9	ML_Lane_2_N	In
GND	GND	19	19	⟷	19	19	GND	GND
In	Hot Plug Detect	2	2	⟷	18	18	Hot Plug Detect	Out
CFG	CONFIG1	4	4	⟷	13	13	CONFIG1	CFG
CFG	CONFIG2	6	6	⟷	14	14	CONFIG2	CFG
GND	GND	8	8	⟷	11	11	GND	GND
Out	ML_Lane_3_P	10	10	⟷	10	10	ML_Lane_3_P	In
Out	ML_Lane_3_N	12	12	⟷	12	12	ML_Lane_3_N	In
GND	GND	14	14	⟷	16	16	GND	GND
I/O	AUX_CH_P	16	16	⟷	15	15	AUX_CH_P	I/O
I/O	AUX_CH_N	18	18	⟷	17	17	AUX_CH_N	I/O
PWR Out	DP_PWR	20	20	⟷	20	20	DP_PWR	PWR Out

Figure 4-42: mDP-to-DP Adapter Wiring

A resizing adapter may be constructed with a DP plug at one end and an mDP connector at the other end. Such an adapter shall carry all 20 signals (including DP_PWR) and shall make the signal connections so that the full-size DP plug adapts to an mDP connector. Figure 4-43 illustrates a passive adapter's wiring with a DP plug at one end and an mDP connector at the other end.

DP DFP Connector			DP-to-mDP Adapter			mDP Cable Plug		
Signal Type	Pin Name	Pin	Plug Pin	Direction	Connector Pin	Pin	Pin Name	Signal Type
GND	GND	2	2	←	1	1	GND	GND
Out	ML_Lane_0_P	1	1	←	3	3	ML_Lane_0_P	In
Out	ML_Lane_0_N	3	3	←	5	5	ML_Lane_0_N	In
GND	GND	5	5	←	7	7	GND	GND
Out	ML_Lane_1_P	4	4	←	9	9	ML_Lane_1_P	In
Out	ML_Lane_1_N	6	6	←	11	11	ML_Lane_1_N	In
GND	GND	8	8	←	13	13	GND	GND
Out	ML_Lane_2_P	7	7	←	15	15	ML_Lane_2_P	In
Out	ML_Lane_2_N	9	9	←	17	17	ML_Lane_2_N	In
GND	GND	19	19	←	19	19	GND	GND
In	Hot Plug Detect	18	18	←	2	2	Hot Plug Detect	Out
CFG	CONFIG1	13	13	←	4	4	CONFIG1	CFG
CFG	CONFIG2	14	14	←	6	6	CONFIG2	CFG
GND	GND	11	11	←	8	8	GND	GND
Out	ML_Lane_3_P	10	10	←	10	10	ML_Lane_3_P	In
Out	ML_Lane_3_N	12	12	←	12	12	ML_Lane_3_N	In
GND	GND	16	16	←	14	14	GND	GND
I/O	AUX_CH_P	15	15	←	16	16	AUX_CH_P	I/O
I/O	AUX_CH_N	17	17	←	18	18	AUX_CH_N	I/O
PWR Out	DP_PWR	20	20	←	20	20	DP_PWR	PWR Out

Figure 4-43: DP-to-mDP Adapter Wiring

An extender may be constructed with an mDP plug at one end and an mDP connector at the other end. Such an adapter shall carry 20 signals and make the signal connections so that the mDP plug connects to an mDP connector. Figure 4-44 illustrates a passive extender's wiring with an mDP plug at one end and an mDP connector at the other end.

mDP DFP Connector			mDP Plug-to-mDP Connector Cable Assembly			mDP Cable Plug		
Signal Type	**Pin Name**	**Pin**	**Plug Pin**	**Direction**	**Connector Pin**	**Pin**	**Pin Name**	**Signal Type**
GND	**GND**	1	1	⟷	1	1	**GND**	GND
Out	ML_Lane_0_P	3	3	⟷	3	3	ML_Lane_0_P	In
Out	ML_Lane_0_N	5	5	⟷	5	5	ML_Lane_0_N	In
GND	**GND**	7	7	⟷	7	7	**GND**	GND
Out	ML_Lane_1_P	9	9	⟷	9	9	ML_Lane_1_P	In
Out	ML_Lane_1_N	11	11	⟷	11	11	ML_Lane_1_N	In
GND	**GND**	13	13	⟷	13	13	**GND**	GND
Out	ML_Lane_2_P	15	15	⟷	15	15	ML_Lane_2_P	In
Out	ML_Lane_2_N	17	17	⟷	17	17	ML_Lane_2_N	In
GND	**GND**	19	19	⟷	19	19	**GND**	GND
In	Hot Plug Detect	2	2	⟷	2	2	Hot Plug Detect	Out
CFG	CONFIG1	4	4	⟷	4	4	CONFIG1	CFG
CFG	CONFIG2	6	6	⟷	6	6	CONFIG2	CFG
GND	**GND**	8	8	⟷	8	8	**GND**	GND
Out	ML_Lane_3_P	10	10	⟷	10	10	ML_Lane_3_P	In
Out	ML_Lane_3_N	12	12	⟷	12	12	ML_Lane_3_N	In
GND	**GND**	14	14	⟷	14	14	**GND**	GND
I/O	AUX_CH_P	16	16	⟷	16	16	AUX_CH_P	I/O
I/O	AUX_CH_N	18	18	⟷	18	18	AUX_CH_N	I/O
PWR Out	DP_PWR	20	20	⟷	20	20	DP_PWR	PWR Out

Figure 4-44: mDP Cable Extender Wiring

4.2.2.2 mDP Connector Mechanical Performance Requirements

Table 4-18 defines the mechanical performance requirements for an mDP connector.

Table 4-18: mDP Connector Mechanical Performance Requirements

Item	Test Condition	Requirement	
Vibration	Amplitude: 1.52mm P-P or 147m/s^2 {15G} Sweep time: 50-2000-50Hz in 20 minutes. Duration: 12 times in each of X, Y, Z axes (Total of 36 times). Electrical load: DC 100mA current shall be conducted during the test. (*EIA-364-28*, Condition III, Method 5A)	Appearance	No Damage
		Contact Resistance	Contact: Change from initial value = 30mΩ maximum Shell Part: Change from initial value = 50mΩ maximum
		Discontinuity	1us maximum
Durability	Measure contact and shell resistance after the following. Automatic cycling: 10,000 cycles at 100 ± 50 cycles per hour (*EIA-364-09*)	Contact Resistance	**Contact:** Change from initial value = 30mΩ maximum Shell Part: Change from initial value = 50mΩ maximum
Insertion/ Withdrawal Force	Insertion and withdrawal speed: 25mm / minute. (*EIA-364-13*)	Withdrawal force	9.8N {1.0kgf} minimum 39.2N {4.0kgf} maximum
		Insertion force	44.1N {4.5kgf} maximum
Cable Flex	100 cycles in each of 2 planes. Dimension: $X = 3.7 \times$ Cable Diameter. (*EIA-364-41*, Condition I)	Discontinuity	1us maximum
		Dielectric Withstanding Voltage and Insulation Resistance.	Conform to item of dielectric withstanding voltage and insulation resistance

4.2.2.3 mDP Connector Electrical Performance Requirements

Table 4-19 defines the electrical performance requirements for an mDP connector.

Table 4-19: mDP Connector Electrical Performance Requirements

Item	Test Condition	Requirement
Low-Level Contact Resistance	Mated connectors. Contact: Measured by dry circuit, 20mV maximum, and 10mA. Shell: Measured by open circuit, 5V maximum, 100mA. (*EIA-364-23*)	Contact: Change from initial value = 30mΩ maximum Shell: Change from initial value = 50mΩ maximum
Dielectric Strength	Unmated connectors, apply 500Vrms between adjacent terminal and ground. (*EIA-364-20*, Method 301) Mated connector, apply 300Vrms between adjacent terminal and ground.	No Breakdown
Insulation Resistance	Unmated connectors, apply $500V_{DC}$ between adjacent terminal and ground. (*EIA-364-21*, Method 302)	Unmated: 100MΩ minimum
	Mated connectors, apply $150V_{DC}$ between adjacent terminal and ground.	Mated: 10MΩ minimum
Contact Current Rating	55°C, maximum ambient 85°C, maximum temperature change. (*EIA-364-70*)	0.5A minimum
Applied Voltage Rating	40Vrms continuous maximum, on any signal pin with respect to the shield.	No Breakdown
Electrostatic Discharge	Test signal and power pins of associated DP components (transmitter IC, receiver IC and associated I/O circuitry) to withstand *ANSI/ESDA/JEDEC JS-001* Class 2 (2000 to < 4000V) strikes.	After test, the DP component meets the part drawing requirements using parametric and functional testing.

4.2.2.4 mDP Connector Environmental Performance Requirements

Table 4-20 defines the environmental performance requirements for an mDP connector.

Table 4-20: mDP Connector Environment Performance Requirements

Item	Test Condition	Requirement	
Thermal Shock	10 cycles of: • -55°C for 30 minutes • +85°C for 30 minutes (*EIA-364-32*, Condition I)	Appearance	No Damage
		Contact Resistance	Contact: Change from initial value = 30mΩ maximum Shell Part: Change from initial value = 50mΩ maximum
Humidity	A) Mate connectors together and perform the test as follows: Temperature: +25 to +85°C Relative Humidity: 80 to 95% Duration: Four cycles (96 hours) Upon completion of the test, specimens shall be conditioned at ambient room conditions for 24 hours, after which the specified measurements shall be performed. (*EIA-364-31*)	Appearance	No Damage
		Contact Resistance	Contact: Change from initial value = 30mΩ maximum Shell Part: Change from initial value = 50mΩ maximum
	B) Unmate connectors and perform the test as follows: Temperature: +25 to +85°C Relative Humidity: 80 to 95% Duration: Four cycles (96 hours) Upon completion of the test, specimens shall be conditioned at ambient room conditions for 24 hours, after which the specified measurements shall be performed. (*EIA-364-31*)	Appearance	No Damage
		Dielectric Withstanding Voltage and Insulation Resistance	Conform to item of Dielectric Withstanding Voltage and Insulation Resistance
Thermal Aging	Mate connectors and expose to (+105 ±2)°C for 250 hours. Upon completion of the exposure period, the test specimens shall be conditioned at ambient room conditions for one to two hours after which the specified measurements shall be performed. (*EIA-364-17*, Condition 4, Method A)	Appearance	No Damage
		Contact Resistance	Contact: Change from initial value = 30mΩ maximum Shell Part: Change from initial value = 50mΩ maximum

4.2.2.5 Connector Performance Test Sequence

To evaluate connector performance, the test sequence shall follow Test Groups 1, 2, 3, and 7 in *EIA-364-1000.01*.

4.2.2.6 mDP Cable-Connector (Plug) Dimensions

Figure 4-45 and Figure 4-46 illustrate the mDP plug dimensions, including maximum external dimensions for the overmold. The external shape of the overmold cross-section is shown for illustration purposes only and is not part of this Standard. A plug shall meet all dimensions and tolerances shown.

All dimensions are in mm. Except where specified otherwise, tolerances are x.x ±0.2, x.xx ±0.10, x.xxx ±0.050, angles ±0.5°.

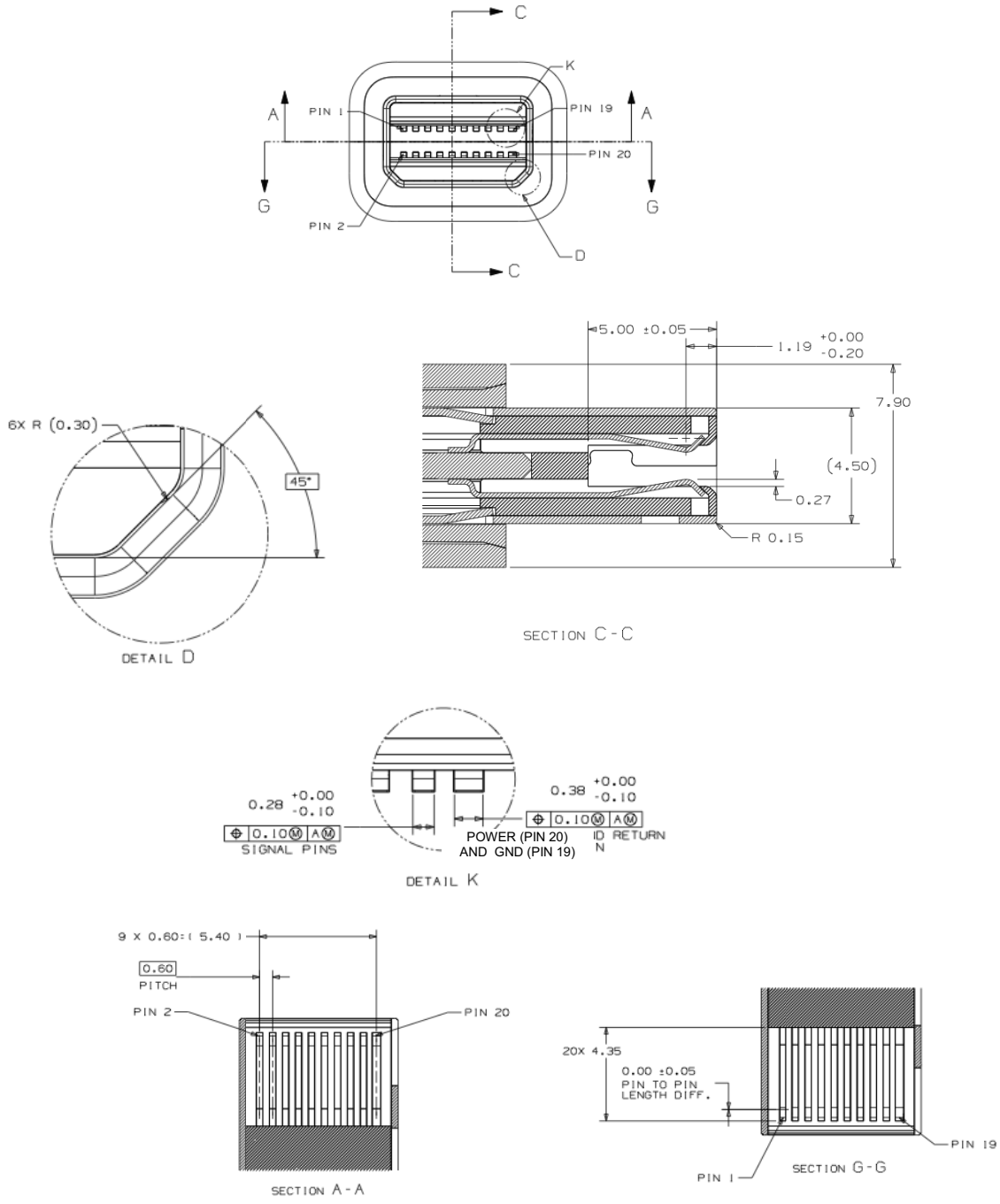


Figure 4-45: mDP Cable-Connector (Plug) Dimensions – 1

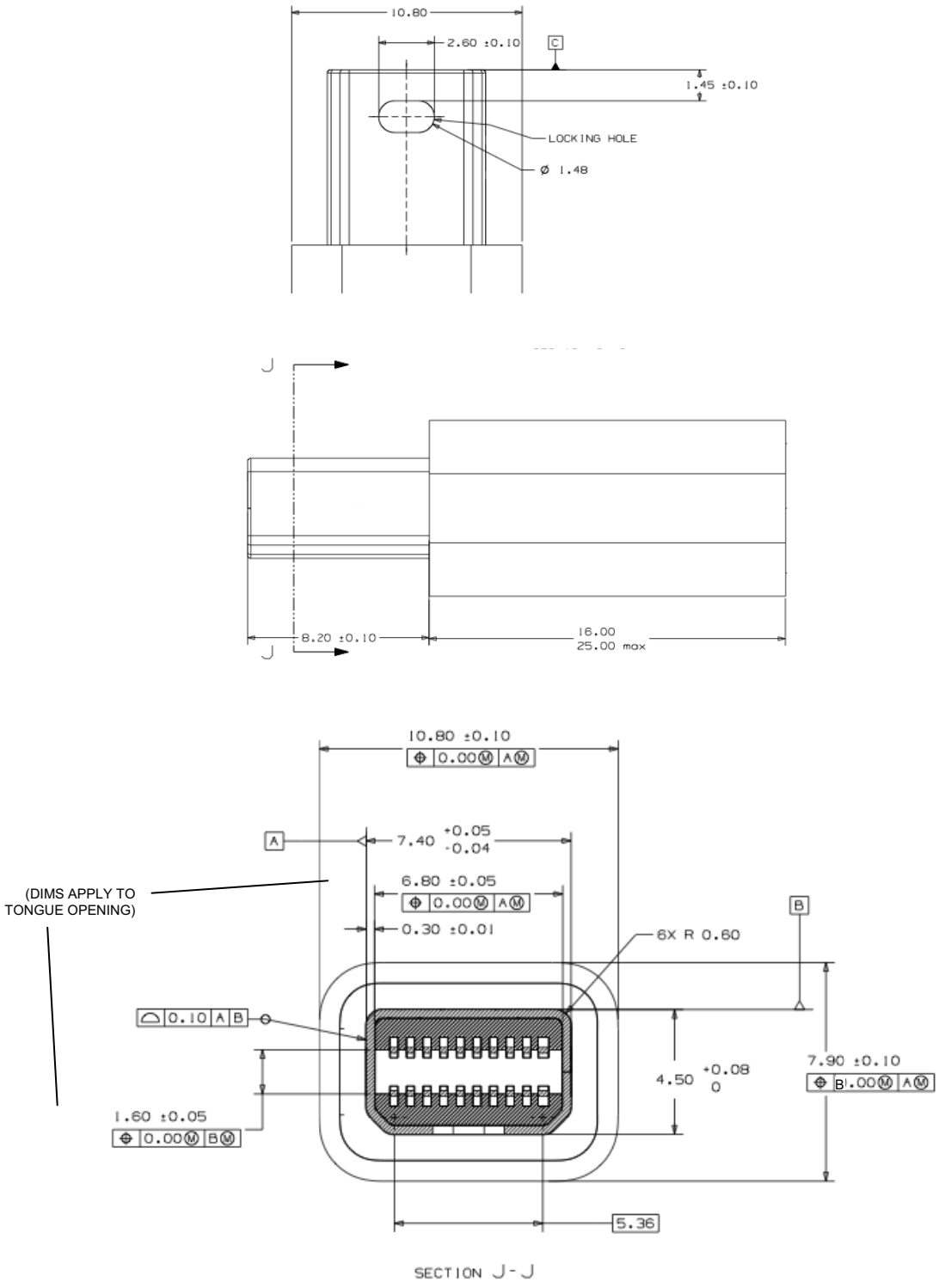


Figure 4-46: mDP Cable-Connector (Plug) Dimensions – 2

4.2.2.7 Mini DisplayPort Connector (Receptacle) Dimensions

Figure 4-47 and Figure 4-48 illustrate the mDP connector dimensions. A connector shall meet all dimensions and tolerances shown.

All dimensions are in mm. Except where specified otherwise, tolerances are x.x ±0.2, x.xx ±0.10, x.xxx ±0.050, angles ±0.5°.

See also Section 4.2.2.8 for the necessary mating sequence, Section 4.2.2.9 for the necessary panel allowance, and Section 4.2.2.10 for an appropriate PCB mounting.

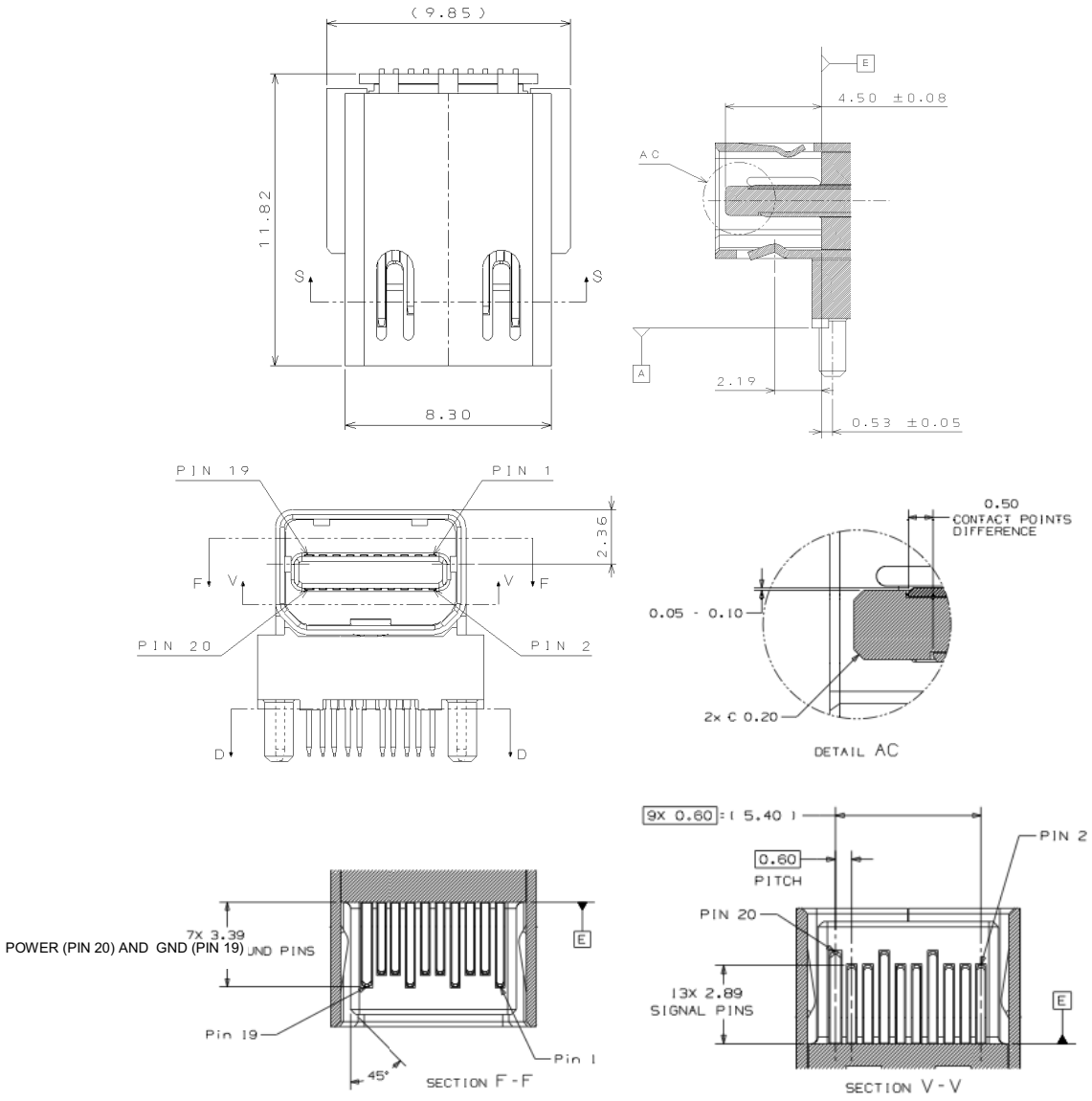


Figure 4-47: Mini DisplayPort Connector (Receptacle) Dimensions – 1

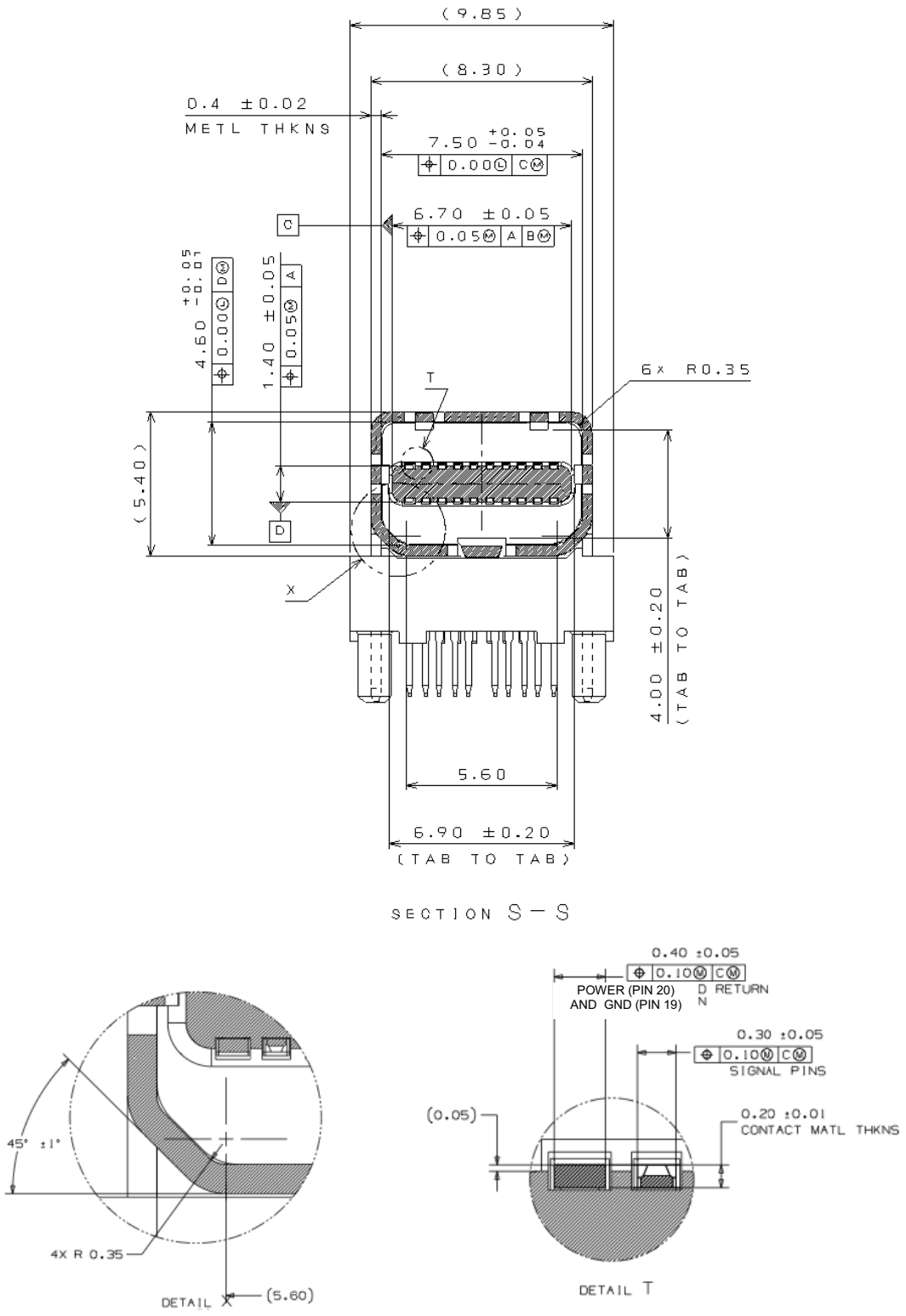


Figure 4-48: Mini DisplayPort Connector (Receptacle) Dimensions – 2

4.2.2.8 mDP Mating Sequence

An mDP receptacle shall be designed to ensure the correct mating sequence. Table 4-21 presents the legend for signal name/type mating level.

Table 4-21: mDP Mating Sequence Level

Signal Type		Level
Connector Shell		First Mate[a]
DP_PWR	GND	Second Mate
AUX_CH_P, AUX_CH_N, ML_Lane_0_P, ML_Lane_0_N, ML_Lane_1_P, ML_Lane_1_N, ML_Lane_2_P, ML_Lane_2_N, ML_Lane_3_P, ML_Lane_3_N	Hot Plug Detect, CONFIG1, CONFIG2	Third Mate

a. EMC fingers on the shell may mate after all contacts have mated.

Figure 4-49 illustrates the mating levels of a fully mated mDP receptacle and plug. All dimensions are in mm. Except where specified otherwise, tolerances are x.x ±0.2, x.xx ±0.10, x.xxx ±0.050, angles ±0.5°.

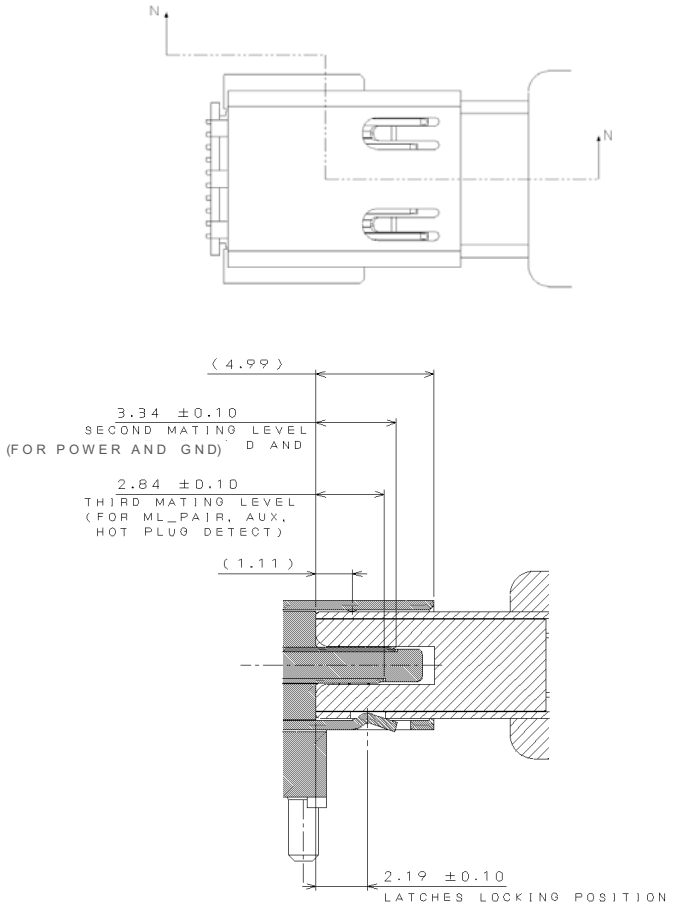


Figure 4-49: Fully Mated mDP Connector Illustrating Mating Levels

4.2.2.9 Mini DisplayPort Panel Allowances

Figure 4-49 illustrates the plug protrusion in the fully mated condition of the plug and the board receptacles. The system design incorporating an mDP receptacle shall be designed so that an mDP plug fully mates with the mDP receptacle with appropriate margin, but with sufficient control to prevent an incorrect mating sequence due to angled insertion. The receptacle design shall provide an appropriate allowance for a panel, bezel or similar (when used) so that this requirement is met. To meet these requirements, the distance from datum E in the receptacle to the externally accessible mating interface on the device shall be at least 5.7mm and shall not exceed 8.0mm.

4.2.2.10 Recommended PCB Mounting

The mounting for the mDP connector to a PCB should use surface-mount contacts for the mating interface top row of pins and thru-hole contacts for the mating interface bottom row of pins. Figure 4-50 illustrates the mDP connector's PCB interface (i.e., the sizes and positions of the surface mount contacts, thru-hole contacts, and locating lugs). The actual landing pad design to receive these contacts shall be system-dependent.

All dimensions are in mm. Except where specified otherwise, tolerances are x.x ±0.2, x.xx ±0.10, x.xxx ±0.050, angles ±0.5°.

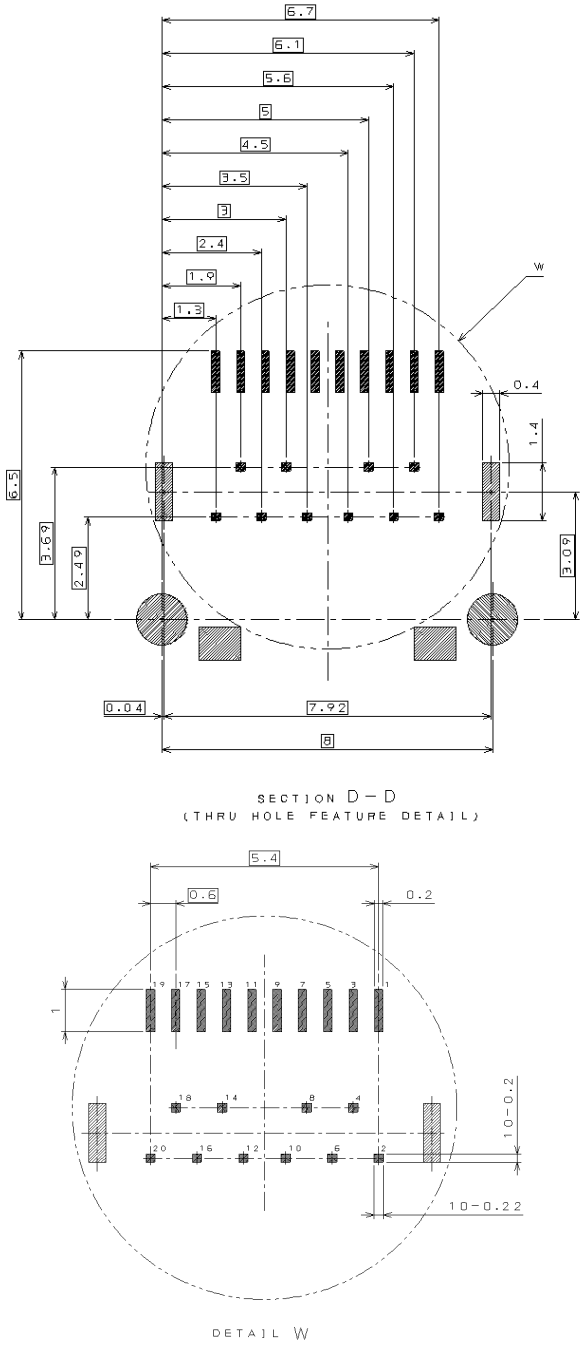


Figure 4-50: Recommended mDP Connector PCB Contacts and Mounting

4.2.2.11 Reference Design for Four mDP Connectors on a Reduced Height PCI Card

Figure 4-51 and Figure 4-52 illustrate a reference application design for four mDP connectors on a low-profile PCI/PCI Express card.

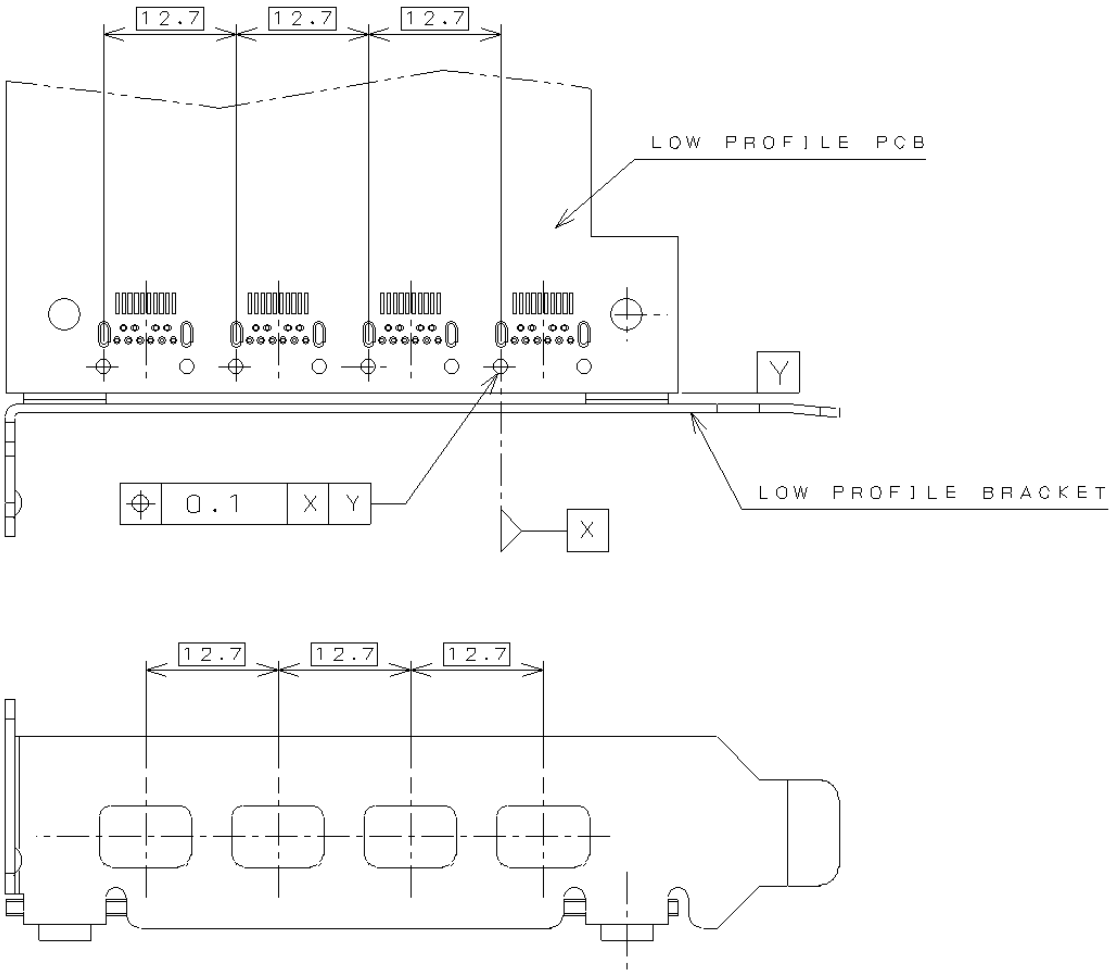


Figure 4-51: Reference Design for Four mDP Connectors on a Reduced Height PCI Card – 1

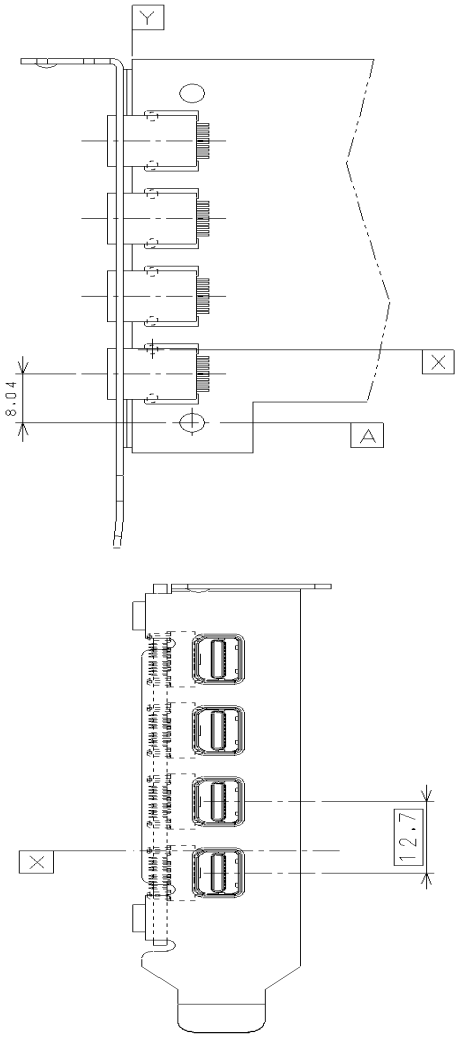


Figure 4-52: Reference Design for Four mDP Connectors on a Reduced Height PCI Card – 2

4.2.3 Panel-side Internal Connector (Informative)

This section covers the specifications for DP panel-side internal connector for reference purposes.

The panel-side internal connector consist of a two-piece, 30-position, low-profile, cable-to-board, co-planar connector. One piece terminates the cable (Plug) and the other is attached to the PCB (Receptacle).

The connector supports up to four Main-Link lanes (Lanes 0, 1, 2, and 3). In an embedded connection, the cable connector assembly may support one, two, or four lanes, depending on the bandwidth requirement of the application.

For one lane and two lane Main-Link configurations, the stuffing rule shall be:

- When only two lanes are needed, Lanes 0 and 1 shall be populated, while Lanes 2 and 3 are unpopulated.
- When only one lane is needed, Lane 0 shall be populated, while Lanes 1, 2, and 3 are unpopulated.

Only the panel TCON (timing controller) side of the connector is defined in this specification. While some cables may have the same connectors on both ends of the cable-connector assembly, others may have more pins for the Source device side (e.g., the side of graphics processor, LCD controller, etc.), such as for LCD backlight control.

4.2.3.1 Panel-side Internal Connector Pin Assignment

Table 4-22 defines the pin assignment of the DP panel-side internal connector. Pin assignment of those pins other than the DP Main-Link and AUX_CH in Table 4-22 is for reference purpose only. For pin 1 location, see Figure 4-53.

Table 4-22: DP Panel-side Internal Connector Pin Assignment

Pin #	Pin Name	Pin Definition
Frame		Outer shell
1	RESERVED	
2	LCDVCC	Power to LCD panel
3	LCDVCC	
4	LCDVCC	
5	LCDVCC	
6	GND	Power Return (Ground)
7	GND	
8	GND	
9	GND	
10	HPD	Hot Plug Detect Optional
11	RESERVED	
12	RESERVED	
13	H_GND	High Speed (Main-Link) Ground
14	ML_Lane_3_N	‘Complement’ Signal-Main-Link
15	ML_Lane_3_P	‘True’ Signal-Main-Link
16	H_GND	High Speed (Main-Link) Ground
17	ML_Lane_2_N	‘Complement’ Signal-Main-Link
18	ML_Lane_2_P	‘True’ Signal-Main-Link
19	H_GND	High Speed (Main-Link) Ground
20	ML_Lane_1_N	‘Complement’ Signal-Main-Link
21	ML_Lane_1_P	‘True’ Signal-Main-Link
22	H_GND	High Speed (Main-Link) Ground
23	ML_Lane_0_N	‘Complement’ Signal-Main-Link
24	ML_Lane_0_P	‘True’ Signal-Main-Link
25	H_GND	High Speed (Main-Link) Ground
26	AUX_CH_P	‘True’ Signal – AUX_CH
27	AUX_CH_N	‘Complement’ Signal – AUX_CH
28	H_GND	High Speed (Main-Link) Ground
29	AUX_PWR	+3.3 Trickle PWR
30	RESERVED	
Frame		Outer shell

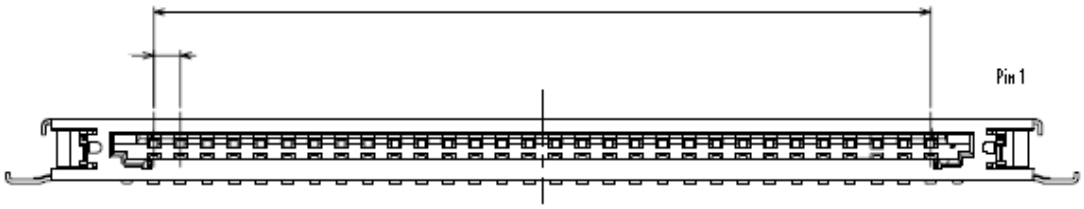
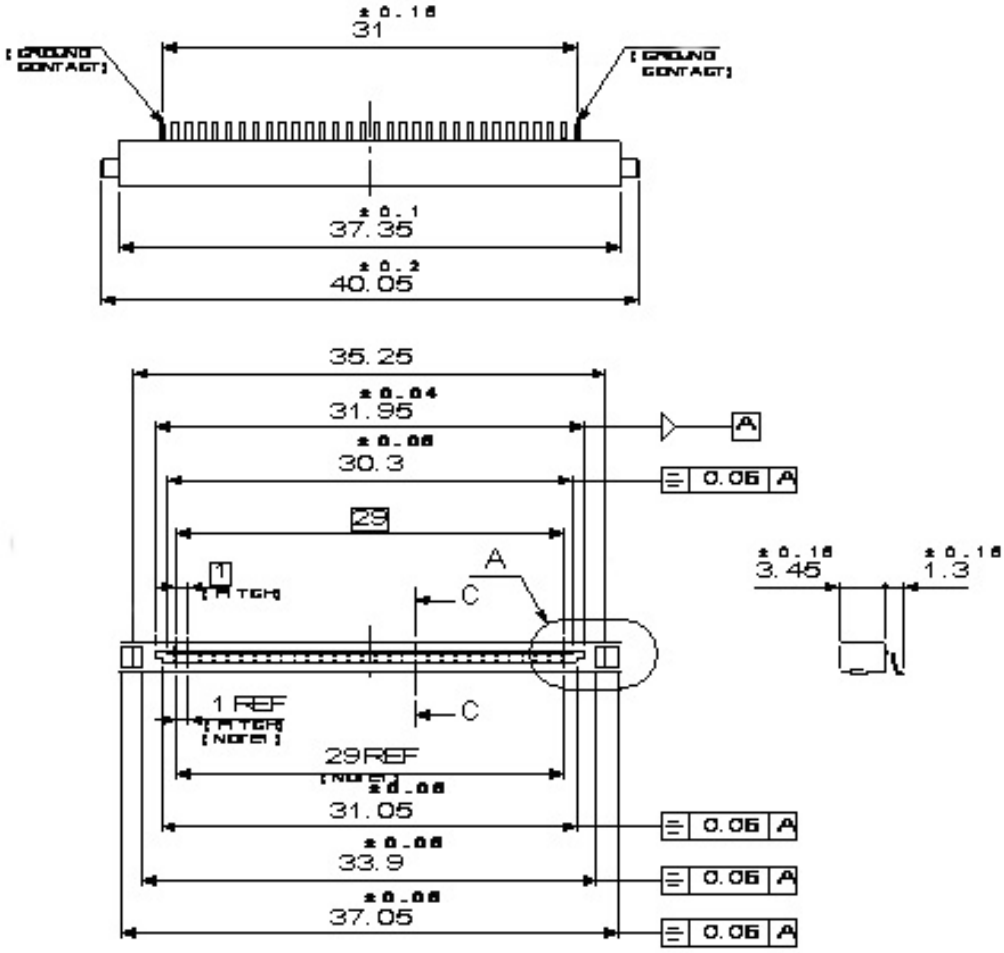


Figure 4-53: Panel-side Internal PCB Mount Receptacle Connector with Pin 1 Shown

4.2.3.2 Panel-side Internal Receptacle Connector

Figure 4-54 through Figure 4-56 illustrate the DP panel-side internal PCB receptacle connector and the recommended footprint layout, respectively.



Note: *This dimension shows ground contact.*

Figure 4-54: Panel-side Internal PCB Mount Receptacle Connector (in mm) – 1

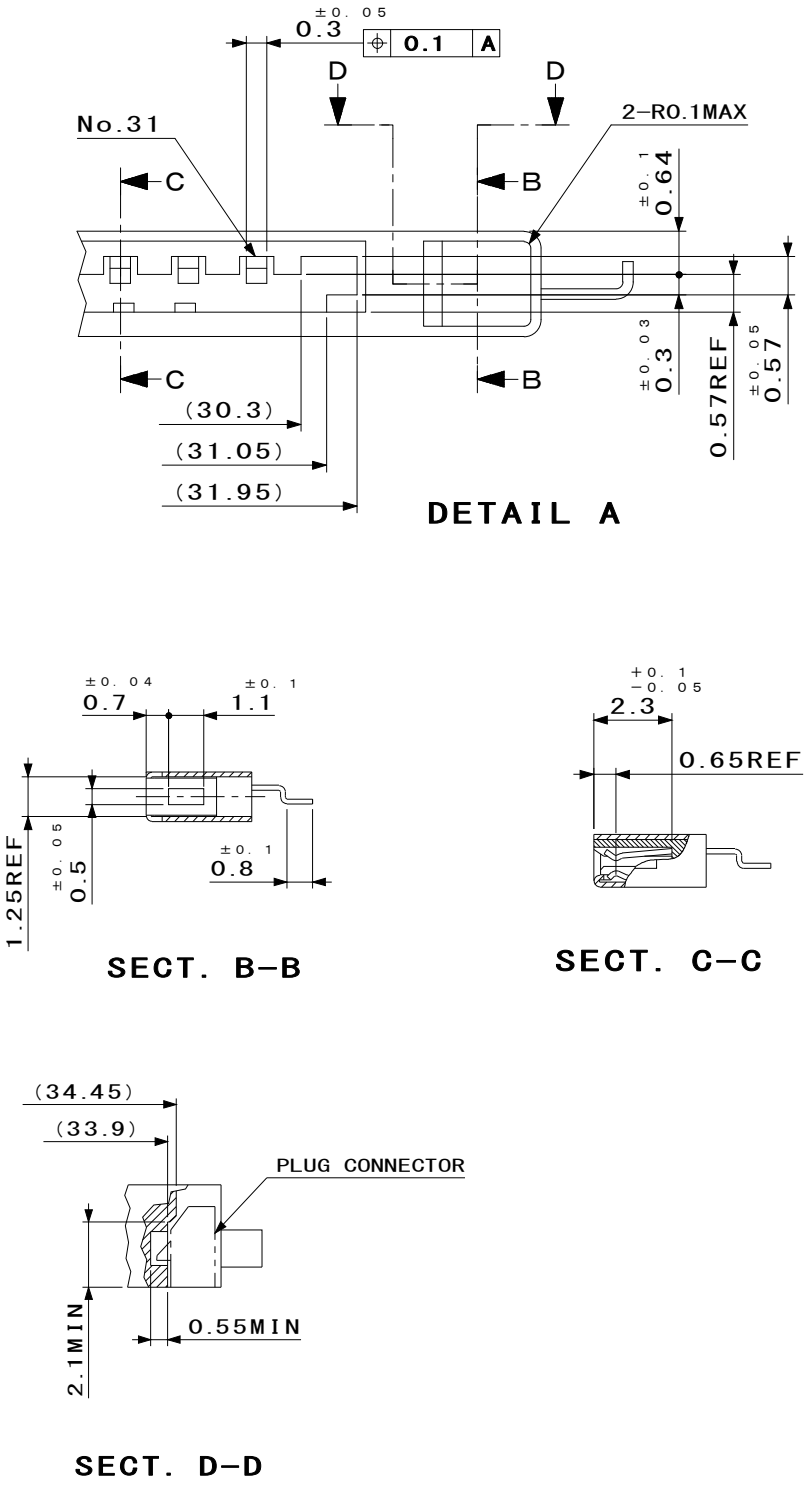


Figure 4-55: Panel-side Internal PCB Mount Receptacle Connector (in mm) – 2

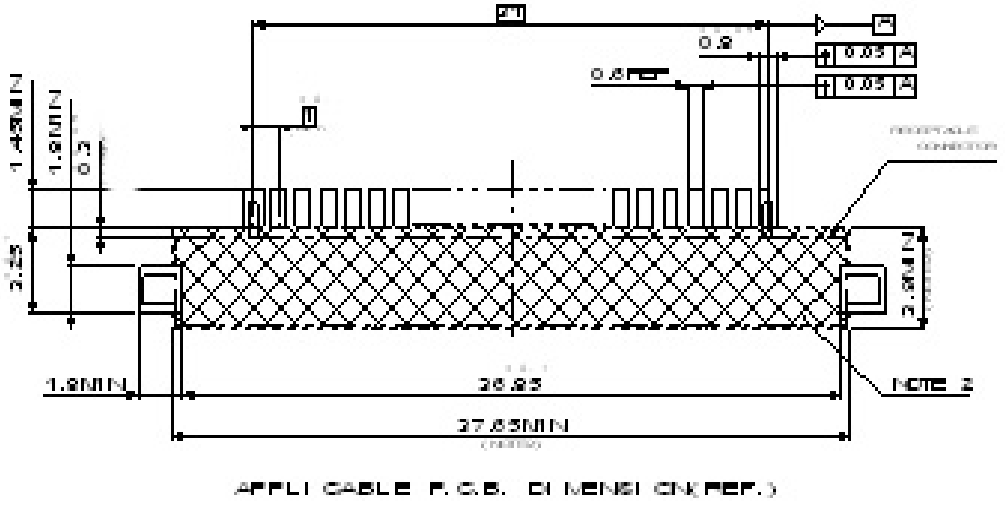
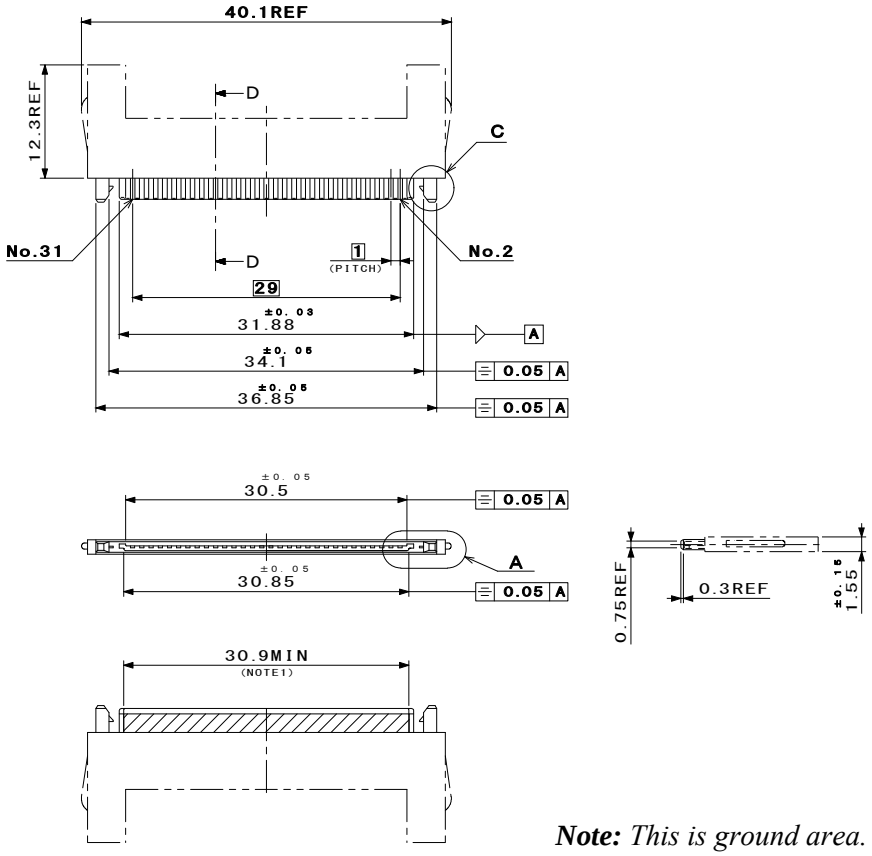


Figure 4-56: PCB Mount Connector Recommended Footprint Layout (in mm)

4.2.3.3 Panel-side Internal Plug Connector

Figure 4-57 illustrates the DP panel-side internal cable plug connector.

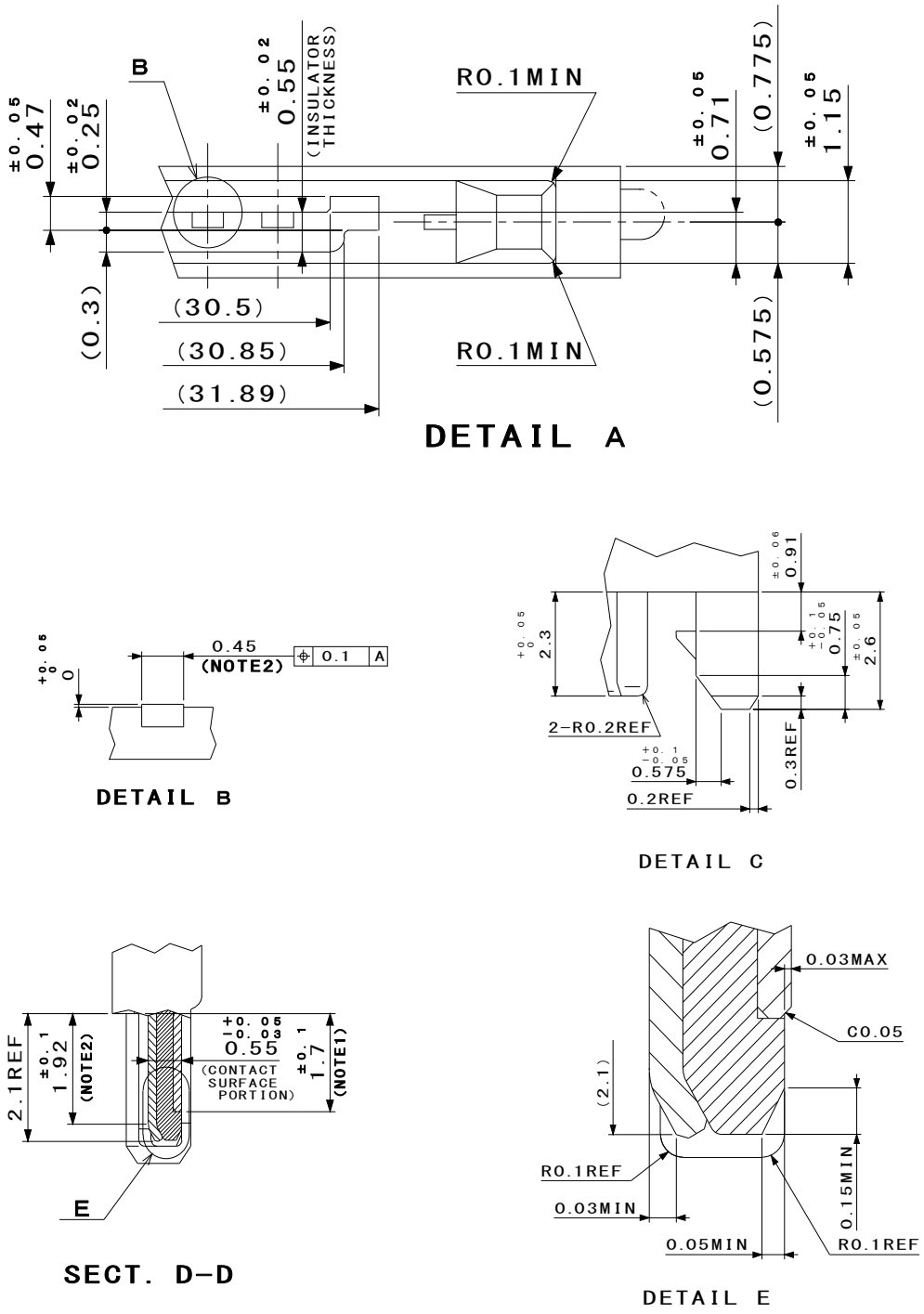


Note: *This is ground area.*

Figure 4-57: Panel-side Internal Cable Plug Connector (in mm)

4.2.3.4 Panel-side Internal Plug Connector – Contact and Mechanical Guide Details

Figure 4-58 and Figure 4-59 illustrate the contact and mechanical guide details.



Note 1: *This area is ground area.*

Note 2: *This area is signal contact area.*

Figure 4-58: Contact and Mechanical Guide Details (in mm)

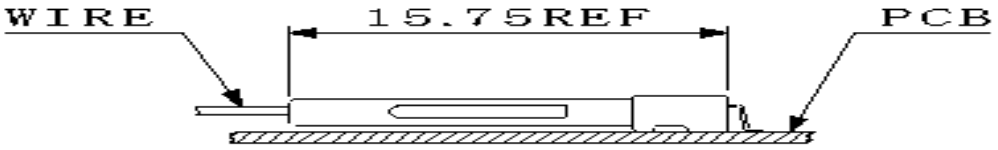


Figure 4-59: Mating Condition (Reference) of Panel Side Internal Cable Connector (in mm)

4.2.3.5 Panel-side Connector Mechanical Requirements

Table 4-23 defines the panel-side connector mechanical requirements.

Table 4-23: Panel-side Connector Mechanical Requirements

Item	Test Condition	Requirement
Vibration (random)	Frequency: 10 to 2000Hz Acceleration Velocity: 30.38m/s^2 (3.1G) RMS. Action direction: In each of three mutually perpendicular planes. Duration: 15 minutes each sample. (*EIA-364-28*, Test condition VII, Test condition D)	100mA applied with no electrical discontinuity greater than 1us.s
Physical shock	Sample should be mounted on the test jig as mounted on the PCB. Acceleration velocity: 490m/s^2 or 50G. Waveform: half sine Duration: 11ms. Number of drops: Three drops each to normal and reversed directions of X,Y, and Z axes. Total 18 drops. (*EIA-364-27*, Method A)	No electrical discontinuity greater than 1us shall occur.
Durability (mating and unmating)	Number of cycles: 50 Automatic Cycling: 100 ±50 cycles per hour (*EIA-364-09*)	R = 40mΩ maximum (initially) ΔR = 20mΩ maximum (final)
Durability (preconditioning)	Number of cycles: 20 (*EIA-364-09*)	No physical damage.
Connector insertion force	Operation speed: 12.5mm/minute Measure the force necessary to mate the connector including the latching mechanism. (*EIA-364-13*)	35N maximum per connector (30 pin).
Connector withdrawal force	Operation speed: 12.5mm/minute Measure the force necessary to unmate the connector excluding the latching mechanism. (*EIA-364-13*)	5N minimum to 25N maximum per connector (30 pin).

4.2.3.6 Panel-side Connector Electrical Requirements

Table 4-24 defines the panel-side connector electrical requirements.

Table 4-24: Panel-side Connector Electrical Requirements

Item	Test Condition	Requirement
Dielectric withstanding voltage	0.25-kV_{AC} for 1 minute. Test between adjacent circuits of unmated connectors. (*EIA-364-20*)	No creeping discharge or flashover shall occur. Current leakage: 0.5-mA maximum
Insulation resistance	Impressed voltage: $100V_{DC}$ Test between adjacent circuits of unmated connectors for 2 minutes. (*EIA-364-21*)	100-MΩ minimum (initial) 50-MΩ minimum (final)
Low-level contact resistance	Subject mated contacts assembled in housing measured by dry circuit 20-mV maximum open circuit at 10mA (*EIA-364-23*)	R = 40-mΩ maximum (initial) ΔR = 40-mΩ maximum (final)
Temperature rise	Measure temperature rise by energizing current. (*EIA-364-70*, Method 1)	30ºC maximum ΔT over ambient at maximum rated current (0.50A) per contact.

4.2.3.7 Panel-side Connector Environmental Requirements

Table 4-25 defines the panel-side connector environmental requirements.

Table 4-25: Panel-side Connector Environmental Requirements

Item	Test Condition	Requirement
Humidity and Temperature Cycling	Cycle Mated connector: 25 to 65ºC and 50 to 80% relative humidity 10 cycles and 10 cycles of cold shock at -10ºC. (*EIA-364-31*, Method 4)	Mating Condition: • Contact Resistance: • R = 80mΩ maximum (final) Unmating condition: • Insulation resistance: • R = 50MΩ maximum (final) • ΔR = 50MΩ maximum
Thermal Shock	Cycle mated connector from -55ºC for 30 minutes to 85ºC for 30 minutes, repeat for 10 cycles. (*EIA-364-32*)	R = 40mΩ minimum (initial) ΔR = 40mΩ maximum (final)
Temperature Life (heat age)	Submit mated connector to 105ºC for 168 hours. (*EIA-364-17*)	R = 40mΩ minimum (initial) ΔR = 40mΩ maximum (final)
Temperature Life (preconditioning)	Submit mated connector to 105ºC for 92 hours. (*EIA-364-17*)	No physical damage

5 Source/Sink/Branch Device Policy Requirements for Interoperability

This section describes support for DisplayPort devices and cable-connector assemblies to maximize the interoperability between Source and Sink devices over an open, box-to-box DP link.

For embedded connections, the system integrator shall ensure that the DP link meets the requirements of a given application. A closed, box-to-box connection between a captive Source and Sink device pair (designed to work only with one another) is regarded as an embedded connection. The Source and Sink device pair shall discover one another by checking the OUI and other device-specific values at the Source Device-specific field (DPCD Addresses 00300h through 003FFh; see Table 2-186) and Sink Device-specific field (DPCD Addresses 00400h through 004FFh; see Table 2-187), or Branch Device-specific field (DPCD Addresses 00500h through 005FFh; see Table 2-188) by way of AUX transactions.

The DisplayPort Logo shall be available only to devices that fully support the open, box-to-box DP connection. These products shall be certified and a license agreement with VESA completed before this logo may be used on products/packaging.

5.1 DP SST Source Device with 8b/10b Channel Coding

This section describes Source device support for box-to-box connections that operate in SST mode.

For embedded connections, the system integrator shall ensure that the Source device meets the requirements of a given application.

5.1.1 Stream Source Requirement

This sub-section describes support for the Stream Source in terms of video colorimetry, video timings, and audio formats.

The Stream Source shall support parsing of EDID r1.4 (or DisplayID) and, when feasible, should support parsing of the Sink device's extension blocks (both CTA Extension Block and DisplayID Extension Block).

5.1.1.1 Video Colorimetry

Updated in *DP v2.0*.

DP Source devices shall support sourcing of both RGB and YCbCr colorimetry formats defined in Table 5-1. A Source device shall indicate the pixel encoding/colorimetry format (including dynamic range) of the transmitted stream in the DP MSA data, as described in Section 2.2.4.

Table 5-1: Pixel Encoding/Colorimetry Format Support

Pixel Encoding/ Colorimetry Format	Bit-depth per Pixel (bpp)	Bit-depth per Component (bpc)	Dynamic Range[a]	Shall Be Supported vs. May Be Supported
RGB	18	6	"VESA range" only	May be supported
	24	8	"VESA range" or "CTA range"	Shall be supported
	30	10		May be supported
	36	12		
	48	16		
Y-only	8	8	"VESA range"	May be supported
	10	10		
	12	12		
	16	16		
YCbCr 4:2:0	12	8	"CTA range" ("VESA range" is also allowed if a DP Sink supports pixel encoding and colorimetry format indication by way of VSC SDP and declares support of the VESA range YCbCr by way of DisplayID or legacy EDID)	May be supported
	15	10		
	18	12		
	24	16		
YCbCr 4:2:2	16	8		Shall be supported when YCbCr is supported on any other display interface
	20	10		May be supported
	24	12		
	32	16		
YCbCr 4:4:4	24	8		Shall be supported when YCbCr is supported on any other display interface
	30	10		May be supported
	36	12		
	48	16		
RAW	6	6	–	May be supported
	7	7		
	8	8		
	10	10		
	12	12		
	14	14		
	16	16		

a. See the following sub-sections for VESA and CTA range definitions.

In determining the colorimetry format, the Source device shall check the Sink device's capability by way of a DisplayID or legacy EDID read. When the Sink device capability is unknown, for example due to the corruption of DisplayID or legacy EDID, the Source device shall fall back to 24bpp RGB, with full dynamic range (referred to as "VESA range" as described in Section 5.1.1.1.1).

When a Source device is transmitting an RGB stream with a video timing format defined by *CTA-861-G*, *Section 5* (except 640x480p) as using CTA range RGB, it should use CTA range RGB.

When a Source device is transmitting 640x480p 24-bit RGB, it shall always use the full dynamic range.

5.1.1.1.1 RGB Colorimetry

DP Source devices shall support RGB colorimetry with pixel depths of 18 and 24bpp. DP Source devices may also support RGB colorimetry with pixel depths of 30, 36, and 48bpp RGB.

"VESA range" and "CTA range" are defined as follows:

- VESA range shall have:
  - Nominal zero intensity level at code value 0
  - Maximum intensity level at maximum code value allowed for bit depth (i.e., 63 for 18bpp RGB, 255 for 24bpp RGB, 1023 for 30bpp RGB, 4095 for 36bpp RGB, and 65535 for 48bpp RGB)
- CTA range shall have:
  - Nominal zero intensity level at 16 for 24bpp, 64 for 30bpp, 256 for 36bpp, and 4096 for 48bpp
  - Maximum intensity level at maximum code value allowed for bit depth (i.e., 235 for 24bpp RGB, 940 for 30bpp RGB, 3760 for 36bpp RGB, and 60160 for 48bpp RGB)

Note: *The RGB CTA range is defined only for 24, 30, 36, 48bpp RGB; the RGB CTA range is* ***not*** *defined for 18bpp RGB.*

When a Source device is transmitting an RGB stream with a video timing format defined by *CTA-861-G*, the device may provide RGB in the VESA range.

A Sink device shall limit the pixel value range, as needed.

Note: *The Source device falls back to 18bpp VESA range RGB when the Sink device capability is unknown.*

5.1.1.1.2 YCbCr Colorimetry

DP Source devices that support YCbCr or YPbPr on any other display interface shall support YCbCr colorimetry, except where the Source device would need to convert RGB video to YCbCr to meet this requirement.

Source devices that support YCbCr shall support at least 24bpp YCbCr 4:4:4 and 16bpp YCbCr 4:2:2 in both 601 (defined in *ITU-R BT.601*, *Section 2.5*, or *CTA-770.2*, *Section 3.3*) and 709 (defined by *ITU-R BT.709*, *Section 3*, or *CTA-770.3*, *Sections 5.4 to 5.7*).

In addition to the minimums specified above, the pixel depth may be 30, 36, and 48bpp for YCbCr 4:4:4 and 20, 24, and 32bpp for YCbCr 4:2:2.

YCbCr dynamic range should be as defined in *CTA-861-G*, *Section 5* (CTA range):

- Y has nominal zero intensity level at 16 for 8bpc, 64 for 10bpc, 256 for 12bpc, and 4096 for 16bpc
- Y has nominal maximum intensity level at 235 for 8bpc, 940 for 10bpc, 3760 for 12bpc, and 60160 for 16bpc
- Cb and Cr have their zero levels at 128 for 8bpc, 512 for 10bpc, 2048 for 12bpc, and 32768 for 16bpc
- Cb and Cr have nominal ranges of 16 to 240 for 8bpc, 64 to 960 for 10bpc, 256 to 3840 for 12bpc, and 4096 to 61440 for 16bpc

However, a Source device may transmit all code values from 0 to the maximum value. A Sink device shall limit the pixel value range. as needed.

5.1.1.1.3 Y-only Colorimetry

Y-Only colorimetry may be supported on DP devices. If a DP device supports Y-Only colorimetry, the devices shall support pixel bit depths of 8, 10, 12, and 16bpp.

The purpose of this format is to reduce the amount of DP bandwidth by 1/3 over RGB to transmit grayscale video from Source to Sink device. The main intended application for this format is for ultra high-resolution medical displays.

For colorimetry, in the medical market it is common to use *DICOM PS3.14* to describe the mapping of values to luminance on the monitor. *DP v1.4a* defines a “perceptual linearized” standard, including a calibration of the monitor to ensure the standard is met. While this is the most common usage, it is not the only use. As such, the only necessary luminance mappings are VESA range.

5.1.1.2 Video Timing Format

Updated in *DP v2.0*.

In determining the video timing format, the stream Source of the Source device shall check the capability of the Sink device by way of a DisplayID or legacy EDID read after the HPD signal goes active. When the Sink device cannot handle the incoming stream, the Sink device shall toggle the HPD signal to notify the Source device of this condition. After detecting an HPD pulse, the Source device shall determine the Sink device status by reading the SINK_STATUS and SINK_STATUS_ESI registers (DPCD Addresses 00205h and 0200Fh, respectively).

When the Sink device capability is unknown (e.g., due to corruption of a DisplayID or legacy EDID), the Source device may fall back to a set of fallback video timing formats of its choice (except for the Fail Safe mode). When none of the fallback video timing formats is acceptable (as indicated by the Sink device in the SINK_STATUS and SINK_STATUS_ESI registers), the Source device shall transmit a supported format defined by the SINK_VIDEO_FALLBACK_FORMATS register (DPCD Address 00020h).

A DP Source device may assume that 640x480 at 60Hz, 18bpp, is supported. Which video format to transmit is a DP Source device policy choice.

DP Sink devices designed prior to the addition of the SINK_VIDEO_FALLBACK_FORMATS will report 00h at this address.

5.1.1.3 Audio Format

Audio may be supported for DP Source devices. Source devices that support audio shall support stereo (two channel) 16-bit per sample L-PCM Audio at one or more of 32, 44.1, or 48kHz.

Audio-capable Source devices may support other coding types, sample rates, sample sizes, and/or number of channels within the limits of the Sink device's audio capability indicated in its DisplayID or legacy EDID.

The Source device shall check by way of DisplayID or legacy EDID, –or– the CTA Timing Extension to DisplayID or legacy EDID, which audio formats the Sink device can support before transmitting audio stream data.

The Source device should determine whether the Sink device is able to sink the audio stream by checking the SINK_STATUS and SINK_STATUS_ESI registers (DPCD Addresses 00205h and 0200Fh, respectively) and take corrective action, as needed.

5.1.2 Source Device Link Configuration Requirement

A DP Source device shall establish the Main-Link between its DPTX and DPRX through the Link Training sequence upon Hot Plug event detection, as described in Section 3.5.1.2.

After Link Training successfully completes (which means that the DPRX is synchronized to incoming Main-Link data) and before transport of a main video stream starts, the Source device shall be transmitting the Idle Pattern consisting of the BS symbol sequence followed by the NoVideoStream_Flag bit in the VB-ID (bit 3) set to 1 every 2^{13} (or 8192) link symbols. Every 512^{th} occurrence of the BS symbol sequence shall be replaced by the corresponding scrambler reset (SR) symbol sequence.

The Source device shall start transmitting the Idle Pattern after it has cleared the TRAINING_PATTERN_SET register (DPCD Address 00102h).

The Source device of a box-to-box DP connection shall support the number of Main-Link lanes that provide for sufficient bandwidth, even at a reduced bit rate-per-lane.

For example, if a required application bandwidth is provided both with two lanes at a high bit rate and four lanes at a reduced bit rate, a detachable Source device shall support four lanes.

Note: *A Source device for an embedded connection shall* ***not*** *be required to follow this rule.*

After it detects a Hot Plug event, the Source Link Policy Maker shall read the Receiver Capability field (DPCD Addresses 00000h through 000FFh; see Table 2-183) of the Sink device and configure the link accordingly, using the link training procedure as described in Section 2.12.4.3 and Section 3.5.1.2.

For link training failure handling, see Section 3.5.1.2.1 and Section 3.5.1.2.2.

After the link is configured, the Source Link Policy Maker shall check the link status whenever it detects an IRQ_HPD pulse. When it detects that the link has lost lock, the Source Link Policy Maker shall retrain the link. A link can be retrained for any reason. A Source device shall be tolerant to the available bandwidth resulting from retraining being lower than the bandwidth resulting from prior link training, and this in turn might require a video mode set change.

The Source device Link Policy Maker shall re-read the Receiver Capability field and take corrective action when it detects one of the following conditions:

- Low-going HPD pulse wider than 2ms (Hot Plug event HPD pulse)
- RX_CAP_CHANGED bit in the LINK_SERVICE_IRQ_VECTOR_ESI0 register (DPCD Address 02005h, bit 0) is set
- Downstream device is a DP Branch device and its DOWNSTREAM_PORT_STATUS_CHANGED bits in the LANE_ALIGN_STATUS_UPDATED and LANE_ALIGN_STATUS_UPDATED_ESI registers (DPCD Addresses 00204h and 0200Eh, respectively, bit 6) are set

When a DP Source device is resuming the transmission (e.g., after waking from sleep), the Source device can skip link training-related AUX transactions when both of the following conditions exist:

- Source device has determined that the HPD signal has remained continuously asserted (apart from IRQ_HPD notifications) since the link was last in full operation
- Source device has read the NO_AUX_TRANSACTION_LINK_TRAINING bit in the MAX_DOWNSPREAD register (DPCD Address 00003h, bit 6) as having been set to 1 after initial Sink device detection

If both of the conditions listed above exist, and if the Source device determines that the bandwidth to be used is the same as that used when the link was last in full operation, the Source device can transmit TPS1 for 500us minimum and one of TPS2, TPS3, or TPS4 (depending on what is supported by both the DPTX and DPRX) for 500us minimum, using the last known good Voltage Swing and Pre-emphasis settings before switching to normal operation without AUX transactions for Link Training. Regardless of whether the full link training is skipped, the DP Sink device shall transmit an IRQ_HPD pulse over the HPD signal line when the device fails to synchronize to the incoming Main-Link stream.

A Source device increases the Main-Link lane count during normal operation, as follows:

1 Stops the transmission of symbols over the Main-Link lanes.

2 Writes the lane count that is needed to the LANE_COUNT_SET field in the LANE_COUNT_SET register (DPCD Address 00101h, bits 4:0).

3 Performs link training. The Source device may use the known-good drive current and pre-emphasis level setting to accelerate the link training sequence.

4 After all the lanes are trained, starts the transmission of Idle Pattern or a stream.

A Source device decreases the Main-Link lane count during normal operation, as follows:

1 Switches the transmitted symbols to Idle Pattern on all active lanes.

2 Writes the lane count that is needed to the Link Configuration field by way of the AUX_CH.

3 Stops the transmission of the Idle Pattern over the lanes that are to be disabled.

4 Verifies that the DPRX has achieved LANE*x*_SYMBOL_LOCKED and INTERLANE_ALIGN_DONE (unless it is 1-lane configuration).

5 Starts the transmission of a stream.

5.1.2.1 Source Device Link Requirement when Other Interfaces are Supported

One of the *DP Standard* objectives is to provide a high-performance display interface that meets user expectations. User expectations may be established by other non-DP video display interfaces that co-exist on a device. As such, for a Source device that provides standard connectors for VGA, DVI, HDMI, Thunderbolt, analog component, and/or composite video, any DP standard receptacles on the same Source device shall meet the requirements described below. The non-DP connectors enumerated above shall be collectively referred to as "non-Native connectors" throughout this section. For a Source device with non-Native connectors and multiple DP outputs, each DP output shall meet these requirements when tested individually.

For a Source device providing non-Native connectors, the DP output(s) shall support up to the maximum video display mode (determined as the maximum bandwidth product from supported pixel clock and color depth combinations) provided on the non-Native connector(s), up to maximum capability of the supported link rate in four-lane configuration. RBR and HBR shall be supported. HBR2 and HBR3 may be supported.

If audio is supported on a non-Native connector, the DP output of a Source device providing non-Native connectors shall support audio.

If HDCP is supported on a non-Native connector, the DP output of a Source device providing non-Native connectors shall support HDCP.

The Audio and HDCP requirements stated above also apply to DP outputs when operating in dual-mode (if supported), unless explicitly precluded by other governing standards or licenses.

5.1.3 Source Device Behavior on Stream Timing Change

5.1.3.1 Video Stream Timing Change

Before changing the timing of the main video stream, the Source device shall transmit the "Idle Pattern" (BS symbol followed by the NoVideoStream_Flag and VerticalBlanking_Flag bits in the VB-ID (bits 3 and 0, respectively) both set to 1 every 2^{13} or 8192 LS_Clk cycles) until it is ready to insert the new MSA data during the main video stream's vertical blanking period. At the very minimum, the Source device shall repeat the Idle Pattern five times before inserting the new MSA.

For eDP connections, the number of inserted Idle Patterns may be fewer than five.

If the Source device stops transmitting Main-Link symbols during the video timing change, the device shall to run Link Training before starting the transport of the new main video stream.

Note: *The Source device is allowed to continue transmitting Audio_Stream SDP framed by SS and SE symbols, even when it is no longer transmitting the main video stream. When the video stream is absent, the Source device shall transmit an Audio INFOFRAME (non-Basic Audio) SDP and Audio_TimeStamp SDP once after every 512th BS symbol set.*

5.1.3.2 Audio Stream Format/Timing Change

For an audio format/timing change, the Source device shall set and keep the AudioMute_Flag bit in the VB-ID (bit 4) to 1 until after the new Audio INFOFRAME (non-Basic Audio) and Audio_TimeStamp SDPs have been transmitted. Those SDPs may be transmitted as soon as the next frame boundary (when the main video stream is present) or after the next 512th BS symbol set (when the main video stream is absent).

5.1.4 Source Device Behavior upon HPD Pulse Detection

The HPD signal notifies the Source device that one of the following events has occurred:

- **IRQ** – A downstream DP Sink device might generate an IRQ_HPD pulse to prompt the Source device that Sink's status has changed so it toggles HPD line, forcing the Source device to read DPCD Addresses 00200h through 00205h or DPCD Addresses 02002h through 0200Fh
- **Unplug** – The Sink device is no longer connected to the Source device and the Source device may then disable its Main-Link as a power-saving measure
- **Plug/Re-plug –** The Sink device is now connected to the Source device, forcing the Source device to read the Receiver Capabilities and stream sink capability in DisplayID or legacy EDID

Figure 5-1 illustrates the events that are signaled by the HPD signal.

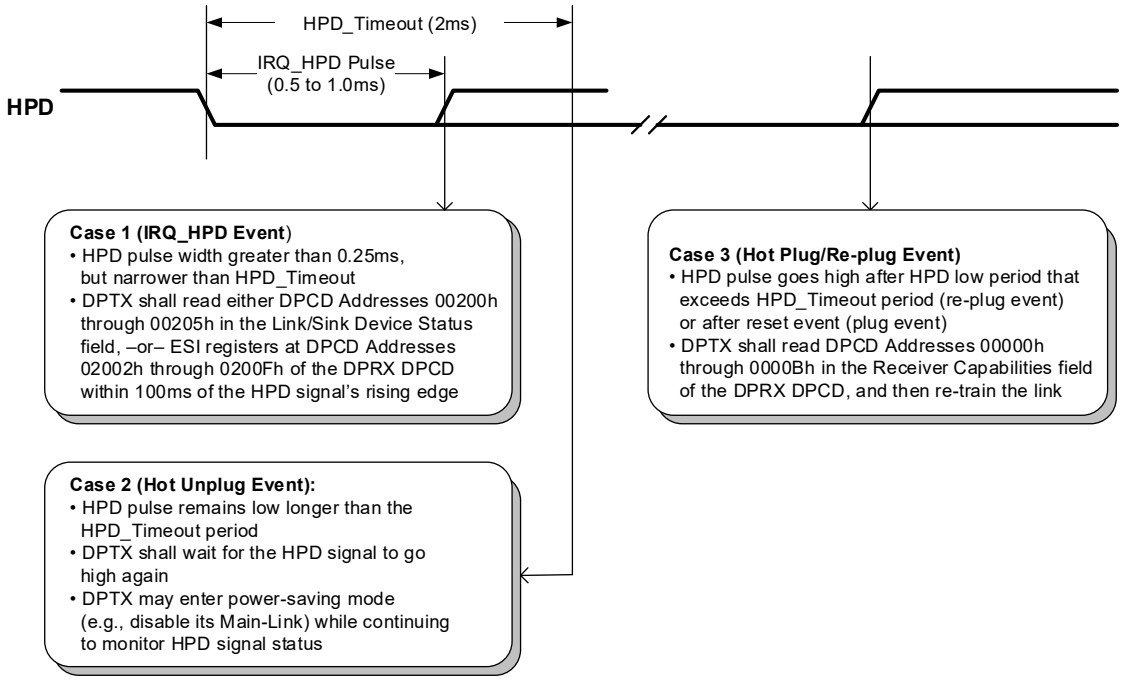


Figure 5-1: HPD Events

Note: *In the subsequent discussions, the Source device state is assumed to be ON because a Source device in the OFF state (e.g., powered off or blocked waiting for user input) shall obviously not be capable (or needed) to respond to HPD signal status changes.*

The Source device shall respond to an IRQ_HPD pulse by starting to read the registers located at DPCD Addresses 00200h through 00205h –or– DPCD Addresses 02002h through 0200Fh, by way of AUX read transactions within 100ms of the HPD signal's rising edge. The Source device shall then perform the necessary corrective action, based on the current Link/Sink status.

The Source device shall not be required to have an explicit response to Hot Unplug events. The Source device may choose to enter a power-saving state in which the device disables its Main-Link after HPD has been de-asserted for longer than the HPD_Timeout (2ms).

Note: *False events may occur due to signal bounce upon cable-assembly unplugging. In this condition, AUX read operations shall likely fail, and the HPD signal shall eventually settle in a de-asserted state for an extended period of time, allowing accurate detection of the Hot Unplug event.*

The Source device shall respond to Hot Plug event/Hot Re-plug event by first reading DPCD Link/Sink Device Status registers at DPCD Addresses 00200h through 00205h or DPCD Addresses 02002h through 0200Fh. If the link is unstable or lost, the Source device then reads the DPCD Receiver Capabilities registers at DPCD Addresses 00000h through 0000Fh to determine the appropriate information needed to train the link. The Source device shall then initiate Link Training.

There are no specified time constraints on the Source device's response to a Hot Plug event/Hot Re-plug event. However, a Source device vendor may want to impose a voluntary constraint similar to that for an IRQ_HPD pulse (e.g., 100ms) to ensure a good user experience with prompt discovery and configuration of newly connected devices.

5.1.5 Downstream Device DPRX Power Management by a Source Device

A Source device shall write 02h to the Sink device's SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h), using an AUX_CH to place a downstream device's DPRX in a power-saving state. In a power-saving state, the DP Source device may disable the Main-Link transmitter for power savings.

The Source device shall write 01h to the downstream device's SET_POWER & SET_DP_PWR_VOLTAGE register, using an AUX write transaction to switch the downstream device's DPRX out of a power-saving state. A DPRX of a downstream device in a power-saving state may not reply to this AUX request transaction. The DPRX of a downstream device in a power-saving state for an open, box-to-box connection is allowed to take up to 1ms until the DPRX is ready to reply to the AUX request transaction. Therefore, the Source device shall retry until the Sink device's 1-ms wake-up timeout period expires.

Note: *For embedded connections, a Sink device may take up to 20ms from a power-saving state until the device is ready to reply to the AUX request transaction.*

Before restarting the Main-Link transmission, the Source device shall verify that the Sink device replies to an AUX transaction. When restarting the Main-Link transmission, the Source device shall initiate Link Training first.

The Source device may keep transmitting Idle Pattern over Main-Link even when there is no stream to transmit. The Source device may start the transmission of a stream without initiating Link Training. Therefore, the downstream device shall keep the Main-Link receiver active as long as it is receiving either a stream or Idle Pattern and as long as it keeps the HPD signal asserted.

5.1.6 Source Device Connected to a Branch Device

Upon detecting HPD signal assertion, the DP Source device shall read the DFP_PRESENT bit in the DOWN_STREAM_PORT_PRESENT register (DPCD Address 00005h, bit 0) to determine whether the downstream device is a Sink or Branch device (bit 0 = 0 or 1, respectively). If it is a Branch device, the Source device shall read the following register bits, depending on the number of ports, to determine:

- Number of downstream-facing ports (DFPs) at the DFP_COUNT field in the DOWN_STREAM_PORT_COUNT register (DPCD Address 00007h, bits 3:0)
- Type of DFP and Port types at the DFP_TYPE field in the DOWN_STREAM_PORT_PRESENT register (DPCD Address 00005h, bits 2:1)
- DFP capabilities at the Detailed Capabilities Info registers (DPCD Addresses 00080h through 0008Fh)

To determine whether the Source device is connected to the Active protocol converter adapter, the Source device shall read the SINK_COUNT field in the SINK_COUNT and SINK_COUNT_ESI registers (DPCD Addresses 00200h and 02002h, bits 7, 5:0).

Upon detecting IRQ_HPD pulse, a Source device interfacing with an Active protocol converter shall check the SINK_COUNT field to determine whether there is a change in the count.

The Source device shall generate timings that are consistent with the output timings of an Active protocol converter adapter. For example, HDCP for HDMI requires a minimum of 56 blanking pixel clock cycles during the horizontal blanking period. A Source device shall generate a stream with sufficient blanking pixel clock cycles.

The Source device shall not transmit Frame/Field Sequential 3D stereo video format unless the adapter has set the FRAME_SEQ_TO_FRAME_PACK bit (Byte 3, bit 0, in the Detailed Capabilities Info register for the HDMI DFP type) to 1.

When the Source device is connected to an Active protocol converter adapter that advertises a DP++ DFP, if the Source device attempts to transmit a resolution that requires a TMDS clock rate or color depth that exceeds the Branch device's advertised capabilities or 165-MHz TMDS clock rate (whichever is less), the Source device should display a warning message to the user. The warning message should ask the user to confirm whether the image is acceptable. If confirmation is not received within a specified time, the resolution should be reverted to one that requires a TMDS clock rate or color depth that does not exceed the lesser of the advertised capabilities or 165MHz.

When the Source device is connected to an Active protocol converter adapter that advertises a VGA DFP, Source devices should support full plug-and-play (PnP) experience, when possible, and revert to non-PnP experience with manual user intervention for other cases when the Sink device connectivity state cannot be identified.

Table 5-2 describes how a DP Source device should behave when connected to a Branch device.

Table 5-2: Recommended DP Source Device Behavior when Connected to a Branch Device

HPD	Sink Count	Valid DisplayID or Legacy EDID Read?	Recommended DP Source Device Behavior
High	1 or 0 → 1 on IRQ_HPD	Yes	PnP experience, automatically drive the Sink device. Video format (video timing, pixel bit depth, colorimetry format) support based on the DisplayID or legacy EDID, link, and converter capability reported in the DPCD. Automatically disable driving the Sink device on transition from 1 → 0 on IRQ_HPD.
High	1 or 0 → 1 on IRQ_HPD	No	Non-PnP experience. Allows a user to manually enable the port and drive video format up to the link and converter capability reported in the DPCD. A DP Source device should not limit video support to only 640x480 for a DP-to-VGA protocol converter if DisplayID or legacy EDID cannot be obtained. Support for higher video format is based on the DP Source device policy. Disabling of the protocol converter's VGA output port requires manual user intervention.
High	0	No	Non-PnP experience, as described for the case above.
High	0	Yes	Non-PnP experience; however, when a user manually enables the protocol converter's VGA output port, a DP Source device should drive the output based on the DisplayID or legacy EDID, link and converter capability reported in the DPCD.
Low	Don't Care	Don't Care	Active protocol converter adapter is not discovered, and therefore, is **not** driven by a DP Source device.

The DP Source device should not transmit non-RGB color encoding, INFOFRAME, or audio-related SDPs unless one of the following conditions exist:

- DFP type is DisplayPort
- DFP type is HDMI
- DFP type is DP++ and the Source device detects that the DFP is connected to an HDMI level-shifting adapter

5.1.7 Source Device DSC Bitstream Transport and FEC Policy

New to *DP v1.4*.

A DSC bitstream sourcing-capable DP Source device shall have FEC encoding capability (see Section 3.5.1.5). Before enabling DSC bitstream transmission, the DP Source device operating in SST mode shall check that the plugged DPRX is capable of both DSC decompression and FEC decoding by reading the DPCD registers.

To enable FEC encoding/decoding, the DP Source device shall set the FEC_READY bit in the FEC_CONFIGURATION register (DPCD Address 00120h, bit 0) to 1 before initiating Link Training.

The DP Source device that is enabling FEC encoding shall take into account the 2.4% transport overhead of FEC when it calculates the maximum transportable AV stream bandwidth over an FEC-enabled DP link (see Section 2.2.1.4.2).

5.1.8 Horizontal Blanking Expansion Support

New to *DP v1.4*. Updated in *DP v1.4a*.

A DPRX that supports Horizontal Blanking Expansion shall indicate the support by doing the following:

- Setting the HBLANK_EXPANSION_CAPABLE bit in the RECEIVE_PORT0_CAP_0 register (DPCD Address 00008h, bit 3) to 1
- Setting the remaining RECEIVE_PORT0_CAP_0 register bits appropriately
- Programming the RECEIVE_PORT0_CAP_1 register (DPCD Address 00009h) appropriately

A DP Source discovers whether a connected DPRX operating in SST mode supports Horizontal Blanking Expansion by reading the RECEIVE_PORT0_CAP_0 and RECEIVE_PORT0_CAP_1 registers.

When connected to a Horizontal Blanking Expansion-capable DPRX, a DP Source device may also prompt the DPRX to enable Horizontal Blanking Expansion. To enable Horizontal Blanking Expansion, the DP Source device shall program the OUTPUT_HTOTAL, OUTPUT_HSTART, and OUTPUT_HSP_HSW registers (DPCD Addresses 03054h through 03059h, respectively) in a single AUX burst write transaction prior to transmitting the video stream to be expanded by a DPRX. To disable Horizontal Blanking Expansion, the DP Source device shall clear the OUTPUT_HTOTAL register to all 0s.

As with normal operation, when Horizontal Blanking Expansion is enabled, the DP Source device shall transmit MSA data field values that represent the DP data's format over the Main-Link. This rule may not apply, however, when the DP Source device is connected to a DPRX that has the MSA_TIMING_PAR_IGNORED bit in the DOWN_STREAM_PORT_COUNT register (DPCD Address 00007h, bit 6) set to 1.

5.2 DP SST Sink Device with 8b/10b Channel Coding

This section describes support for the SST-only mode Sink device for a box-to-box connection.

For embedded connections, the system integrator shall ensure that the Sink device meets the requirement of a given application.

5.2.1 Stream Sink Requirement

This sub-section describes support for the stream Sink in terms of video colorimetry, video timing, and audio formats. A Sink device shall describe its capabilities (supported video colorimetry, video timing, and audio formats) in the base DisplayID or legacy EDID and/or the *CTA-861-G* Timing Extension Block (**optional**). The Sink device shall support EDID r1.4.

5.2.1.1 Video Colorimetry

DP Sink devices support sinking of RGB, YCbCr, and Y-only colorimetry formats, as defined in Table 5-1. Sink devices shall read the colorimetry format of the transmitted stream from the DP MSA.

When receiving a CTA range video stream, the Sink device should anticipate that all the code values may be used by the Source device and clamp the dynamic range if needed.

5.2.1.2 Video Timing Format

Updated in *DP v2.0*.

A DP Sink device shall indicate whether it is able to sink the transmitted video stream by setting or clearing its RECEIVE_PORT_1_STATUS and RECEIVE_PORT_0_STATUS bits in the SINK_STATUS and SINK_STATUS_ESI registers (DPCD Addresses 00205h and 0200Fh, respectively, bits 1:0).

All detachable DP Sink devices shall support the SINK_VIDEO_FALLBACK_FORMATS register (DPCD Address 00020h) and at least 1920x1080 at 60Hz, 24bpp format.

5.2.1.3 Audio Format

A DP Sink device that outputs audio shall support an audio input stream by way of a DP link. The audio output may be sound waves (speakers) or electrical analog or digital audio output.

Sink devices that support audio shall support stereo 16-bit L-PCM Audio at 32, 44.1, and 48kHz. Audio-capable Sink devices may support other sample rates, sample sizes, and/or number of channels.

Sink device shall indicate by way of DisplayID or legacy EDID, –or– the CTA Timing Extension to DisplayID or legacy EDID, which audio formats are supported.

Note: *As of this writing, only the CTA Timing Extension to EDID provides this information. (See CTA-861-G for further details.)*

As is the case with sinking a video stream, the Sink device shall indicate whether it is able to sink the transmitted audio stream, by setting or clearing its RECEIVE_PORT_1_STATUS and RECEIVE_PORT_0_STATUS bits in the and SINK_STATUS_ESI registers (DPCD Addresses 00205h and 0200Fh, respectively, bits 1:0).

5.2.2 Sink Device Link Configuration Requirement

The Sink device requirement for a supported link configuration depends on whether the device is a "lean-back" or "lean-in" display. A lean-back Sink device is a display device that is meant to be viewed from more than 1.2m (approximately 4 feet) away. For the purposes of this standard, a lean-back Sink device is any display device that is capable of supporting an image that has a diagonal measurement of 30 inches or greater. A lean-in Sink device is any display device that is **not** capable of supporting an image with a diagonal measurement of 30 inches or greater.

A lean-back Sink device shall support the number of Main-Link lanes that provides sufficient bandwidth, even at a reduced bit rate per lane. This shall enable the lean-back display device to support a long cable length over which support of only a reduced bit rate is needed.

Some examples of lean-back Sink devices are TV displays and data projectors. Table 5-3 and Table 5-4 lists examples of the lane counts that are needed for TV displays and data projectors, respectively.

The Sink device of an eDP connection is regarded as a lean-in Sink device and therefore shall **not** be required to follow the rule of the lean-back Sink device described above.

Table 5-3: Lane Counts Needed for Typical TV Display Timings at RBR

Timing	Lane Count	Comments
Up to 480p/576p at 50/60Hz	One	
Up to 720p/1080i at 50/60Hz	One (50Hz)	
	Two (60Hz)	One at 60Hz if 16bpp YCbCr 4:2:2.
Up to 1080p at 50/60Hz	Four	

Table 5-4: Lane Counts Needed for Typical Data Projector Timings at RBR

Timing	Lane Count	Comments
Up to 1024x768	One	18bpp.
Up to 1680x1050	Two	18bpp.
Up to 1600x1200		18bpp with reduced blanking.
Up to 2048x1536	Four	18bpp with reduced blanking.

A lean-in display device (such as a desktop monitor) may choose to minimize the lane count for lowest cost.

For example, a 1400x1050 desktop monitor may have only one Main-Link lane.

Note: *This example monitor cannot receive its Native input resolution over the one lane at the reduced bit rate.*

A Sink device with a captive cable assembly is regarded as a lean-in device, and may therefore choose to minimize the lane count.

5.2.2.1 Sink Device Link Requirement when Other Interfaces are Supported

For a Sink device that supports other display interfaces in addition to DisplayPort, the DP input interface shall provide performance equal to or better than the other display input interfaces. However, there is no requirement for the DP interface to support beyond HBR with four lanes. This display interface performance requirement includes pixel resolution, color depth, and refresh rate.

Link support beyond HBR over four lanes shall **not** be required. HBR2 and HBR3 may supported. RBR shall be supported for "lean-back" displays as defined in Section 5.2.2. However, if fewer that than four lanes are supported for RBR, the number of lanes available when using RBR shall support the highest display performance capability, including pixel resolution, color depth, and refresh rate.

HDCP shall be supported through the DP interface if HDCP is supported through any other digital display input interface.

5.2.3 Sink Device Behavior on Stream Timing Change

5.2.3.1 Main Video Stream Timing Change

As described in Section 5.1.3, the DP Source device shall insert the "Idle Pattern" (BS + VB-ID + Mvid[7:0] + Maud[7:0] with the NoVideoStream_Flag and VerticalBlanking_Flag bits in the VB-ID (bits 3 and 0, respectively) both set to 1 every 2^{13} or 8192 LS_Clk cycles) at least five times before switching to a new video timing. Upon detecting this condition, a Sink device shall prepare to receive the new MSA and main video stream data.

Note: *The number of inserted Idle Patterns may be fewer than five for an eDP connection.*

Whether to blank the display during this transition is implementation-specific. Whatever method is selected, showing a visual image that is neither the incoming video stream nor a blank screen should be avoided.

5.2.3.2 Audio Stream Format/Timing Change

For an audio format/timing change, the Source device should set and keep the AudioMute_Flag bit in the VB-ID (bit 4) set to 1 until after the new Audio INFOFRAME (non-Basic Audio) and Audio_TimeStamp SDPs have been transmitted. An audio format change is caused by any of the following:

- Change between the compressed and non-compressed audio
- Change in the sampling rate
- Change in the number of channels

Those packets may be transmitted as soon as the next frame boundary (when the main video stream is present) or after the next 512^{th} BS symbol set (when the main video stream is absent).

The Sink device shall mute the audio when the AudioMute_Flag bit in the VB-ID (bit 4) is set, and should be ready to receive a new audio format upon detecting the change in Audio INFOFRAME and Audio_TimeStamp SDPs.

5.2.4 Toggling of HPD Signal for Status Change Notification

When there is a change either in the link status (e.g., loss of link synchronization) or the device status (e.g., remote control command pending), the Sink device shall clear the HPD signal to low for (0.5 to 1ms) before setting it to high again, thus generating IRQ_HPD pulse, to notify the Source device of the status change. A Hot Plug event, detected by an upstream DP device as a long HPD pulse (wider than 2ms), prompts the DP Source device to take many actions, such as LT-tunable PHY Repeater (LTTPR) recognition or reading of DisplayID or legacy EDID, as well as the Receiver Capability field (DPCD Addresses 00000h through 000FFh; see Table 2-183), and the communication to its operating system. Therefore, a DP Sink device shall use IRQ_HPD pulse to notify its upstream device of link status and device status change, instead of generating a long HPD pulse to emulating a Hot Plug event, unless it is prompting the DP Source device to re-read DisplayID or legacy EDID and the Receiver Capability field. Especially, a DP Sink device shall abstain periodic generation of long HPD pulses until the upstream device's initiating AUX transactions, because such actions may lead to soft lock-up condition of a DP Source device.

5.2.5 Sink Device DPRX Power State

This section describes the DP Sink device Active, Standby, Sleep, and Off power states. The extensions to the power state specification added in this Standard are discussed in Section 5.2.5.1.

The power state specification applies to all the DP devices with DPRX (i.e., DP Sink and Branch devices).

A Source device shall write 2h to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h) of a Sink device by way of the AUX_CH to place the Sink device's DPRX in a power-saving state. In a power-saving state, the Sink device may disable Main-Link receiver of DPRX for power saving.

The Sink device shall keep HPD signal asserted unless it is powered off. Therefore, the HPD signal shall remain asserted when the Sink device is in a power-saving state.

When the Sink device receives the AUX request transaction while it is in a power-saving state, the Sink device shall not have to immediately reply. However, the Sink device shall monitor the presence of a differential signal on the AUX_CH. The Sink device for an open, box-to-box connection shall fully enable the AUX_CH circuit within 1ms after detecting a differential signal so that the device can reply to the Source device's request transaction retry.

Note: *For an embedded connection, a Sink device may take up to 20ms from a power-saving state until it is ready to reply to an AUX request transaction.*

The Source device shall write 1h to the SET_POWER & SET_DP_PWR_VOLTAGE register by way of the AUX_CH to switch the Sink device out of a power-saving state. Upon this AUX write transaction, the Sink device shall be ready for the Source device to initiate Link Training.

The Source device may keep transmitting Idle Pattern over Main-Link even when there is no stream to transmit. The Source device may start the transmission of a stream without initiating Link Training. Therefore, the Sink device shall keep the Main-Link receiver of DPRX active as long as it is receiving either a stream or Idle Pattern and as long as it keeps the HPD signal asserted.

The Sink device shall implement the power state machine illustrated in Figure 5-2.

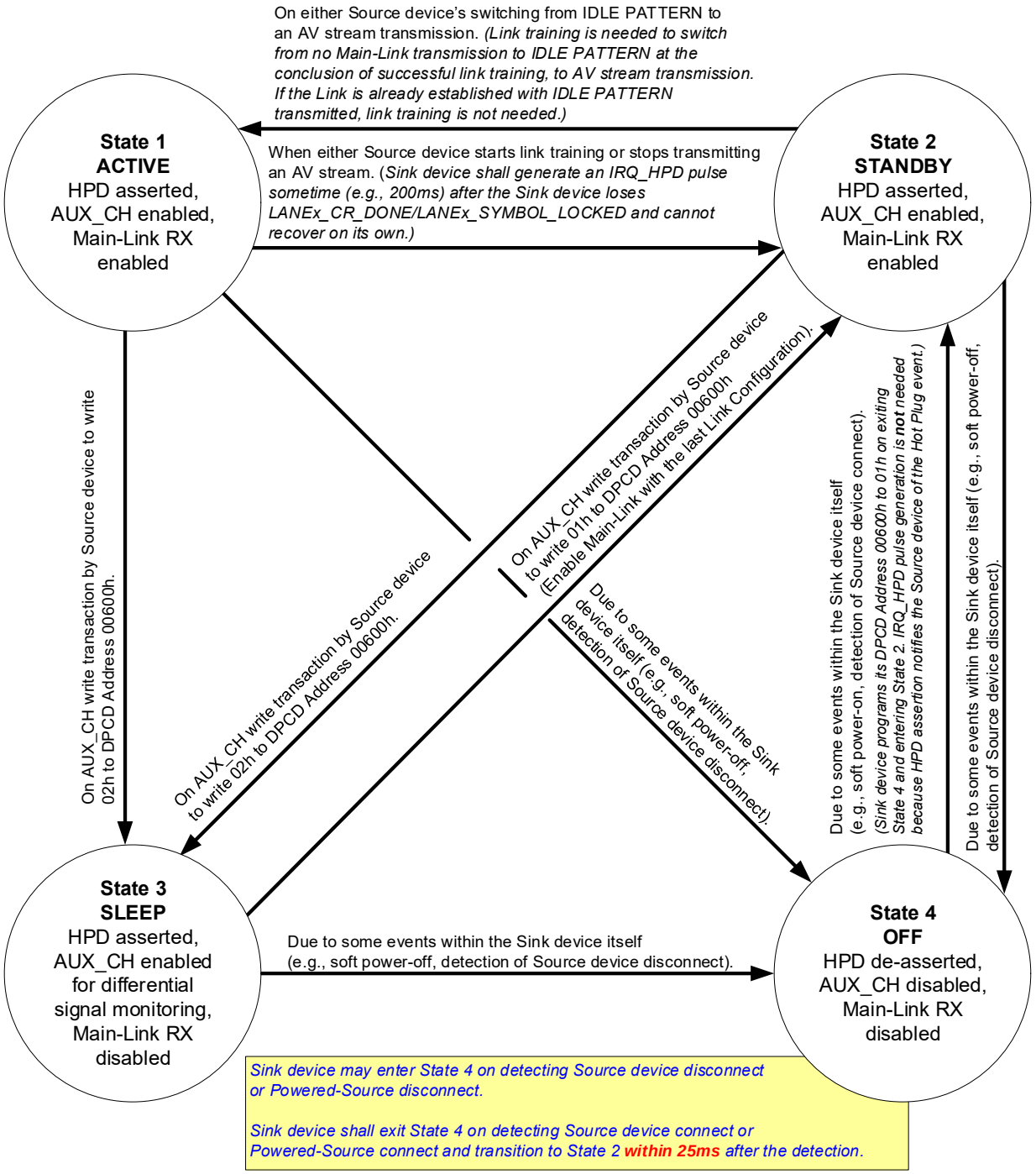


Figure 5-2: Sink Device Power State Machine

Table 5-5: Sink Device Power State Machine Notes

PM_State	Description
1	**ACTIVE** The Sink device has asserted HPD, and enabled AUX_CH and Main-Link RX, and is receiving an AV stream. While optionally supporting PSR as defined by *eDP v1.3* (or higher), a Source device may stop Main-Link signal transmission while in a PSR active state. When in a PSR active state, the Sink device shall not generate IRQ_HPD to indicate the loss of LANE*x*_CR_DONE and LANE*x*_SYMBOL_LOCKED, and shall continue to refresh the display from its internal Remote Frame Buffer. When the Source device stops the Main-Link signal transmission, the Sink device may disable the Main-Link RX, but shall monitor the AUX_CH. See *eDP v1.3* (or higher) for further details on Sink and Source device behavior when supporting PSR. Entered from one state: • State 2 (STANDBY), upon either a Source device switching from Idle Pattern to an AV stream transmission (Link Training shall switch from no Main-Link transmission to Idle Pattern at the conclusion of successful Link Training, to AV stream transmission: If the Link is already established with Idle Pattern transmitted, Link Training shall not be required). Exits to one of three states: • State 2 (STANDBY), when the Source device starts Link Training or stops transmitting an AV stream; either transmitting Idle Pattern or no Main-Link signal at all. • State 3 (SLEEP), AUX write transaction by the Source device to write 02h to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h). • State 4 (OFF), due to some events within the Sink device itself (e.g., soft power-off).
2	**STANDBY** The Sink device has asserted HPD, and enabled AUX_CH and Main-Link RX, but is receiving either Idle Pattern or no Main-Link signal (LANE*x*_CR_DONE and LANE*x*_SYMBOL_LOCKED both lost). Entered from one of three states: • State 4 (OFF), due to some events in the Sink device itself (e.g., soft power-on). (Sink device programs its SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h) to 01h upon exiting from State 4 (OFF) and entering State 2 (STANDBY). The IRQ_HPD pulse generation is not needed, because the action of HPD assertion notifies the Source device of Hot Plug event.) • State 3 (SLEEP), upon AUX write transaction by the Source device to write 01h to the SET_POWER & SET_DP_PWR_VOLTAGE register. • State 1 (ACTIVE), when the Source device stops transmitting an AV stream (Sink device shall generate an IRQ_HPD pulse sometime (e.g., 200ms) after it has stopped receiving the Main-Link signal, that is, neither AV stream nor Idle Pattern). Exits to one of three states: • State 4 (OFF), due to some events in the Sink device itself (e.g., soft power-off). • State 3 (SLEEP), upon AUX write transaction by the Source device to write 02h to the SET_POWER & SET_DP_PWR_VOLTAGE register. • State 1 (ACTIVE), upon either the Source device's switching from Idle Pattern to an AV stream transmission (Link Training shall switch from no Main-Link transmission to Idle Pattern at the conclusion of successful Link Training, to AV stream transmission: If the Link is already established with Idle Pattern transmitted, Link Training shall not be required).

Table 5-5: Sink Device Power State Machine Notes (Continued)

PM_State	Description
3	**SLEEP** The Sink device has asserted HPD, and sufficiently enabled the AUX_CH to at least monitor incoming AUX_CH differential signals. The Main-Link RX is disabled. Entered from one of two states: • State 2 (STANDBY), upon AUX write transaction by the Source device to write 02h to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h). • State 1 (ACTIVE), upon AUX write transaction by the Source device to write 02h to the SET_POWER & SET_DP_PWR_VOLTAGE register. This state exits to one of two states: • State 4 (OFF), due to some events within the Sink device itself (e.g., soft power-off). • State 2 (STANDBY), upon AUX write transaction by the Source device to write 01h to the SET_POWER & SET_DP_PWR_VOLTAGE register.
4	**OFF** The Sink device has de-asserted HPD, and disabled AUX_CH/Main-Link. Entered from one of three states: • State 3 (SLEEP), due to some events in the Sink device itself (e.g., soft power-off). • State 2 (STANDBY), due to some events in the Sink device itself (e.g., soft power-off). • State 1 (ACTIVE), due to some events in the Sink device itself (e.g., soft power-off) (the Sink device may enter this state upon detecting Source disconnect or Powered-Source disconnect). This state exits to one state: • State 2 (STANDBY), due to some events in the Sink device itself (e.g., soft power-on) (the Sink device may exit this state upon detecting Source connect or Powered-Source connect).

5.2.5.1 DP Sink Device Power State Specification Extensions

This section covers two extensions added to the DP Sink device power state specification in this Standard:

- Extended wake timeout from SLEEP power state
- CONNECTED_OFF power state addition

5.2.5.1.1 Extended Wake Timeout from SLEEP Power State

A DP Sink device can request an extended timeout for the wake from SLEEP power state. Unless the request for the extended timeout is granted by the upstream DP device, the DP Sink device shall wake up within 1ms after receiving the first AUX transaction over AUX_CH while in the SLEEP power state, using the registers listed in Table 5-6. (For complete register descriptions, see Table 2-184 and Table 2-193 for DPCD Addresses 00119h and 02211h, respectively.)

Table 5-6: Extended Wake Timeout from SLEEP Power State Request/Grant Registers

DPCD Address	Register
00119h	EXTENDED_DPRX_SLEEP_WAKE_TIMEOUT_GRANT
02211h	EXTENDED_DPRX_SLEEP_WAKE_TIMEOUT_REQUEST

5.2.5.1.2 CONNECTED_OFF Power State

The CONNECTED_OFF Power State is identical to the OFF Power State defined above, with one exception. In the CONNECTED_OFF power state, the DP Sink Device shall keep its HPD asserted.

An upstream DP device cannot prompt a downstream device (including a DP Sink device) in the CONNECTED_OFF power state to exit the state, just as the upstream device cannot prompt the DP Sink device in the OFF power state to exit the state. When to exit the CONNECTED_OFF power state is a decision that shall be made by the downstream DP device (e.g., another soft power button press on a DP display by a user).

5.2.5.1.2.1 Entry into CONNECTED_OFF Power State

To request an entry into CONNECTED_OFF power state, a DP Sink device shall set the CONNECTED_OFF_ENTRY_REQUESTED bit in the LINK_SERVICE_IRQ_VECTOR_ESI0 register (DPCD Address 02005h, bit 4) to 1 and generates an IRQ_HPD pulse. The DP Sink device shall enter into the CONNECTED_OFF power state only after the upstream device writes 1 to clear the bit. If the upstream device does ***not*** clear the bit within 1 second after IRQ_HPD generation, the DP Sink device shall de-assert HPD, clear the bit, and then enter into the OFF power state (***not*** the CONNECTED_OFF power state).

During the CONNECTED_OFF state, the DP Sink device shall continue to monitor the presence of an upstream device and whether the upstream device is powered.

5.2.5.1.2.2 Exit from CONNECTED_OFF Power State

The power state to which a DP Sink device in the CONNECTED_OFF power state can transition is the STANDBY power state. When a DP Sink device decides to exit the CONNECTED_OFF power state, it notifies the event by generating an IRQ_HPD. The DP device shall be able to handle AUX transactions from the upstream DP device by the time it generates an IRQ_HPD. Because the IRQ_HPD is simply a notification of exit to the STANDBY power state to the upstream device, an IRQ_HPD flag bit does not need to be set.

The DP Sink device also exits the CONNECTED_OFF power state upon detecting a disconnect of the upstream device and transitions to the OFF power state.

Upon detection of an upstream DP device connection, the DP Sink device supporting the CONNECTED_OFF power state shall first transition to the STANDBY power state. Once in the STANDBY power state, the DP Sink device may request re-entry into the CONNECTED_OFF state by generating an IRQ_HPD after setting the CONNECTED_OFF_ENTRY_REQUESTED bit in the LINK_SERVICE_IRQ_VECTOR_ESI0 register (DPCD Address 02005h, bit 4).

5.2.6 Sink Device DSC Bitstream Handling and FEC Policy

New to *DP v1.4*.

A DSC bitstream decompression-capable DP Sink device shall have FEC decoding capability (see Section 3.5.1.5).

When a DP Source device sets the FEC_READY bit in the FEC_CONFIGURATION register (DPCD Address 00120h, bit 0) to 1 before initiating Link Training, the DP Sink device shall delay Link Layer Code forwarding to the 8b/10b decoder and descrambler blocks by the same amount needed for FEC decoding, even when the device is not performing FEC decoding (i.e., the DP Sink device shall ensure that enabling and disabling of FEC decoding is transparent to its HDCP decryption block and Link Layer block).

The DP Sink device shall be able to regenerate a stable main video, despite the skew of the BE and BS symbol sequence locations caused by FEC parity code insertion.

5.3 DP SST-only Branch Device with 8b/10b Channel Coding

This section describes support for DP SST-only Branch devices. Branch device types are summarized in this section.

5.3.1 DisplayID or Legacy EDID Access Handling Requirement

A Branch device shall ensure that the stream transmitted by the Source device can be sunk by at least one Sink device in the link. Therefore, a Branch device without its own local stream sink shall forward the DisplayID or legacy EDID access request from its upstream device to its downstream device.

When a Branch device has multiple DFPs, it has multiple choices regarding which downstream device(s) should receive the DisplayID or legacy EDID access request.

The DP Branch device shall route the DisplayID or legacy EDID access to the lowest numbered, unassigned, DFP to which a downstream device is connected. If the DP Branch device is a matrix switch with multiple input and output ports capable of multiple connections (e.g., Input Port N to Output Port M, Input Port $N + 1$ to Output Port $M + 1$), then the subsequent SST Source devices connected shall be assigned the lowest numbered, unassigned, connected DFP among the remaining ones. If there is no unassigned, connected DFP, the Branch device shall wait until a DFP becomes connected or another DP SST Source device is disconnected before assigning a port to the DP SST Source device. The adapter shall neither cache nor modify the DisplayID or legacy EDID contents.

5.3.2 Branch Device Link Configuration Requirements

For the requirement link configuration of a DP Branch device with DP output port, see Section 2.1.4.1.

If a DP SST Branch device needs to change the DPCD Receiver Capability register values based on the capability of the connected DP device to its downstream-facing port (DFP), the DP SST Branch device shall generate a long HPD pulse from its upstream-facing port (UFP). The long HPD pulse prompts the upstream DP SST device to read the updated Receiver Capability register values.

Protocol converters (either DP-to-Legacy or Legacy-to-DP) may have fewer than four Main-Link lanes, as long as the DP link provides sufficient bandwidth for the legacy link at the DP Main-Link rate of HBR or RBR.

Protocol converters shall support the lane count that meets the bandwidth requirement at a reduced bit rate per lane.

5.3.2.1 Branch Device's Power State Transition Handling

A Branch device shall ensure that a Source device is correctly updated if a connect or disconnect event occurs on one of the Branch device's DFPs while the Branch device is in a power-saving state. If the Branch device detects a change in HPD on a DFP or is a protocol converter and keeps its DFP connect/disconnect detection circuitry (where implemented) active during a low-power state, the Branch device shall update the SINK_COUNT register (DPCD Address 00200h) and generate an interrupt (IRQ_HPD) whenever it detects a connect/disconnect event on a DFP.

Note: *The Source device can decide whether to ignore the interrupt or bring the Branch device out of a low-power state to read the new SINK_COUNT register value. The Branch device shall not exit a low-power state when it detects a connect/disconnect event. If the Branch device has downstream connect/disconnect detection circuitry but disables that circuitry during a low-power state –or– its HPD detection circuitry during a power-saving state (as appropriate), the Branch device shall preserve the sense of the connected display during sleep, and on exit from a low-power state, the Branch device shall re-activate its DFP connect/disconnect detection or HPD detection circuitry, update the SINK_COUNT register (only when necessary), and then generate an IRQ_HPD if the result of this update is to change the preserved value that is stored in the SINK_COUNT register.*

5.3.2.2 Branch Device DSC Bitstream Handling and FEC Policy

New to *DP v1.4*. Updated in *DP v2.0*.

Enabling of FEC encoding and decoding varies, depending on the channel coding method used, as follows:

- **8b/10b channel coding** – A DSC bitstream decompression-capable DP SST Branch device (i.e., DP-in, DP-out Link-Rate/Lane-Count protocol converter, and Active protocol converter) is a DP DSC Sink device and shall have FEC decoding capability (see Section 3.5.1.5). A DP SST Branch device should set the FEC_READY bit in the FEC_CONFIGURATION register (DPCD Address 00120h, bit 0) to 1 on its downstream link if the downstream device supports FEC decoding.

  When a DP Source device sets the FEC_READY bit to 1 before initiating link training, the DP Branch device shall delay Link Layer Code forwarding to the 8b/10b decoder and descrambler blocks by the same amount needed for FEC decoding, even when the device is not performing FEC decoding (i.e., the DP Branch device shall ensure that enabling and disabling of FEC decoding is transparent to its HDCP decryption block and Link Layer block).
- **128b/132b channel coding** – Automatically enabled after link training.

The DP Branch device shall be able to regenerate a stable main video, despite the skew of the BE and BS symbol sequence locations caused by FEC parity code insertion.

5.3.3 Active Protocol Converter Adapters

5.3.3.1 General Requirements

An Active protocol converter adapter shall assert the HPD signal whenever it is plugged into the Source device that has its DP_PWR enabled, regardless of whether the protocol converter has a connected display (Sink device) on its DFP.

The adapter shall set the DFP_PRESENT bit in the DOWN_STREAM_PORT_PRESENT register (DPCD Address 00005h, bit 0) to 1 to indicate the presence of DFPs to its upstream device. The adapter shall also set the DFP_COUNT field in the DOWN_STREAM_PORT_COUNT register (DPCD Address 00007h, bits 3:0) to indicate the number of DFPs.

The adapter shall set the DFP_TYPE field bits in the DOWN_STREAM_PORT_PRESENT register (DPCD Address 00005h, bits 2:1) to indicate the type of the main DFP (DFP 0). In addition, the adapter shall set the Detailed Capabilities Info registers (DPCD Addresses 00080h through 0008Fh) to show all the downstream types, including DFP 0. Either one or four bytes are used, per DFP type indication. Therefore, up to 16 (with 1-byte descriptor) or four (with 4-byte descriptor) DFP capabilities can be stored.

Note: *DP protocol converters with DPCD r1.4 (or higher) shall support the Detailed Capabilities Info register. DP protocol converters with DPCD r1.3 (or lower) should support the Detailed Capabilities Info register's 4-byte format to provide detailed capability information.*

The adapter shall implement a circuitry to detect plug/unplug status of its Sink device if the DFP type provides for the means for detection. When plug/unplug detection is possible, the adapter shall dynamically update the number of connected Sink devices in the SINK_COUNT field in the SINK_COUNT and SINK_COUNT_ESI registers (DPCD Addresses 00200h and 02002h, respectively, bits 7, 5:0). Whenever the Sink device count changes, the adapter shall do the following:

1 Update the SINK_COUNT and SINK_COUNT_ESI registers.

2 Set the DOWNSTREAM_PORT_STATUS_CHANGED bit in the LANE_ALIGN_STATUS_UPDATED and LANE_ALIGN_STATUS_UPDATED_ESI registers (DPCD Addresses 00204h and 0200Eh, respectively, bit 6).

3 Issue an IRQ_HPD pulse.

The adapter shall clear the DOWNSTREAM_PORT_STATUS_CHANGED bit immediately after the Source device reads the bit.

The adapter shall indicate whether the DPRX's Receive Ports within the adapter are properly receiving and regenerating the incoming streams, using the RECEIVE_PORT_1_STATUS and RECEIVE_PORT_0_STATUS bits in the SINK_STATUS and SINK_STATUS_ESI registers (DPCD Addresses 00205h and 0200Fh, respectively, bits 1:0).

Note: *This definition of SINK_STATUS and SINK_STATUS_ESI register bits is in contrast with that for a Sink device, for which these bits indicate whether the Sink device is in synchronization with the receiving streams.*

The adapter shall allow the DP Source device to drive display modes that are not specified in the DisplayID or legacy EDID mode list and to drive display modes that are beyond the range specified in DisplayID or legacy EDID (if DisplayID or legacy EDID is accessible).

The adapter shall put the connected Sink device into a low power state (the means of which is dependent on the cable converter's type of downstream display interface) whenever the following conditions exist:

- DP Source device has not transmitted video, and
- Source device has written 02h to its SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h)

The adapter should have an ability to adjust the DDC bit rate down to 1k to 10kbps on its DFP(s). Furthermore, the adapter should have the ability to indicate its default I^2C bit rate and supported bit rates to the Source device and that it allows the Source device to select the bit rate (using the I^2C Speed Control Capabilities Bit Map and I^2C Speed Control/Status Bit Map registers (DPCD Addresses 0000Ch and 00109h, respectively)).

The Detailed Capabilities Info registers apply when the FORMAT_CONVERSION bit in the DOWN_STREAM_PORT_PRESENT register (DPCD Address 00005h, bit 3) is 0. An Active protocol converter shall transmit a stream that it has received from a DP Source device as is, without timing format change or pixel data processing. The corollary is that the Source device shall limit the audio/video formats and resolutions to those that the Sink device advertises that it supports.

A Branch device with a DFP type of DisplayPort shall implement at least two Receive Ports, be capable of transporting an audio stream, and support HBR audio.

5.3.3.2 VGA Protocol Converter Adapters

When the DETAILED_CAP_INFO_AVAILABLE bit in the DOWN_STREAM_PORT_PRESENT register (DPCD Address 00005h, bit 4) is cleared to 0 and DFP**X_TYPE** field in the Detailed Capabilities Info register (DPCD Address 00080h, bits 2:0) is programmed to 001b (Analog VGA), the analog VGA DAC shall support the maximum pixel rate for 24bpp color depth (= 3 Bytes/pixel, 8bpc) within the maximum Link Bandwidth of its upstream DPRX.

Example: The maximum Link Rate is HBR (2.7Gbps/lane) and the maximum Lane Count is two lanes. The maximum Link Bandwidth = 540MBps. The maximum pixel rate for 24bpp (= 3 Bytes per pixel) is 180MP/s.

The adapter shall permit the VGA outputs to be driven with an image provided by the DP Source device as long as it is receiving a valid DisplayPort video stream even when it does not detect a connected display and before the DP Source device has attempted a DisplayID or legacy EDID read.

A VGA protocol converter shall only update the SINK_COUNT fields in the SINK_COUNT and SINK_COUNT_ESI register(s) (DPCD Address(es) 00200h and 02002h, respectively, bits 7, 5:0) when the protocol converter can identify a connectivity state change by way of load detection, I^2C probe, or other method.

The adapter should implement load sensing on the VGA pins or an equivalent method to make a best-effort detection of the presence of a connected display. The adapter shall advertise this capability in the ADAPTER_CAP register (DPCD Address 0000Fh). Additionally, the adapter shall set the FORCE_LOAD_SENSE bit in the ADAPTER_CTRL register (DPCD Address 001A0h, bit 0) to 1, by default.

Note: *Given the wide variation of display implementations, VGA load sensing may* ***not*** *be reliable.*

5.3.3.3 DVI, HDMI, and DP++ Protocol Converter Adapters

DVI, HDMI, and DP++ protocol converter adapters shall support capabilities as indicated in Table 5-7. The table includes additional requirements for protocol converters with DPCD r1.4 (and higher).

Table 5-7: DVI, HDMI, and DP++ Protocol Converter Adapter Requirements

Requirement	DFP Type[a]		
	DVI	HDMI	DP++
Shall support I^2C-over-AUX to facilitate an EDID read of an HDMI Sink device by a DP Source device.	Y	Y	Y
Shall support all TMDS character clock rates on its DFP between 25MHz and the maximum declared TMDS character clock rate supported on the adapter's DFP.	Y	Y	Y
Input DP bandwidth shall support the maximum TMDS character clock rate supported on the adapter's DFP.	Y	Y	Y
Shall support all blank, total and active combinations that are valid within the maximum TMDS clock rate supported on the adapter's DFP. For example, if 594MHz is reported as the DFP's maximum TMDS character clock rate, the protocol converter shall support 4kx2k at 60Hz with RGB/YCbCr 4:4:4 pixel encoding format at 8bpc (24bpp).	Y	Y	Y
When the DETAILED_CAP_INFO_AVAILABLE bit in the DOWN_STREAM_PORT_PRESENT register (DPCD Address 00005h, bit 4) is 0 the maximum TMDS character clock rate supported on the DFP shall be at least 165MHz, and the maximum color depth supported shall be 8bpc.	Y	Y	Y
Shall support RGB, YCbCr 4:4:4, and YCbCr 4:2:2 formats. Color format conversion (e.g., YCbCr <–> RGB, or YCbCr 4:4:4 <–> YCbCr 4:2:2) shall not be required.	N/A	Y	Y
Shall support all color depths (bits/component) up to the declared Maximum Bits/component, as long as the DFP's declared Maximum TMDS character clock rate is not exceeded.	N/A	Y	Y
Shall generate INFOFRAME SDPs to the downstream device.	N/A	Y	Y
Shall be able to accept and pass-through the following 3D formats: • Frame pack using CTA INFOFRAME • Side-by-side, and Top-to-bottom	N/A	Y	Y

Table 5-7: DVI, HDMI, and DP++ Protocol Converter Adapter Requirements (Continued)

Requirement	DFP Type[a]		
	DVI	HDMI	DP++
May support conversion of DP Frame/Field Sequential 3D stereo video format (with left- and right-eye view indicated by the MSA MISC1 field, bits 2:1) to frame pack HDMI 3D format. If supported, the adapter shall set the FRAME_SEQ_TO_FRAME_PACK bit in the Detailed Capabilities Info register (DPCD Address 0008Fh, bit 0) to 1 for the appropriate port type. If supported, the adapter shall be able to detect Frame/Field Sequential 3D stereo video format and automatically perform the conversion to frame pack. A DP-to-HDMI protocol converter with DPCD r1.4 (or higher) shall support conversion of DP Frame/Field Sequential 3D stereo video format (with left- and right-eye view indicated by the MISC1 field, bits 2:1) to frame pack HDMI 3D format.	N/A	O/Y	O/Y
Shall implement at least two receive ports, be capable of transporting an audio stream, and support HBR audio.	N/A	Y	Y
May support DVI Dual Link on its DFP. If supported, the adapter sets the DUAL_LINK bit in the Detailed Capabilities Info register (DPCD Address 0008Fh, bit 1) to 1 for DVI DFPs. Additionally, the adapter shall be capable of supporting higher pixel clocks and/or deeper color consistent with *DVI r1.0* Dual Link requirements. Note that the declared maximum TMDS clock rate capability is not the same as the maximum pixel rate in Dual Link configurations.	O	N/A	N/A
Shall be able to operate as an *HDCP for DP r1.3* repeater.	Y	Y	Y
Additional Requirements for DP-to-HDMI/DP++ Protocol Converter with DPCD r1.4 for the UFP DPRX for Supporting *HDMI v2.0b*[b]			
600MHz TMDS character clock support.	N/A	Y	Y
Shall have the DETAILED_CAP_INFO_AVAILABLE bit in the DOWN_STREAM_PORT_PRESENT register(s) (DPCD Addresses 00005h and 02205h, bit 4) set to 1 with all the detailed info (at Bytes 1 through Byte 3).	N/A	Y	Y
Shall be able to convert to DVI (instead of HDMI) when instructed by an upstream DP Source device with the PROTOCOL_CONVERTER_CONTROL_0 register (DPCD Address 03050h) value.	N/A	Y	Y
Shall monitor and report downstream *HDMI v2.0b* link status including IRQ_HPD generation with the HDMI_LINK_STATUS_CHANGED bit in the LINK_SERVICE_IRQ_VECTOR_ESI0 register (DPCD Address 02005h, bit 3) set to 1. This capability is reported in the DOWNSTREAM_LINK_ERROR_REPORTING_SUPPORTED bit in the DOWNSTREAM_LINK_ERROR_REPORTING_SUPPORTED register (DPCD Address 03030h, bit 0).	N/A	Y	Y
Shall autonomously enable *HDMI v2.0b* scrambling and TMDS Clock Channel clock frequency division by 4, when needed. Whenever the downstream *HDMI v2.0b* sink device is capable of supporting scrambling, the protocol converter shall enable scrambling without DP Source device instruction.[c]	N/A	Y	Y
Shall interpret a portion of *HDMI v2.0b* EDID to determine YCbCr 4:2:0 component bit depth support capability and update the 16bpc_Supported, 12bpc_Supported, and 10bpc_Supported bits in the HDMI_SINK_YCBCR420_COMPONENT_BIT_DEPTH_SUPPORT register (DPCD Address 03034h, bits 2:0, respectively).[c]	N/A	Y	Y

Table 5-7: DVI, HDMI, and DP++ Protocol Converter Adapter Requirements (Continued)

Requirement	DFP Type[a]		
	DVI	HDMI	DP++
Shall support pixel encoding format conversion to YCbCr 4:2:0 from YCbCr 4:4:4, as instructed by an upstream DP Source device. INFOFRAME SDPs shall match the converted pixel encoding format with the PROTOCOL_CONVERTER_CONTROL_1 register (DPCD Address 03051h) value.	N/A	Y	Y
Shall support pixel encoding format conversion to YCbCr 4:2:2 from YCbCr 4:4:4, as instructed by an upstream DP Source device. INFOFRAME SDPs shall match the converted pixel encoding format with the PROTOCOL_CONVERTER_CONTROL_2 register (DPCD Address 03052h) value.	N/A	O	O
YCbCr 4:2:0 pass-through from DP input port to *HDMI v2.0b* output port.	N/A	Y	Y
Shall support CEC-Tunneling-over-AUX, as defined in Section 5.3.3.3.1.	N/A	Y	Y
Shall be able to operate as an *HDCP to DP r2.2* repeater.	N/A	O	O

a. Y = Shall be supported, O = May be supported, N/A = Not Applicable.
b. When a DP Source and DP-to-HDMI protocol converter are placed within a device of a single physical enclosure, such a device functions as an HDMI Source device. Which features to enable at the HDMI connector of an HDMI Source device is an implementation-specific choice. Therefore, the type of feature support indicated within this table does not apply.
c. See also the PROTOCOL_CONVERTER_CONTROL_1 register (DPCD Address 03051h).

The DPCD r1.4 (and higher) data structure includes the Protocol Converter Extension field (DPCD Addresses 03000h through 030FFh; see Table 2-194). Furthermore, two IRQ_HPD vector bits are added:

- CEC_IRQ bit in the DEVICE_SERVICE_IRQ_VECTOR_ESI1 register (DPCD Address 02004h, bit 2)
- HDMI_LINK_STATUS_CHANGED bit in the LINK_SERVICE_IRQ_VECTOR_ESI0 register (DPCD Address 02005h, bit 3)

A DP Source device shall source an under-scanned image. A DP-to-HDMI protocol converter shall indicate an under-scanned image type by way of an Auxiliary Video Information (AVI) INFOFRAME SDP.

When the HDMI_AUTONOMOUS_SCRAMBLING_DISABLE and HDMI_EDID_PROCESSING_DISABLE bits in the PROTOCOL_CONVERTER_CONTROL_1 register (DPCD Address 03051h, bits 2:1, respectively) are both cleared to 0, an HDMI protocol converter shall process the HDMI Sink device's EDID to determine appropriate support for HDMI scrambling and population of the 16bpc_Supported, 12bpc_Supported, and 10bpc_Supported bits in the HDMI_SINK_YCBCR420_COMPONENT_BIT_DEPTH_SUPPORT register (DPCD Address 03034h, bits 2:0, respectively).

When the HDMI_EDID_PROCESSING_DISABLE is set to 1, an HDMI protocol converter shall **not** process the HDMI Sink device's EDID to determine appropriate support for HDMI scrambling (scrambling shall **not** be automatically enabled if the TMDS Character Rate is less than or equal to 340Mcsc and the population of the 16bpc_Supported, 12bpc_Supported, and 10bpc_Supported bits in the HDMI_SINK_YCBCR420_COMPONENT_BIT_DEPTH_SUPPORT register (DPCD Address 03034h, bits 2:0, respectively) shall read 000b).

When the HDMI_AUTONOMOUS_SCRAMBLING_DISABLE bit is set to 1, HDMI scrambling for all TMDS Character Rates shall be controlled by the HDMI_FORCE_SCRAMBLING bit in the PROTOCOL_CONVERTER_CONTROL_1 register (DPCD Address 03051h, bit 3).

Table 5-8 summarizes the HDMI protocol converter's EDID processing and HDMI scrambling control.

Table 5-8: HDMI Protocol Converter EDID Processing and Scrambling Control

HDMI_FORCE_SCRAMBLING Bit Value[a]	HDMI_AUTONOMOUS_SCRAMBLING_DISABLE Bit Value[a]	HDMI_EDID_PROCESSING_DISABLE Bit Value[a]	*x*bpc_Supported Bit Values[b]	Scrambling
Don't care	0	0	Set according to HDMI EDID	TMDS > 340Mcsc: Enabled TMDS ≤ 340Mcsc: Enabled/ Disabled according to HDMI EDID
Don't care	0	1	000b	TMDS > 340Mcsc: Enabled TMDS ≤ 340Mcsc: Disabled
0	1	0	Set according to HDMI EDID	Disabled for all TMDS rates
0	1	1	000b	Disabled for all TMDS rates
1	1	0	Set according to HDMI EDID	Enabled for all TMDS rates
1	1	1	000b	Enabled for all TMDS rates

a. HDMI_FORCE_SCRAMBLING, HDMI_AUTONOMOUS_SCRAMBLING_DISABLE, and HDMI_EDID_PROCESSING_DISABLE bits in the PROTOCOL_CONVERTER_CONTROL_1 register (DPCD Address 03051h, bits 3:1, respectively).

b. 16bpc_Supported, 12bpc_Supported, and 10bpc_Supported bits in the HDMI_SINK_YCBCR420_COMPONENT_BIT_DEPTH_SUPPORT register (DPCD Address 03034h, bits 2:0, respectively).

The protocol converter shall **not** perform an autonomous HDMI EDID read that might collide (or overlap) with an attempt by the DP Source device to read the HDMI Sink device's EDID. The protocol converter may either perform an autonomous HDMI EDID read before programming the SINK_COUNT field in the SINK_COUNT register (DPCD Address 00200h, bits 7, 5:0) to a value greater than 0, –or– should snoop an HDMI EDID read performed by the DP Source device. The DP Source device shall perform a full HDMI EDID read of all HDMI EDID blocks before initiating video signaling.

5.3.3.3.1 CEC-Tunneling-over-AUX

5.3.3.3.1.1 Terminology

Table 5-9: CEC-Tunneling-over-AUX Terminology

Terminology	Definition
CEC Frame	The representation of a CEC Message on the CEC Line as defined in *HDMI Specification*. Start bit followed by a number of data bits (including all EOM and ACK bits).
CEC Message	Addressing and data content of a CEC Frame (excluding the START bit and EOM/ACK bits). An array of 8-bit bytes consisting of a Header block and 0 to 15 Data blocks. The (first) block of the CEC Frame with EOM = 1 is the last block of the CEC Message. If any block of a CEC frame is negatively acknowledged, that block becomes the last block of the CEC Message, even if EOM = 0.
Broadcast Message	As defined in *HDMI Specification*.
CEC Line Error	
Destination	
Follower	
Initiator	
Logical Address (LA)	
Logical HPD	Pertains to the HDMI HPD input signal for the DFP of a DP-to-HDMI protocol converter. De-asserted only after 100ms of a low period on the HDMI HPD signal, which is needed upon an HDMI EDID change and is otherwise de-bounced to avoid a spurious state transition.
Snooping	Receiving CEC messages where the DP-to-HDMI protocol converter does not function as a Follower on the CEC bus (in the CEC specification sense, which carries obligations of controlling ACK and CEC Line Error reporting).

5.3.3.3.1.2 Overview

CEC-Tunneling-over-AUX is the tunneling of CEC messages using Native AUX transactions across the AUX_CH between a DP Source device and a DP-to-HDMI protocol converter. The DP Source device operates as a CEC message consumer and producer, while the DP-to-HDMI protocol converter capable of CEC-Tunneling-over-AUX operation tunnels CEC messages between the DP Source device and CEC bus, as illustrated in Figure 5-3. DPCD address mapping for CEC-Tunneling-over-AUX is valid only for DPCD r1.4 (or higher).

Besides tunneling CEC messages that are targeted at the CEC logical address of the DP-to-HDMI protocol converter (i.e., the DP-to-HDMI protocol converter is the Follower) or broadcast (which has the logical address of Fh as the destination address), CEC-Tunneling-over-AUX as defined in this Standard allows for the DP Source device to monitor all CEC messages, regardless of whether they are successfully ended/acknowledged, as long as the DP-to-HDMI protocol converter is capable of Snooping mode. Additionally, the DP Source device can assign multiple logical addresses to which the DP-to-HDMI protocol converter shall function as the Follower if the DP-to-HDMI protocol converter supports multiple logical addresses.

Because the first block of the CEC message contains both the destination logical address and initiator's logical address, the DP Source device, upon receiving the message, can determine whether the message was targeted to the DP-to-HDMI protocol converter.

For a DP-to-HDMI protocol converter with DPCD r1.4 (or higher), CEC-Tunneling-over-AUX shall be supported. For a DP Source device, CEC-Tunneling-over-AUX may be supported. If a DP Source device supports CEC-Tunneling-over-AUX, the DP Source device should comply with *HDMI v2.0b* CEC functionality.

A DP-to-HDMI protocol converter with more than one HDMI DFP shall use only one of the HDMI DFPs for CEC-Tunneling-over-AUX.

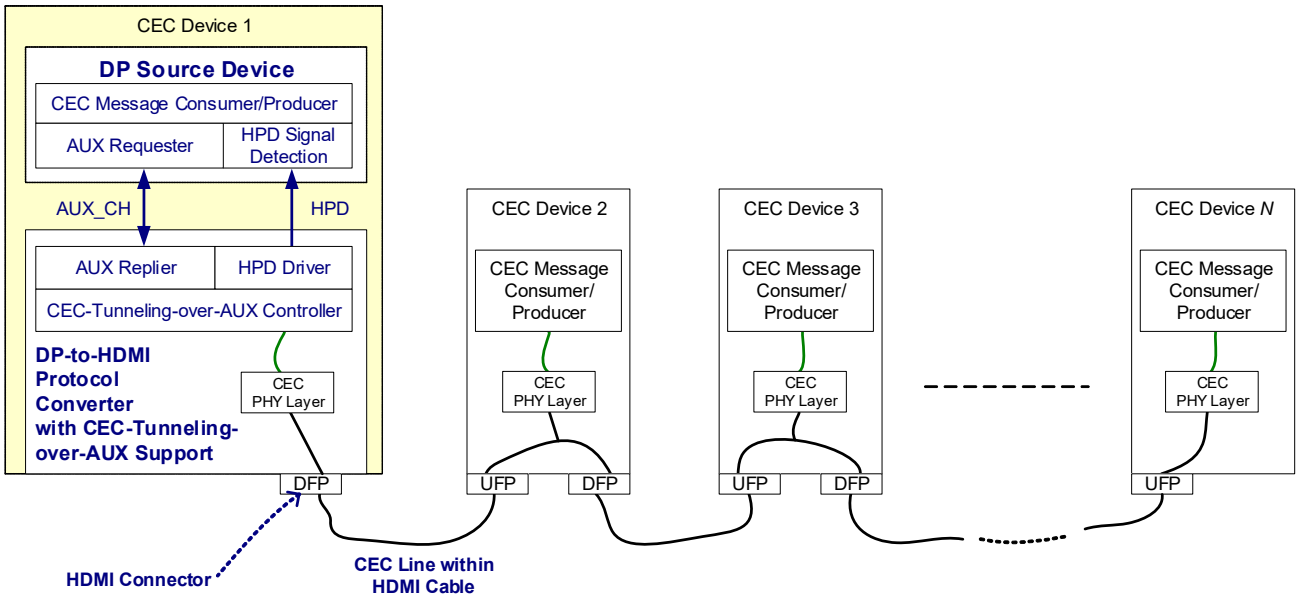


Figure 5-3: CEC Topology

5.3.3.3.1.3 DPCD Registers Used for CEC-Tunneling-over-AUX

Table 5-10 lists the DPCD registers that are used for CEC-Tunneling-over-AUX support. (For complete register descriptions, see Table 2-194.)

Table 5-10: DPCD Registers Used for CEC-Tunneling-over-AUX

DPCD Address	Register
03000h	CEC_TUNNELING_CAPABILITY
03001h	CEC_TUNNELING_CONTROL
03002h	CEC_RX_MESSAGE_INFO
03003h	CEC_TX_MESSAGE_INFO
03004h	CEC_TUNNELING_IRQ_FLAGS
0300Eh and 0300Fh	CEC_LOGICAL_ADDRESS_MASK
03010h through 0301Fh	CEC_RX_MESSAGE_BUFFER
03020h through 0302Fh	CEC_TX_MESSAGE_BUFFER

5.3.3.3.1.4 Power Management Considerations

The Source device might support CEC power management, in which case the Source device shall interpret CEC power management commands, either directed or broadcast standby, and shall put the DP-to-HDMI protocol converter into a lower power state by writing to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h).

The DP-to-HDMI protocol converter shall not enter a low power state by interpreting the CEC power management command. Rather, the protocol converter is placed into a lower power state (DPRX SLEEP power state) when the Source device programs the SET_POWER & SET_DP_PWR_VOLTAGE register to 02h. Even when placed into the DPRX SLEEP power state, the DP-to-HDMI protocol converter shall keep the HPD output to the DP Source device to a high level and keep the CEC-tunneling-related block sufficiently active so that the protocol converter can receive a CEC message and generate an IRQ_HPD with the corresponding IRQ flag bits set.

The Source device supporting CEC-Tunneling-over-AUX shall support being awakened by an IRQ_HPD from the DP-to-HDMI protocol converter. The extent to which a Source device implements a low-power state is dependent on Source device policy. Typically, the Source device would do no more than place the GPU that is sourcing a stream into a low-power state while maintaining the unrelated functionality in full operation.

5.3.3.4 S-Video/Composite/Other Analog Video Protocol Converter Adapters

An adapter from DisplayPort to S-Video, composite video, or other analog video may implement a method of detecting a connected display. Such an adapter shall not support I^2C-over-AUX to DDC pass-through for DisplayID or legacy EDID.

5.3.3.5 Dual-link DVI Protocol Converter Adapters

A DP to dual-link DVI protocol converter adapter is used for connecting a DP Source device to a dual-link DVI Sink device, as illustrated in Figure 5-4. The adapter shall use HPD on the DVI port to detect the presence of a connected display.

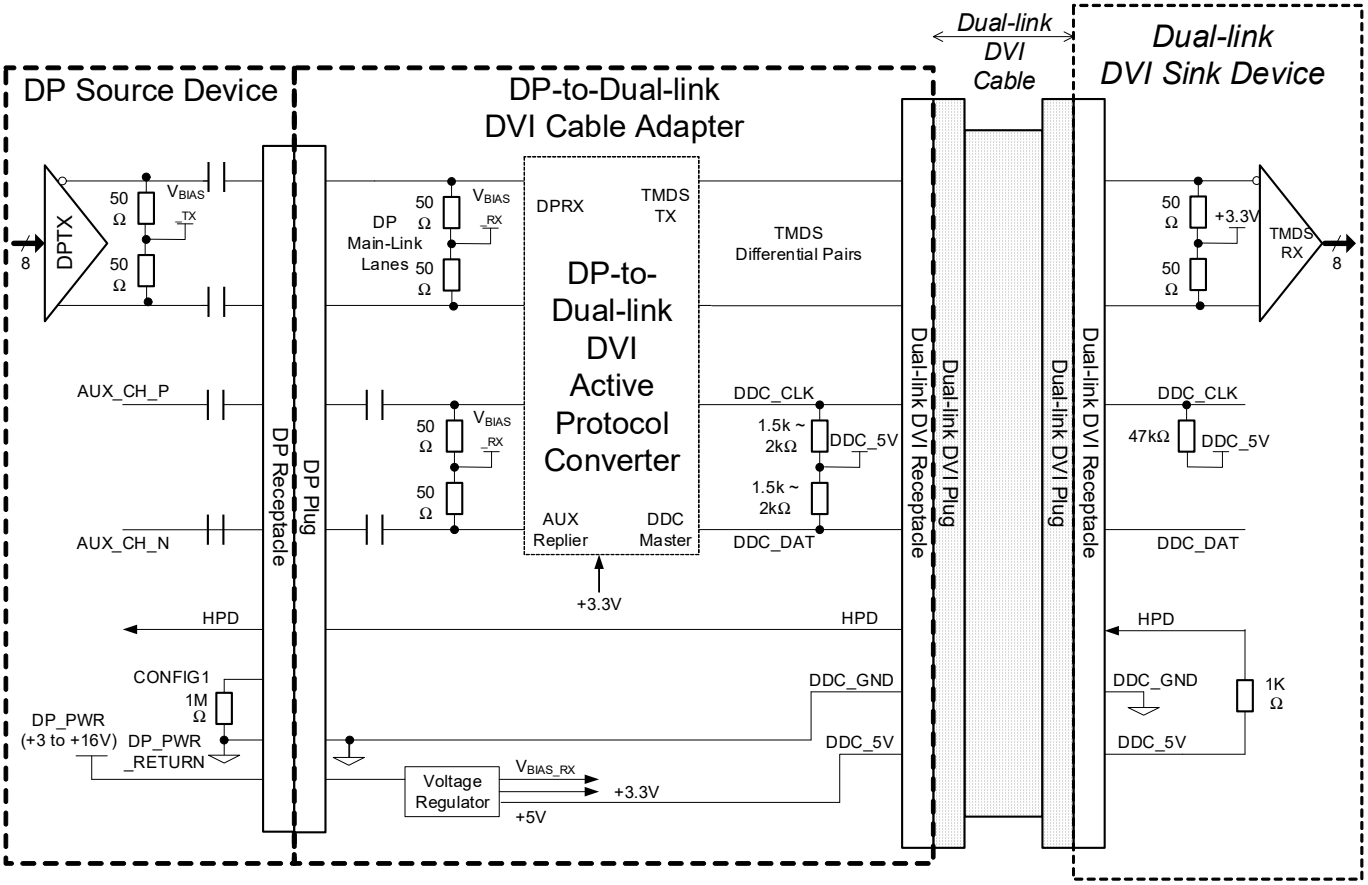


Figure 5-4: DP-to-Dual-link DVI Cable Adapter

5.3.3.6 Horizontal Blanking Expansion Support

New to *DP v1.4*.

As described in Section 2.2.4.1.2, a DP Branch device that is capable of supporting Horizontal Blanking Expansion shall express its capability in the RECEIVE_PORT0_CAP_0 and RECEIVE_PORT0_CAP_1 registers (DPCD Addresses 00008h and 00009h, respectively).

5.3.4 Link Rate and Lane Count

New to *DP v1.4*.

PHY Repeaters shall have the same link rate and lane count between the UFP DPRX_PHY and DFP DPTX_PHY. PHY Repeaters shall use the upstream DP link's serial bit rate to drive the downstream DP link.

5.3.5 Forward Error Correction

New to *DP v1.4*.

Forward Error Correction (FEC) may support LT-tunable bit-level PHY Repeaters.

5.4 DP MST Source Device with 8b/10b Channel Coding

Entire section rewritten for *DP v1.4*.

An MST Source device shall support either TPS4 or POST_LT_ADJ_REQ, as described in Section 3.5.1.2, to avoid link fragility when switching from link training to AV stream transmission.

5.4.1 Prompting the Downstream Device MST/SST Capabilities Transition

The downstream device is in SST mode, by default, as described in Section 5.5.1.1 and Section 5.6.1.1.

An MST Source device shall discover whether the downstream device is MST-capable by reading the MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0). The DP MST Source device shall set the UPSTREAM_IS_SRC, UP_REQ_EN, and MST_EN bits of the MSTM_CTRL register (DPCD Address 00111h, bits 2:0, respectively) to program the MST downstream device to MST mode and indicate itself as an MST device. The Source device shall change the MSTM_CTRL register value only while the link to the MST downstream device is inactive and FEC is disabled.

To set the downstream device back to SST mode, the DP MST Source device shall clear the MST_EN bit after inactivating the link to the MST downstream device and FEC is disabled.

5.4.2 Atomic Message Transaction Generation

There are MST Sink/Branch devices in the field that do **not** handle interleaved message transactions.

To facilitate message transaction handling by downstream devices, an MST Source device shall generate message transactions in an atomic manner (i.e., the MST Source device shall **not** concurrently interleave multiple message transactions). Therefore, an MST Source device shall clear the Message_Sequence_No value in the Sideband_MSG_Header to 0.

MST Source devices that support field policy updates by way of software should update the policy to forego the generation of interleaved message transactions.

5.4.3 Connection Status Notify Message Transaction Handling

A DP MST Source device should ACK the Connection Status Notify (CSN) Message Transaction for unplug events after the device has removed the time slots associated with the VC Payloads routed to the unplugged port.

5.4.4 Power Management

A DP MST Source device shall use the POWER_DOWN_PHY path message transaction to power-down the DPRX ports that are connected to the entire path. Additionally, the DP MST Source device shall write 010b to the SET_POWER_STATE field in the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h, bits 2:0) to its immediate downstream device, to prompt only that downstream device's DPRX port to transition to the D3 (power-down mode) state.

5.4.5 DSC Bitstream Transport and FEC Policy

Updated in *DP v2.0*.

An MST Source device with DSC bitstream sourcing capability shall support FEC encoding. (See Section 3.5.1.5.) A DP MST Source device shall enable DSC bitstream transport and FEC encoding only after discovering the following:

- Presence of a DSC decompression-capable device at the end of the path (either the last MST Branch or SST Sink device) by reading the DSC SUPPORT register(s) (DPCD Address(es) 00060h and 02260h) through a REMOTE_DPCD_READ message transaction.
- FEC capability of the entire path by reading the FEC_Capability field of the reply to an ENUM_PATH_RESOURCES message transaction targeted at the device (if any) immediately upstream of the device that is currently performing DSC decompression. If the Sink device is responsible for DSC decompression, the ENUM_PATH_RESOURCES message transaction is targeted at the last Branch device.

To enable FEC encoding and decoding, the DP MST Source shall first set the FEC_READY bit in the FEC_CONFIGURATION register (DPCD Address 00120h, bit 0) to 1 before initiating link training.

A DP MST Source device that enables FEC encoding shall take into account the 2.4% transport overhead of FEC when it calculates the PBN value of the AV stream that it is about to transmit.

The DP MST Source device shall **not** enable FEC encoding until after link training completes.

5.5 DP MST Sink Device with 8b/10b Channel Coding

Entire section rewritten for *DP v1.4*.

5.5.1 MST Sink Device with a DPRX in a Single UFP

An MST Sink device shall set the MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0) to 1 to indicate its MST capability to the upstream device.

An MST Sink device shall support either TPS4 or POST_LT_ADJ_REQ, as described in Section 3.5.1.2, to avoid link fragility when switching from link training to AV stream transmission.

5.5.1.1 Transition to SST Mode

Updated in *DP v2.0*.

An MST Sink device shall configure itself to SST mode when any of the following conditions exist:

- Power is cycling
- Disconnection of an upstream device is detected
  - An MST Sink device shall implement the detection of both an upstream device connection and a powered upstream device connection
- Upstream device's MST_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 0) is cleared to 0
  - An MST Sink device shall consistently monitor the MSTM_CTRL register value
- User selects SST mode through the Sink device's user interface (e.g., by way of a menu option)
  - An MST Sink device shall generate a long HPD pulse to the upstream device when this condition occurs

An MST Sink device shall take the following actions to configure itself to SST mode:

- Clear its own MSTM_CTRL register (DPCD Address 00111h)
- Clear its own VC Payload Mapping Table registers and bits, as appropriate:
  - PAYLOAD_ALLOCATE_SET register (DPCD Address 001C0h)
  - PAYLOAD_ALLOCATE_START_TIME_SLOT register (DPCD Address 001C1h)
  - PAYLOAD_ALLOCATE_TIME_SLOT_COUNT register (DPCD Address 001C2h)
  - ACT Handled and VC Payload ID Table Updated bits in the PAYLOAD_TABLE_UPDATE_STATUS register (DPCD Address 002C0h, bits 1:0, respectively)
  - VC_PAYLOAD_ID_SLOT*x* registers (where *x* is 1 through 63, DPCD Addresses 002C1h through 002FFh, respectively, bits 6:0)

- Clear outstanding request fragments from the Sideband MSG buffer fields in the following registers:
  - DOWN_REP registers (DPCD Addresses 01400h through 015FFh)
  - UP_REQ registers (DPCD Addresses 01600h through 017FFh)

In SST mode, the MST Sink device shall follow the policy requirement of an SST Sink device, as described in Section 5.2.

5.5.1.2 Transition to MST Mode

After an upstream device sets the UP_REQ_EN and MST_EN bits of the MSTM_CTRL register (DPCD Address 00111h, bits 1:0, respectively), the MST Sink device shall configure itself to MST mode and be ready for receiving message transactions from an upstream device and for Link Training to MST mode.

5.5.1.3 Issuance of Connection Status Notify Message Transactions

Because the local stream sinks are permanently connected to its MST Branching Unit (BU), the MST Sink device shall not issue a CSN message transaction. In other words, a CSN shall never be issued for Logical ports (i.e., Port Numbers 8h through Fh). The issuance of a CSN is limited to Physical ports (i.e., Port Numbers 0h through 7h).

5.5.1.4 Issuance of Resource Status Notify Message Transactions

DP MST Source devices currently available in the market can handle CSN message transactions, but not Resource Status Notify (RSN) message transactions. Therefore, an MST Sink device shall **not** issue RSN message transactions.

5.5.1.5 Power Management Handling

After an upstream device writes 010b to the SET_POWER_STATE field in the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h, bits 2:0), a DP MST Sink device shall disable the DPRX UFP's Main-Link RX.

A DP MST Sink device shall keep the VC Payload Mapping Table registers (see Section 5.5.1.1) set while in a lower power state. The MST Sink device shall clear the VC Payload Mapping Table registers only after the device receives a CLEAR_PAYLOAD_ID_TABLE message transaction, –or– when the device transitions to SST mode (as defined in Section 5.5.1.1).

5.5.1.6 Mvid/Nvid and Maud/Naud Handling

The link rate between the MST Sink device and its immediate-upstream MST Branch device may be different from that which the DP MST Source device is driving. In other words, the Mvid/Nvid and Maud/Naud values that the MST Sink device receives may not match the ratio between the Link Symbol clock rate and pixel clock rate, and Link Symbol clock rate and audio clock rate, respectively.

The DP MST Sink device shall be able to regenerate the pixel clock and audio clock without resorting to Mvid/Nvid and Maud/Naud values.

5.5.1.7 Split SDP Handling

An MST Sink device shall support handling of a split SDP.

5.5.1.8 DSC Bitstream Handling and FEC

An MST Sink device with DSC bitstream decompression capability shall support FEC decoding (see Section 3.5.1.5).

When the upstream DPTX sets the FEC_READY bit in the FEC_CONFIGURATION register (DPCD Address 00120h, bit 0) to 1 before initiating Link Training, the DP MST Sink device shall delay forwarding of Link Layer codes to the 8b/10b decoder and descrambler blocks by the same amount needed for FEC decoding, even when the device is not performing FEC decoding.

The MST Sink device shall be able to regenerate a stable main video, despite the skew of the BE and BS symbol sequence locations caused by FEC parity code insertion.

5.5.1.9 Interleaved Message Transactions Handling

As described in Section 5.4.2, an MST Source device is no longer allowed to generate interleaved message transactions. However, there are MST Source devices out in the field that issue interleaved message transactions. Therefore, an MST Sink device shall continue being able to handle interleaved message transactions.

5.5.2 MST Sink Device with a DPRX in Multiple UFPs

The policy of an MST Sink device with a DPRX in multiple UFPs is an implementation-specific choice. For example, the device may either choose to map fixed local stream sinks to each UFPs' DPRX without any overlap among the ports, –or– take a first-come, first-serve policy.

5.6 DP MST Branch Device with 8b/10b Channel Coding

Entire section rewritten for *DP v1.4*.

5.6.1 MST Branch Device with a DPRX in a Single UFP

An MST Branch device shall set the MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0) to 1 to indicate its MST capability to the upstream device. The MST Branch device shall support four lanes on the UFP's DPRX and DFPs' DPTX.

An MST Branch device shall support either TPS4 or POST_LT_ADJ_REQ, as described in Section 3.5.1.2, to avoid link fragility when switching from link training to AV stream transmission.

Additionally, an MST Branch device should support FEC decoding on the UFP's DPRX and re-encoding on the DFPs' DPTX to support routing of VC Payloads containing the DSC bitstream.

5.6.1.1 Transition to SST Mode

Updated in *DP v2.0*.

If any of the following three conditions exist, the MST Branch device shall configure itself to SST mode:

- Power is cycling
- Disconnection of an upstream device is detected
  - An MST Branch device shall implement the detection of both an upstream device connection and a powered upstream device connection
- Upstream device's MST_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 0) is cleared to 0
  - An MST Branch device shall consistently monitor the MSTM_CTRL register value

The MST Branch device shall take the following actions to configure itself to SST mode:

- Clear its own MSTM_CTRL register (DPCD Address 00111h)
- Clear its own VC Payload Mapping Table registers and bits, as appropriate:
  - PAYLOAD_ALLOCATE_SET register (DPCD Address 001C0h)
  - PAYLOAD_ALLOCATE_START_TIME_SLOT register (DPCD Address 001C1h)
  - PAYLOAD_ALLOCATE_TIME_SLOT_COUNT register (DPCD Address 001C2h)
  - ACT Handled and VC Payload ID Table Updated bits in the PAYLOAD_TABLE_UPDATE_STATUS register (DPCD Address 002C0h, bits 1:0, respectively)
  - VC_PAYLOAD_ID_SLOT*x* registers (where *x* is 1 through 63, DPCD Addresses 002C1h through 002FFh, respectively, bits 6:0)

- Clear the MSTM_CTRL register (DPCD Address 00111h) of all MST downstream devices
- Clear outstanding request fragments from the Sideband MSG buffer fields in the following registers:
  - DOWN_REP registers (DPCD Addresses 01400h through 015FFh)
  - UP_REQ registers (DPCD Addresses 01600h through 017FFh)

In SST mode, an MST Branch device shall follow the policy requirement of an SST Branch device, as described in Section 5.3.

5.6.1.2 Transition to MST Mode

After an upstream device sets the UP_REQ_EN and MST_EN bits of the MSTM_CTRL register (DPCD Address 00111h, bits 1:0, respectively), a DP Branch device shall configure itself to MST mode by doing the following:

- Be ready for receiving message transactions from an upstream device and for link training to MST mode
- Sets the UP_REQ_EN and MST_EN bits of the MSTM_CTRL register (DPCD Address 00111h, bits 1:0, respectively) of the MST downstream devices after disabling the Main-Link signal transmission before initiating link training

The DP MST Branch device shall always set the downstream links to the MST devices to the maximum link bandwidth and initiate link training with the MST_EN bit set to enable MST mode. Additionally, the MST Branch device that is capable of FEC decoding and re-encoding shall set the FEC_READY bit in the FEC_CONFIGURATION register (DPCD Address 00120h, bit 0) to 1 when it trains the FEC decoding-capable downstream DPRX.

An MST Branch device shall transmit an FEC_DECODE_EN and FEC_DECODE_DIS control link symbol sequence to the downstream link as it receives the sequence from the upstream link.

5.6.1.3 Issuance of Connection Status Notify Message Transactions

The HPD input is used to detect the plugging and unplugging of downstream devices. A Sink device, regardless of whether it is a DP Sink device or other type of Sink device (e.g., an HDMI Sink device), has a tendency of toggling its HPD output for various reasons. An MST Branch device shall avoid issuing a CSN message transaction for a hot unplug or a hot plug in immediate response to the HPD input level change. Rather, the Sink device shall scatter and possibly minimize the number of CSN message transactions that it issues, using the policy described in this sub-section.

An MST Branch device shall issue a CSN message transaction for hot unplug of a DFP. An MST Branch device shall then wait for the unplug CSN message transaction to be ACKed by its immediate upstream device before issuing the CSN message transaction for hot plug of the DFP should the DFP DPTX's HPD input signal go active before the ACK. The MST Branch device, in addition to waiting for the ACK from its immediate upstream device, should either wait for the ALLOCATE_PAYLOAD message transaction with a PBN value equal to 0 from the MST Source device for de-allocating the time slot assigned to the VC Payload that is routed to the unplugged DFP or for 2 seconds, whichever occurs first.

The MST Branch device shall generate a CSN message transaction corresponding to the DFP DPTX's HPD input signal's status at the time the device is ready to generate the CSN. If, for example, the DFP DPTX's HPD input signal goes low (which prompts the issuance of a CSN message transaction for hot unplug), goes high, and then goes low again, by the time the MST Branch device has confirmed that the upstream devices have handled the hot unplug CSN message transaction, the device shall not generate CSN message transactions that indicate hot plug and unplug events that have occurred since the last hot unplug CSN message transaction. Rather, the MST Branch device shall not issue any CSN message transactions because the current connection status is unplugged, which matches the status conveyed by the last CSN message transaction.

Additionally, some DP Sink devices that are in a low-power state are known to not reply to AUX transactions while asserting the DFP DPTX's HPD input signal (which is non-compliant with *DP Standard*). The MST Branch device should check that the connected downstream DP device replies to AUX transactions before issuing CSN message transactions for hot plug. In case the downstream DP Sink device does not respond to an AUX transaction, the MST Branch device shall periodically issue an AUX transaction so that it can detect when the DP Sink device becomes responsive.

When an MST Branch device has multiple DFPs and detects unplug/plug events on multiple ports, the device shall generate CSN message transactions for one port at a time. The device shall generate each port's CSN message transaction only after the CSN message transaction for the current port has been handled.

5.6.1.4 Issuance of Resource Status Notify Message Transactions

The DP MST Source devices currently available in the market are capable of handling CSN message transactions, but not Resource Status Notify (RSN) message transactions. Therefore, an MST Branch device shall **not** issue RSN message transactions.

If, for example, the downstream link bandwidth happens to become reduced, a DP MST Branch device shall issue a CSN message transaction for "disconnection" notification, and another CSN message transaction for "connection" notification. The device shall also reply to the ENUM_PATH_RESOURCES message transaction, stating the current link bandwidth capability. As noted earlier in this section, an MST Branch device shall support either TPS4 or POST_LT_ADJ_REQ to avoid link fragility that could reduce the link rate.

5.6.1.5 Power Management Handling

After an upstream device writes 010b to the SET_POWER_STATE field in the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h, bits 2:0), a DP MST Branch device shall disable the UFP's DPRX Main-Link RX while keeping the DFPs' DPTX to the MST downstream ports active with the transmission of VCPF symbol sequences in the allocated time slots.

When an MST Branch device receives a POWER_DOWN_PHY path message transaction, the device shall forward the transaction to the downstream path, and then write 010b to the SET_POWER_STATE field in the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h, bits 2:0) of its immediate downstream device along the message path. When an MST Branch device receives a POWER_DOWN_PHY node message transaction, the device shall write 010b to the SET_POWER_STATE field of all immediate downstream devices.

The MST Branch device shall hold the VC Payload Mapping Table registers (see Section 5.5.1.1) set while in a lower power state. The MST Branch device shall clear the VC Payload Mapping Table registers only after the device receives a CLEAR_PAYLOAD_ID_TABLE message transaction, –or– when the device transitions to SST mode (as described in Section 5.6.1.1).

5.6.1.6 Multi-function MST Branch Device Enumeration

As described in Section 2.6.1.1, a multi-function MST Branch device (i.e., an MST Branch device that is capable of protocol conversion and/or pixel processing in the DFPs) shall enumerate the multi-function capability through a virtual DP output port (logical port) and a virtual DP peer device with DPCD registers.

5.6.1.7 Mvid/Nvid and Maud/Naud Handling

An MST Branch device as the last MST Branch shall replace the Mvid/Nvid and Maud/Naud values with its own calculations and/or measurements when generating the SST output stream.

5.6.1.8 Split SDP Handling

An MST Branch device that is the last MST Branch device in the path shall support handling of a split SDP.

5.6.1.9 DSC Bitstream Handling and FEC

A DSC bitstream decompression-capable DP MST Branch device, as the last MST Branch device, shall have FEC decoding capability (see Section 3.5.1.5).

An MST Branch device may perform DSC decompression only when it is positioned as the last MST Branch device. The intermediate MST Branch devices shall not perform DSC decompression (and thus, also no re-compression). However, the intermediate MST Branch devices shall perform FEC decoding and re-encoding when routing VC Payloads that carry DSC bitstreams. Therefore, an MST Branch device that is capable of FEC decoding and re-encoding shall set the FEC_READY bit in the FEC_CONFIGURATION register (DPCD Address 00120h, bit 0) to 1 when the device trains the downstream DPRX that is capable of FEC decoding.

When the upstream DPTX sets the FEC_READY bit before initiating Link Training, the DP MST Branch device shall delay forwarding of Link Layer Codes to the 8b/10b decoder and descrambler blocks by the same amount needed for FEC decoding, even when the device is not performing FEC decoding.

The last MST Branch device shall be able to regenerate a stable main video, despite the skew of the BE and BS symbol sequence locations caused by FEC parity code insertion.

An MST Branch device that is capable of FEC decoding and re-encoding shall be able to regenerate an SST DSC stream from an MST DSC stream when the device is the last Branch device in the path, regardless of whether the device supports DSC decompression.

5.6.1.10 Interleaved Message Transactions Handling

As described in Section 5.4.2, an MST Source device is no longer allowed to generate interleaved message transactions. However, there are MST Source devices out in the field that issue interleaved message transactions. Therefore, an MST Branch device shall continue being able to handle interleaved message transactions.

5.6.2 MST Branch Device with a DPRX in Multiple UFPs

The policy of an MST Branch device with a DPRX in multiple UFPs is an implementation-specific choice. For example, an MST Branch device that combines multiple SST streams into an MST stream with multiple VC Payloads may choose to either pre-allocate an equal number of time slots among the multiple SST UFPs, –or– take a first-come, first-serve policy.

5.7 DP Source Device with 128b/132b Channel Coding Enabled

New to *DP v2.0*.

This section summarizes the policy of a DP Source device operating with 128b/132b channel coding. All policies of a DP Source device operating with 8b/10b channel coding, as defined in Section 5.1 (SST) and Section 5.4 (MST), apply.

5.7.1 Video Fallback Mode

In case a DP Source device needs to operate in video fallback mode, a DP Source device should operate with 8b/10b channel coding as the mandated Video Fallback mode of 1920x1080 at 60Hz, 24bpp fits in 1-lane of HBR2 link.

5.7.2 Configuring LTTPR-capable PHY Repeaters

As defined in Section 3.6.1.3, a DPTX operating with 128b/132b channel coding shall discover the presence/absence of LTTPR-capable PHY Repeaters and, if present, configure them to Non-transparent mode. In case the DPTX is under basic software control that is incapable of configuring PHY Repeaters to Non-transparent mode, the DPTX shall operate with 8b/10b channel coding, and should program the link rate to the minimum practical to minimize the possibility of link establishment difficulty.

5.7.3 DSC Support

See Section 2.9.1 for the DSC support mandate for a 128b/132b channel coding-capable DP Source device. See Section 2.8.3.2 for the DSC bitstream bpp support mandate.

5.7.4 HDCP Encryption Status Change

A DP Source device operating with 128b/132b channel coding shall:

- Transition from link encryption disable to enable (or vice versa) by changing the HDCP Encryption Indicator bit in the LLCP at the beginning of every link frame
- Enable/disable encryption of each MTP link symbol by setting the ECF field in the LLCP to 1

5.7.5 Allocation Change Trigger

A DP Source device operating with 128b/132b channel coding shall:

- Issue a Time Slot Allocation AUX write transaction, irrespective of transmitting a single stream or multiple streams
- Trigger the time-slot allocation change of DP link symbols transmitted over the DP Main-Link by setting the ACT bit in the LLCP to 1

5.7.6 AUX Message Transaction Support

AUX message transaction support is mandatory for a DP Source device transmitting multiple streams.

A DP Source device transmitting a single stream should also support AUX message transactions for as long as the connected-to DPRX supports AUX message transactions (i.e., either the SINGLE_STREAM_SIDEBAND_MSG_SUPPORT or MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bits 1:0, respectively) is set to 1).

5.7.7 Panel Replay Optimization for DP Tunneling

A DP Source device operating with 128b/132b channel coding should support Panel Replay optimization, as defined in Section 5.14.1.

5.8 DP Sink Device with 128b/132b Channel Coding Enabled

New to *DP v2.0*.

This section summarizes the policy of a DP Sink device operating with 128b/132b channel coding. All policies of a DP Sink device operating with 8b/10b channel coding, as defined in Section 5.2 (SST) and Section 5.5 (MST), apply.

5.8.1 Video Fallback Mode

Support for the SINK_VIDEO_FALLBACK_FORMATS register (DPCD Address 00020h) is mandatory.

5.8.2 DSC Support

See Section 2.9.2 for the DSC support mandate for a 128b/132b channel coding-capable DP Sink device. See Section 2.8.3.1 for the DSC bitstream bpp support mandate.

5.8.3 HDCP Encryption Status Change

A DP Sink device operating with 128b/132b channel coding shall handle the HDCP encryption status change, as indicated by the HDCP Encryption Indicator bit or ECF field in the LLCP, without visual glitch.

5.8.4 Allocation Change Trigger

A DP Sink device operating with 128b/132b channel coding shall handle the time-slot allocation change of link symbols transmitted over the DP Main-Link, as indicated by the ACT bit in the LLCP, without visual glitch.

5.9 DP Branch Device with 128b/132b Channel Coding Enabled

New to *DP v2.0*.

This section summarizes the policy of a DP Branch device operating with 128b/132b channel coding on the UFP. All policies of a DP Branch device operating with 8b/10b channel coding, as defined in Section 5.3 (SST) and Section 5.6 (MST), apply.

5.9.1 DFP Configurations

Support for DFPs, operating either with 128b/132b or 8b/10b channel coding, and either in MST or SST mode, is mandatory.

5.9.2 Virtual DP Peer Device

Support for the following is mandatory:

- Virtual DP Peer devices, as defined in Section 2.6.1.1
- AUX message transactions of DP-to-DP Virtual DP Peer devices (i.e., SINGLE_STREAM_SIDEBAND_MSG_SUPPORT in the MSTM_CAP register (DPCD Address 00021h, bit 1) is set to 1)

5.9.3 DSC Support

See Section 2.9.3 for the DSC support mandate for a 128b/132b channel coding-capable DP Branch device. See Section 2.10 for the DSC Extended Capability and DSC Configuration DPCD registers *DSC v1.3* (and higher) for DSC bitstream bpp support mandate.

5.9.4 Encryption Status Change

A DP Branch device operating with 128b/132b channel coding on the UFP shall handle the HDCP encryption status change, as indicated by the HDCP Encryption Indicator bit or ECF field in the LLCP, without visual glitch.

A DP Branch device operating with 128b/132b channel coding on the DFP shall indicate an HDCP encryption status change by the HDCP Encryption Indicator bit or ECF field in the LLCP.

5.9.5 Allocation Change Trigger

A DP Branch device operating with 128b/132b channel coding on the UFP shall handle the time-slot allocation change of DP link symbols transmitted over the DP Main-Link, as indicated by the ACT bit in the LLCP, without visual glitch.

A DP Branch device operating with 128b/132b channel coding on the DFP shall:

- Issue a Time Slot Allocation AUX write transaction, irrespective of transmitting a single stream or multiple streams
- Trigger the time-slot allocation change of DP link symbols transmitted over the DP Main-Link by setting ACT bit in the LLCP to 1

5.10 Branch-Sink Device in 8b/10b MST Mode

New to *DP v1.4*.

An MST Branch-Sink device (e.g., a daisy-chainable MST display) shall follow the policy requirements of both an MST Sink device and MST Branch device with an embedded PHY Repeater on the DFP or UFP, as described in Section 5.5 and Section 5.6, respectively.

5.11 DP Source or Branch Device with an Embedded PHY Repeater on the DFP

New to *DP v1.4a*.

Figure 5-5 illustrates a DP Source or Branch device ("DPTX") with a PHY Repeater on the DFP. A DPTX with an embedded PHY Repeater on the DFP, upon enabling the transition to LTTPR Non-transparent mode, shall control the PHY Repeater's DFP TX drive setting by writing to either the DPTX TRAINING_LANE*x*_SET register(s) (DPCD Addresses 00103h through 00106h, respectively) –or– LTTPR TRAINING_LANE*x*_SET_PHY_REPEATER*y* register(s) (e.g., DPCD Address F0011h for LTTPR1, Lane 0), where *x* = 0, 1, 2, or 3 and *y* = the PHY_REPEATER_CNT register's (DPCD Address F0002h) count of its immediate downstream device. (That is, a DPTX with an embedded PHY Repeater on the DFP that is incapable of controlling the PHY Repeater's DFP TX drive setting as described above shall **not** enable the transition to LTTPR Non-transparent mode.)

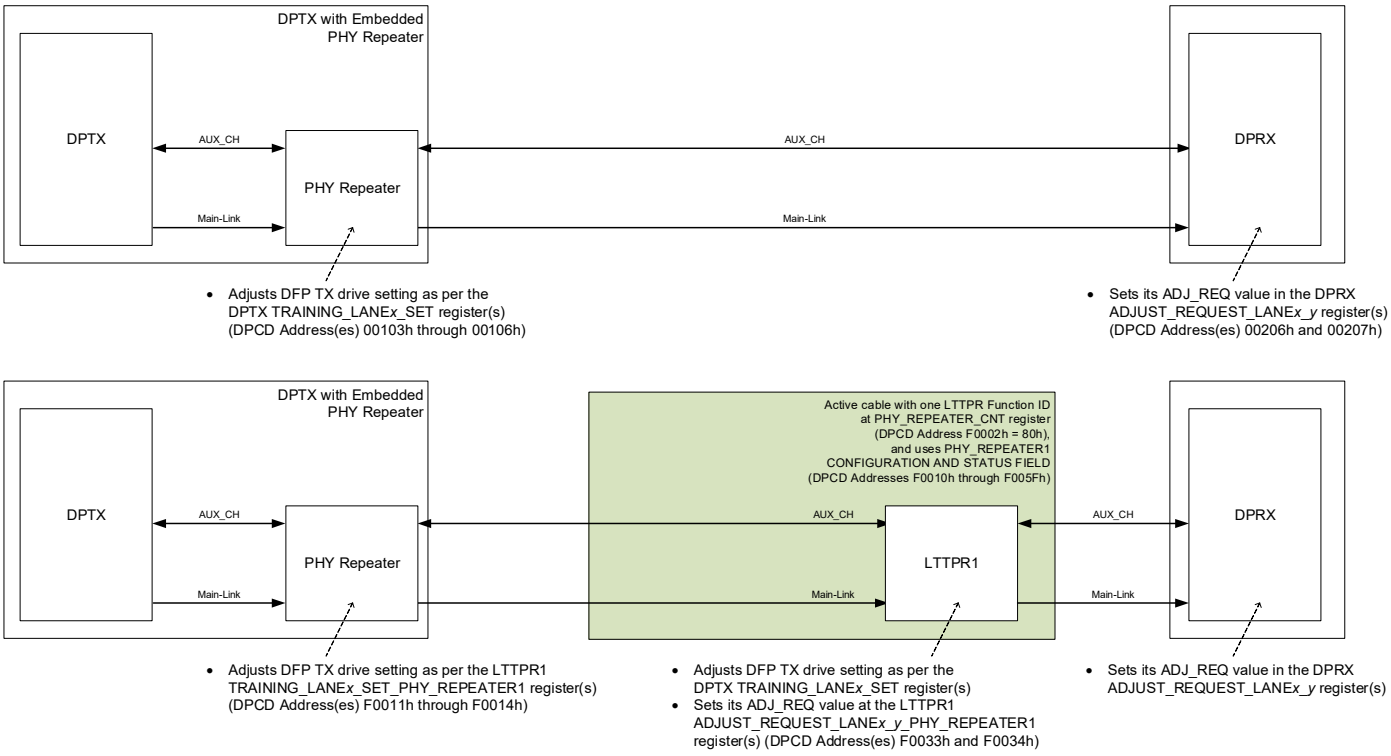


Figure 5-5: DPTX with an Embedded PHY Repeater

5.12 DP Sink or Branch Device with an Embedded PHY Repeater on the UFP

New to *DP v1.4a*.

Figure 5-6 illustrates a DP Sink or Branch device ("DPRX") with an embedded PHY Repeater on the UFP. A DPRX with an embedded PHY Repeater on the UFP may use either a PHY Repeater with an LTTPR function –or– a "legacy mode PHY Repeater" without an LTTPR function that does not handle LTTPR-specific DPCD registers.

How to control a legacy mode PHY Repeater within the device, if used, is an implementation-specific choice and is beyond the scope of this Standard.

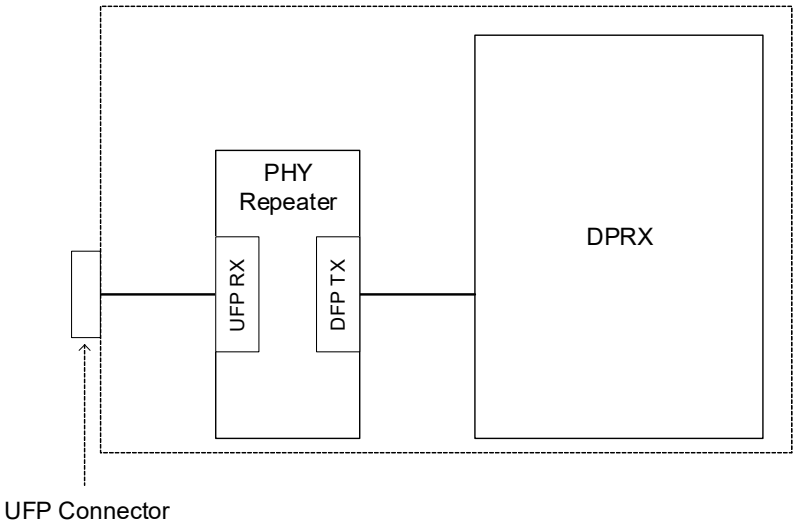


Figure 5-6: DPRX with an Embedded PHY Repeater

5.13 Cable-Connector Assembly

This section describes support for the cable-connector assembly.

5.13.1 Box-to-Box, User-Detachable Cable Assembly

A box-to-box, user-detachable DP cable assembly shall support four Main-Link lanes.

Box-to-box, user-detachable DP cable assemblies of 2m or less shall meet the high bit rate cable specification, as detailed in Section 4.

All box-to-box, user-detachable DP cable assemblies shall meet the low bit rate cable specification, as defined in Section 4.

Mating connectors of the box-to-box DP connection shall meet the connector specification, as defined in Section 4.

5.13.2 Embedded and Captive Cable Assembly

An embedded or captive DP cable assembly may support fewer than four Main-Link lanes as long as "sufficient" link bandwidth is provided for the design application with fewer lanes.

For embedded and captive connections, the system integrator shall select a cable assembly with sufficient bandwidth capacity.

5.13.3 Active Cable Assembly

Updated in *DP v2.0*.

Active cable assemblies shall contain one or two LTTPR functions with Main-Link signal conditioning capability, with the objective to enable a longer cable. The LTTPR function may be located in the Source-side plug connector, the Sink-side plug connector, or both. The Source-side and Sink-side ends of an active cable assembly generally cannot be reversed; therefore, the manufacturer shall clearly identify each end if an active cable is **not** reversible (i.e., in a user's manual and/or through labeling). The transmission medium is not explicitly specified. Thus, active cable assemblies may be optical, or copper using various types of bulk cable (i.e., there is no requirement to use bulk cable, as described in Section 4.1.2). Active cable assemblies may belong to Types C1A, C2A, C3A, or Type E1A, as described in Section 4.1.1.

Type E1A is intended to be used with a DPRX that has a captive cable. Cascading of Type E1A and Types C1A, C2A, and C3A is **not** supported.

Mating connectors of active cable assemblies shall meet the connector specification, as defined in Section 4.

5.13.3.1 Active Cable Assembly Electrical Parameters

Entire section rewritten for *DP v1.4a*.

Active cable assemblies shall support four Main-Link lanes. Active cable assemblies shall support the HBR3, HBR2, HBR, and RBR bit rates. An active cable assembly shall have an AUX_CH that meets the specifications of Section 3.4.

An active cable assembly shall provide connection between the Hot Plug Detect pins at both ends. If the active cable assembly has plug connectors at both ends (Types C1A, C2A, or C3A), there shall be connections between pins CONFIG1 and CONFIG2 of the plug connectors at both ends, similar to the passive external cable assembly wiring illustrated in Figure 4-29. If the active cable assembly has a receptacle connector on one end (Type E1A), there shall be no connections between the pins CONFIG1 and CONFIG2 of the connectors at both ends. Thus, the pins CONFIG1 and CONFIG2 of the receptacle connector end shall be shorted by a less than 100Ω resistor if the active cable consumes power at the receptacle connector end.

5.13.3.1.1 Main-Link Requirements

A DPTX shall insert 20UI nominal of skew between adjacent Main-Link lanes. The deviation from this nominal inter-lane skew shall be kept within ±2UI.

DP active cables are divided into two categories, as listed in Table 5-11.

Table 5-11: DP Active Cable Categories

Category	Description	Type
Active Cable Assembly	Plug connectors on both ends.	C1A, C2A, or C3A
Active Extension Cable Assembly	Plug connector on the UFP and a receptacle connector on the DFP.	E1A

For Types C1A, C2A, and C3A, and Type E1A, the UFP RX of an active cable shall meet the RX JTOL specification, as defined in Table 3-44 through Table 3-46 in Section 3.5.4 with the TP1 and TP2/TP2_CTLE stressed signals. Stressed signal generation for the TP1 EYE shall use the maximum allowable differential voltage swing of 1.38V_diff_pp to exercise the RX in the over-driven condition.

The DFP TX of an active cable shall meet the TX EYE opening and TX drive setting monotonicity test specifications defined in Table 5-12.

Table 5-12: DFP TX of an Active Cable TX EYE Opening and TX Drive Setting Monotonicity Test Specifications

Cable Assembly Type	Bit Rate	Description[a]
C1A/ C2A/ C3A	HBR3/ HBR2	• DFP TX EYE opening, tested at the mated DFP connector without a cable (i.e., TP2_EQ), shall meet the TP3_EQ EYE mask specification, as defined in Table 3-41 or Table 3-42 for HBR3 or HBR2, respectively • DFP TX drive setting monotonicity, tested at the mated DFP connector without a cable (i.e., TP2), shall meet the TX drive setting monotonicity specification, as defined in Table 3-39
	HBR	• DFP TX EYE opening, tested at the mated DFP connector without a cable (i.e., TP2), shall meet the TP3_EQ EYE mask specification, as defined in Table 3-48 • DFP TX drive setting monotonicity, tested at the mated DFP connector without a cable (i.e., TP2), shall meet the TX drive setting monotonicity specification, as defined in Table 3-40
	RBR	• DFP TX EYE opening, tested at the mated DFP connector without a cable (i.e., TP2), shall meet the TP3 EYE mask specification, as defined in Table 3-49 • DFP TX drive setting monotonicity, tested at the mated DFP connector without a cable (i.e., TP2), shall meet the TX drive setting monotonicity specification, as defined in Table 3-40
E1A	HBR3/ HBR2	• DFP TX EYE opening, tested at the mated DFP connector both with and without a cable (i.e., TP3_EQ and TP2_EQ, respectively), shall meet the TP3_EQ EYE mask specification, as defined in Table 3-41 or Table 3-42 for HBR3 or HBR2, respectively • DFP TX drive setting monotonicity, tested at the mated DFP connector without a cable (i.e., TP2), shall meet the TX drive setting monotonicity specification, as defined in Table 3-39
	HBR	• DFP TX EYE opening, tested at the mated DFP connector both with and without a cable (i.e., TP3 and TP2, respectively), shall meet the TP3_EQ EYE mask specification, as defined in Table 3-50 • DFP TX drive setting monotonicity, tested at the mated DFP connector without a cable (i.e., TP2), shall meet the TX drive setting monotonicity specification, as defined in Table 3-40
	RBR	• DFP TX EYE opening, tested at the mated DFP connector both with and without a cable (i.e., TP3 and TP2, respectively), shall meet the TP3 EYE mask specification, as defined in Table 3-51 • DFP TX drive setting monotonicity, tested at the mated DFP connector without a cable (i.e., TP2), shall meet the TX drive setting monotonicity specification, as defined in Table 3-40

a. All referenced tables are in Section 3.5.4.

The DFP TX of an active cable shall adjust the signal level outputs during link training according to either the DPTX TRAINING_LANE*x*_SET DPCD register(s) (DPCD Addresses 00103h through 00106h, respectively) –or– LTTPR TRAINING_LANE*x*_SET_PHY_REPEATER*y* register(s) (e.g., DPCD Address F0011h for LTTPR1, Lane 0), where *x* = 0, 1, 2, or 3 and *y* = the PHY_REPEATER_CNT register's count (DPCD Address F0002h, 1 through 8), depending on the number of LTTPRs between the DFP TX and DPRX, as illustrated in Figure 5-7.

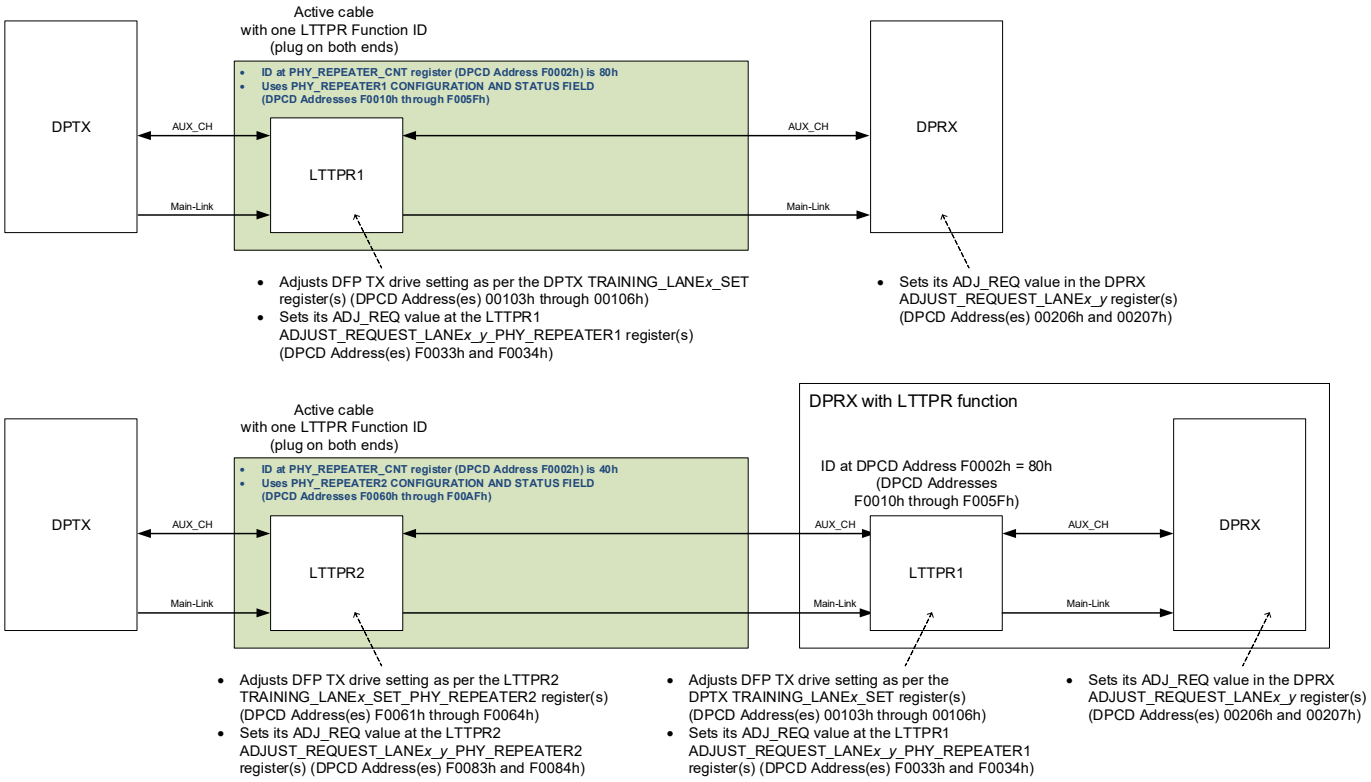


Figure 5-7: PHY Layer Topologies without and with One LTTPR Function between DFP of an Active Cable and a DPRX

LTTPR Non-transparent mode is enabled by an AUX transaction to the LTTPR DPCD registers, as described in Section 3.6. Before Non-transparent mode is enabled, the LTTPR function operates in Transparent mode and adjusts the DFP TX drive setting according to the DPTX TRAINING_LANE*x*_SET DPCD register value(s). Even in Transparent mode, the active cable's output signal at the mated DFP connector pins shall meet the EYE mask and TX drive setting requirements.

A DPRX plugged to the DFP of an active cable may be DC-coupled and assume that its input is externally AC-coupled. It would therefore set the common mode voltage that is appropriate to its implementation. The implementation of active cables shall ensure that PHY Repeater(s) do **not** impact the plugged DPRX's (e.g., a DP Sink device) common mode assumptions. An appropriate method to ensure this is to AC-couple the active cable's output on the Main-Link, following the same specification for AC-coupling of a DPTX (e.g., a DP Source device).

5.13.3.1.2 AUX_CH Requirements

New to *DP v1.4a*.

The active cable shall handle AUX transactions to LTTPR registers, as specified in Section 3.6.

Table 5-13 defines the active cable unidirectional AUX latency requirements.

Table 5-13: Active Cable Unidirectional AUX Latency Requirements

Mode	Requirement
Transparent	• Unidirectional AUX latency shall not exceed 40us, –or– • Use a store-and-forward mechanism, providing a response within the timeouts defined in Section 2.11.2 at its DPRX using an AUX_DEFER, re-issuing the AUX request at its DPTX, and then providing the response at its DPRX when the DP Source device retries
Non-transparent	• Meet the LTTPR delay, as defined in Section 3.6

The AUX latency requirement shall apply to AUX transaction transmission in both directions.

The AUX output shall meet the slew rate and AUX RX input EYE requirements defined in Table 3-5, Table 3-7, and Figure 3-10 in Section 3.4.2. These output requirements shall be met as long as the input matches the slew rate and minimum stressed EYE requirements defined in Table 3-5, Table 3-8, and Figure 3-11 in Section 3.4.2. The active cable shall meet these requirements for AUX transmission in both directions.

An LTTPR in an active cable shall be in Transparent mode after a cable reset or upstream device disconnect event.

5.13.3.1.3 HPD and DP Source Device Connect/Disconnect Requirements

New to *DP v1.4a*.

The active cable shall forward the HPD signal from its DFP to its UFP. Additionally, the active cable shall forward an upstream device disconnect event from its UFP to its DFP.

5.13.3.1.4 Active Cable Sleep

New to *DP v2.0*.

5.13.3.1.4.1 Active Cable Sleep Entry In Transparent and Non-transparent Modes

See Section 3.6.10.3 for using the following registers when using active cables in Transparent and Non-transparent modes:

- **Transparent mode** – EXTENDED_DPRX_SLEEP_WAKE_TIMEOUT_REQUEST and EXTENDED_DPRX_SLEEP_WAKE_TIMEOUT_GRANT register (DPCD Address 02211h and 00119h, respectively)
- **Non-transparent mode** – PHY_REPEATER_EXTENDED_WAKE_TIMEOUT register (DPCD Address F0005h)

If a DP Source device grants an extended timeout request, an active cable shall snoop AUX write transactions to the SET_POWER_STATE field in the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h, bits 2:0). After the cable detects a write of 010b to this field, the active cable shall transition to the SLEEP power state. (See Section 5.13.3.1.4.1 for the power consumption limits in this state.)

If the active cable detects a write of 101b to the SET_POWER_STATE field, the cable may go to a lower power state (separate from the SLEEP power state) by disabling circuitry that is related to the Main-Link. When the SET_POWER_STATE field is programmed to 101b, the active cable shall handle AUX transactions without any timeout. Note that the Section 5.13.3.1.4.1 power consumption limits do **not** apply when the SET_POWER_STATE field is programmed to 101b.

5.13.3.1.4.2 Active Cable Sleep Power

The active cable's current consumption from the power rail, either DP_PWR or V_{CONN}, in the SLEEP power state (SET_POWER_STATE field in the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h, bits 2:0) is programmed to 010b) shall be limited to 150mW. The transition to SLEEP state power consumption shall be completed within 250ms after an AUX_ACK to the AUX write request transaction to program the field to 010b.

Note: *A DPTX shall not reduce the power to DP_PWR or V_{CONN} to 150mw until granting an extended wakeup timeout request (if requested).*

5.13.3.1.5 Active Cable Wake

New to *DP v2.0*.

An active cable shall monitor for the presence of differential signaling on the AUX_CH for a wake indication. The active cable shall wake in 1ms unless an extended wake timeout has been granted, as indicated by the following register bits being set to 1:

- **Transparent mode** – DPRX_SLEEP_WAKE_TIMEOUT_PERIOD_GRANTED bit in the EXTENDED_DPRX_SLEEP_WAKE_TIMEOUT_GRANT register (DPCD Address 00119h, bit 0)
- **Non-transparent mode** – EXTENDED_WAKE_TIMEOUT_GRANT bit in the PHY_REPEATER_EXTENDED_WAKE_TIMEOUT register (DPCD Address F0005h, bit 7)

5.13.3.1.6 Active Cable Flow and Process (Informative)

New in *DP v2.0*.

An active cable may have either one or two LTTPR functions inside, as illustrated in Figure 5-8.

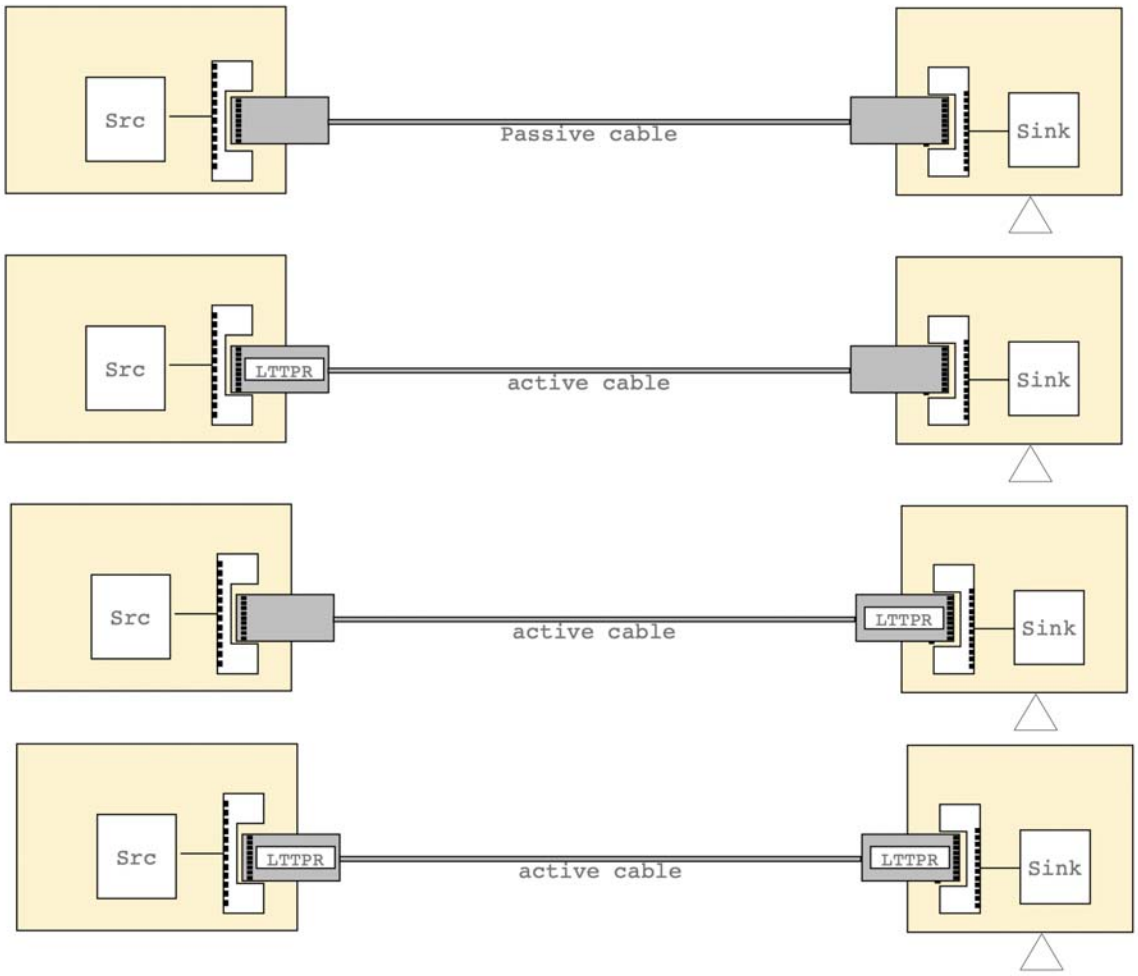


Figure 5-8: Active Cable Topology

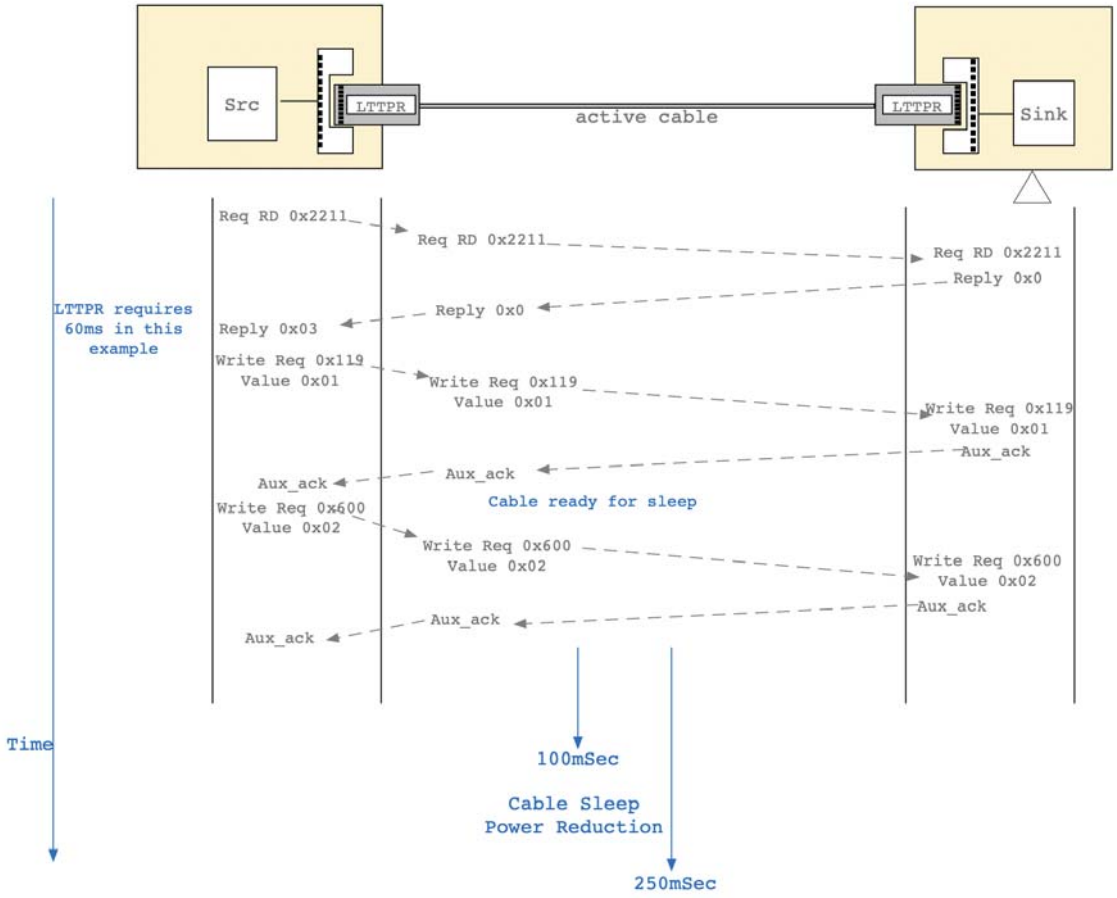


Figure 5-9: Extended Wake Request and SLEEP Power State Entry Flow when Active Cable Requests Extended Wake

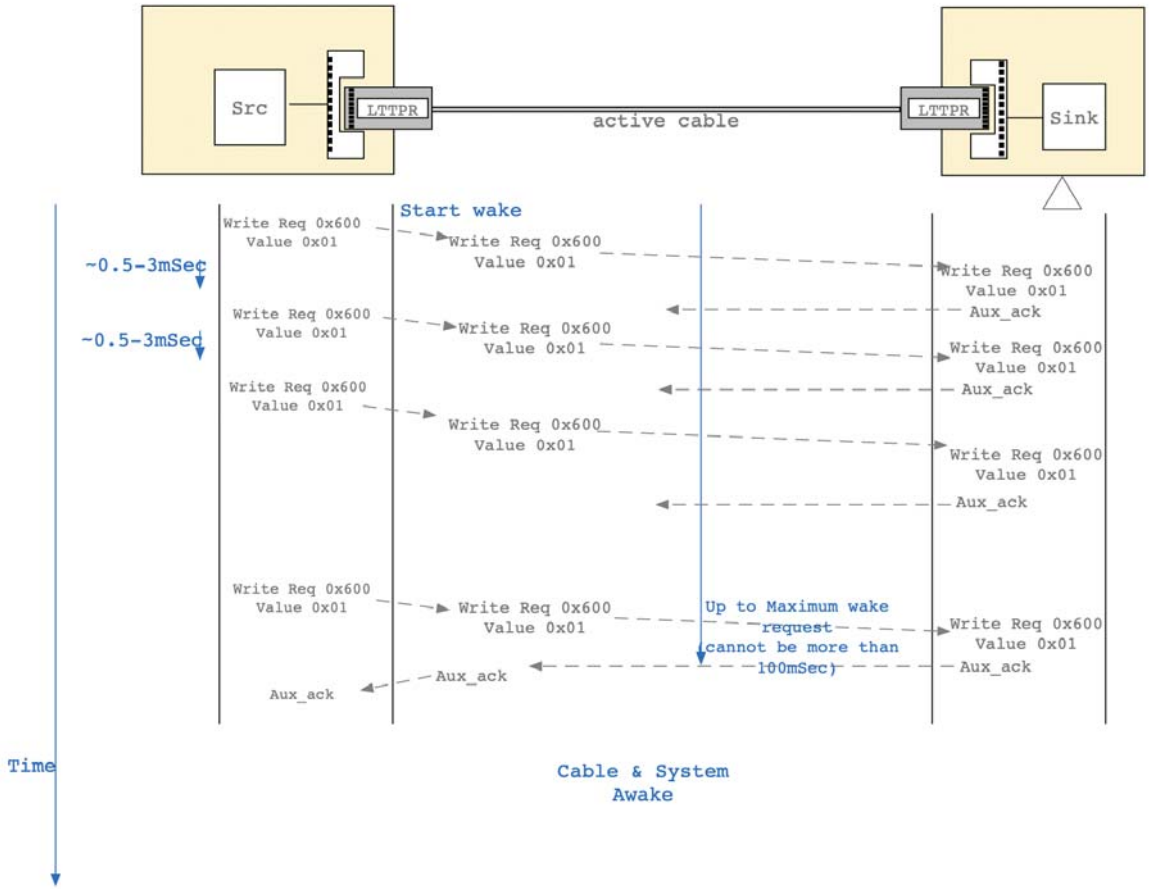


Figure 5-10: Wake from SLEEP Power State after Extended Wake Request from Active Cable Is Granted

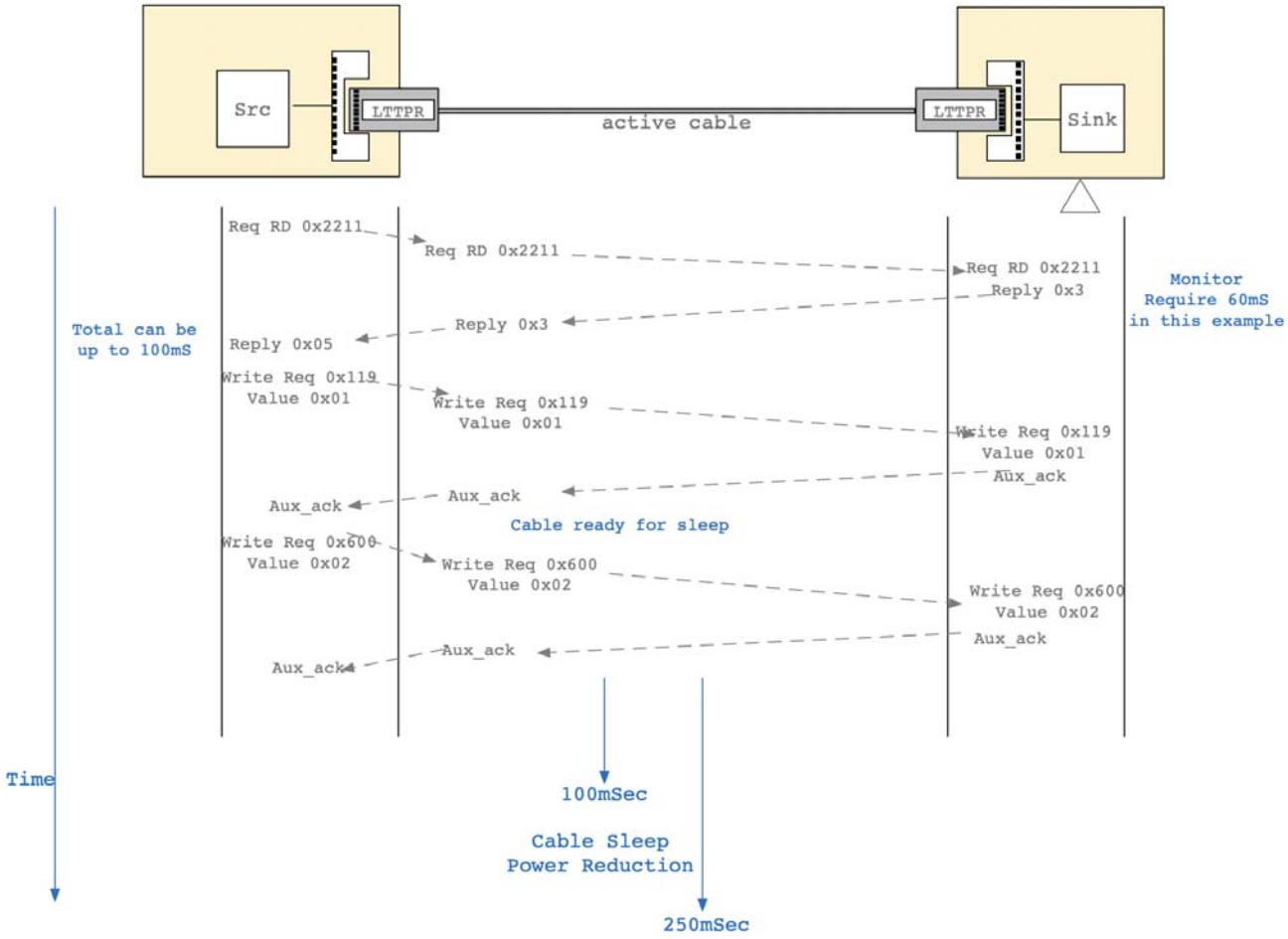


Figure 5-11: Extended Wake Request and SLEEP Power State Entry Flow when Active Cable and DP Sink Device Both Request Extended Wake

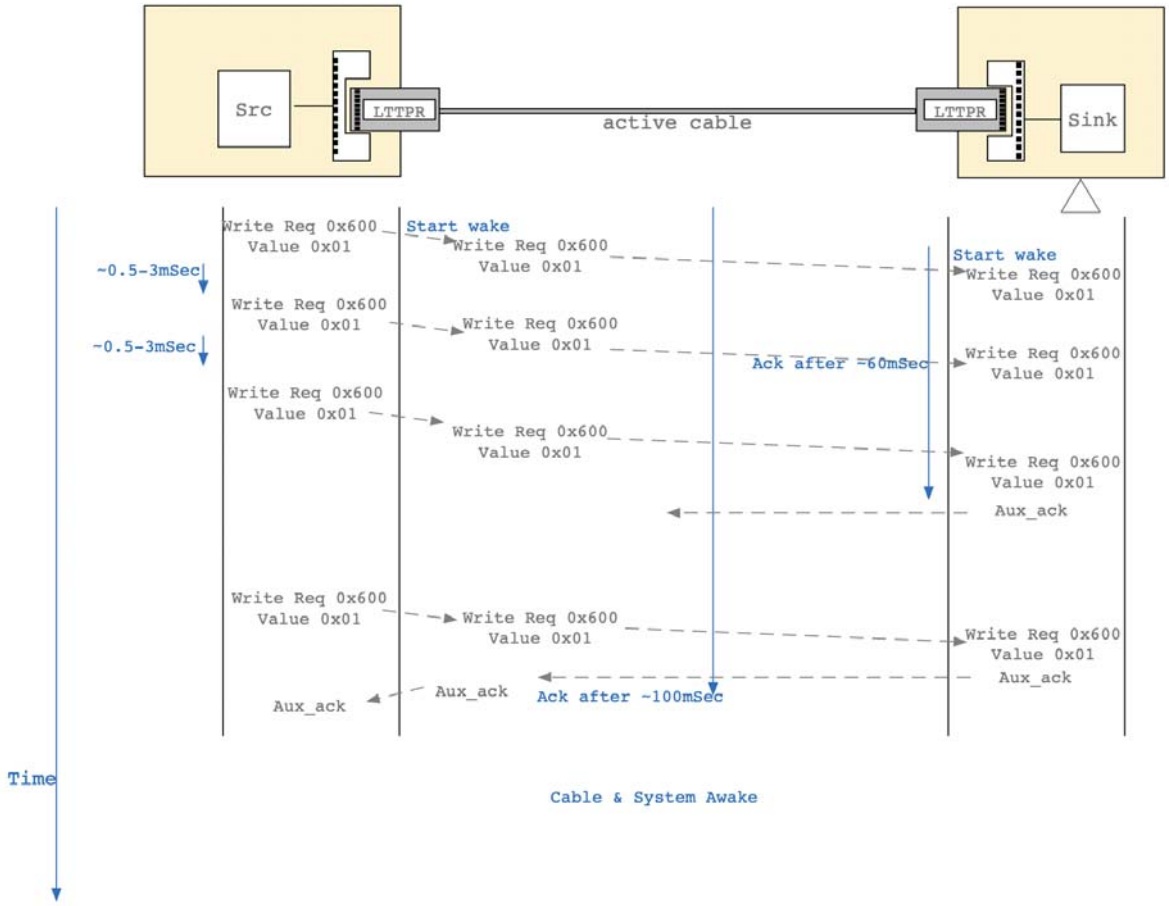


Figure 5-12: Wake from SLEEP Power State after Both Extended Wake Requests from Active Cable and DP Sink Device Are Granted

5.13.3.2 Active Cable Assembly DP_PWR Requirements

Active cable assemblies are devices that consume DP_PWR. An active cable assembly may use power provided by the upstream device, the downstream device, or both. Active cable assemblies shall meet the requirements for devices that consume DP_PWR as detailed in Section 3.2, with the exception of the DP_PWR wire requirement of Section 3.2.2. Even though an active cable assembly may have a power wire running through the cable, there shall be no connection between the DP_PWR pins of the plug connectors at the two ends of the assembly.

5.14 DP Tunneling

New to *DP v1.4a*.

DisplayPort may be tunneled over another transport protocol (e.g., Thunderbolt).

Typically, the DP output from a DP Source device is presented as an input to a Downstream-facing Tunneling Bridge device within the system that contains the DP Source device. The DP output from a DP Source device is tunneled over the other transport protocol to a system that includes an Upstream-facing Tunneling Bridge device that extracts the DP stream, and then presents the DP stream to a DP Sink or Branch device (or possibly a DP Source connector). This configuration is illustrated in Figure 5-13.

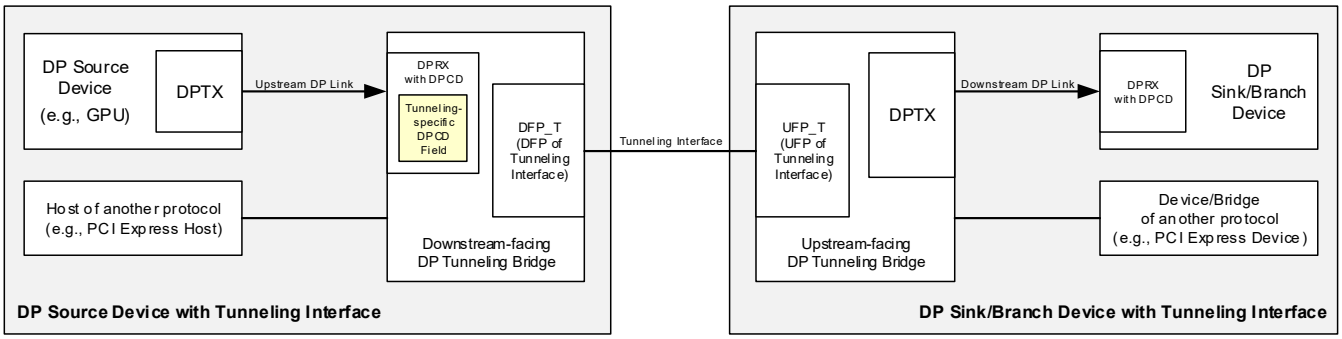


Figure 5-13: DP Tunneling from DP Source Device to DP Sink/Branch Device

In some implementations, the Downstream-facing Tunneling Bridge device can operate in a mode in which the device directly generates the DP stream if the system is connected to a DP Sink device. This configuration is illustrated in Figure 5-14.

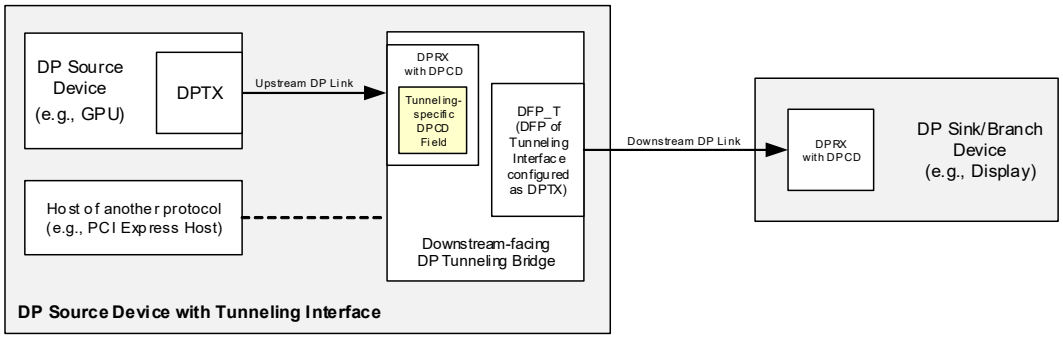


Figure 5-14: DP Output from a DP Downstream-facing Tunneling Bridge Device

In either of these configurations, the provision of vendor-specific features should be supported. To support this, an **optional** set of Tunneling-specific registers at DPCD Addresses E0000h through E000Bh and E000Dh is used (see Table 2-197 on page 573), by which the Tunneling device can provide additional information to a tunneling-aware DP Source device. The registers contain the IEEE_OUI of the organization responsible for the tunneling protocol in use and device identification information. The remaining registers at DPCD Addresses E000Ch, and E000Eh through E00FFh are specified by the organization.

5.14.1 Panel Replay Optimization with DP Tunneling

New to *DP v2.0*.

In Panel Replay mode, a DP Source device indicates the mode to a DP Sink device by way of the VSC SDP, as defined in Section 2.17. This section defines the normative method by which a DP Source device in Panel Replay mode signals the presence of "dummy" pixel data DP link symbols (to be discarded by DP Sink device) to the Downstream-facing Tunneling Bridge without the bridge having to perform HDCP decryption to parse the VSC SDP's content. The signaling allows the Downstream-facing Tunneling Bridge to convey the locations and number of dummy link symbols to the Upstream-facing Tunneling Bridge instead of tunneling all those link symbols. This allows the transport protocol to allocate additional bandwidth to the tunneling of non-display data. In turn, the Upstream-facing Tunneling Bridge regenerates the dummy symbols, thereby enabling the tunneling of Panel Replay without affecting the Panel Replay-capable DP Sink device.

The DP Source device may **optionally** enable Panel Replay optimization with DP tunneling. The device shall query the Tunneling Bridge's Panel Replay tunneling optimization capability by way of the Panel Replay Tunneling Optimization Support bit in the DP TUNNELING and PANEL REPLAY OPTIMIZATION SUPPORT register (DPCD Address E000Dh, bit 6), and then enable Panel Replay only when the Tunneling Bridge is capable.

5.14.1.1 Dummy Symbol Signaling with SST Mapping Protocol

A DP Source device shall replace the K27.7 BE control link symbol of the dummy pixel lines (where all the pixel data is dummy data) with K28.7. The Upstream-facing Tunneling Bridge device shall reissue the dummy pixel lines, with the transfer units (TUs) as transmitted by the DP Source, and then revert K28.7 back to the regular K27.7 BE control link symbol.

Figure 5-15 illustrates the dummy symbol signaling with SST mapping protocol when Panel Replay optimization with DP Tunneling is enabled.

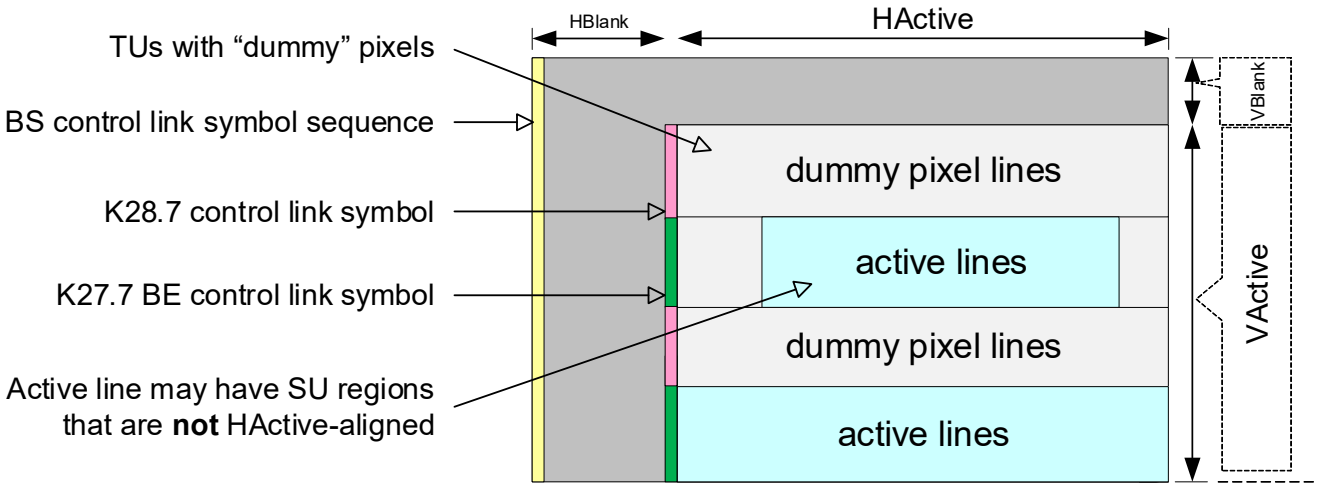


Figure 5-15: Dummy Symbol Signaling with SST Mapping Protocol when Panel Replay Optimization with DP Tunneling Is Enabled

The DP Source device shall use the K27.7 BE control link symbol on the lines that have a portion that includes active pixel data (as in the case of SU operation). All the dummy data DP link symbols on those lines are tunneled.

5.14.1.2 Dummy Symbol Signaling with MST Mapping Protocol and 128b/132b Channel Coding

In DP Tunneling mode, a DP Source device shall insert Active Video Fill control link symbol in place of the "dummy" data in dummy pixel lines (i.e., lines that do **not** have pixels that need to be refreshed on the display). The Stream Fill (SF) control link symbol sequence is **not** replaced with Active Video Fill control link symbols.

With the MST mapping protocol, the Active Video Fill control link symbol shall be C7-C7-C7-C7.

When 128b/132b channel coding is enabled (the MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h) is programmed to 02h), 1011b control-character encoding shall be used for Active Video Fill control link symbols.

The Upstream-facing Tunneling Bridge device shall revert those Active Video Fill control link symbols to dummy pixel data DP link symbols.

Figure 5-16 illustrates the dummy symbol signaling with MST mapping protocol and 128b/132b channel coding when Panel Replay optimization with DP Tunneling is enabled.

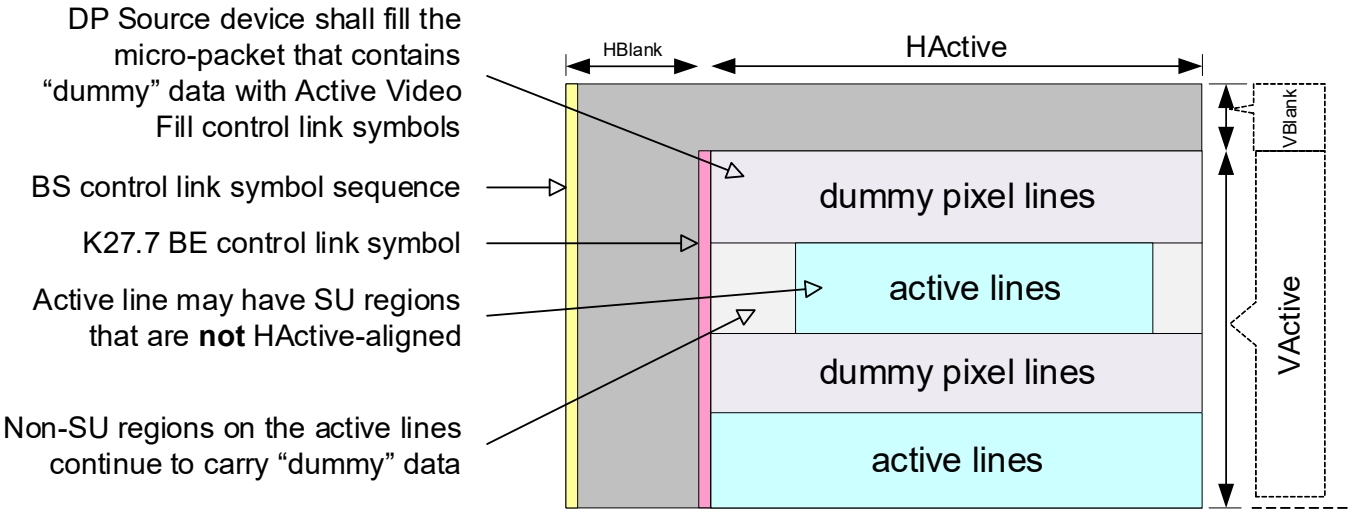


Figure 5-16: Dummy Symbol Signaling with MST Mapping Protocol and 128b/132b Channel Coding when Panel Replay Optimization with DP Tunneling Is Enabled

5.14.1.3 DPCD Register Used with Panel Replay Optimization with DP Tunneling

Table 5-14 lists the DPCD register that is used for Panel Replay Optimization with DP Tunneling. (For complete register description, see Table 2-197.)

Table 5-14: DPCD Register Used with Panel Replay Optimization with DP Tunneling

DPCD Address	Definition	Read/Write over AUX_CH
E000Dh	**DP TUNNELING and PANEL REPLAY OPTIMIZATION SUPPORT**	Read/Write

A Audio Transport (Informative)

Audio-related secondary-data packets (SDPs) are covered in Section 2.2.5. This appendix, intended to be read along with that section, aims to add clarification to the Standard and reduce ambiguity, to improve the interoperability between audio-capable DP devices.

A.1 Audio Stream Components

An audio stream is composed of the following components:

- Audio_Stream SDPs
- Audio_TimeStamp SDPs
- Audio INFOFRAME SDPs (as defined in *CTA-861-G*)
- Partial audio time stamps within VB-ID

In DP Standards, all audio-related packets except VB-ID are transported as part of the SDP stream.

An Audio_Stream SDP includes audio stream itself and some attribute information such as audio coding type and channel count. Depending on the coding type of Audio_Stream SDP, it may contain status information about parameters of the audio stream. For example, the L-PCM Audio and specific compressed audio formats follow the *IEC 60958* and transfer this information in serial format, using a block of samples (see *IEC 60958-1* and *IEC 60958-3*). One Bit audio and DST audio coding types follow the *CSA ISO/IEC 14496-3*, *Subpart 10*, encoding standard. These coding types stream single-bit audio samples as serial blocks (also referred to as "frames") with limited in-band meta data. Additional attribute information for these coding types (e.g., Sample Frequency) shall be programmed in the Audio INFOFRAME SDP.

An Audio INFOFRAME SDP is used for transferring audio stream attributes in a separate packet. Depending on the Audio_Stream SDP's coding type, there is some overlap between the information carried by Audio_Stream SDP and that carried by Audio INFOFRAME SDP. Whenever there is an overlap, the information carried by the Audio_Stream SDP takes precedence. The Audio INFOFRAME SDP shall be referred to in limited cases and for limited information in *DP v1.4a*:

- Audio channel to speaker mapping for uncompressed coding types with more than two channels (e.g., 8-channel L-PCM Audio, 8-channel One Bit, –or– 16- or 32-channel L-PCM 3D Audio)
- Sample frequency for the One Bit and DST audio coding types

Audio INFOFRAME SDP transmission may be omitted altogether when Basic Audio is transmitted.

An Audio_TimeStamp SDP is used for audio clock regeneration to restore the audio master clock frequency that is needed for further audio processing.

Additional signals such as "audio mute" signal for disabling audio are carried in the VB-ID byte that is transmitted next to each BS control link symbol.

Section A.2 describes how the time slot for Audio_Stream SDP transmission shall be scheduled. An Audio_TimeStamp SDP and Audio INFOFRAME (non-Basic Audio) SDP shall be transmitted once per frame, and should be transmitted during the main video stream's vertical blanking period.

Note: *The Audio_TimeStamp SDP may be transferred more than once per frame. How many times to transfer the Audio_TimeStamp SDP is DPTX implementation-specific.*

A.2 Association of Three SDP Types by way of Packet ID

Audio stream transport over a DP link involves the transmission of three SDP types:

- Audio_Stream SDP
- Audio_TimeStamp SDP
- Audio INFOFRAME SDP

These SDPs for a single audio stream are associated with one another by having the same Secondary-data Packet ID (00h) carried as HB0 (Header Byte 0) of each SDP.

A.3 Scheduling of Audio_Stream SDP Transmission

An audio stream is a continuous (i.e., isochronous) stream of audio samples, each of which may contain several channels of audio signals at a pre-defined sample frequency (*Fs*). The sample frequency is typically within the range of 32 to 192kHz for L-PCM Audio, L-PCM 3D Audio, and non-HBR compressed audio. The sample frequency of HBR audio is within the range of 256 to 1536kHz. The sample frequency of One Bit and DST audio is within the range of 2048 to 24576kHz.

The transmission scheduler for an Audio_Stream SDP shall wait for a time slot for audio transmission during which there are no main video stream, MSA packet, and other higher priority secondary-data packets in-queue. Therefore, the DPTX and DPRX shall have some buffer space to hold the audio data while the Audio_Stream SDP is waiting for its time slot.

Figure A-1 illustrates how the Audio_Stream SDPs are transferred over the DP link when there is no video being transmitted. Figure A-2 illustrates the Audio_Stream SDP transfer with main video stream being transmitted. The transmission of Audio_Stream SDPs is withheld from BE symbol assertion until BS symbol assertion because the main video stream occupies the link during that period. Instead, Audio_Stream SDPs are transmitted between BS and BE. During the main video stream's vertical blanking period, the Audio_Stream SDP transfer pattern shall be similar to Figure A-1.

Note: *The presence or absence of main video stream is indicated in the NoVideoStream_Flag bit in the VB-ID (bit 3).*

As noted earlier, Audio_Stream SDPs may be transmitted over the link at any time, as long as the time slot is available. Because the video line period of a given video format and audio sample rate are constant throughout a video vertical frame period, the number of audio samples that shall be transmitted over DP per a main video stream line period is fairly constant for the given video format. No special audio bandwidth allocation calculation shall achieve this scheduling control.

The higher the audio data rate (in MBps) and the longer the main video line period, the larger the buffer size requirement. An implementer should determine the buffer size by determining the maximum audio data rate and the longest main video line period that need to be supported.

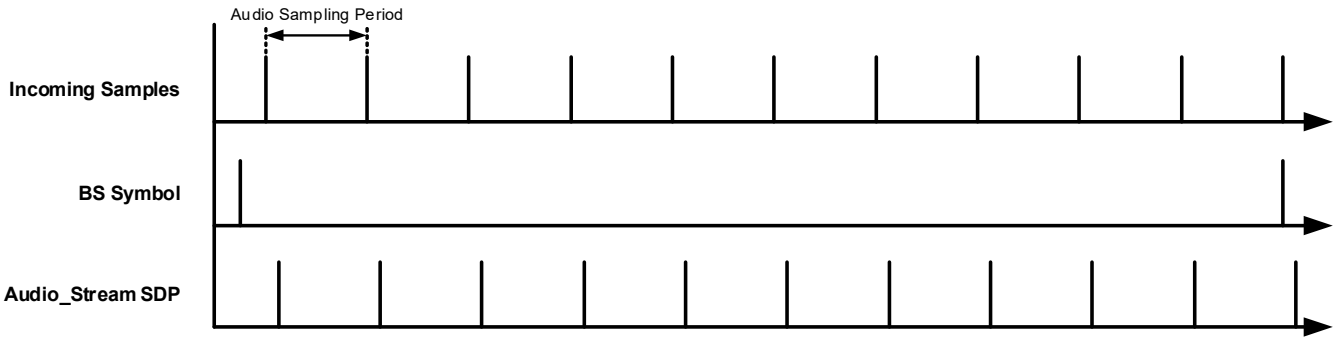


Figure A-1: Audio_Stream SDPs Transfer with No Video or during Video Vertical Blanking

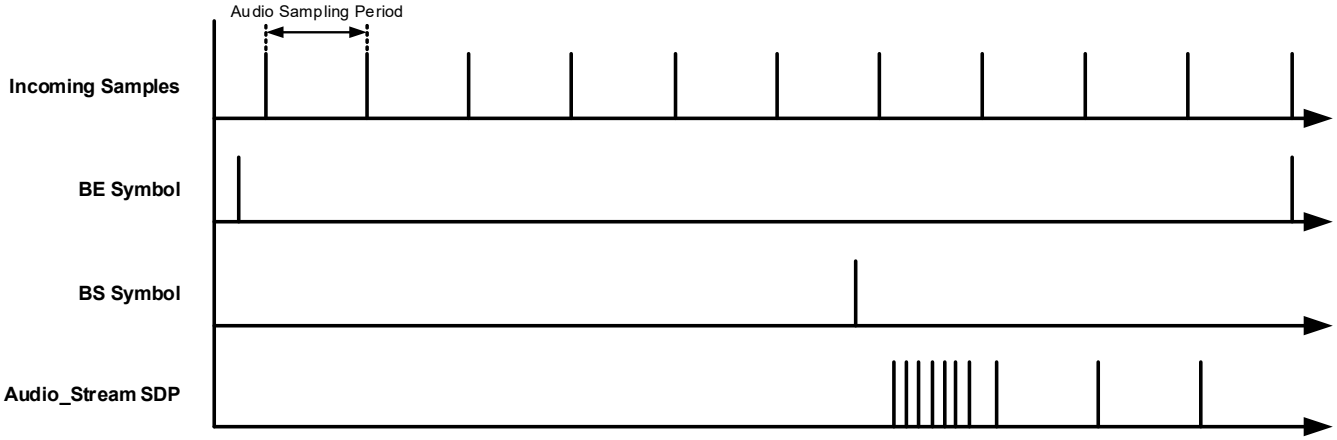


Figure A-2: Audio_Stream SDPs Transfer with Video during Video Vertical Active Period

A.3.1 Audio Format Change Handling

The transported audio format may be changed at any time. The DPTX should start transmitting an audio mute signal prior to the audio format change by setting the AudioMute_Flag bit in the VB-ID (bit 4), which is transmitted once per main video stream line period (or once per 8192 link symbols when the main video stream is absent). An audio format change is caused by a change in any of the following:

- Between the compressed and non-compressed audio
- Between different coding types
- In the sampling rate
- In the number of channels

This signal indicates to the DPRX that the audio system is in a transient process and the audio stream may be not valid at this time. When the AudioMute_Flag bit is 1, a DPRX shall disable its audio output while continuing to receive and process Audio_TimeStamp SDPs.

The DPTX should clear the AudioMute_Flag bit to 0 only after finishing the transient process at the audio source input, finishing audio clock measurement with a correct and stable value and providing information about this change to the DPRX. The DPTX should clear the audio mute signal only after transferring Audio_TimeStamp SDP and Audio INFOFRAME SDP (if needed).

After the DPTX clears the AudioMute_Flag bit to 0, a DPRX should enable its audio output only after the regenerated audio clock becomes stable and after it has collected sufficient audio status information.

A.4 Audio_Stream SDP Structure

DP v1.4a defines four audio coding types, as specified in the HB3 Coding Type field (bits 7:4) of an Audio_Stream SDP. These audio coding types follow *IEC 60958* or *CSA ISO/IEC 14496-3*, *Subpart 10*, encoding standards. Additional coding types are expected to be added in the future. Therefore, a DPRX shall check the Coding Type field to remain compatible with future versions/ revisions of this Standard.

The HB3 ChannelCount field (bits 2:0) of an Audio_Stream SDP carries information about the count of non-L-PCM Audio or One Bit audio channels transmitted through a DP Main-Link. This field shall have following values:

- 000b for 1-channel L-PCM Audio or One Bit audio
- 001b for 2-channel L-PCM Audio or One Bit audio
- Up to 111b for 8-channel LPCM or One Bit audio

The HB2 3DChannelCount field (bits 4:0) of an Audio_Stream SDP carries information about the number of L-PCM 3D Audio channels transmitted over the DP Main-Link. The 3DChannelCount field shall have the following values:

- 0000b to 1111b for 16-channel L-PCM 3D Audio
- 10000b to 11111b for 32-channel L-PCM 3D Audio

The audio stream payload data structure has seven configurations:

- 1- or 2-channel L-PCM Audio (see Section A.4.1)
- 3- to 8-channel L-PCM Audio (see Section A.4.2)
- 1- or 2-channel One Bit audio (see Section A.4.3)
- 3- to 8-channel One Bit audio (see Section A.4.4)
- 1- to 16-channel L-PCM 3D Audio (see Section A.4.5)
- 17- to 32-channel L-PCM 3D Audio (see Section A.4.6)
- DST audio (see Section A.4.7)

An Audio_Stream SDP may have a variable payload size. At the minimum, Audio_Stream SDP size is described in the following sub-sections.

A.4.1 1- or 2-channel L-PCM Audio

The 1- or 2-channel L-PCM Audio layout structure is composed of four header bytes protected by four ECC parity bytes, followed by 16 payload data bytes protected by four ECC parity bytes. The 16 payload data bytes consist of four 32-bit audio channel samples. Each of the 16 payload data bytes carries two audio samples, each consisting of first and second channel audio samples. For 1-channel L-PCM Audio, the second channel audio sample data shall be zero-padded.

Figure 2-32 in Section 2.2.5.2.5 illustrates the data mapping within the 4-byte payload of an Audio_Stream SDP that contains data with *IEC 60958*-encoding or *IEC 61937* transport.

A.4.2 3- to 8-channel Audio

The 3- to 8-channel L-PCM Audio layout structure is composed of four header bytes protected by four ECC parity bytes, followed by two sets of 16 payload data bytes, each protected by four ECC parity bytes (resulting in 32 data bytes plus eight ECC parity bytes). As is the case with 1- or 2-channel L-PCM Audio, each of the 16 payload data bytes consists of four 32-bit audio samples. When the channel count is fewer than eight, unused audio channel sample data shall be zero-padded.

Figure 2-32 in Section 2.2.5.2.5 illustrates the data mapping within the 4-byte payload of an Audio_Stream SDP that contains data with *IEC 60958*-encoding or *IEC 61937* transport.
The DPTX may use one common Audio_Stream SDP size for both 1- and 2-channel and 3- to 8-channel L-PCM Audio modes. In this case, the SDP payload configuration consisting of 32 data bytes plus eight ECC parity bytes (the payload configuration for 3- to 8-channel L-PCM Audio described in the previous paragraph) shall be used.

The DPTX may concatenate multiple sets of minimum SDP payload to form a long packet that has up to 256 data bytes for 1- or 2-channel L-PCM Audio and 1024 data bytes for 3- to 8-channel L-PCM Audio.

Regardless of the payload size, each packet shall be framed with SS and SE symbols and start with 4 header bytes protected by 4 ECC parity bytes, and then payload is present with sets of 16 bytes of data and 4 bytes of ECC parity.

Note: *All data channels within a single audio sample should be transferred in one packet. Dividing one sample into multiple Audio_Stream SDPs is* ***not*** *allowed.*

Within the 32-bit audio channel data, the least significant 24 bits carry audio sample data while the most significant eight bits carry control, status, and parity. The most significant bit (bit 7 of Byte 3), SP, indicates whether an audio sample is present. All channels of one audio sample, whether used or unused, shall have the same state for this flag.

For example, even when 1-channel L-PCM Audio is being transported and, therefore, all 24 bits of the second channel sample data are zero-padded, the SP bit of this second channel shall be set to 1 whenever the SP bit of the first channel is set to 1. The same situation applies to long packets (more than 32 bytes of data) when gaps between samples can be marked present by the SP bit being cleared to 0.

When 1- or 2-channel L-PCM Audio is transported, the 16 payload data bytes consist of two audio samples, as noted earlier. Of these two samples, the second sample may have the SP bits cleared to 0. For 3- to 8-channel L-PCM Audio transport, the SP bits shall always be set to 1.

Of the remaining seven control, status, and parity bits, of note is the PR field (bits 5:4 of Byte 3). The PR field is inserted only for the first and second channel data, regardless of the channel count. The PR field is omitted from the remainder of the channels.

A.4.3 1- to 2-channel One Bit Audio

Support for One Bit audio is new to *DP v1.4*.

The 1- to 2-channel One Bit audio layout structure is identical to the 1- to 2-channel L-PCM Audio layout described in Section A.4.1. The two formats differ, however, in their payload bit definition. As described in Section 2.2.5.2.5, LPCM audio contains LPCM audio data in Bytes 2 through 0, with Byte 3 (bits 7:0) = (SP, R (RESERVED), PR, P, C, U, and V, respectively). One Bit audio contains single-bit audio samples in Byte 3 (bits 3:0) and Bytes 2 through 0, with Byte 3 (bits 7:4) = (SP, V, C, and F, respectively).

Figure 2-33 in Section 2.2.5.2.5 illustrates the data mapping within the 4-byte payload of a One Bit Audio_Stream SDP, which follows the *CSA ISO/IEC 14496-3*, *Subpart 10*, encoding standard.

A.4.4 3- to 8-channel One Bit Audio

Support for One Bit audio is new to *DP v1.4*.

The 3- to 8-channel One Bit audio layout structure is identical to the 3- to 8-channel LPCM audio layout described in Section A.4.2. The two formats differ, however, in their payload bit definition. As described in Section 2.2.5.2.5, LPCM audio contains LPCM audio data in Bytes 2 through 0, with Byte 3 (bits 7:0) = (SP, R (RESERVED), PR, P, C, U, and V, respectively). One Bit audio contains single-bit audio samples in Byte 3 (bits 3:0) and Bytes 2 through 0, with Byte 3 (bits 7:4) = (SP, V, C, and F, respectively).

One Bit audio does **not** have a PR field insertion requirement. Instead, the Frame Start Flag (F) control bit (Byte 4) shall be set at the frame boundary for all eight channels.

Figure 2-33 in Section 2.2.5.2.5 illustrates the data mapping within the 4-byte payload of a One Bit Audio_Stream SDP, which follows the *CSA ISO/IEC 14496-3*, *Subpart 10*, encoding standard.

A.4.5 1- to 16-Channel L-PCM 3D Audio

Support for L-PCM 3D Audio is new to *DP v1.4*.

The 1- to 16-channel L-PCM 3D Audio layout structure is composed of four header bytes that are protected by four ECC parity bytes. These parity bytes are followed by four sets of 16 payload data bytes, each of which is protected by another four ECC parity bytes. The end result is 64 data bytes plus 16 ECC parity bytes. As is the case with 3- to 8-channel L-PCM Audio, each of the 16 payload data bytes consists of four 32-bit audio samples. When the channel count is fewer than 16, unused audio channel sample data shall be zero-padded.

The DPTX may concatenate multiple sets of minimum SDP payloads to form a long packet that has up to 2048 data bytes for 1- to 16-channel L-PCM 3D Audio.

Regardless of the payload size, each packet shall be framed with SS and SE symbols and start with four header bytes protected by four ECC parity bytes, and then payload is present with sets of 16 data bytes and four ECC parity bytes.

Note: *All data channels within a single audio sample should be transferred within one packet. Dividing one sample into multiple Audio_Stream SDPs is* ***not*** *allowed.*

Figure 2-32 in Section 2.2.5.2.5 illustrates the data mapping within the 4-byte payload of an Audio_Stream SDP that contains data with *IEC 60958*-encoding or *IEC 61937* transport. Within the 32-bit audio channel data, the least significant 24 bits carry audio sample data, while the most significant eight bits carry control, status, and parity. The most significant bit (bit 7 of Byte 3), SP, indicates whether an audio sample is present. All channels of one audio sample, whether used or unused, shall have the same state for this flag.

Of the remaining seven control, status, and parity bits, of note is the PR field (bits 5:4 of Byte 3). The PR field is inserted for only the first and second channel data, regardless of the channel count. The PR field is omitted from the remainder of the channels.

A.4.6 17- to 32-Channel L-PCM 3D Audio

Support for L-PCM 3D Audio is new to *DP v1.4*.

The 17- to 32-channel L-PCM 3D Audio layout structure is composed of four header bytes that are protected by four ECC parity bytes. These parity bytes are followed by eight sets of 16 payload data bytes, each of which is protected by another four ECC parity bytes. The end result is 128 data bytes plus 32 ECC parity bytes.

Figure 2-32 in Section 2.2.5.2.5 illustrates the data mapping within the 4-byte payload of an Audio_Stream SDP that contains data with *IEC 60958*-encoding or *IEC 61937* transport. As is the case with 3- to 8-channel L-PCM Audio, each of the 16 payload data bytes consist of four 32-bit audio samples. When the channel count is fewer than 32, unused audio channel sample data shall be zero-padded.

The DPTX may concatenate multiple sets of minimum SDP payloads to form a long packet that has up to 4096 data bytes for 17- to 32-channel audio.

Regardless of the payload size, each packet shall be framed with SS and SE symbols and start with four header bytes protected by four ECC parity bytes, and then payload is present with sets of 16 data bytes and four ECC parity bytes.

Note: *All data channels within a single audio sample should be transferred within one packet. Dividing one sample into multiple Audio_Stream SDPs is* ***not*** *allowed.*

Within the 32-bit audio channel data, the least significant 24 bits carry audio sample data, while the most significant eight bits carry control, status, and parity. The most significant bit (bit 7 of Byte 3), SP, indicates whether an audio sample is present. All channels of one audio sample, whether used or unused, shall have the same state for this flag.

Of the remaining seven control, status, and parity bits, of note is the PR field (bits 5:4 of Byte 3). The PR field is inserted for only the first and second channel data, regardless of the channel count. The PR field is omitted from the remainder of the channels.

A.4.7 DST Audio

Support for DST audio is new to *DP v1.4*.

The DST audio layout structure is identical to the 8-channel L-PCM Audio layout described in Section A.4.2. The two formats differ, however, in their payload bit definition. As described in Section 2.2.5.2.5, L-PCM Audio contains L-PCM Audio data in Bytes 2 through 0, with Byte 3 (bits 7:0) = (SP, R (RESERVED), PR, P, C, U, and V, respectively). DST audio contains single-bit audio samples in Byte 3 (bits 3:0) and Bytes 2 through 0, with Byte 3 (bits 7:4) = (SP, V, C, and F, respectively).

Figure 2-34 in Section 2.2.5.2.5 illustrates the data mapping within each of the eight 4-byte sub-layout payloads of a DST Audio_Stream SDP, which follows the *CSA ISO/IEC 14496-3*, *Subpart 10*, encoding standard.

The single bit sample data is continuous across all eight sub-layouts, for a total of 224 bits/DST layout. The SP bit shall be set to 1 for all eight sub-layouts. Unlike multi-channel L-PCM Audio or L-PCM 3D Audio, channel allocation is **not** applicable for the DST layout, and therefore, there are no inactive sub-layouts in the DST layout.

DST audio does **not** have a PR field insertion mandate. Instead, the Frame Start Flag (F) control bit (Byte 3) shall be set at the frame boundary for all eight sub-layouts.

A.5 Channel-to-Speaker Mapping

Channel position in the DP stream with more than two channels should exactly correspond to *CTA-861-G*. This means that gaps between channels can be present. Table A-1 shows channel-placing for one of the possible channel mappings described in *CTA-861-G*.

Table A-1 describes transmission of 3-channel L-PCM Audio with CA programmed to 04h in Byte 3 of the Audio INFOFRAME SDP.

Table A-1: Channel-to-Speaker Mapping of 3-channel L-PCM Audio with Audio INFOFRAME SDP CA = 04h

4-lane Main-Link			
Lane 0	**Lane 1**	**Lane 2**	**Lane 3**
SS	SS	SS	SS
HB0	HB1	HB2	HB3
PB0	PB1	PB2	PB3
S0_Ch1_B0	S0_Ch2_B0	00h	00h
S0_Ch1_B1	S0_Ch2_B1	00h	00h
S0_Ch1_B2	S0_Ch2_B2	00h	00h
S0_Ch1_B3	S0_Ch2_B3	80h	80h
PB4	PB5	PB6	PB7
S0_Ch5_B0	00h	00h	00h
S0_Ch5_B1	00h	00h	00h
S0_Ch5_B2	00h	00h	00h
S0_Ch5_B3	80h	80h	80h
PB8	PB9	PB10	PB11
SE	SE	SE	SE

Note: *The msb (bit 7 of Byte 3) of the 32-bit audio sample data, the SP bit, indicates whether an audio sample is present.*

The channel-to-speaker mapping information is provided in an Audio INFOFRAME SDP, as described in *CTA-861-G*, *Table 35*. When 1-channel L-PCM Audio is transported, it shall use the FL channel (Channel 1).

The channel-to-speaker mapping information for L-PCM 3D Audio is provided as a speaker mask or channel index setting in Audio INFOFRAME SDP Data Bytes 6 through 9, and as a channel ordering instruction (as described in *CTA-861-G*, *Section 6.6.3* and *Section 6.6.4*, respectively).

A.6 Transfer of Sample Frequency Information

Information about audio sampling frequency is transferred in an Audio_TimeStamp SDP, which provides the audio clock frequency information (Maud and Naud), using the following formula:

$$Maud / Naud = 512 \times Fs / f\_LS\_Clk$$

where:

- *Fs* is the sampling frequency of the audio stream being transported

In accordance with the DP Standard, this information is transferred at least once per video frame (or following 512th BS symbol when the main video stream is not present). A DPTX is allowed to transmit it more frequently if it chooses to do so. In addition, the Standard allows for the transmission of the least significant eight bits of the Maud value (Maud[7:0]) once per line of main video stream line and it is up to the DPRX whether to use this information.

How a DPRX regenerates the audio sampling frequency is implementation-specific and is beyond the scope of this Standard.

For example, some implementations may use the Maud and Naud values to set the initial frequency of the audio clock recovery circuit and perform the fine frequency adjustment based on the audio FIFO fill rate. With this method, a DPRX may ignore Maud[7:0] data from the VB-ID packet.

B Sink Event Notification Example (Informative)

This appendix describes a mechanism through which the SST-only mode DP Sink device can notify the DP Source device of a Sink event such as a display orientation switch between portrait and landscape. An MST Sink device connected to an MST upstream device shall notify a Sink event, by way of a SINK_EVENT_NOTIFY broadcast message transaction.

B.1 Mutual Identification by Source and Sink Devices

Upon a Hot-Plug Event, the Source and Sink devices may identify one another by accessing the Source Device-specific field (DPCD Addresses 00300h through 003FFh; see Table 2-186) and Sink Device-specific field (DPCD Addresses 00400h through 004FFh; see Table 2-187). A Source device that needs to enable its "Extension" feature should write its own 24-bit IEEE_OUI (Organizational Unique ID) to DPCD Addresses 00300h through 00302h, and read the 24-bit IEEE_OUI of the Sink device from DPCD Addresses 00400h through 00402h. The Source device may write and read more than three bytes of IEEE OUI to exchange further identification information (e.g., Chip ID and Revision ID). The "Extension" feature is enabled only when each device recognizes that the other device supports the feature.

B.2 IRQ_HPD Pulse and Sink Device-specific IRQ

A Sink device that supports the Sink Device Event Notification feature indicates what Sink device event types are supporting by setting "Sink_Event_Type" byte(s) in the Sink Device-specific field (DPCD Addresses 00400h through 004FFh; see Table 2-187). The Source device, upon reading the Sink_Event_Type byte(s), by way of the AUX_CH, enables certain Sink device events by writing to the "Sink_Event_Mask" byte(s) in the Sink Device-specific field. Sink_Event_Type and Sink_Event_Mask byte address mapping is implementation-specific.

When the selected Sink device event (e.g., the display orientation switch) occurs, the device takes the following actions:

- Programs a set of parameters to a pre-defined address range of the Sink Device-specific field
- Sets the SINK_SPECIFIC_IRQ bit in the SINK_COUNT register (DPCD Address 00201h, bit 6)
- Generates an IRQ_HPD pulse on the HPD signal line

The Source device, upon detecting the IRQ_HPD pulse, takes the following actions:

- Reads the Link/Sink Device Status field (DPCD Addresses 00200h through 002FFh; see Table 2-185) and identifies that the cause of the IRQ is Sink device-specific
- Reads a set of parameters from the pre-defined address range of the Sink Device-specific field
- Performs an operation according to the read parameters:
  - If the notified Sink device event is a display orientation change, it may change the orientation of video data it is transmitting

C Link Quality Management (Informative)

This appendix provides guidelines for ensuring link quality, with the goal of providing minimal disruption during normal operation.

C.1 Marginal Link Quality

The link training procedure does not necessarily take sufficient time to be able to perform a full link quality analysis. The consequence is that a connection between a DPTX and DPRX may be fully trained, but operating with marginal performance. This is more likely to occur with long cables, the use of non-retiming repeaters (implementation of which is beyond the scope of this Standard), and systems and cables that for whatever reason are out of specification.

The symptoms are one or more of the following:

- No video (despite successful link training)
- Flickering/flashing video
- Display artifacts, including “sparkling” video (individual pixel errors) and line tears
- Other video distortions

C.2 Analysis

Analysis of configurations demonstrating these symptoms have shown:

- Both low bit error rates (< 10 bit errors per lane per second) and high bit error rates (thousands of bit error rates per second)
- Loss of LANE*x*_SYMBOL_LOCKED after successful training
- Loss of INTERLANE_ALIGN_DONE after training[a]
- Inconsistent training results on multiple re-plugs

Inconsistent training results can result in available bandwidth changing from one training cycle to the next. In particular, it has been observed that the available bandwidth can change over a “sleep-wake” cycle.

a. *INTERLANE_ALIGN_DONE bits in the LANE_ALIGN_STATUS_UPDATED and LANE_ALIGN_STATUS_UPDATED_ESI registers (DPCD Addresses 00204h and 0200Eh, respectively, bit 0).*

C.3 Tolerance to Bit Errors

The following guidelines should be followed for tolerance to bit errors:

- An isolated bit error should typically result in nothing worse than single pixel sparkles
- On an isolated bit error during active video, the receiver should **not** reset the screen
- Receivers should implement robustness that is supported by control packet redundancy
- Isolated bit errors should **not** result in any of the following:
  - Loss of LANE*x*_SYMBOL_LOCKED
  - Clearing of the LANE*x*_*y*_STATUS register(s) (DPCD Addresses 00202h and 00203h) and LANE*x*_*y*_STATUS_ESI register(s) (DPCD Addresses 0200Ch and 0200Dh)
  - Clearing of the LANE_ALIGN_STATUS_UPDATED and LANE_ALIGN_STATUS_UPDATED_ESI registers (DPCD Addresses 00204h and 0200Eh, respectively)
  - Link retraining request
- Transmitters are **not** expected to monitor bit error counters

C.4 Link Retraining

On loss of LANE*x*_CR_DONE, LANE*x*_SYMBOL_LOCKED, and/or INTERLANE_ALIGN_DONE, the receiver should request link retraining, as follows:

1 Clearing the INTERLANE_ALIGN_DONE bits in the LANE_ALIGN_STATUS_UPDATED and LANE_ALIGN_STATUS_UPDATED_ESI registers (DPCD Addresses 00204h and 0200Eh, respectively, bit 0).

2 Setting the LINK_STATUS_UPDATED bits in the LANE_ALIGN_STATUS_UPDATED and LANE_ALIGN_STATUS_UPDATED_ESI registers (DPCD Addresses 00204h and 0200Eh, respectively, bit 7).

3 Generating a distinct IRQ_HPD.

The receiver should avoid using the current voltage swing/pre-emphasis level/bit-rate/RX EQ setting combination in subsequent link training.

C.5 Long-term Link Quality Monitoring (Guidelines)

The receiver should monitor the bit error rate for each lane, but without clearing the Bit Error-related DPCDs.

If the bit error rate exceeds an implementation-specific threshold (e.g., 32 errors within a 10-sec window), the receiver should:

- Internally mark the current voltage swing/pre-emphasis level/bit rate/RX EQ setting as “unsupportable”
- Request link retraining
- Avoid all unsupportable settings during training

The receiver should reset the “unsupportable” flags on a new connection.

A Sink device may decide to fall back to RBR. To do this, the Sink device should do the following:

1 Change its capability in 8b/10b_MAX_LINK_RATE and/or MAX_LANE_COUNT registers (DPCD Addresses 00001h and 00002h, respectively).

2 Setting the RX_CAP_CHANGED bit in the LINK_SERVICE_IRQ_VECTOR_ESI0 register (DPCD Address 02005h, bit 0).

3 Issue an IRQ_HPD.

A Source device may decide to fall back to RBR. To do this, the Source device should do the following:

1 Allow for an initial period (e.g., 30sec) during which the Sink device is using “long-term” link quality monitoring to find suitable settings.

2 On receiving a high rate of retraining requests (approximately two requests within 30sec or higher) following training at HBR, a Source device should avoid retraining at HBR, and should instead try training at RBR as if the RX capability is RBR.

A Source device shall never attempt to transmit a video mode that exceeds the actual trained bandwidth, and therefore shall be tolerant to the result of retraining being at a lower bandwidth than the prior training.

D HBR2 Electrical Specifications (Informative)

D.1 AUX Parameters

The AUX_CH EYE mask at the transmitting IC package pins and minimum voltage values (informative) are illustrated in Figure D-1 and listed in Table D-1, respectively. The normative specification for the AUX_CH voltage swing at the transmitting device connector pins (DFP connector pins for AUX request transaction, and UFP connector pins for AUX reply transaction) is 290mV_diff_pp (minimum). At the transmitting IC package pins, the AUX_CH voltage swing shall be higher than 290mV_diff_pp to account for the voltage drop over the PCB traces.

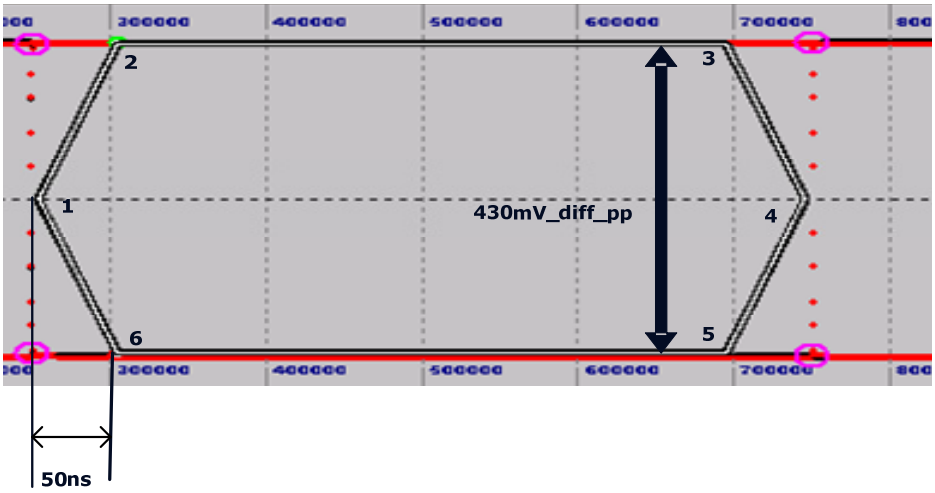


Figure D-1: AUX_CH EYE Mask at Transmitting IC Package Pins (Informative)

Table D-1: AUX_CH EYE Mask Minimum Voltage at Transmitting IC Package Pins (Informative)

Point	Time (UI)	Minimum Voltage Value at Six Vertices (mV)
1	0.01	0
2	0.11	Higher than 145
3	0.89	Higher than 145
4	0.99	0
5	0.89	Lower than -145
6	0.11	Lower than -145

The AUX_CH EYE mask at the receiving IC package pins and minimum voltage values (informative) are illustrated in Figure D-2 and listed in Table D-2, respectively. The normative specification for the AUX_CH voltage swing at the transmitting device connector pins (UFP connector pins for AUX request transaction, and DFP connector pins for AUX reply transaction) is 270mV_diff_pp. At the receiving IC package pins, the AUX_CH voltage swing is bound to be lower than 270mV_diff_pp minimum due to the voltage drop over the PCB traces.

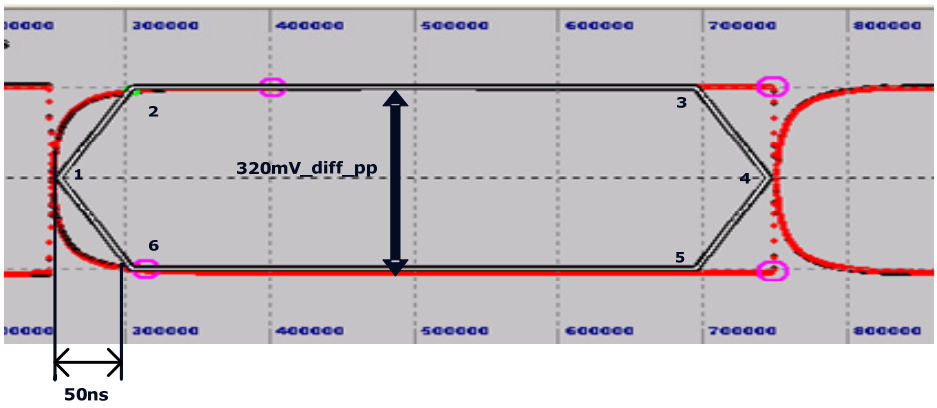


Figure D-2: AUX_CH EYE Mask at Receiving IC Package Pins (Informative)

Table D-2: AUX_CH EYE Mask Minimum Voltage at Receiving IC Package Pins (Informative)

Point	Time (UI)	Minimum Voltage Value at Six Vertices (mV)
1	0.01	0
2	0.11	Lower than 135
3	0.89	Lower than 135
4	0.99	0
5	0.89	Higher than -135
6	0.11	Higher than -135

D.2 Main-Link Parameters

This section describes the informative Main-Link PHY Layer electrical parameters, up to the 5.4Gbps/lane link rate (HBR2).

Table D-3 and Table D-4 specify informative Transmitter parameters at the silicon pads and TX pins, respectively, that are intended to serve as a reference for Transmitter design. These informative parameter values serve as a reference from which Source TP2 parameters are defined. A Source that passes compliance does not have to meet these parameter values. A Transmitter design that meets these informative parameter values may still fail compliance due to the Source device's system design. Both the Transmitter and the Source device's system should be carefully designed to ensure Source-device compliance.

Table D-3: DP Main-Link TX Silicon Parameters (Informative)

Symbol	Parameter	Min	Nom	Max	Units	Comments
V_{BIAS_TX}	TX DC Bias Voltage	0		2.0	V	
$V_{TX\text{-}AC\text{-}CM\_HBR\_RBR}$	TX AC Common Mode Voltage			20	mVrms	Measured using an 8b/10b valid pattern with 50% transition density. Measured at supported frequencies within the frequency tolerance range. Time-domain measurement.
$V_{TX\text{-}AC\text{-}CM\_HBR2}$	TX AC Common Mode Voltage			30	mVrms	
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level0}$	Differential Peak-to-peak Output Voltage Swing Level 0	0.34	0.4	0.46	V	See Figure 3-2 for definition of differential voltage. May support Voltage Swing Level 3 for RBR and HBR. For embedded connection, may support programmable voltage swing levels. Voltage Swing Level 3 shall be greater than Voltage Swing Level 2.
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level1}$	Differential Peak-to-peak Output Voltage Swing Level 1	0.51	0.6	0.68	V	
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level2}$	Differential Peak-to-peak Output Voltage Swing Level 2	0.69	0.8	0.92	V	
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level3\_RBR\_HBR}$	Differential Peak-to-peak Output Voltage Swing Level 3	0.85	1.2	1.38	V	
$V_{TX\text{-}PREEMP\text{-}RATIO}$	Pre-emphasis Level 0	0.0	0.0	0.0	dB	Shall support Pre-emphasis Levels 0, 1, and 2. May support Pre-emphasis Level 3. For an embedded connection, support of programmable pre-emphasis levels is optional.
	Pre-emphasis Level 1	2.8	3.5	4.2	dB	
	Pre-emphasis Level 2	4.8	6.0	7.2	dB	
	Pre-emphasis Level 3	7.5	9.5	11.4	dB	
$F_{TX\text{-}REJECTION\text{-}BW}$	Clock Jitter Rejection Bandwidth			4	MHz	Transmitter jitter shall be measured at source connector pins using a signal analyzer that has a second-order PLL with closed-loop tracking bandwidth of 20MHz (for D10.2 pattern) and damping factor of 1.428.
$C_{TX\text{-}OUTPUT}$	TX Output Capacitance for Return Loss			1.5	pF	For HBR2. Represents only the effective lump capacitance seen at the package/die interface that shunts the on-die TX termination.

Table D-4: DP Main-Link TX TP1 Package Pin Parameters (Informative)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$T_{TX-EYE\_CHIP\_HBR2}$	Minimum TX EYE Width at TX package pins	0.73			UI	For HBR2 using a D10.2 pattern.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER\_CHIP\_HBR2}$	Maximum time between the jitter median and maximum deviation from the median at TX package pins			0.135	UI	
$T_{TX-EYE\_CHIP\_HBR}$	Minimum TX EYE Width at TX package pins	0.72			UI	For HBR.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER\_CHIP\_HBR}$	Maximum time between the jitter median and maximum deviation from the median at TX package pins			0.147	UI	
$T_{TX-EYE\_CHIP\_RBR}$	Minimum TX EYE Width at TX package pins	0.82			UI	For RBR.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER\ CHIP\_RBR}$	Maximum time between the jitter median and maximum deviation from the median at TX package pins			0.09	UI	
$T_{TX-RISE\_CHIP}$, $T_{TX-FALL\_CHIP}$	D+/D- TX Output Rise/Fall Time at TX package pins	50		130	ps	At 20 to 80%.
$V_{TX-DC-CM}$	TX DC Common Mode Voltage	0		2.0	V	Common mode voltage is equal to V_{BIAS_TX} voltage.
$I_{TX-SHORT}$	TX Short Circuit Current Limit			50	mA	Total drive current of the transmitter when it is shorted to its ground.
$RL_{TX-DIFF}$	Differential Return Loss at 0.675GHz at TX package pins	12			dB	Straight loss line between 0.675 and 1.35GHz.
	Differential Return Loss at 1.35GHz at TX package pins	9			dB	
$L_{TX-SKEW-INTRA\_PAIR\ CHIP}$	Lane Intra-pair Output Skew at TX package pins			20	ps	Applies to all supported lanes.
$T_{TX-RISE\_FALL\_MISMATCH\_CHIPDIFF}$	Lane Intra-pair Rise-fall Time Mismatch at TX package pins.			5	%	D+ rise to D- fall mismatch and D+ fall to D- rise mismatch.

Table D-5 through Table D-7 specify Receiver parameters at the RX pins and silicon pads that are intended to serve as a reference for Receiver design. These informative parameter values serve as a reference from which Sink TP3 parameters are defined. A Sink device that passes compliance does not have to meet these informative parameter values. A Receiver design that meets these informative parameter values may still fail compliance due to the Sink device's system design. Both the Receiver and the Sink device system should be carefully designed to ensure Sink-device compliance.

Table D-5: DP Main-Link RX TP4 Package Pin Parameters (Informative)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{RX-DIFFp-p}$	Differential Peak-to-peak Input Voltage at RX package pins	120			mV	For HBR. See Figure 3-2 for definition of differential voltage.
$V_{RX-DIFFp-p}$	Differential Peak-to-peak Input Voltage at RX package pins	40			mV	For RBR. See Figure 3-2 for definition of differential voltage.
T_{RX-EYE_CHIP}	Minimum Receiver EYE Width at RX package pins	0.47			UI	For HBR. $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specifies the total allowable DJ.
$T_{RX-EYE-MEDIAN-to-MAX-ITTER\_CHIP}$	Maximum time between the jitter median and maximum deviation from the median at RX package pins			0.265	UI	
T_{RX-EYE_CHIP}	Minimum Receiver EYE Width at RX package pins	0.22			UI	For RBR. $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specifies the total allowable DJ.
$T_{RX-EYE-MEDIAN-to-MAX-ITTER\_CHIP}$	Maximum time between the jitter median and maximum deviation from the median at RX package pins			0.39	UI	
$V_{RX-DC-CM}$	RX DC Common Mode Voltage	0		2.0	V	Common mode voltage is equal to V_{BIAS_RX} voltage.
$I_{RX-SHORT}$	RX Short Circuit Current Limit			50	mA	Total drive current of the transmitter when it is shorted to its ground.
$RL_{RX-DIFF}$	Differential Return Loss at 0.675GHz at RX package pins	12			dB	Straight loss line between 0.675 and 1.35GHz.
	Differential Return Loss at 1.35GHz at RX package pins	9			dB	
$C_{RX-INPUT}$	RX Input Capacitance for Return Loss			1.1	pF	For HBR2.

Table D-6: DP Main-Link RX Silicon Pads with HBR2 (Informative)

Symbol	Parameter	Min	Nom	Max	Units	Comments
V_{BIAS_RX}	RX DC Bias Voltage	0		2.0	V	
$T_{RX\text{-}TJ\_8b10b\_HBR2}$	Minimum Receiver EYE Width	0.30			UI	For HBR2. Measured at $1E^{-9}$ BER using the HBR2 Compliance EYE pattern.
$T_{RX\text{-}DIFFp\text{-}p\_HBR2}$	RX Differential Peak-to-Peak EYE Voltage	50			mV	For HBR2. Measured at $1E^{-9}$ BER using the HBR2 Compliance EYE pattern.

Table D-7: DP Main-Link RX Silicon Pads with HBR/RBR (Informative)

Symbol	Parameter	Min	Nom	Max	Units	Comments
V_{BIAS_RX}	RX DC Bias Voltage	0		2.0	V	

D.3 Dual-Dirac Jitter Model[a]

It should be understood that although jitter can be described using a Dual-Dirac model; however, it should **not** be understood that the jitter in the system is really Dual-Dirac. Typically, jitter shall be distributed or structured, and the Dual-Dirac description is merely the linearization of the CDF at a particular BER. It should also be understood that use of the Dual-Dirac model here and in system budgeting is only as a language to help define the jitter in the system, and does **not** imply that this should be the normative derivation methodology for the derivation of the jitter in the system.

Three tools are needed to describe the Dual-Dirac model:

- The Dirac-delta function:

$$\delta(x - x_0) \equiv \begin{cases} 0, & x \neq x_0 \\ \to \infty, & x = x_0 \end{cases} \quad \text{with} \quad \int \delta(x - x_0)dx = 1$$

- The RJ PDF is a Gaussian:

$$PDF_{RJ}(x) = \frac{1}{\sqrt{2\pi}\sigma}\exp\left[-\frac{x^2}{2\sigma^2}\right]$$

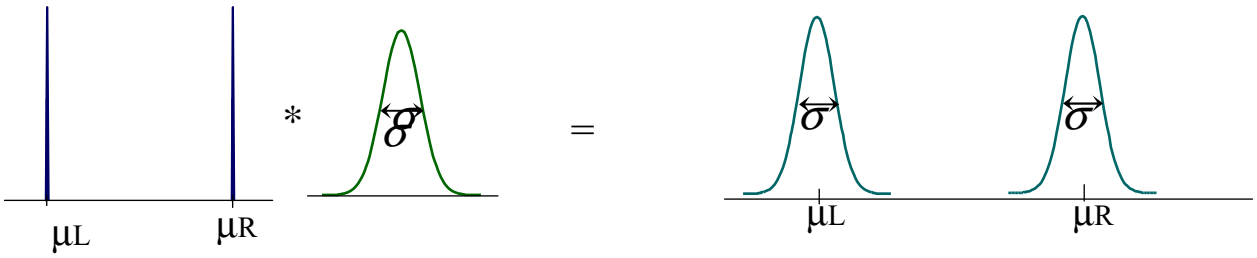
- The different jitter components combine through convolution:

$$\begin{aligned} \mathrm{PDF}(x) &= \mathrm{PDF}_{DJ}(x) * \mathrm{PDF}_{RJ}(x) \\ &= \int \mathrm{PDF}_{DJ}(u) * \mathrm{PDF}_{RJ}(x-u)du \end{aligned}$$

a. Referenced and reused with permission from Ransom Stephens, from "What The Dual-Dirac Model is and What it is Not."

The Dual-Dirac is composed from the following elements:

$$[\delta(x-\mu_L)+\delta(x-\mu_R)] * \frac{1}{\sqrt{2\pi}\sigma}\exp\left(-\frac{x^2}{2\sigma^2}\right) = \frac{1}{\sqrt{2\pi}\sigma}\left[\exp\left(-\frac{(x-\mu_L)^2}{2\sigma^2}\right)+\exp\left(-\frac{(x-\mu_R)^2}{2\sigma^2}\right)\right]$$



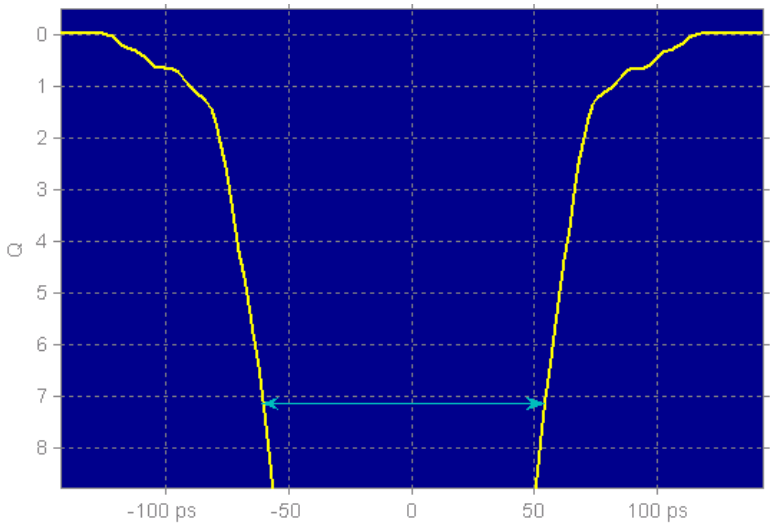
Dual-Dirac DJ

$DJ(p\text{-}p) = \mu R - \mu L$

Gaussian RJ

$RJ = \sigma$

The derivation of TJ(BER) in Dual-Dirac: Generally we can define the bathtub plot.



$$\mathrm{BER}(x) = \rho_T \int_x^{\infty} \mathrm{PDF}(x')dx' + \rho_T \int_{-\infty}^{x} \mathrm{PDF}(x'-T)dx'$$

Plug in Dual-Dirac:

$$\mathrm{BER}_{\delta\delta}(x) = \rho_T \left[\mathrm{erfc}\left(\frac{x - \mu_L}{\sqrt{2}\sigma} \right) + \mathrm{erfc}\left(\frac{(x - T) - \mu_R}{\sqrt{2}\sigma} \right) \right]$$

Evaluate the complementary error functions, erfc(x), and get:

$$TJ(BER) = 2Q_{BER} \times RJ(\delta\delta) + DJ(\delta\delta)$$

For 50% density patterns such as PRBS7 and the HBR2 compliance pattern at BER = 10^{-9}, $Q_{BER} = 5.884$.

The jitter model under these conditions would be:

$$11.77RJ + DJ = TJ$$

E HBR*x*/RBR Scrambler C Code Reference (Informative)

The following sample C code provides an informative reference to the scrambler definition used by HBR3, HBR2, HBR, and RBR. Similar coding is used for the UHBR*x* bit rates.

Note: *In the C code that follows, the following terms within the code are those whose names have since been modified in later versions of this Standard:*

- *"control symbol" represents "control link symbol"*
- *Multi-stream format" represents "MST mode"*
- *"DP receiver" represents "DPRX"*
- *"DP transmitter" represents "DPTX"*

```
/*
 *  lfsr.h
 *  Scrambler
 *
 */

void resetLfsr();

void advanceLfsr();

extern unsigned short lfsr;
extern unsigned short lfsrSeed;

/*
 *  lfsr.c
 *  Scrambler
 *
 */

#include "DPScramble.h"
#include "lfsr.h"

/*
 this routine implements the serial scrambling/descrambling algorithm in parallel form
 for the internal LFSR polynomial: X^16+x^5+x^4+x^3+1
 this advances the LFSR 8 bits every time it is called
 this requires fewer than 25 xor gates to implement (with a static register)

 The XOR required to advance 8 bits/clock is
 bit   0   1   2   3   4   5   6   7   8   9  10  11  12  13  14  15

       8   9  10  11  12  13  14  15   0   1   2   3   4   5   6   7
                   8   9  10  11  12  13  14  15
                       8   9  10  11  12  13  14  15
                           8   9  10  11  12  13  14  15
*/
```

```
unsigned short lfsr;
unsigned short lfsrSeed;

void resetLfsr() {
  lfsr = lfsrSeed;
}

void advanceLfsr() {

  int i;
  int bit[16];
  int bitOut[16];
  for (i=0; i<16; i++)                 // convert LFSR to bit array for legibility
    bit[i] = (lfsr >> i) & 1;

  //  Advance the LFSR 8 serial clocks
  bitOut[ 0] = bit[ 8];
  bitOut[ 1] = bit[ 9];
  bitOut[ 2] = bit[10];
  bitOut[ 3] = bit[11] ^ bit[ 8];
  bitOut[ 4] = bit[12] ^ bit[ 9] ^ bit[ 8];
  bitOut[ 5] = bit[13] ^ bit[10] ^ bit[ 9] ^ bit[ 8];
  bitOut[ 6] = bit[14] ^ bit[11] ^ bit[10] ^ bit[ 9];
  bitOut[ 7] = bit[15] ^ bit[12] ^ bit[11] ^ bit[10];
  bitOut[ 8] = bit[ 0] ^ bit[13] ^ bit[12] ^ bit[11];
  bitOut[ 9] = bit[ 1] ^ bit[14] ^ bit[13] ^ bit[12];
  bitOut[10] = bit[ 2] ^ bit[15] ^ bit[14] ^ bit[13];
  bitOut[11] = bit[ 3]           ^ bit[15] ^ bit[14];
  bitOut[12] = bit[ 4]                     ^ bit[15];
  bitOut[13] = bit[ 5];
  bitOut[14] = bit[ 6];
  bitOut[15] = bit[ 7];

  lfsr = 0;
  for (i=0; i<16; i++)              // convert the LFSR back to an integer
    lfsr += (bitOut[i] << i);
}

/*
 *
 *  DisplayPort Scrambler
 *
 *  Includes scrambling of DP control symbols, and conversion between
 *  DP control symbols and K codes
 *
 */

extern bool TrainingSequence;      // TRUE if in training sequence
extern bool Multistream;           // TRUE if using Multi-stream format
extern bool DP_TX;                 // TRUE at DP transmitter, FALSE at DP receiver
extern bool EnhancedFraming;       // TRUE for SST-mode connection using Enhanced Framing
extern int srSeq[4];

//      K-code            Single-stream Multi-stream
#define K28d0   0x11c //  SR            GP1 index 2
#define K28d1   0x13c //  CP            GP2 rsvd
#define K28d2   0x15c //  SS            GP1 index 3
#define K28d3   0x17c //  BF            GP1 index 4
#define K28d4   0x19c //  rsvd          GP2 rsvd
#define K28d5   0x1bc //  BS            GP2 SR
```

```
#define K28d6   0x1dc //  rsvd          GP1 index 5
#define K28d7   0x1fc //  rsvd          GP2 rsvd
#define K23d7   0x1f7 //  FE            GP1 index 0
#define K27d7   0x1fb //  BE            GP1 index 1
#define K29d7   0x1fd //  SE            GP1 index 6
#define K30d7   0x1fe //  FS            GP1 index 7

// Control symbols for single stream operation

enum {SR=K28d0, CP=K28d1, SS=K28d2,
      BF=K28d3, BS=K28d5, FE=K23d7, BE=K27d7, SE=K29d7, FS=K30d7 };

// Control symbols for multi stream operation

enum {MS_SR=K28d5};

extern const int scrControlToKcode[8];

void resetSRSeq();

enum MS_SR_States {MS_SR_Reset, MS_SR_Lock1, MS_SR_Lock2, MS_SR_Locked, MS_SR_Error1, MS_SR_Error2};

int scrambleByte(int inByte);

/*
 *
 *  DisplayPort Scrambler
 *
 */

#include "DPScramble.h"
#include "lfsr.h"

/*
  this routine implements the scrambling/descrambling algorithm in parallel form
  The data is scrambled with the top byte of the lfsr. Note that the effect of scrambling
  in parallel form is to bit reverse the top byte of the lfsr
  data bit      7   6   5   4   3   2   1   0
  lfsr bit      8   9  10  11  12  13  14  15

 this routine is called on the TX side to scramble the outgoing symbol
 and on the RX side to descramble the incoming symbol

 the parameter inByte is either
   a data value in the range 0 - 255
   a representation of a K-code, represented as 0x100+val
   a representation of a DP Control Symbol, represented by 0x200+index
     (applies only on the transmit/scrambling side)
   a representation of an errored symbol, represented by 0x400

 the return value is encoded similarly
   a data value in the range 0 - 255
   a representation of a K-code, represented as 0x100+val
   a representation of a DP Control Symbol, represented by 0x200+index
     (applies only on the receive/descrambling side)

 for robustness scrambler reset purposes, this function maintains the state variable
 inEnhSRSeq between calls

*/
```

```
// the following defines the conversion between scrambled symbol index to K code
//                                      0      1      2      3      4      5      6      7
const int scrControlToKcode[8] = { K23d7, K27d7, K28d0, K28d2, K28d3, K28d6, K29d7, K30d7 };

int srSeq[4];
bool inEnhSRSeq; // TRUE if have recognized the start of an Enhanced Framing scrambler reset sequence

enum MS_SR_States MS_SR_State = MS_SR_Reset;
unsigned short int MS_SR_symbol_count = 0;  // 16 bit, wraps to zero after counting to 65535

void resetSRSeq() {
  int i;
  for (i=0; i<4; i++)
    srSeq[i] = 0;
}


int scrambleByte(int inByte)
{

  int scrambit[16];
  int bit[16];
  int i, outbyte;
  int temp; // for debugging

  if (inByte < 0)  // called after the end of stream has been met
    return -1;
  // on descramble at the receiver in multistream mode, convert Kcodes in group 1 to
  // control symbol indices

  if (Multistream && !DP_TX)
  {
    for (i=0; i<8; i++)
      if (inByte==scrControlToKcode[i])
      {
        inByte=i+0x200;
        break;
      }
  }

  for (i=0; i<16; i++) {                // convert LFSR to bit array for legibility
    bit[i] = (lfsr >> i) & 1;
  }

  for (i=0; i<11; i++)                  // convert byte to be (un-)scrambled for legibility
    scrambit[i] = (inByte >> i) & 1;    // preserve Kcode and control symbol distinctive bits

  if ((!((inByte & 0x100) == 0x100)) && // if not a Kcode,
      (!((inByte & 0x400) == 0x400)) && // and not an errored symbol
      (!(TrainingSequence == TRUE)))    // and not in the middle of a training sequence
  {                                  // scramble or unscramble the data
    scrambit[0] ^= bit[15];         // data and multistream control symbol bit 0
    scrambit[1] ^= bit[14];             // data and multistream control symbol bit 1
    scrambit[2] ^= bit[13];             // data and multistream control symbol bit 2
    scrambit[3] ^= bit[12];             // data bit 3
    scrambit[4] ^= bit[11];             // data bit 4
    scrambit[5] ^= bit[10];             // data bit 5
    scrambit[6] ^= bit[9];              // data bit 6
    scrambit[7] ^= bit[8];              // data bit 7
```

```
 }

 advanceLfsr();

 // reset scrambler at scrambler reset time

if (Multistream)
 { // Multistream as defined in DP Standard
   MS_SR_symbol_count++;
   if (inByte == MS_SR)
   {
     // robustness scrambler reset mechanism here, based on SR reception
     // at the correct interval (every 65536 symbols) - see DP MST section
     switch (MS_SR_State)
     {
       case MS_SR_Reset:
         resetLfsr();
         MS_SR_symbol_count = 0;  // reset counter on entry to Lock1
         MS_SR_State = MS_SR_Lock1;
         break;
       case MS_SR_Lock1:
         if (MS_SR_symbol_count == 0)
         {
           resetLfsr();
           MS_SR_State = MS_SR_Lock2;
         }               // else stay in this state
         MS_SR_symbol_count = 0; // reset counter on re-entry to state
         break;
       case MS_SR_Lock2:
         if (MS_SR_symbol_count == 0)
         {
           resetLfsr();
           MS_SR_State = MS_SR_Locked;
         } else {       // Invalid position for a reset symbol
           MS_SR_symbol_count = 0;  // reset counter on entry to Lock1
           MS_SR_State = MS_SR_Lock1;
         }
         break;
       case MS_SR_Locked:
         if (MS_SR_symbol_count == 0)
         {
           resetLfsr();
         } else {      // Invalid position for a reset symbol
           MS_SR_State = MS_SR_Error1;
           // don't adjust symbol count
         }
         break;
       case MS_SR_Error1:
         if (MS_SR_symbol_count == 0)
         {
           resetLfsr();
           MS_SR_State = MS_SR_Locked;
         } else {      // Invalid position for a reset symbol
           MS_SR_State = MS_SR_Error2;
           // don't adjust symbol count
         }
       case MS_SR_Error2:
         if (MS_SR_symbol_count == 0)
```

```
          {
            resetLfsr();
            MS_SR_State = MS_SR_Locked;
          } else {      // Invalid position for a reset symbol
            MS_SR_symbol_count = 0;  // on entry to Lock1
            MS_SR_State = MS_SR_Lock1;  // to restart the sync
          }
          break;
      } // end of MS_SR robustness state machine
    } // end of processing SR
   } else
  { // Single stream
    if (EnhancedFraming) {
      if (((inByte == SR) || (inByte == CP)) || (inByte == BF) || inEnhSRSeq)
      {
        // robustness scrambler reset mechanism here for enhanced framing, based on
        // detection of two correctly placed symbols in the sequence SR+BF+BF+SR or SR+CP+CP+SR
        // note that ??+BF+BF+?? is assumed to be BS, not SR
        if ((inByte == SR) || (inByte == CP) || (inByte == BF))
          inEnhSRSeq = TRUE;
        for (i=0; i<3; i++)
          srSeq[i]=srSeq[i+1]; // shuffle up
        srSeq[3]=((inByte == SR) || (inByte == CP) || (inByte == BF)) ? inByte : 0;
        if (((srSeq[0] == SR) && ((srSeq[1] == BF) || (srSeq[1] == CP))) ||
            ((srSeq[0] == SR) && ((srSeq[2] == BF) || (srSeq[2] == CP))) ||
            ((srSeq[0] == SR) && (srSeq[3] == SR))                       ||
            (((srSeq[1] == CP) || (srSeq[1] == BF)) && (srSeq[3] == SR)) ||
            (((srSeq[2] == CP) || (srSeq[2] == BF)) && (srSeq[3] == SR)))
        { // reset scrambler
          resetLfsr();
          resetSRSeq();
          inEnhSRSeq = FALSE;
        }
        if ((srSeq[0] == 0) && (srSeq[1] == 0) && (srSeq[2] == 0) && (srSeq[3] == 0))
          inEnhSRSeq = FALSE;   // must have got into this as a result of
                                // a bit error generating an isolated CP or SR
      } // end of robustness mechanism
    } else
    { // Default Framing
    if (inByte == SR)
      resetLfsr();
    }
  }

  outbyte = 0;
  for (i=0; i<11; i++) {       // convert data back to an integer
    temp = scrambit[i] << i;
    outbyte += (scrambit[i] << i);
  }

  // Convert control symbol to Kcode in multistream mode at the transmitter

  if (Multistream && DPTX && ((outbyte & 0x200) == 0x200))
    outbyte = scrControlToKcode[outbyte & 0x7];

  return outbyte;
}
```

F Topology Management/Payload Bandwidth Management Usage Examples (Informative)

This subject matter is to be covered in *MST Use Case Example Ver.1* for informative purposes.

G Link Management during System Initialization (Informative)

G.1 Background

Some DP Source device solutions rely heavily on an operating system video/display driver to handle many of the higher-level functions in the DP protocol.

Immediately after boot (before the operating system is loaded) and when operating in system safe mode, the product-specific video driver is not loaded. In these scenarios, the Video BIOS or equivalent is used to configure the graphics outputs. However, VBIOS does not typically implement interrupt handling, and as a result it cannot respond to link state changes that occur after the BIOS was initially invoked.

Implementing BIOS exception handling causes system incompatibility issues for discrete graphics cards, so this is not a feasible long-term solution.

G.2 Problem Statements

G.2.1 Problem #1 – Sink Device Connected and Powered, but HPD Low

Description – If a Sink device does not keep HPD asserted at all times when powered, the Source device may not detect the Sink device when the VBIOS is invoked. In this case, the Source device shall not enable the output in question, even if that output is available.

Solution – The DP Sink device shall keep HPD asserted unless it is in the OFF state.
See Section 5.2.5.

G.2.2 Problem #2 – Sink Device HPD Unplug Event Followed by Plug Event

Description – If a Sink device is turned on, or is unplugged and re-plugged after a Source device is turned on and VBIOS invoked, the Source device that depends on VBIOS to do Link Training (LT) shall not be able to train the link.

Solution Case 1 – In this case, the DP Source can detect HPD, but can run only Fast LT (training without using AUX transactions).

DP Source Device

- If video needs to be transmitted, run Fast LT to 1-lane RBR link configuration, and transmit 640x480 Fail Safe mode over the link
  - 1-lane RBR/640x480 is supported by all DP Sink devices, and is the most likely to work without Full LT
  - For this to work, the solution the DP Sink device shall support Fast LT. which is capable of anticipating 1-lane RBR link configuration

DP Sink Device

- If capable of supporting Fast LT (optional RX feature in *DP v1.4a*)
  - Be ready to receive Fast LT to 1-lane RBR link configuration and, upon LANE*x*_CR_DONE/LANE*x*_SYMBOL_LOCKED, a 640x480 video stream

This Standard:

- Defines 1-lane RBR as the “default” link configuration for both the DP Source and DP Sink devices when no “last-known-good” link configuration exists, and
- Has no impact on operation of or interoperation with a DP Source device fielding HPD and capable of running Full LT

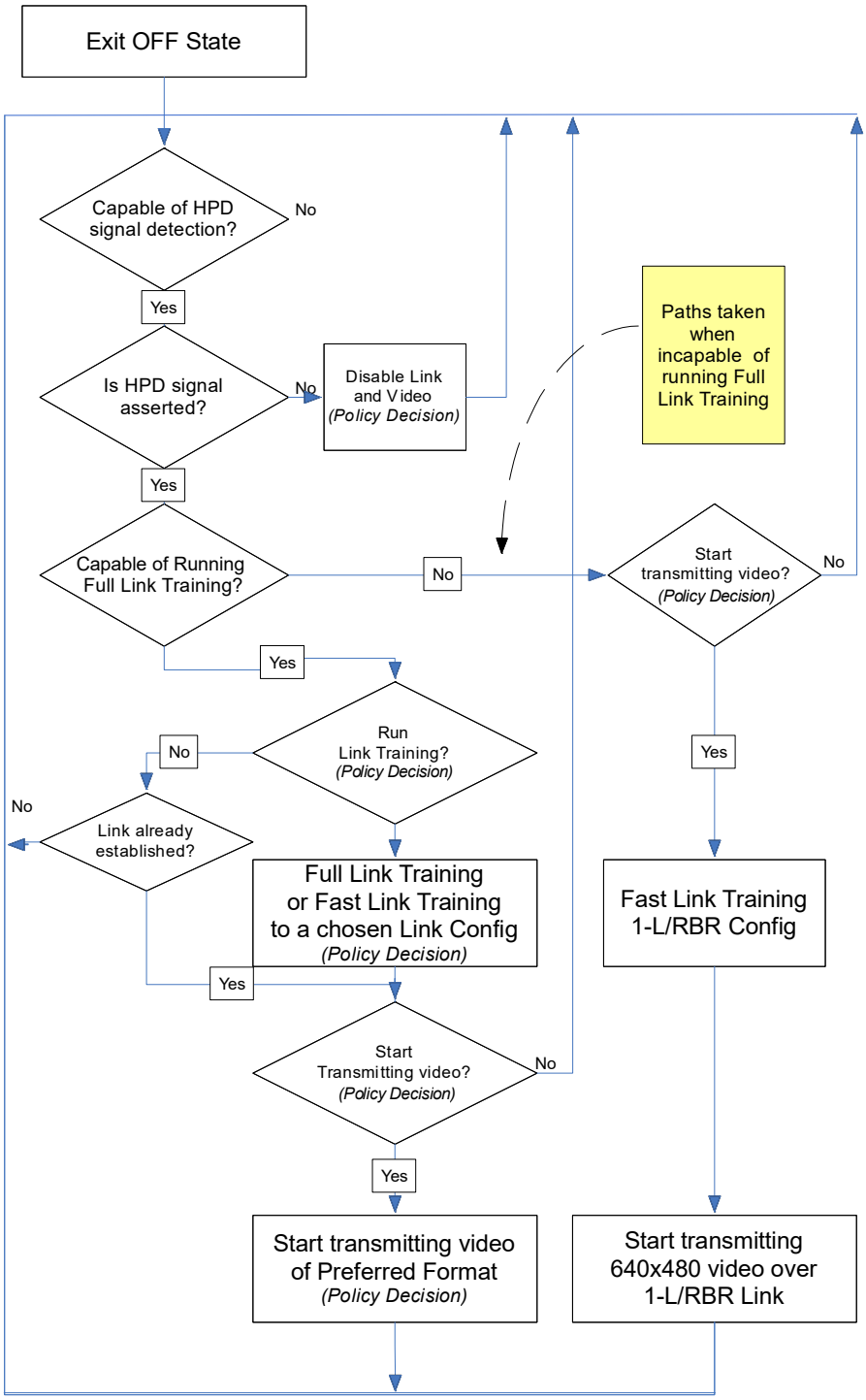


Figure G-1: Link Quality Management with Fast Link Training

Solution Case 2 – In this case, the DP Source device cannot detect HPD.

DP Source Device

- If no known-good link configuration (monitor connected or powered up after the DP Source is powered up) **and** video needs to be transmitted, transmit 640x480 Fail Safe mode over 1-lane RBR Main-Link
  - 1-lane RBR/640x480 supported by all DP Sink devices, and the most likely to work without Full LT
  - To avoid No Display, a DP Sink device that is capable of receiving the Main-Link signal without LT anticipating 1-lane RBR link configuration shall be used
- If a cable is unplugged and re-plugged after the link was established, a DP Source device shall continue transmitting video over the previously established link configuration
  - To avoid No Display, a DP Sink device that is capable of receiving the Main-Link signal without LT anticipating the “last-known-good” link configuration shall be used; works if the same DP Sink device is re-plugged

DP Sink Device

- If capable of receiving the Main-Link signal without LT (RX feature not described in *DP v1.4a*)
  - Be ready to receive the Main-Link signal either to 1-lane RBR or the last-known-good link configuration

This proposal has no impact on operation of or interoperation with a DP Source device fielding HPD and capable of running Full LT.

Figure G-2 illustrates the Source device-side behavior. Figure G-3 illustrates the Sink device-side Power State machine. In this case, the Sink Power State diagram is extended by the addition of State 2S for avoiding No Display when the DP Source device is not capable of fielding HPD.

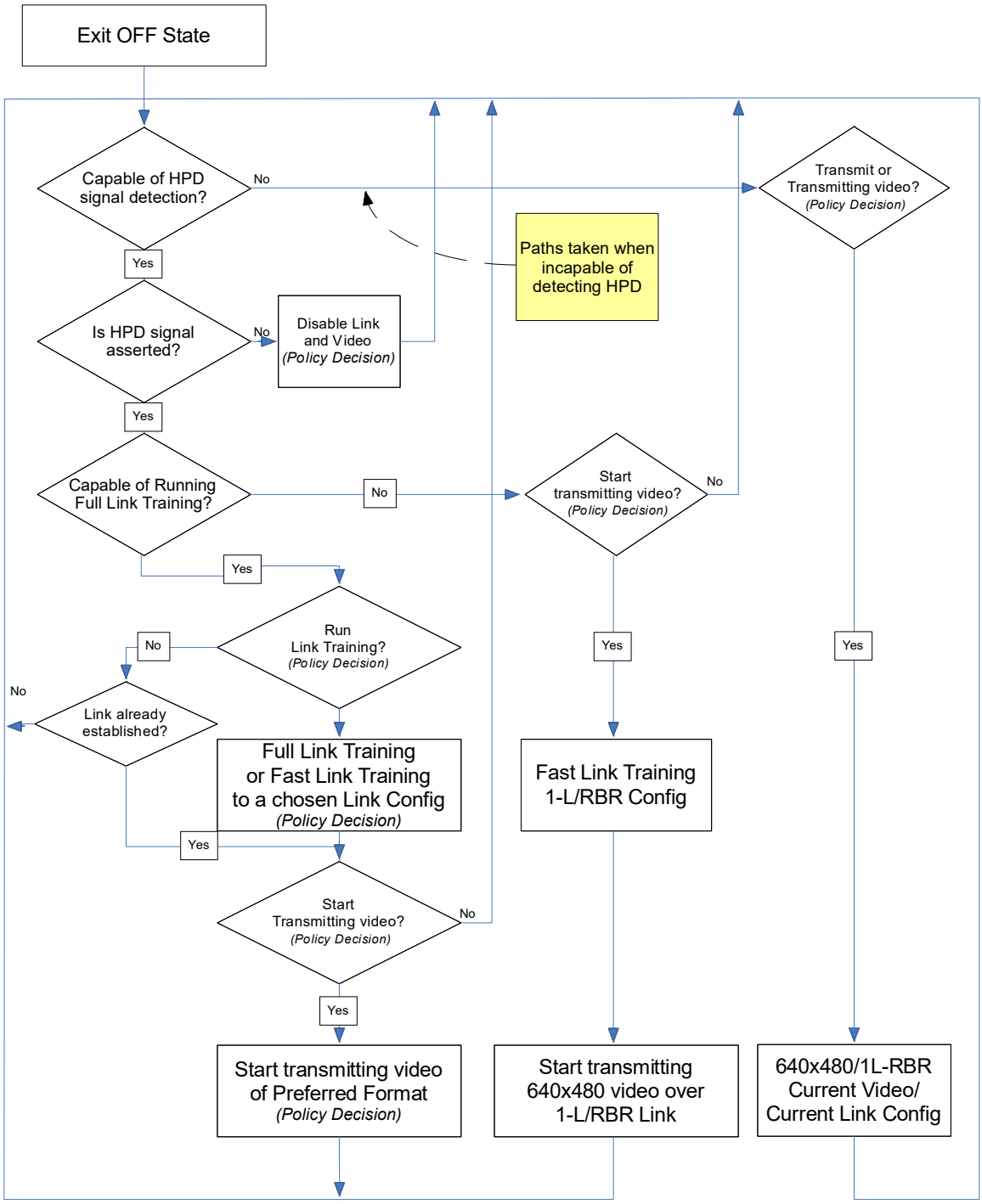


Figure G-2: Link Quality Management Source Fail Safe Mode

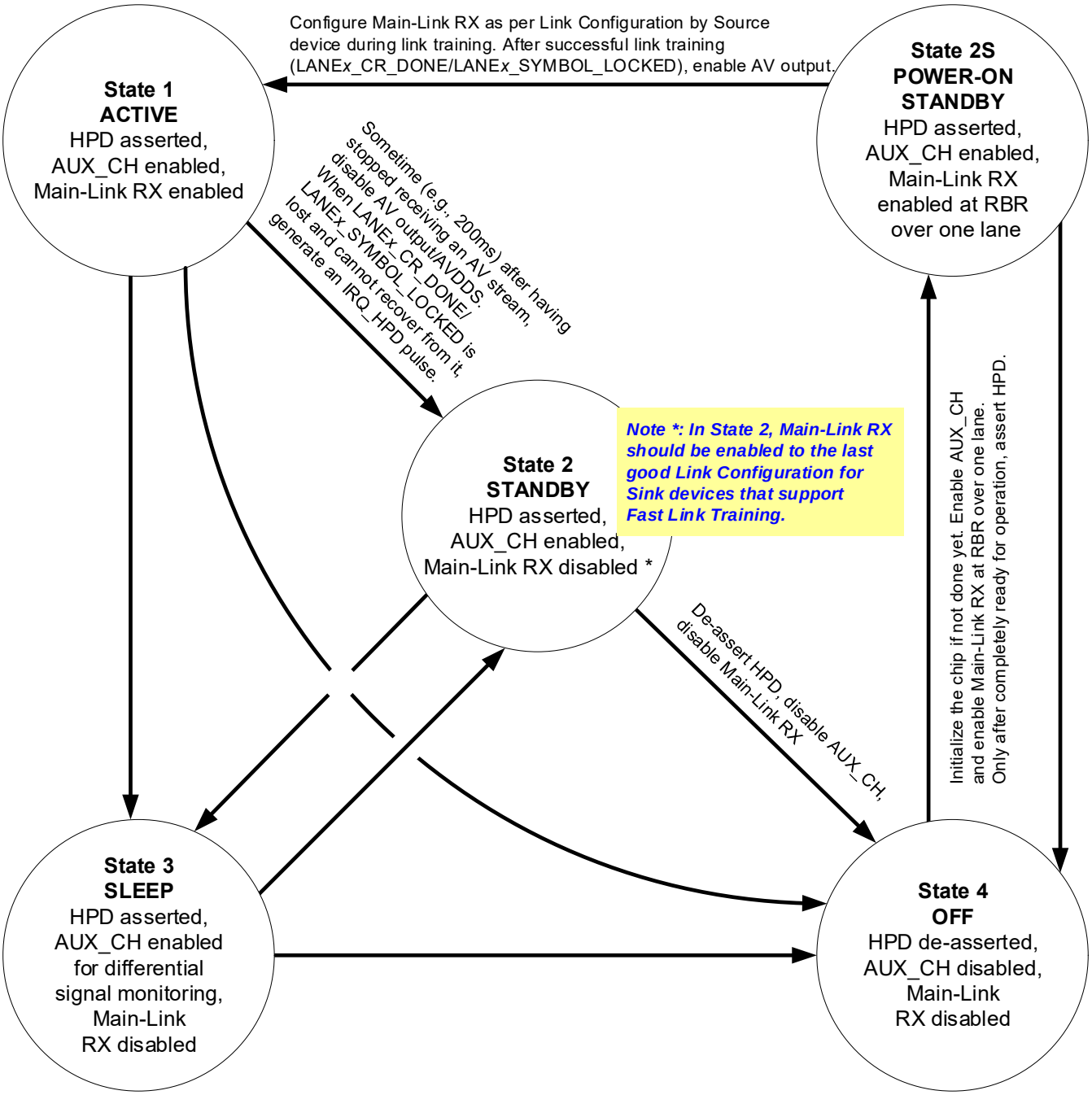


Figure G-3: DP Sink Device Power Management State Diagram with State 2S for a DP Upstream Device Not Capable of HPD Assertion Handling

H 3D Stereo Display Protocol Support

Entire appendix rewritten for *DP v1.4a*.

At 32.4Gbps over four lanes, the DP link bandwidth is sufficient for transporting 1080p 3D Stereo video at 240Hz (i.e., 120Hz each for left- and right-eye view frames).

H.1 In-band 3D Stereo Signaling Methods

This Standard provides for two in-band mechanisms through which a DP Source device can specify the 3D stereo video format attribute that the device is transmitting:

- MSA MISC1 field is used
- VSC SDP is used

A DP Sink device with DPCD r1.2 or higher shall support both methods.

H.1.1 MSA MISC1 Method

Table H-1 defines bits 2:1 of the MSA MISC1 field.

Table H-1: MSA MISC1 Field, bits 2:1 Definitions

Value	Definition
00b	• 3D stereo in-band signaling does **not** use this field; either 3D stereo is **not** being transmitted, –or– 3D stereo video metadata is being transmitted with the VSC SDP in-band signaling mechanism
01b	• **Progressive video** – Next (upcoming) video frame is right-eye view • **Interlaced video** – TOP field is right-eye view, BOTTOM field is left-eye view
10b	RESERVED
11b	• **Progressive video** – Next (upcoming) frame is left-eye view • **Interlaced video** – TOP field is left-eye view, BOTTOM field is right-eye view

H.1.2 VSC SDP Method

A DP Source device may transmit 3D stereo video metadata in-band signaling using a VSC SDP by clearing the MSA MISC1 field, bits 2:1, to 00b.

H.1.2.1 VSC SDP Header

Table H-2 describes the VSC SDP header bytes.

Table H-2: VSC SDP Header Bytes

Byte #	Bit #	Content
HB0	7:0	**Secondary-data Packet ID** 00h.
HB1	7:0	**Secondary-data Packet Type** 07h.
HB2	4:0	**Revision Number** See Section 2.2.5.6 for details.
	7:5	**RESERVED** Read all 0s.
HB3	4:0	**Number of Valid Data Bytes** 3D stereo video metadata is transported on DB0. See Section 2.2.5.6 for further details.
	7:5	**RESERVED** Read all 0s.

H.1.2.2 3D Stereo Video Metadata VSC SDP Payload

Entire section rewritten for *DP v1.4a*.

Table H-3 describes Data Byte 0 (DB0) of a VSC SDP payload. The DB0 bit definitions are the same for VSC rev 1 (HB2 = 01h) through Rev 5 (HB2 = 05h) SDPs.

Table H-3: VSC SDP DB0 Payload

VSC SDP DB0, bits 3:0 = Stereo Interface Method Code	VSC SDP DB0, bits 7:4 = Stereo Interface Method Specific Parameter
0h = Non-stereo Video	Shall be cleared to 0h.
1h = Frame/Field Sequential See Figure H-1 for the left- and right-eye view frame mapping and the transport timing. The left-eye view frame is the top view frame.	**Frame/Field Sequential Type** 0h = Left- and right-eye views, based on the MSA MISC1 field, bits 2:1. 1h = Right-eye view when Stereo Signal = 1. 2h = Left-eye view when Stereo Signal = 1. All other values (3h through Fh) are RESERVED for future use. ***Note:*** *Stereo Signal refers to an out-of-band signaling, indicating the left- and right-eye view frames, and can be conveyed using a VESA stereo connector or other equivalent means.*
2h = Stacked Frame See Figure H-2 for the left- and right-eye view frame mapping and the transport timing.	**Stacked Frame Type** 0h = Left-eye view is on the top. Right-eye view is on the bottom. All other values (1h through Fh) are RESERVED for future use.
3h = Pixel Interleaved See Figure H-3 for the left- and right-eye pixel mapping. See Figure H-4 for the transport timing.	**Interleave Pattern Type** For Interleave Pattern Types 1 through 4, a 2x2 pattern grid is used to illustrate the interleaving pattern of the composited stereo frame. 0h = Interleave pattern corresponding to 2-way horizontally interleaved stereo in which the right-eye view pixels are on even lines. 1h = Interleave pattern corresponding to 2-way horizontally interleaved stereo in which the right-eye view pixels are on odd lines. 2h = Interleave pattern corresponding to a checkerboard pattern with alternating left- and right-eye view pixels, starting with a left-eye view pixel. 3h = Interleave pattern corresponding to 2-way vertically interleaved stereo, starting with left-eye view pixels. 4h = Interleave pattern corresponding to 2-way vertically interleaved stereo, starting with right-eye view pixels. All other values (5h through Fh) are RESERVED for future use.
4h = Side-by-side See Figure H-5 for the left- and right-eye view frame mapping and the transport timing.	**Side-by-side Type** 0h = Left half of the image represents the left-eye view. Right half of the image represents the right-eye view. 1h = Left half of the image represents the right-eye view. Right half of the image represents the left-eye view. All other values (2h through Fh) are RESERVED for future use.

Table H-3: VSC SDP DB0 Payload (Continued)

VSC SDP DB0, bits 3:0 = Stereo Interface Method Code	VSC SDP DB0, bits 7:4 = Stereo Interface Method Specific Parameter
5h = Top-to-bottom See Figure H-6 for the left- and right-eye view frame mapping and the transport timing.	**Top-to-bottom Type** 0h = Top half of the image represents the left-eye view. Bottom half of the image represents the right-eye view. 1h = Top half of the image represents the right-eye view. Bottom half of the image represents the left-eye view. All other values (2h through Fh) are RESERVED for future use.
Values 6h through Fh are RESERVED.	RESERVED

Figure H-1 illustrates Frame/Field Sequential 3D stereo video transport left- and right-eye view frame mapping, transport timing, and CRC value calculation.

The CRC value calculation depends on whether the DP Source device selects CRC Option 0 or 1, as illustrated in Figure H-1. (See Section H.1.2.4.)

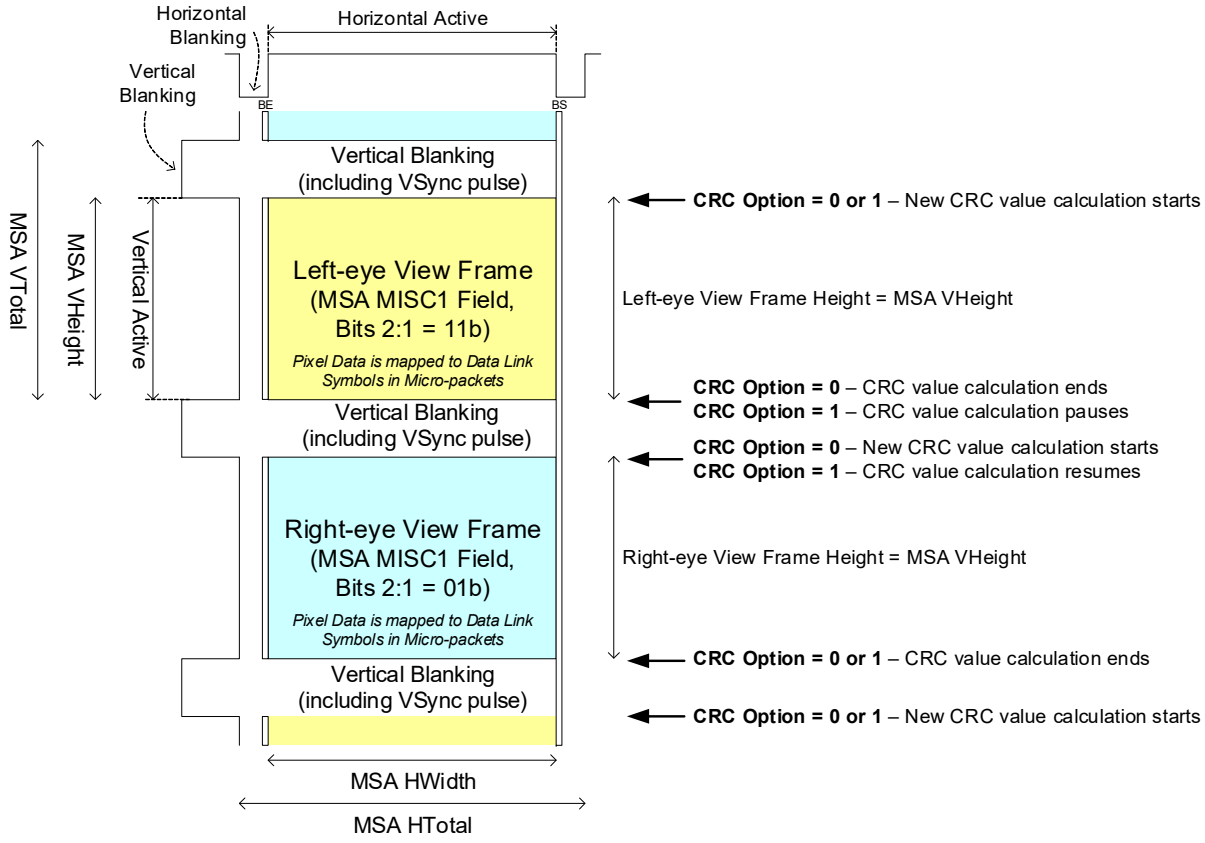


Figure H-1: Frame/Field Sequential 3D Stereo Video Left- and Right-eye View Frame Mapping, Transport Timing, and CRC Value Calculation

Figure H-2 illustrates Stacked Frame 3D stereo video transport left- and right-eye view frame mapping, transport timing, and CRC value calculation.

Vertical active lines consist of vertical active lines for the left-eye (top) view, vertical space region (VSR) lines, and vertical active lines for the right-eye (bottom) view. The VSR line count is equal to the vertical blank line count (= MSA VTotal – MSA VHeight) between the right-eye (bottom) view and left-eye (top) view.

A DP Source device shall transmit 00h pixel data in micro-packets on the VSR video lines in the same way that it maps pixel data to Data Link Symbols and places the pixel data into micro-packets on the left- and right-eye view frame active video lines.

The CRC value calculation depends on whether the DP Source device selects CRC Option 0 or 1, as illustrated in Figure H-2. (See Section H.1.2.4.)

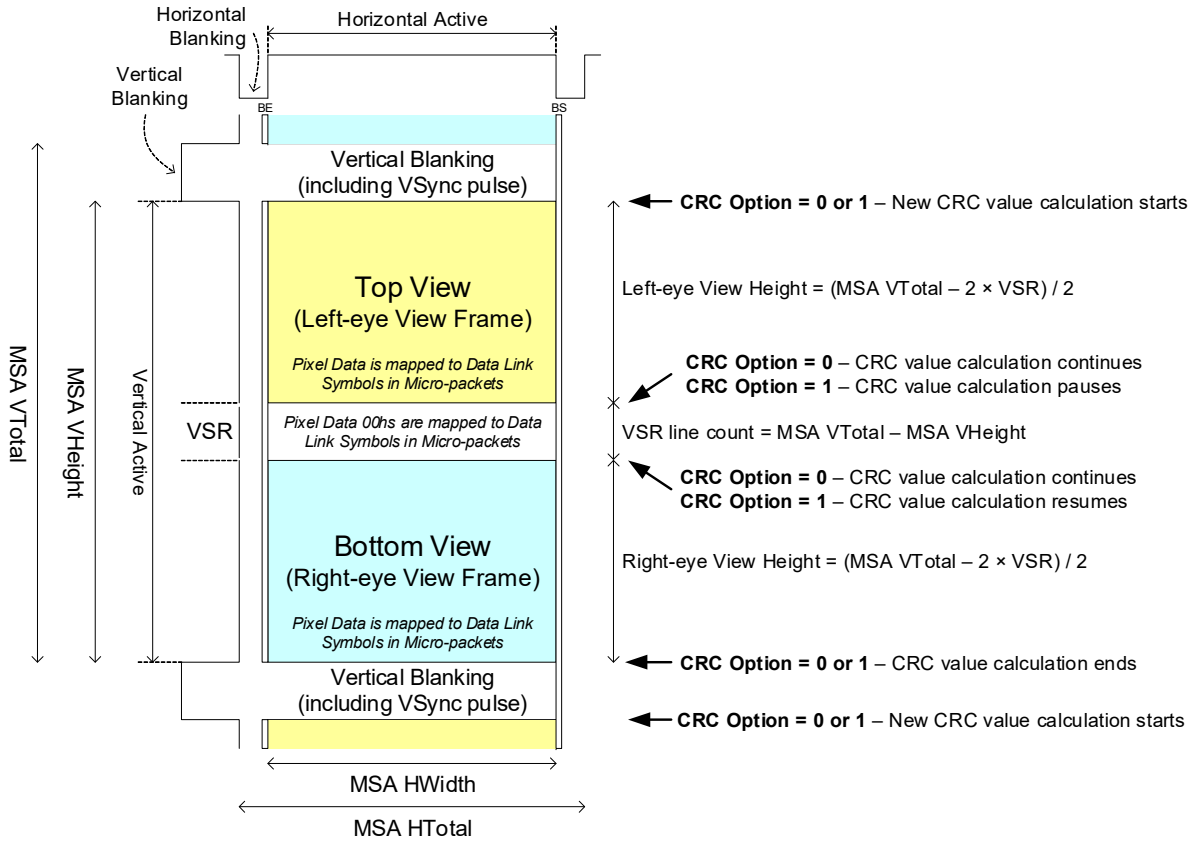


Figure H-2: Stacked Frame 3D Stereo Video Left- and Right-eye View Frame Mapping, Transport Timing, and CRC Value Calculation

Figure H-3 illustrates Pixel Interleaved 3D stereo video left- and right-eye view frame pixel mapping.

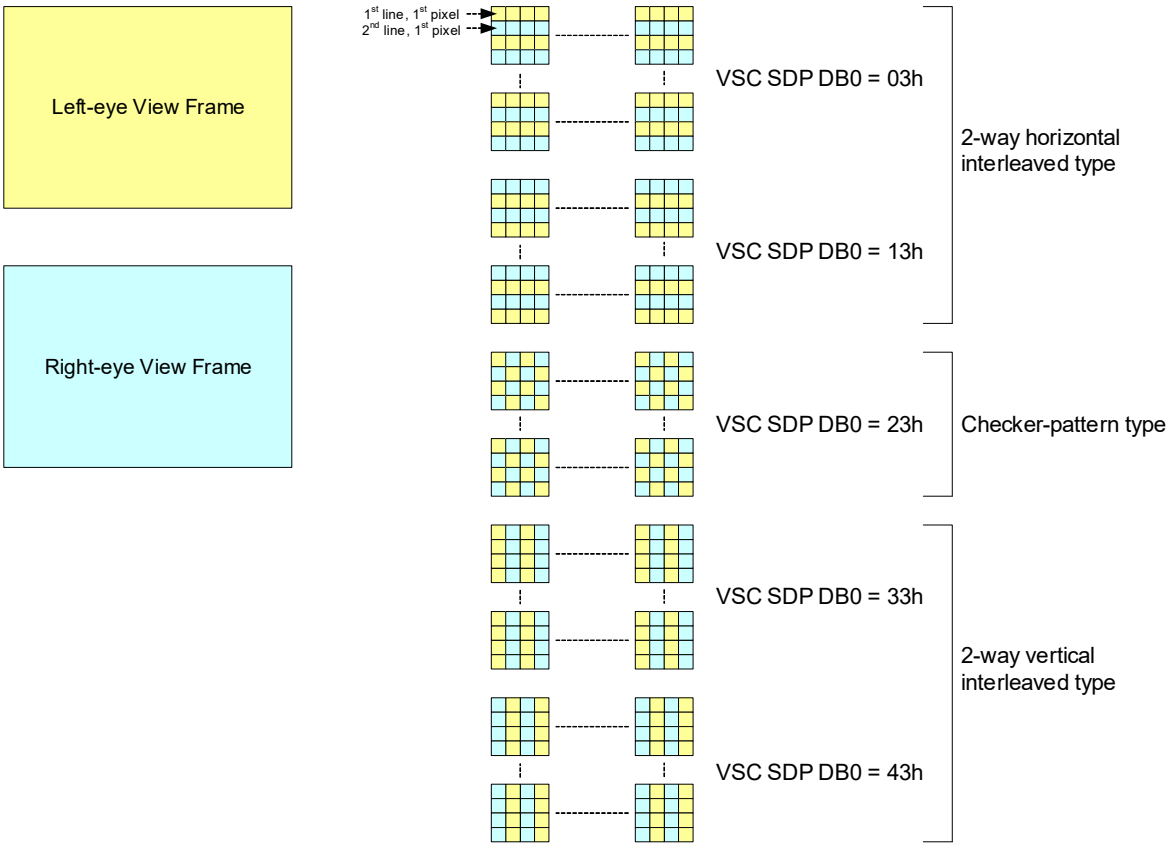


Figure H-3: Pixel Interleaved 3D Stereo Video Left- and Right-eye View Frame Pixel Mapping

Figure H-4 illustrates Pixel Interleaved 3D stereo video transport timing and CRC value calculation.

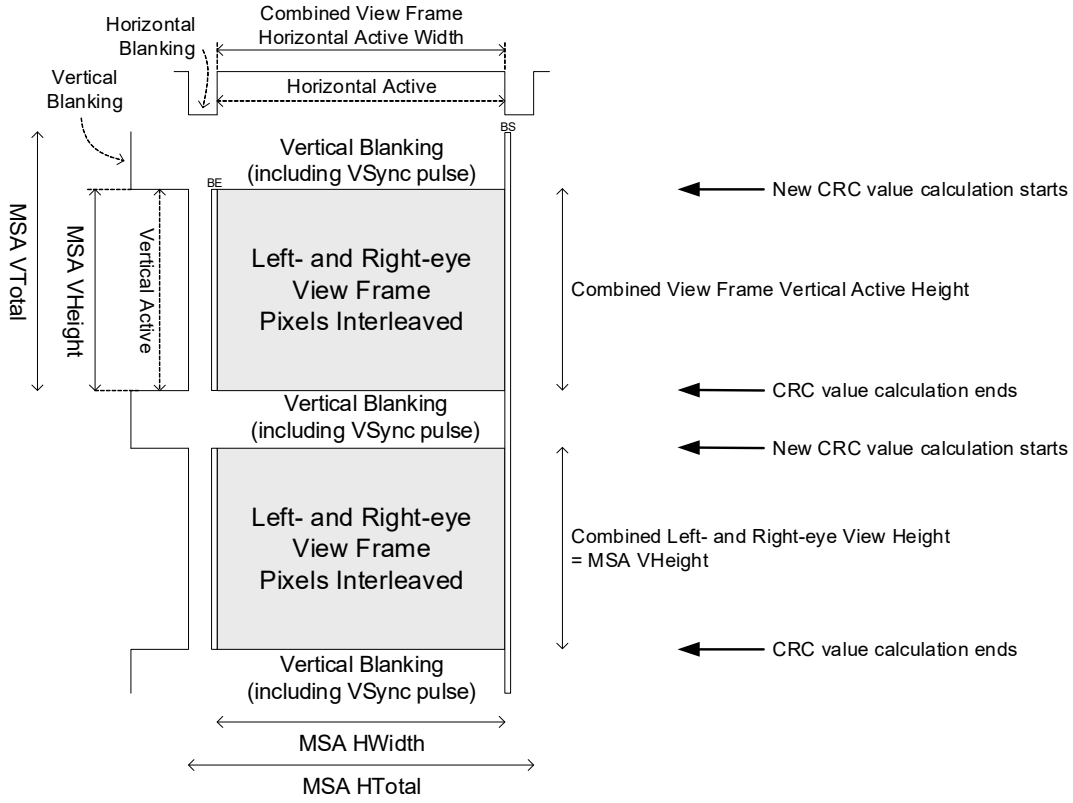


Figure H-4: Pixel Interleaved 3D Stereo Video Left- and Right-eye View Transport Timing and CRC Value Calculation

Figure H-5 illustrates Side-by-side 3D stereo video (with DB0 bits 7:4 = 0x0) left- and right-eye view frame pixel mapping, transport timing, and CRC value calculation.

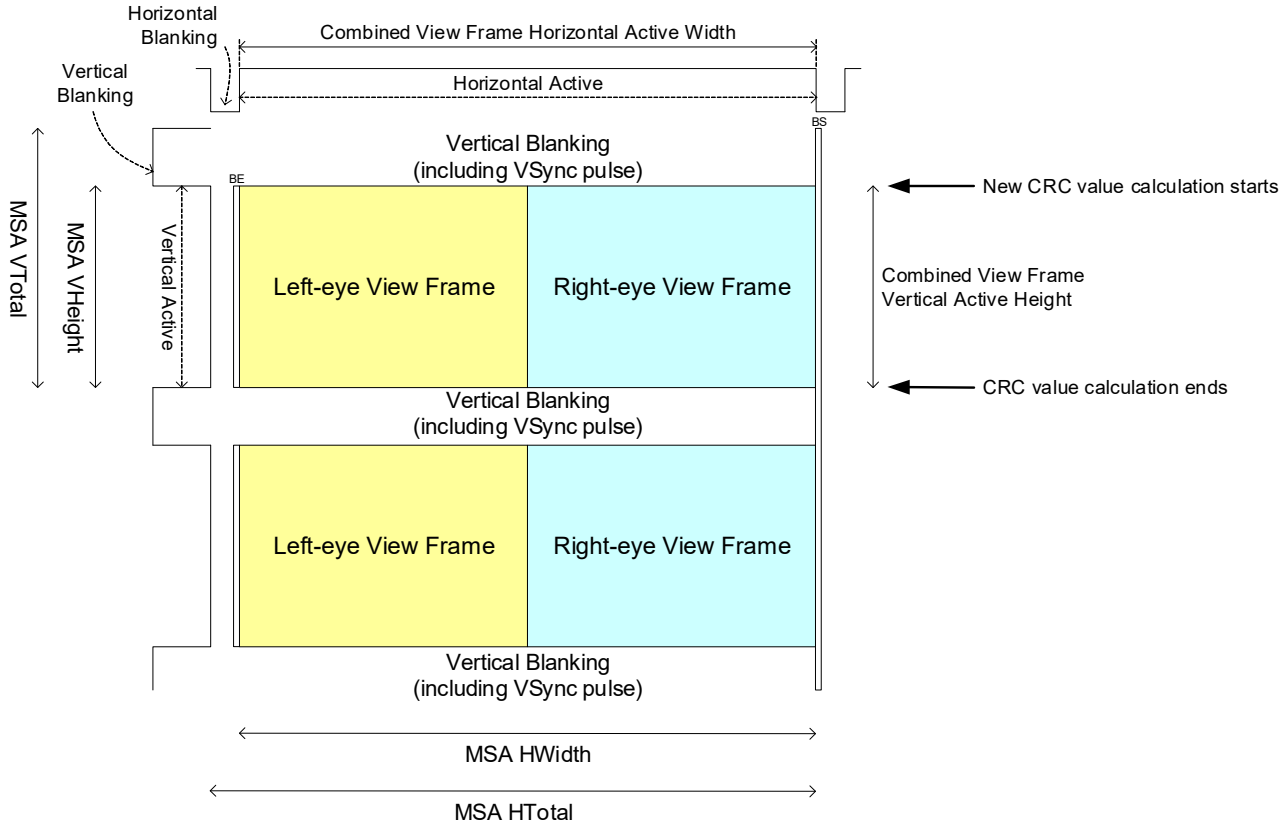


Figure H-5: Side-by-side 3D Stereo Video Left- and Right-eye View Frame Mapping, Transport Timing, and CRC Value Calculation

Figure H-6 illustrates Top-to-bottom 3D stereo video (with DB0 bits 7:4 = 0x0) left- and right-eye view frame pixel mapping, transport timing, and CRC value calculation.

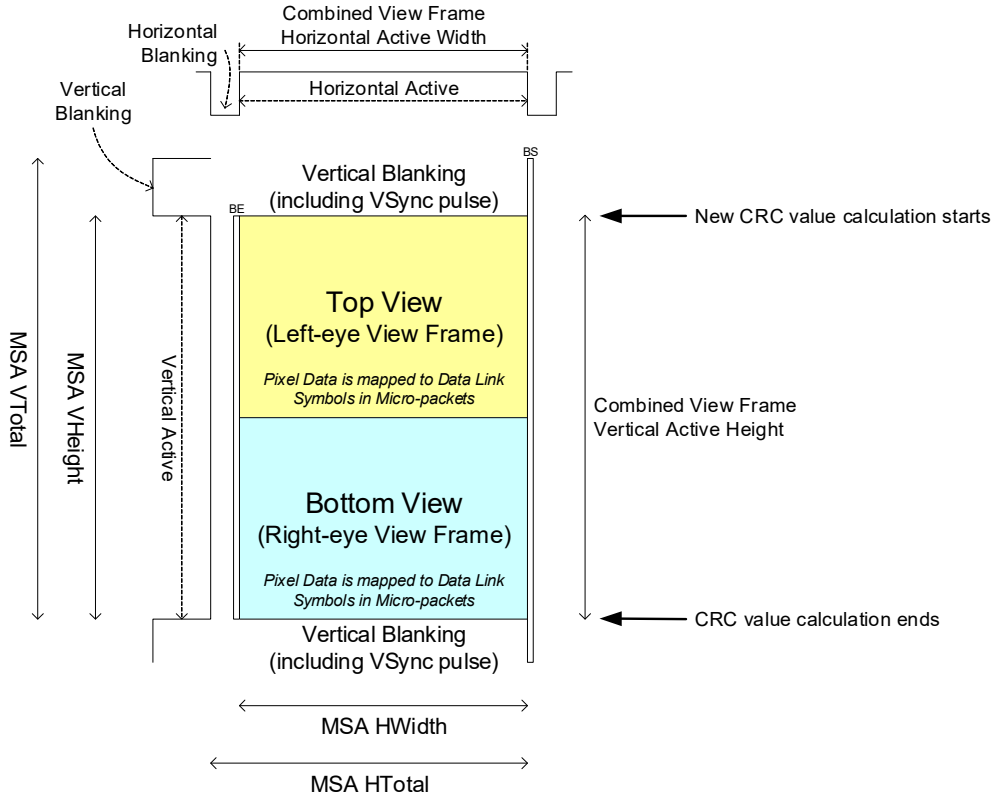


Figure H-6: Top-to-bottom 3D Stereo Video Left- and Right-eye View Frame Mapping, Transport Timing, and CRC Value Calculation

H.1.2.3 MSA for 3D Stereo Video

New to *DP v1.4a*.

MSA video timing parameters, namely, HTotal[15:0], HStart[15:0], HWidth[15:0], HSyncPolarity[0] (HSP), HSyncWidth[14:0] (HSW), VTotal[15:0], VStart[15:0], VHeight[15:0], VSyncPolarity[0] (VSP), and VSyncWidth[14:0] (VSW), for 3D stereo video represent those parameters between adjacent VSync pulses.

Left- and right-eye views may be sub-sampled prior to DPTX transmission. The MSA video timing parameters represent those of the transmitted frames.

For Frame/Field Sequential 3D stereo format, a DP Source device indicates left- and right-eye view using the MSA MISC1 field, bits 2:1.

A DPRX receiving Stacked Frame 3D stereo video shall determine the left- and right-eye view active height, using the following equation:

Left- and right-eye view active height = (MSA VHeight – VSR) / 2

where:

- VSR (vertical separation region) = MSA VTotal – MSA VHeight

If the optional Adaptive-Sync feature is enabled when Stacked Frame 3D stereo video is selected, the VSR line count remains constant and the VBlank line count between the right-eye (bottom) view and left-eye (top) view is altered.

H.1.2.4 CRC Calculation for 3D Stereo Video

New to *DP v1.4a*.

For Frame/Field Sequential and Stacked Frame 3D stereo video, there are two options (Option 0 or 1) for calculating the CRC value, as listed in Table H-4. (See also Figure H-1 and Figure H-2.)

A DPRX that supports Option 1 shall also support Option 0 and set the CRC_3D_OPTIONS_SUPPORTED bit in the NORP & DP_PWR_VOLTAGE_CAP register (DPCD Address 00004h, bit 1) to 1.

A DPTX that needs to use Option 1 shall set the CRC_3D_OPTION1_SELECT bit in the TEST_SINK register (DPCD Address 00270h, bit 1) to 1.

A DPRX shall clear the CRC_3D_OPTION1_SELECT bit to 0 at power-on or when an upstream device disconnect event occurs.

Table H-4: CRC Calculation Method for 3D Stereo Video Summary

VSC SDP DB0, bits 3:0 (Stereo Interface Method Code)	CRC Calculation Method
1 (Frame/Field Sequential)	• **Option 0** – CRC calculation starts at the beginning of each view frame and then completes at the end of the view frame[a] • **Option 1** – CRC calculation starts at the beginning of the left-eye view frame, pauses on the ensuing vertical blanking lines, resumes at the beginning of the right-eye view frame, and then completes at the end of the right-eye view frame[b]
2 (Stacked Frame)	• **Option 0** – CRC calculation starts at the beginning of the top view frame, frame continues through the VSR lines, and then completes at the end of the bottom view frame[a] • **Option 1** – CRC calculation starts at the beginning of the top view frame, pauses on the VSR lines, resumes at the beginning of the bottom view frame, and then completes at the end of the bottom view frame[b]
3 (Pixel Interleaved)	• CRC is calculated for the combined left- and right-eye view frames[c]
4 (Side-by-side)	
5 (Top-to-bottom)	

a. CRC_3D_OPTION1_SELECT bit in the TEST_SINK register (DPCD Address 00270h, bit 1) is cleared to 0.
b. CRC_3D_OPTION1_SELECT bit is set to 1.
c. CRC_3D_OPTION1_SELECT bit value is "don't care."

H.2 3D Stereo Display Capability Declaration

The 3D stereo capability can be exposed in DisplayID and legacy EDID. A 3D stereo format is usually associated with specific timing; therefore it is desirable to indicate which timings support 3D stereo format and which do not. Furthermore, for a given timing that supports 3D stereo format, the timing shall indicate which stereo format(s) it supports. Both DisplayID and legacy EDID have the ability to expose 3D stereo capability per timing; however, DisplayID provides for a more-efficient and flexible format declaration.

H.2.1 Legacy EDID 3D Stereo Display Capability Declaration

The 18-byte detailed timing descriptor has a field that provides information about stereo viewing support. The field described in Table H-5 allows a timing to be declared without any 3D stereo support or a specific 3D stereo format.

Table H-5: Legacy EDID r1.4 3D Stereo Display Capability Declaration

Byte 17 Bit Definitions								Detailed Timing Definitions
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Signal Interface Type:**
0	_	_	_	_	_	_	_	Non-Interlaced (1 frame = 1 field)
1	_	_	_	_	_	_	_	Interlaced (1 frame = 2 fields)
_	**6**	**5**	_	_	_	_	**0**	**Stereo Viewing Support:**
	0	0	_	_	_	_	x	Normal Display – No Stereo; the value of bit 0 is “don’t care”
	0	1	_	_	_	_	0	Field sequential stereo, right image when stereo sync signal = 1
	1	0	_	_	_	_	0	Field sequential stereo, left image when stereo sync signal = 1
	0	1	_	_	_	_	1	2-way interleaved stereo, right image on even lines
	1	0	_	_	_	_	1	2-way interleaved stereo, left image on even lines
	1	1	_	_	_	_	0	4-way interleaved stereo
	1	1	_	_	_	_	1	Side-by-Side interleaved stereo
_	_	_	**4**	**3**	**2**	**1**	_	**Analog Sync Signal Definitions:**
			0	0	_	_	_	Analog Composite Sync:
			0	1	_	_	_	Bipolar Analog Composite Sync:
			0	_	0	_	_	---------- Without Serrations;
			0	_	1	_	_	---------- With Serrations (Hsync during Vsync);
			0	_	_	0	_	---------- Sync On Green Signal only
			0	_	_	1	_	---------- Sync On all three (RGB) video signals
_	_	_	**4**	**3**	**2**	**1**	_	**Digital Sync Signal Definitions:**
			1	0	_	_	_	Digital Composite Sync:
			1	0	0	_	_	---------- Without Serrations;
			1	0	1	_	_	---------- With Serrations (Hsync during Vsync);
			1	1	_	_	_	Digital Separate Sync:
			1	1	0	_	_	---------- Vertical Sync is Negative;
			1	1	1	_	_	---------- Vertical Sync is Positive;
			1	_	_	0	_	---------- Horizontal Sync is Negative (outside of Vsync)
			1	_	_	1	_	---------- Horizontal Sync is Positive (outside of Vsync)

A legacy EDID base block does **not** have a field that indicates Top-to-bottom 3D stereo video support. However, a DP Source device may determine whether the DP Sink device supports use of Left-beside-Right or Left-over-Right in Side-by-side 3D stereo video by examining the display Aspect Ratio, as well as the Vertical Active line (VA) and Horizontal Active pixel (HA) fields in the legacy EDID Detailed Timing Descriptor (DTD). If the aspect ratio in legacy EDID Bytes 15 and 16 indicates a normal 4:3 or 16:9 H vs. V ratio for Landscape/Portrait mode, and yet HA vs. VA indicates that HA is greater than 2x VA, this is a Left-beside-Right mode. Similarly, if VA indicates at least twice the expected size for a given aspect ratio, it is a Left-above-Right mode.

Alternately, a DP Sink device that supports Top-to-bottom 3D stereo video may expose it by using vendor-specific or display transport interface-specific (if available) capability declaration.

With respect to the Addressable Image Size fields in legacy EDID Bytes 12, 13, and 14 for the Left-beside-Right packing, the Vertical Addressable Image size is set as normal, and the Horizontal size is set to the size of one eye view only. In the case of Left-above-Right packing, the Horizontal size is set as normal, and the Vertical size is set to the size of one eye view only.

H.2.2 DisplayID 3D Stereo Display Capability Declaration

In DisplayID, the Timing Options field of the Type VII detailed timing data block (described in Table H-6) exposes the capability that indicates whether timing is displayed with no stereo, with stereo, or dynamically configured based on the content that is being shown.

Table H-6: *DisplayID Standard*, 3D Stereo Display Capability Declaration

Byte 3 Bits								Type VII Detailed Timing Data Block	
7	_	_	_	_	_	_	_	**Timing Options**	**FLAGS**
1	_	_	_	_	_	_	_	Preferred Detailed Timing	
_	**6**	**5**	_	_	_	_	_	**3D Stereo Support**	**FLAG**
_	0	0	_	_	_	_	_	This timing shall always be displayed in mono (no stereo)	
_	0	1	_	_	_	_	_	This timing shall always be displayed in stereo	
_	1	0	_	_	_	_	_	This timing shall be displayed in mono or stereo, depending on a user action (such as wearing stereo glasses)	
_	1	1	_	_	_	_	_	RESERVED	
_	_	_	**4**	_	_	_	_	**Interface Frame Scanning Type**	**FLAG**
_	_	_	0	_	_	_	_	Progressive scan frame	
_	_	_	1	_	_	_	_	Interlaced scan frame	
_	_	_	_	**3**	**2**	**1**	**0**	**Aspect Ratio**	
_	_	_	_	0	0	0	0	1:1	
_	_	_	_	0	0	0	1	5:4	
_	_	_	_	0	0	1	0	4:3	
_	_	_	_	0	0	1	1	15:9	
_	_	_	_	0	1	0	0	16:9	
_	_	_	_	0	1	0	1	16:10	
				0	1	1	0	64:27	
				0	1	1	1	256:135	
				1	0	0	0	Aspect ratio shall be calculated by using the Horizontal Active Image Pixels and Vertical Active Image Lines fields (Bytes 5:4 and 13:12, respectively) in the Type VII Detailed Timing Descriptor.	
_	_	_	_	_	_	_	_	All other values are RESERVED	

Apart from declaring per-timing 3D stereo capability, DisplayID has a more-flexible format for declaring the various 3D stereo formats. The Stereo Display Interface Data Block section of *DisplayID Standard* describes the various 3D stereo formats.

Table H-7 lists the supported *DisplayID Standard* 3D stereo display formats. As is the case with the legacy EDID base block, the DisplayID block in *DisplayID Standard* does **not** have a field that indicates Top-to-bottom 3D stereo video support. As noted in Section H.2.1, a DP Source device may determine Top-to-bottom 3D stereo video support based on the aspect ratio information. Alternately, a DP Sink device that supports Top-to-bottom 3D stereo video may expose Top-to-bottom 3D stereo video by using vendor-specific or display transport interface-specific (if available) capability declaration.

Table H-7: 3D Stereo Display Format Method Codes Supported in *DisplayID Standard*

Code	Interface Method
00h	Frame/Field Sequential Stereo
01h	Side-by-side Stereo
02h	Pixel-interleaved Stereo
03h	Dual Interface, Left and Right Separate
04h	Multi-view
05h	Stacked Frame Stereo
FEh through 06h	RESERVED
FFh	Proprietary Stereo Interface Methods

H.2.3 Pixel Sub-sampling/Non-Sub-sampling Capabilities Declaration

New to *DP v1.4a*.

Neither the legacy EDID base block nor DisplayID block in *DisplayID Standard* has a field that indicates pixel sub-sampling/non-sub-sampling support. A DP Sink device that supports those capabilities may expose them by using vendor-specific or display transport interface-specific (if available) capability declaration.

H.3 DP 3D Stereo Interoperability Policy

This section describes support for Source and Sink devices that support DP 3D Stereo. The needs of this policy shall be met to ensure 3D Stereo interoperability between 3D Stereo-enabled Source and Sink devices over an open, box-to-box DP link.

H.3.1 DP 3D Stereo Sink Device Support

This section describes support for a DP 3D Stereo Sink device. A DP Sink device may support 3D Stereo.

A DP 3D Stereo Sink device shall support at least one of the following display resolutions in 3D Stereo format:

- 1920x1080
- 1600x900
- 1440x900
- 1366x768
- 1280x720

Timing requirements for the above display resolutions are described in the sections that follow. Sink devices shall support HBR and RBR link rates, and may support HBR3 and HBR2 link rates. Sink devices may also support other 3D Stereo display resolutions; however, such resolutions may or may not be supported by a given Source device.

A DP 3D Stereo Sink device shall support both of the following timing formats:

- Frame/Field Sequential Stereo format, as illustrated in Figure H-1
- Stack Frame 3D Stereo Video format, as illustrated in Figure H-2

H.3.1.1 3D Stereo Sink Frame/Field Sequential Stereo Format

A DP 3D Stereo Sink device shall support Frame/Field Sequential Stereo format, as illustrated in Figure H-1. This format shall support at least one of the display resolutions listed in Table H-8, using HBR or RBR, with a specified pixel rate within the indicated ranges. The DP Sink device shall expose supported timing in the detailed timing structure. The minimum and maximum pixel rates listed in Table H-8 are derived from *CVT Standard*:

- Minimum pixel clock frequency shall be the same as *CVT Standard* reduced blanking
- Maximum pixel clock frequency shall be the same as *CVT Standard* normal blanking

The minimum VBlank and HBlank periods shall be limited as follows:

- Minimum horizontal blanking shall be that specified by *CVT Standard* reduced blanking
- Minimum vertical blanking shall be that specified by *CVT Standard* reduced blanking

Table H-8: Allowed Timing Range for 3D Stereo Sink, for Frame/Field Sequential Stereo Format

Display Resolution	Vertical Blank Rate (Hz)[a]	Pixel Rate (MP/s)[b]	
		Min	Max
1920x1080	120	285.5	369.5[c]
1600x900		201.25	254.25
1440x900		182.75	228.25
1366x768		148.75	185.0
1280x720		131.75	162.0

a. Vertical blanks occur for each frame, as illustrated in Figure H-1. The 120-Hz vertical blank rate provides one left- and right-eye view frame pair at 60Hz each.
b. Minimum and maximum pixel rate values have a tolerance of ±0.5%, as per DMT Standard.
c. For 4-lane HBR implementations, 360MP/s is the maximum achievable pixel rate when using 24bpp. Rates beyond 360MP/s can be achieved by using 18bpp.

H.3.1.2 3D Stereo Sink Stacked Frame 3D Stereo Video Format

A DP 3D Stereo Sink device shall support Stacked Frame 3D Stereo Video format, as illustrated in Figure H-2. This format shall support at least one of the display resolutions listed in Table H-9, using RBR or HBR, with a specified pixel rate within the indicated ranges. The Sink device shall expose supported timing in the DisplayID extension, as described in *DisplayID v1.2* (or higher). With the exception of the 1920x1080 24-Hz format, the minimum and maximum pixel rates listed in Table H-9 are derived from *CVT Standard*:

- Minimum pixel clock frequency shall be the same as *CVT Standard* reduced blanking
- Maximum pixel clock frequency shall be the same as *CVT Standard* normal blanking

The minimum VBlank and HBlank periods shall be limited as follows:

- Minimum horizontal blanking shall be that specified by *CVT Standard* reduced blanking
- Minimum vertical blanking shall be that specified by *CVT Standard* reduced blanking

Table H-9: Allowed Timing Range for 3D Stereo Sink, for Stacked Frame 3D Stereo Video Format

Display Resolution	Vertical Blank Rate (Hz)[a]	Pixel Rate (MP/s)[b]	
		Min	Max
1920x1080	23.976 (24)	74.176	74.25
1920x1080	59.94 (60)	285.5	369.5[c]
1600x900	60	201.25	254.25
1440x900		182.75	228.25
1366x768		148.75	185.0
1280x720		131.75	162.0

a. One vertical blank occurs for each left- and right-eye view pair, as illustrated in Figure H-2. The 24-Hz vertical blank rate delivers one left-eye view frame and one right-eye view frame at 24Hz. The 60-Hz vertical blank rate delivers one left-eye view frame and one right-eye view frame at 60Hz.

b. Minimum and maximum pixel rate values have a tolerance of ±0.5%, as per DMT Standard.

c. For 4-lane HBR implementations, 360MP/s is the maximum achievable pixel rate when using 24bpp. Rates beyond 360MP/s can be achieved by using 18bpp.

H.3.2 DP 3D Stereo Video Source Device Support

This section describes support for a DP 3D Stereo Video Source device. A DP Source device may support 3D Stereo.

A DP 3D Stereo Video Source device shall support one of the following timing formats:

- Frame/Field Sequential Stereo format, as illustrated in Figure H-1
- Stacked Frame 3D Stereo Video format, as illustrated in Figure H-2

Note: *In keeping with the above-stated requirements, the DP Source device shall support 4-lane Main-Link operation up to HBR. A DP 3D Stereo Source device may support HBR3 and HBR2.*

For a Source device that supports Frame/Field Sequential Stereo format, the Source device shall support any Sink device that meets the timing criteria described in Section H.3.1.1. The Frame/Field Sequential Stereo format from the Source device shall be identified with the MSA MISC1 field, bits 2:1. The VSC SDP may be used.

For a Source device that supports Stacked Frame 3D Stereo Video format, the Source device shall support any Sink device that meets the timing criteria described in Section H.3.1.2. The Stacked Frame 3D Stereo Video format shall be identified through use of the VSC SDP, and the MISC1 field, bits 2:1, shall be cleared to 00b.

I QUERY_STREAM_ENCRYPTION_STATUS Message Transaction Handling in a CP Tree Topology

Entire appendix updated in *DP v2.0*.

Prior to the introduction MST mode and MST topology features in this Standard, each of one or multiple DP display output ports was controlled by each transmitter of an MST Source device (e.g., a GPU), and the status of content on each display output port was known and controlled by the GPU.

Because the GPU is typically a "licensed source component" of Content Protection (CP) technology, it has been required to robustly convey the status of the CP protocols on those output ports to content players supporting approved output protection protocols. In an MST topology, however, the routing of content streams occur external to the GPU, typically by unsecured software control through unsecured Sideband MSGs over the AUX_CH.

I.1 Self-checking by MST Branch Devices

By CP license, MST Branch devices are likely to be required to apply a "Self-Checking" policy. Complying with the policy, MST Branch devices are to detect misconfigurations and apply license policy control directly, for example, by disabling an unauthenticated output port or by down sampling at the MST Branch device level, and reflect the success/failure to the upstream transmitter (e.g., by aborting authentication upon failure).

The difficulty with Self-Checking at the MST Branch device level is that the policy varies among content licenses and CP technology. Some content licenses (DTCP, for example) prohibit the devices from interfering with the displaying of content (by disabling a display output port, for example), regardless of whether the authentication has been successfully established, when a "copy-always" policy is presented even when the content itself may be protected. Other licenses (AACS, for example) require content down-sampling when the connected display does not support the approved CP protocols.

I.2 Merit of QUERY_STREAM_ENCRYPTION_STATUS Message Transaction

As a usage model, it is desirable that the encryption state of independent output streams in an MST topology not affect the other output streams. For example, consider the scenario in which a non-CP device is hot plugged to an MST Branch device while the link driven by an MST Source device of the MST topology has already been authenticated and stream outputs from the MST Source device have been encrypted. In this usage scenario, it is desirable that the failure to authenticate a newly added, non-CP device not cause authentication to be aborted on unrelated stream outputs; such behavior would not be consistent with the behavior of an MST Source device outputting multiple display streams from multiple physical display output ports, or display connectors (i.e., one display stream per display connector).

Conversely, when a CP-capable device is hot plugged to an MST Branch device and authentication succeeds, the input stream to the MST Branch device may enable encryption on the specific stream routed to the newly plugged CP-capable device, and this enablement of encryption to that specific stream output should not require unrelated output streams to also become encrypted.

An MST Branch device may be considered as the collection of multiple independent virtual repeater devices. To facilitate the authentication status of a stream output as discernible from its upstream (or parent) link state, the QUERY_STREAM_ENCRYPTION_STATUS message transaction provides for this information on a per-stream basis to an MST Source device.

I.3 QUERY_STREAM_ENCRYPTION_STATUS Message Transaction Handling in a CP Tree Topology

Whenever any device is plugged in to an already authenticated CP tree topology that contains an MST Source device and MST devices with Branching Unit (with the one MST Source device being the most upstream transmitter), a CONNECTION_STATUS_NOTIFY message transaction is propagated upstream, directly the Transmitter. When a stream is added to the new device, the MST Source device may query the stream's authentication status by initiating a QUERY_STREAM_ENCRYPTION_STATUS request message transaction.

The MST Source device targets the QUERY_STREAM_ENCRYPTION_STATUS message transaction at the MST Branch device that is directly connected to the MST Source device. After receiving the message transaction, MST devices with a Branching Unit that supports a QUERY_STREAM_ENCRYPTION_STATUS message transaction prepare the status, and then pass the message transaction to the upstream device until the message transaction reaches the MST Source device. Upon receiving the message transaction, the MST Source device may enable encryption on the output stream to the newly added device, in compliance with CP license policy. The MST Source device shall wait for the QUERY_STREAM_ENCRYPTION_STATUS reply message transaction before initiating another such message. The MST Source device can have only one outstanding QUERY_STREAM_ENCRYPTION_STATUS message transaction at a time.

To populate the message reply fields, the MST Branch device shall query the status of all connected downstream devices to which the specified Stream ID is being transmitted. The reply is a summary of all downstream status.

I.3.1 IDs Provided by MST Source Device for QUERY_STREAM_ENCRYPTION_STATUS Request Message Transaction

After the MST Source device originates a QUERY_STREAM_ENCRYPTION_STATUS message transaction, the device shall provide for the IDs listed in Table I-1.

QUERY_STREAM_ENCRYPTION_STATUS Message Transaction Handling in a CP Tree Topology

Table I-1: IDs Provided by MST Source Device for QUERY_STREAM_ENCRYPTION_STATUS Request Message Transaction

Bit #	Definition
7:0	**Stream_ID** The Client (the MST Source device) specifies an ID of the Stream (*S_id*) for which Status is requested. MST Branch devices, because they forward the request message transaction, shall update the Stream_ID, because the Stream_ID is governed by Branch Payload Bandwidth Manager of each MST Branch device and is bound to be unique on each link, as described in Section 2.6.
63:8	**Client_ID** A 56-bit Client (the MST Source device) supplied nonce (*Q_id*). The nonce is provided in Little Endian format, and shall be non-repeatable (e.g., pseudo random number).
65:64	**Stream_Event** 00b = CP_IRQ event generated on stream status (*Stream-Status*) change. (Default state after initial power-on.) 01b = No event generated on stream status change. 10b, 11b = RESERVED for future use. If an MST Branch device supports the QUERY_STREAM_ENCRYPTION_STATUS method, the device shall support both options within this field.
66	**Stream_Event_Mask** 0 = Ignore Stream_Event field in this message. 1 = Indicates that the Stream_Event field has valid changes to be applied.
68:67	**Stream_Behavior** Reflects the policy to apply to the stream contents. 00b = Force re-authentication of the parent link. (Default state after initial power-on.) 01b = Block flow of encrypted content to unauthenticated outputs (e.g., black raster). 10b, 11b = RESERVED for future use. This may influence the MST Branch device's behavior when encrypted content (e.g., using HDCP encryption) is directed toward an unauthenticated output (e.g., not HDCP-capable, not authenticated, etc.). If an MST Branch device supports the QUERY_STREAM_ENCRYPTION_STATUS method, the device shall support both options within this field.
69	**Stream_Behavior_Mask** 0 = Ignore Stream_Behavior field in this message. 1 = Indicates that the Stream_Behavior field has valid changes to be applied.
71:70	**RESERVED FOR FUTURE USE**

QUERY_STREAM_ENCRYPTION_STATUS Message Transaction Handling in a CP Tree Topology

I.3.2 Stream Status in QUERY_STREAM_ENCRYPTION_STATUS Reply Transaction

MST Branch devices shall reply to QUERY_STREAM_ENCRYPTION_STATUS message transaction with the status information listed in Table I-2.

Table I-2: Stream Status Information Replied by the MST Branch Device

Bit #	Definition[a]
1:0	**Stream_State** Reports the state of the stream specified in the Stream_ID field of the QUERY_STREAM_ENCRYPTION_STATUS message transaction. Not a summary of downstream status. Based only on the MST Branch device's state that is forming the reply. 00b = Stream does not exist. The Stream ID specified in the request message is not present in the Payload Allocation table. All other fields in the reply can be ignored. 01b = Stream Not Active. The stream exists in the Payload Allocation Table, but it is not being driven to an output port (possibly due to a POWER_DOWN_PHY request). If all downstream-facing ports (DFPs) report this status, the MST Branch device shall report this status in the reply. All other fields in the reply can be ignored. 10b = Stream Active. The stream exists and is being actively driven to an output port. 11b = RESERVED.
2	**Stream_Repeater_Function** 0 = Simple Sink termination within the MST Branch device. For example, the MST Branch device has a display, and the stream terminates in this device, and is not subsequently presented on any other physical output ports on this MST Branch device. Physical output ports are described in Section 2.5.1. 1 = Repeater Function is present on this stream in this MST Branch device. The stream is directed to one or more MST Branch device outputs.
3	**Stream_Encryption** 0 = Stream Encryption is Off. 1 = Stream Encryption is On (i.e., the combination of Link Encryption and VC Payload Encryption as described in ECF (Encryption Control Field) in Section 2.6).
4	**Stream_Authentication** 0 = Stream has not completed authentication. 1 = Stream completed all parts of authentication. Indicates all the downstream MST Branch devices and Leaf devices connected to this stream have completed all applicable parts of authentication.
7:5	**RESERVED** Shall be all 0s.

QUERY_STREAM_ENCRYPTION_STATUS Message Transaction Handling in a CP Tree Topology

Table I-2: Stream Status Information Replied by the MST Branch Device (Continued)

Bit #	Definition[a]
10:8	**Stream_Output_Sink_Type** Reports the MST Branch Device output connected to this stream. Stream unconnected state is indicated when all the output type bits are cleared to 0.
8	1 = Stream is connected by way of an MST Branch Device Output to has one or more non-authenticatable legacy devices (e.g., analog CRT, TV) connected.
9	1 = Stream has one or more devices connected that do **not** support content protection on DP links or the QUERY_STREAM_ENCRYPTION_STATUS message transaction. This includes DVI/HDMI Sink devices or Sink/Repeater devices designed for *DP v1.1a* (or lower).
10	1 = Stream has one or more DP MST-capable Sink/Branch devices connected that support the QUERY_STREAM_ENCRYPTION_STATUS message transaction.
12:11	**Stream_Output_CP_Type** Reports the type of Content Protection supported on all devices connected to this stream. This field is a bit mask. All bits that apply to the specified stream shall be set appropriately. Each MST Branch device shall include its own capabilities, as well as the capabilities reported from downstream devices, in the reply.
11	1 = H*DCP for DP r1.x* (no *r2.x* support) devices connected to the stream.
12	1 = *HDCP for DP r2.x* capable devices attached to the stream.
14:13	**RESERVED** Shall be cleared to 0.
15	**Signed** 0 = Signature L' is not provided. 1 = Signature L' is provided. MST Branch devices shall clear this bit to 0 when generating a reply. MST Branch and Source devices shall ignore this bit when receiving a reply message.
23:16	**Stream_ID** Stream_ID of the stream for which status is being reported. Should match the Stream_ID contained in the QUERY_STREAM_ENCRYPTION_STATUS request message.

a. Stream refers to VC Payload.

I.3.3 Stream Status Signature in QUERY_STREAM_ENCRYPTION_STATUS Reply Message Transaction

The Signature field L' in the QUERY_STREAM_ENCRYPTION_STATUS message shall be omitted when the Signed bit is cleared to 0. MST Branch and Source devices shall ignore the Signature field when present.

I.3.4 Usage of Sink Type in Stream Status by an MST Source Device

The purpose of the Stream Sink Type in the Status Information of a QUERY_STREAM_ENCRYPTION_STATUS reply message transaction is to allow an MST Source device to identify whether the connected device is a simple DVI/HDMI, SST-mode Sink device, or Repeater device, or an MST device. In cases where the stream is cloned onto more than one MST Branch device output, the type field present is a bitmask of all the connected types.

I.3.5 Status Query

Updated in *DP v1.4a*.

The MST Source device may use a QUERY_STREAM_ENCRYPTION_STATUS message transaction to query the downstream status for a particular stream (i.e., VC Payload). Every query is initiated with a 64-bit unique ID – a 56-bit query nonce (*Q_id*) and 8-bit Stream ID (*S_id*). The downstream MST Branch device forwards the request message transaction to its next immediate downstream device after updating the *S_id* to the outgoing VC Payload ID that it has assigned (as described in Section 2.6).

Table I-3 lists the values that are calculated by the MST Branch device.

Table I-3: MST Branch Device Status Query Calculated Values

Value	# of Bits	Description
Stream-Status	16	MST Branch device determined status value as defined above.
Q_id	56	Client (MST Source device) supplied nonce. Unused.
S_id	8	Client specifies an ID of the Stream for which Status is requested; the downstream MST Branch device updates the *S_id* to the outgoing VC Payload ID it has assigned to the stream.

QUERY_STREAM_ENCRYPTION_STATUS Message Transaction Handling in a CP Tree Topology

Figure I-1 and Figure I-2 illustrate how QUERY_STREAM_ENCRYPTION_STATUS message transactions are forwarded and executed within various CP topologies.

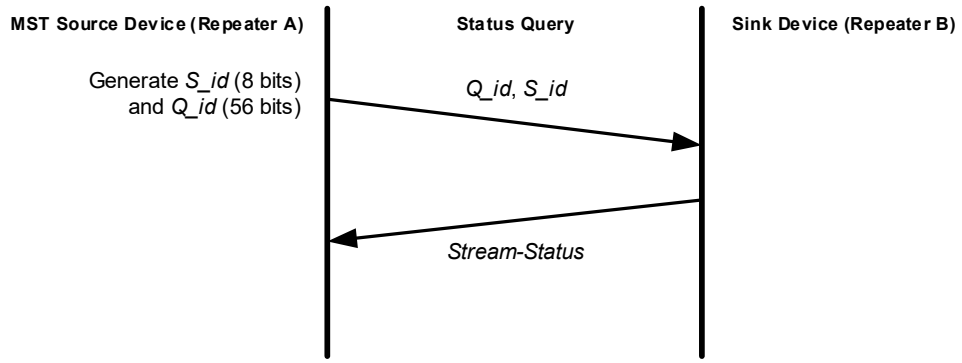


Figure I-1: QUERY_STREAM_ENCRYPTION_STATUS Message Transaction Execution when MST Source Device Is Directly Connected to Sink Device

As illustrated in Figure I-2, when an MST Source device is connected to a Sink device by way of MST Branch device(s), the MST Source device targets the QUERY_STREAM_ENCRYPTION_STATUS request message transaction at the MST Branch device (Repeater B) that is directly connected to the MST Source device. Each MST Branch device shall generate its own QUERY_STREAM_ENCRYPTION_STATUS messages downstream until the status request reaches the last MST Branch device. As replies are generated, the upstream device (Repeater C) generates a new Stream Status as a combination of its own status and the downstream status. The upstream device repeats the process until it reaches the MST Source device.

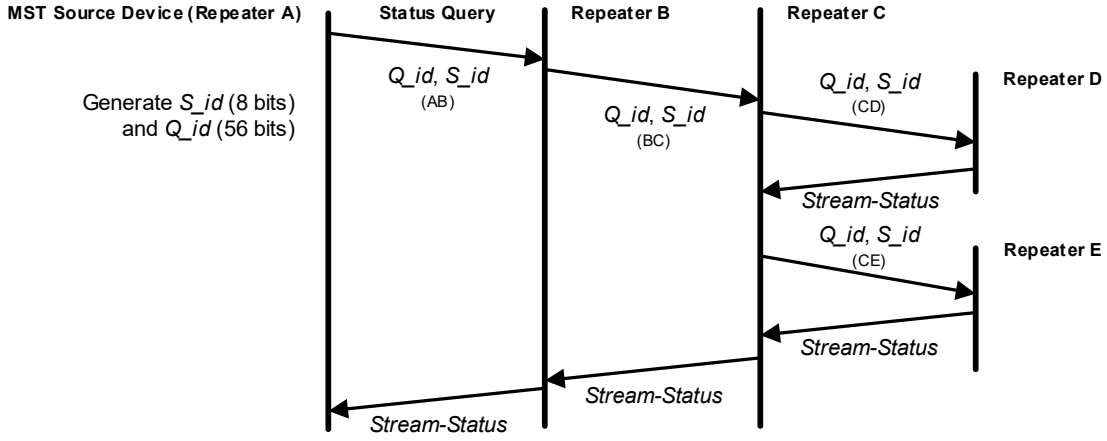


Figure I-2: QUERY_STREAM_ENCRYPTION_STATUS Message Transaction Forwarding and Execution when MST Source Device Is Connected to Sink Device by way of MST Branch Devices

QUERY_STREAM_ENCRYPTION_STATUS Message Transaction Handling in a CP Tree Topology

At each level, the Encryption Status and Authentication Status in Stream Status reported upward shall be the AND of all MST Branch device output ports connected to this stream, and status provided by the immediate downstream device. If Repeater C authenticated the output port connected to Repeater D, but any of the stream's output ports on Repeater D were not authenticated, the collective Stream Status presented by Repeater C to Repeater B shall reflect that the stream is not authenticated. By this means, the Stream Status that is replied to the MST Source device is always the lowest common denominator of the topology.

J 16-Bit Frame CRC Example (Informative)

Updated in *DP v2.0*.

The CRC calculation is performed on the entire frame. A 16-bit CRC is generated per color component, based on the following polynomial:

$$f(x) = x^{16} + x^{15} + x^2 + 1$$

The CRC calculation is performed only on active pixels. The msb is shifted in first. For any colorimetry format that is less than 16bpc, the lsb is zero-padded.

CRC values are calculated after pixel data link symbols are unpacked into pixel data for each color component (e.g., Y, Cb, and Cr). If the pixel encoding format is YCbCr 4:2:2 or YCbCr 4:2:0, the number of active Cb or Cr pixel data in the video frame is either one half or one quarter, respectively, of the active Y pixel data in the video frame. How the YCbCr 4:2:2 or YCbCr 4:2:0 pixel data maps to pixel data link symbols has no relevance to how CRC values are calculated for Y, Cb, and Cr.

The following is an example of a parallel 16-bit CRC generation for one color component.

```
module crc16_16(
// Outputs
dout,

// Inputs
reset, clk, d, enable
);

// Inputs and Outputs
input   [ 15: 0] d;
input   clk;
input   reset;
input   enable;
output  [ 15: 0] dout;

// Internal Signals
reg     [ 15: 0] b;
wire    [ 15: 0] dout;

// Internal Assignments
assign dout = b;
// Define LFSR
always @(posedge clk)
begin
        if (reset)
        begin
               b <= 16'h0;
        end
        else
        begin
               if (enable)
                begin
```

```
b[15] <= b[ 0] ^ b[ 1] ^ b[ 2] ^ b[ 3] ^ b[ 4] ^ b[ 5] ^ b[ 6] ^
b[ 7] ^ b[ 8] ^ b[ 9] ^ b[10] ^ b[11] ^ b[12] ^ b[14] ^ b[15] ^
d[ 0] ^ d[ 1] ^ d[ 2] ^ d[ 3] ^ d[ 4] ^ d[ 5] ^ d[ 6] ^ d[ 7] ^
d[ 8] ^ d[ 9] ^ d[10] ^ d[11] ^ d[12] ^ d[14] ^ d[15];

b[14] <= b[12] ^ b[13] ^ d[12] ^ d[13];
b[13] <= b[11] ^ b[12] ^ d[11] ^ d[12];
b[12] <= b[10] ^ b[11] ^ d[10] ^ d[11];
b[11] <= b[ 9] ^ b[10] ^ d[ 9] ^ d[10];
b[10] <= b[ 8] ^ b[ 9] ^ d[ 8] ^ d[ 9];
b[ 9] <= b[ 7] ^ b[ 8] ^ d[ 7] ^ d[ 8];
b[ 8] <= b[ 6] ^ b[ 7] ^ d[ 6] ^ d[ 7];
b[ 7] <= b[ 5] ^ b[ 6] ^ d[ 5] ^ d[ 6];
b[ 6] <= b[ 4] ^ b[ 5] ^ d[ 4] ^ d[ 5];
b[ 5] <= b[ 3] ^ b[ 4] ^ d[ 3] ^ d[ 4];
b[ 4] <= b[ 2] ^ b[ 3] ^ d[ 2] ^ d[ 3];
b[ 3] <= b[ 1] ^ b[ 2] ^ b[15] ^ d[ 1] ^ d[ 2] ^ d[15];
b[ 2] <= b[ 0] ^ b[ 1] ^ b[14] ^ d[ 0] ^ d[ 1] ^ d[14];

b[ 1] <= b[ 1] ^ b[ 2] ^ b[ 3] ^ b[ 4] ^ b[ 5] ^ b[ 6] ^ b[ 7] ^
b[ 8] ^ b[ 9] ^ b[10] ^ b[11] ^ b[12] ^ b[13] ^ b[14] ^ d[ 1] ^
d[ 2] ^ d[ 3] ^ d[ 4] ^ d[ 5] ^ d[ 6] ^ d[ 7] ^ d[ 8] ^ d[ 9] ^
d[10] ^ d[11] ^ d[12] ^ d[13] ^ d[14];

b[ 0] <= b[ 0] ^ b[ 1] ^ b[ 2] ^ b[ 3] ^ b[ 4] ^ b[ 5] ^ b[ 6] ^
b[ 7] ^ b[ 8] ^ b[ 9] ^ b[10] ^ b[11] ^ b[12] ^ b[13] ^ b[15] ^
d[ 0] ^ d[ 1] ^ d[ 2] ^ d[ 3] ^ d[ 4] ^ d[ 5] ^ d[ 6] ^ d[ 7] ^
d[ 8] ^ d[ 9] ^ d[10] ^ d[11] ^ d[12] ^ d[13] ^ d[15];
              end
       end
end
endmodule
```

K Adaptive-Sync

New to *DP v1.4*. Updated in *DP v1.4a*.

For many years, the display industry has operated with the understanding that displays run at a fixed refresh rate (e.g., 60Hz). This is in contrast with the fact that there are many types of content that can be transmitted to a display, each with its own unique, and sometimes varying, frame rate. When the display refresh rate is not synchronized to the content frame rate, the user can experience undesirable effects (e.g., tearing and stutter). For mobile applications (e.g., table and laptop), unnecessarily high display refresh rates for static and video content can increase power draw and reduce battery life. These factors have given rise to the need for a technology that seamlessly allows the display's refresh rate to adapt to the content's frame rate. VESA has developed an industry standard that enables interoperable, variable refresh rate capabilities over DisplayPort and Embedded DisplayPort (eDP) interfaces, referred to as "Adaptive-Sync." Adaptive-Sync, an optional feature supported by *DP v1.4* (and higher), leverages the Ignore MSA option described in Section 2.2.4.1.1 to enable Source and Sink devices to seamlessly and dynamically vary the refresh rate.

This appendix describes the Source and Sink device needs for implementing Adaptive-Sync:

- Source and Sink devices shall support the Ignore MSA option, as described in Section 2.2.4.1.1 and *eDP Standard*, *Section 3.7*.
  - Prior to enabling an Adaptive-Sync video transmission, an Adaptive-Sync-capable DP Source device shall use an AUX write transaction to write 1 to the MSA_TIMING_PAR_IGNORE_EN bit in the DOWNSPREAD_CTRL register (DPCD Address 00107h, bit 7).
- Source device shall pass the test cases of the Source device test procedures described in *DP EDID CTS*, *Section 3.3.5*.
- Sink device shall pass the test cases of the Sink device test procedures described in *DP EDID CTS*, *Section 4.8*.
  - As part of this test, the Sink device shall render the Source device frame within a fraction of a frame time immediately upon receiving the frame from the Source device, without delay.
- Sink devices that support Adaptive-Sync shall indicate support for the Adaptive-Sync range in DisplayID or legacy EDID, and the Ignore MSA option in DPCD.
- Source devices that support Adaptive-Sync shall read the Sink device DPCD capability and Adaptive-Sync range capability from DisplayID or legacy EDID and ensure that the Source device frame duration falls within the range.
- If audio support is reported in DisplayID or legacy EDID along with Adaptive-Sync capability, the Sink device shall support audio rendering while the Ignore MSA option is enabled.

- If multiple resolution support is reported in DisplayID or legacy EDID, for all resolutions that are within the Adaptive-Sync range of the stream Sink device, a Sink device shall support operation of the resolution in Normal mode, both with and without the Ignore MSA option enabled.
  - For example, if a Sink device reports an Adaptive-Sync vertical refresh rate range of 30 to 100Hz by declaring it in the Display Range Limit Descriptor, timings reported in DisplayID or legacy EDID's established, standard and detailed DisplayID timing blocks that lie within the range (i.e., vertical refresh rate for those timings within the 30 to 100Hz range), shall be able to support the Adaptive-Sync range from the nominal vertical refresh rate defined by the timing in DisplayID or legacy EDID to the minimum supported range.

Note: *Timing exposed in DisplayID or legacy EDID is usually optimized for bandwidth by using minimum horizontal and vertical blank (i.e., using CVT Standard timing standards). To achieve a lower refresh rate at same pixel and line rate, vertical blank is extended.*

- If timing exposed in DisplayID or legacy EDID is beyond the Sink device's Adaptive-Sync range (i.e., 24Hz timing for the above example), the Source device shall not enable the Ignore MSA option on that timing.
- For a timing that can be supported both with the Ignore MSA option and conventional non-ignore MSA operation, it is the Source device's responsibility to determine which operation mode it enables, based on the use cases that the Source device supports.

Adaptive-Sync Refresh rate range and use cases for which Adaptive-Sync operation is enabled is beyond the scope of this Standard and is Source device policy-dependent.

DP v1.4a (and higher) enables forwarding of Adaptive-Sync video through a DP protocol converter (see Section 2.2.5.11).

L Information and Examples for DSC Slice/Display Line Calculations (Informative)

New to *DP v1.4*. Updated in *DP v1.4a* to be compliant with *DSC v1.2a* or higher.

L.1 Derivation of Slice Count Requirements

The normative slices/display line listed in Table 2-155 are derived from the following calculations:

- Total pixel throughput rate (display peak pixel rate (ppr)), in units of MP/s, is the cumulative rate for all streams that feed a single display
- DSC engines shall support, at a minimum, one of two maximum encoder throughput rates, depending on the display's ppr:
  - **Throughput rates less than or equal to 2720MP/s** – Use 340MP/s
  - **Throughput rates greater than 2720MP/s** – Use 400MP/s (assumes that these high-end displays shall be built with a faster processor)
- Formula used:
  - Final slice count shall be rounded up to one of the following values – 1, 2, 4, 8, 12, 16, 20, or 24
  - **If ppr is less than or equal to 2720** – Slice count = ppr / 340 (round up if needed)
  - **If ppr is greater than 2720** – Slice count = ppr / 400 (round up if needed)

Note: *See Table 2-155 and information related to the table in Section 2.8.4. Section 2.8.4 addresses a maximum slice width, as well as a special case for display modes that support only Native 4:2:2 (DSC v1.2 or higher) and/or Native 4:2:0 modes (DSC v1.2a or higher).*

L.2 Usage Example

Updated in *DP v2.0*.

The example provided here assumes a maximum slice width (MaxSliceWidth) of 2560 pixels. If the DSC Maximum Slice Width register(s) (DPCD Address(es) 0006Ch and 0226Ch) allow for a larger slice width, the DP DSC Source device may use that width instead of the 2560 value.

For a display that supports the modes listed in Table L-1, the display shall support the number of slices indicated in Table 2-155 for each mode that the display advertises.

Table L-1: Sample Display Configurations

Sample Display Configuration	Resolution	Refresh Rate (Hz)	Mode[a]	Peak Pixel Rate (ppr) (MP/s)[b]	YCbCr Native 4:2:0 Support Bit Value[c d]	YCbCr Native 4:2:2 Support Bit Value[c d]	YCbCr Simple 4:2:2 Support Bit Value[c d]
a	8Kx4K	120	4:2:0	~ 4260	1	X	X
b		90	4:2:2 or 4:2:0	~ 3150	1	1	0
c		60	4:4:4 or 4:2:0	~ 2100	1	X	X
d	5Kx2880	120	4:2:2 or 4:2:0	~ 1900	1	X	1
e		60	4:4:4 or 4:2:0	~ 940	1	X	X
f		15	4:4:4 or 4:2:0	~ 230	1	X	X
g	4Kx2K	60	4:4:4 or 4:2:0	~ 525	1	X	X
h		30	4:4:4	~ 260	X	X	X
i	8Kx4K	120	Simple 4:2:2	~ 4260	X	X	1

a. YCbCr Native 4:2:2 mode is supported only by DSC v1.2 (or higher). YCbCr Native 4:2:0 mode is supported only by DSC v1.2a (or higher).

b. Actual ppr values shall vary; the values used here are for illustrative purposes only.

c. YCbCr Native 4:2:0 Support, YCbCr Native 4:2:2 Support, and YCbCr Simple 4:2:2 Support bits in the DSC DECODER PIXEL ENCODING FORMAT CAPABILITY register(s) (DPCD Address(es) 00069h and 02269h, bits 4:2, respectively).

d. 1 = Supported, 0 = Not supported, X = Don't Care.

Table L-2 describes how to determine the number of slices/display line that shall be supported for the examples listed in Table L-1:

- Sample configurations a through h assume that if a display has more than one DP DSC Sink device, the number of Sink devices divided into the slice/display line mandate, as per Table 2-155, provides a value that is supported in the following registers:
  - DSC SLICE CAPABILITIES 1 register(s) (DPCD Address(es) 00064h and 02264h)
  - DSC SLICE CAPABILITIES 2 register(s) (DPCD Address(es) 0006Dh and 0226Dh)
- Sample configuration i provides an example in which the resulting value is not available in the DSC SLICE CAPABILITIES 1 and DSC SLICE CAPABILITIES 2 registers

Table L-2: Determining Number of Slices/Display Line that Are Supported by Table L-1 Examples

Sample Display Configuration	Description
a	**8Kx4K / 120Hz / 4:2:0, ppr ~ 4260MP/s** Because this configuration is available only in Native 4:2:0, *DSC v1.2a* (or higher) is needed for support. Additionally, the YCbCr Native 4:2:0 Support bit in the DSC DECODER PIXEL ENCODING FORMAT CAPABILITY register(s) (DPCD Address(es) 00069h and 02269h, bit 4) needs to be set to 1. Assuming that these conditions exist, the Alternative Slice/Display Line Mandate column in Table 2-155 may be used, which allows 8 slices/line. Dividing the line width (7680 pixels) by eight slices results in a 960-pixel slice width, which is less than 2560 pixels = okay. If the display also offered the resolution/refresh rate in any mode other than Native 4:2:2 or 4:2:0, it would then need to support 12 slices.
b	**8Kx4K / 90Hz / 4:2:2 or 4:2:0, ppr ~ 3150MP/s** For this configuration to be able to use the Alternative Slice/Display Line Mandate column in Table 2-155, all available display modes shall use Native 4:2:2 (*DSC v1.2* or higher) or Native 4:2:0 (*DSC v1.2a* or higher) mode. Checking that the YCbCr Native 4:2:2 Support and YCbCr Native 4:2:0 Support bits in the DSC DECODER PIXEL ENCODING FORMAT CAPABILITY register(s) (DPCD Address(es) 00069h and 02269h, bits 3 and 4, respectively) are both set to 1 meets this requirement. Checking that the register's YCbCr Native 4:2:2 Support bit (bit 2) is cleared to 0 indicates that the only modes available here are the Native modes. Therefore, the Alternative Slice/Display Line Mandate column may be used. Using the Alternative Slice/Display Line Mandate column for 3150 MP/s, 4 slices/line is given. Dividing the line width (7680 pixels) by four slices results in a 1920-pixel slice width, which is less than 2560 pixels = okay. If the display also included 4:4:4 or Simple 4:2:2 options, it would then need to support eight slices.
c	**8Kx4K / 60Hz / 4:4:4 or 4:2:0, ppr ~ 2100MP/s** Because this configuration supports a mode other than 4:2:0 and Native 4:2:2, it shall use the Slice/Display Line Mandate column in Table 2-155, with no modifications. At 2100MP/s, Table 2-155 indicates that the display shall support 8 slices/pixel-line, which is an allowed value. Dividing the line width (7680 pixels) by eight slices results in a 960-pixel slice width, which is less than 2560 pixels = okay.

Table L-2: Determining Number of Slices/Display Line that Are Supported by Table L-1 Examples (Continued)

Sample Display Configuration	Description
d	**5Kx2880 / 120Hz / 4:2:2 or 4:2:0, ppr ~ 1900MP/s** For this configuration to be able to use the Alternative Slice/Display Line Mandate column in Table 2-155, all available display modes shall use Native 4:2:2 (*DSC v1.2* or higher) or Native 4:2:0 (*DSC v1.2a* or higher) mode. Checking that the YCbCr Native 4:2:0 Support bit in the DSC DECODER PIXEL ENCODING FORMAT CAPABILITY register(s) (DPCD Address(es) 00069h and 02269h, bit 4) is set to 1 meets this requirement. However, checking the supported modes for 4:2:2, the register's YCbCr Simple 4:2:2 Support bit (bit 2) is set to 1, which indicates that Simple 4:2:2 mode is supported. This is a supported mode other than the two native modes. Therefore, the Slice/Display Line Mandate column shall be used. In this case, the table lists 8 slices/line. Dividing the line width (5120 pixels) by eight slices results in a 640-pixel slice width, which is less than 2560 pixels = okay.
e	**5Kx2880 / 60Hz / 4:4:4 or 4:2:0, ppr ~ 940MP/s** Because this configuration supports a mode other than 4:2:0 and Native 4:2:2, it shall use the Slice/Display Line Mandate column in Table 2-155, with no modifications. At 940MP/s, Table 2-155 indicates that the display shall support 4 slices/pixel-line, which is an allowed value. Dividing the line width (5120 pixels) by four slices results in a 1280-pixel slice width, which is less than 2560 pixels = okay.
f	**5Kx2880 / 15Hz / 4:4:4 or 4:2:0, ppr ~ 230MP/s** Because this configuration supports a mode other than 4:2:0 and Native 4:2:2, it shall use the Slice/Display Line Mandate column in Table 2-155, with no modifications. At 230MP/s, Table 2-155 indicates that the display shall support 1 slice/pixel-line, which is an allowed value. Dividing the line width (5120 pixels) by one slice results in a 5120-pixel slice width. This is greater than the 2560-pixel maximum. Therefore, the next higher slice count from the acceptable values shall be used. In this case, it is 2 slices/line, which results in a 2560-pixel slice width = okay.
g	**4Kx2K / 60Hz / 4:4:4 or 4:2:0, ppr ~ 525MP/s** Because this configuration supports a mode other than 4:2:0 and Native 4:2:2, it shall use the Slice/Display Line Mandate column in Table 2-155, with no modifications. At 525MP/s, Table 2-155 indicates that the display shall support 2 slices/pixel-line, which is an allowed value. Dividing the line width (3840 pixels) by two slices results in a 1920-pixel slice width, which is less than 2560 pixels = okay.
e	**4Kx2K / 30Hz / 4:4:4, ppr ~ 260MP/s** Because this configuration supports a mode other than 4:2:0 and Native 4:2:2, it shall use the Slice/Display Line Mandate column in Table 2-155, with no modifications. At 260MP/s, Table 2-155 indicates that the display shall support 1 slice/pixel-line, which is an allowed value. Dividing the line width (3840 pixels) by one slice results in a 3840-pixel slice width. This is greater than the 2560-pixel maximum. Therefore, the next higher slice count from the acceptable values shall be used. In this case, it is 2 slices/line, which results in a 1920-pixel slice width = okay.

Table L-2: Determining Number of Slices/Display Line that Are Supported by Table L-1 Examples (Continued)

Sample Display Configuration	Description
i	**8Kx4K / 120Hz / Simple 4:2:2, ppr ~ 4260MP/s** Because this configuration supports a mode other than 4:2:0 and Native 4:2:2, it shall use the Slice/ Display Line Mandate column in Table 2-155. The table provides a value of 12 slices. If the display is multi-tiled (i.e., has more than one DP DSC Sink device), it needs to be checked that the resulting slices across a horizontal line per DP DSC Sink is supported in the following registers: • DSC SLICE CAPABILITIES 1 register(s) (DPCD Address(es) 00064h and 02264h) • DSC SLICE CAPABILITIES 2 register(s) (DPCD Address(es) 0006Dh and 0226Dh) For example, if there are three separate Sink devices, the number of slices needed in the display line (12) divided by Sink device count (3) would provide 4 slices/horizontal line/Sink device. This is allowed, per the 4_Slices_per_DP_DSC_Sink_Device bit in the DSC SLICE CAPABILITIES 1 register(s) (bit 3). However, for this example, assume that the display has four separate Sink devices. This shall provide 3 slices/horizontal line/Sink device (12 / 4 = 3). Looking at the DSC SLICE CAPABILITIES 1 and DSC SLICE CAPABILITIES 2 registers, there is no support for 3 slices/horizontal display line. Therefore, it is necessary to take the next higher value in the registers, which in this case is 4 slices (DPCD Address(es) 00064h and 02264h, bit 3). This now makes the number of slices in the display line equal to 4 × 4 = 16 (versus the 12 that is in Table 2-155). Dividing the line width (7680 pixels) by 16 slices results in a 480-pixel slice width, which is less than 2560 pixels = okay.

M 128b/132b Channel Coding without Using Place Holders

New to *DP v2.0*.

Section 2.7 and Section 3.5.2 describe place holders at the Link Layer and the PHY Logical Sub-layer:

- For a DP Source device, PHY sync symbol place holders are inserted at the Link Layer, and then replaced by PHY sync symbols at the PHY Logical Sub-layer. Similarly, coding overhead place holders are inserted at the Link Layer, which are then replaced by CDI bits, RS padding bits, and RS parity symbols at the PHY Logical Sub-layer.
- For a DP Sink device, PHY sync symbols are replaced by PHY sync place holders at the PHY Logical Sub-layer. CDI bits, RS Padding bits, and RS Parity symbols are replaced by coding overhead place holders at the PHY Logical Sub-layer. Both sets of place holders are then removed at the Link Layer.

This appendix describes an alternative approach to *DP v2.0* 128b/132b channel coding that does **not** use place holders. In this alternative approach, there are **no** place holders. Instead, for a DP Source device, PHY sync symbols, CDI bits, RS padding bits, and RS parity symbols are directly inserted at the PHY Logical Sub-layer. For a DP Sink device, PHY sync symbols, CDI bits, RS padding bits, and RS parity symbols are directly removed at the PHY Logical Sub-layer.

M.1 Stream Data-to-Link Symbol Mapping with 128b/132b Link Layer without Place Holders

Note: *Because there are no place holders, Section 2.7.8 and Figure 2-114 do* ***not*** *apply in the alternative approach.*

Figure M-1, Figure M-2, and Figure M-3 illustrate the informative, logical views of 128b/132b Link Layer without the use of place holders for DP Source, Sink, and Branch devices, respectively. The three figures are alternatives to Figure 2-104, Figure 2-105, and Figure 2-106, respectively, which illustrate the use of place holders in Section 2.7.

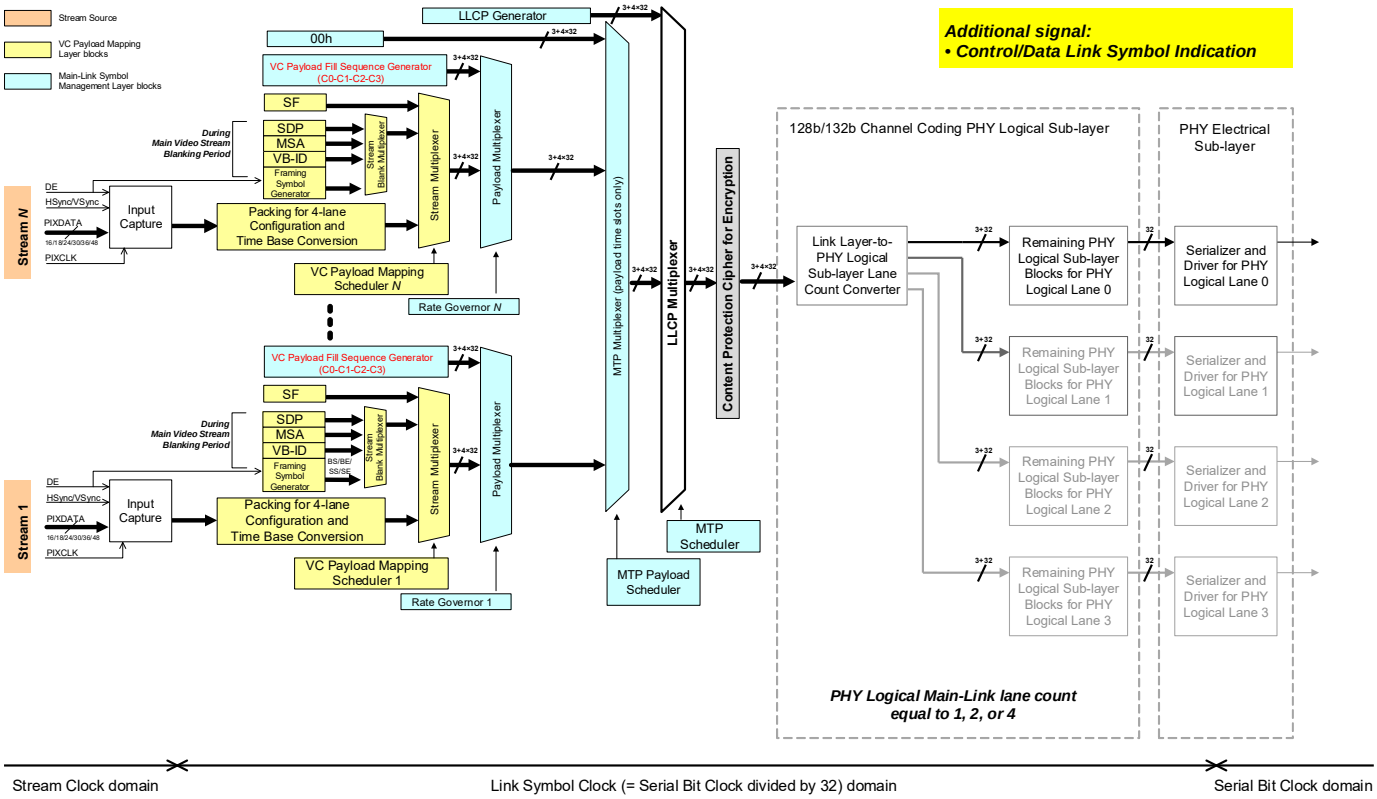


Figure M-1: DP Source Device 128b/132b Link Layer Logical View without Place Holders (Informative) (Alternative to Figure 2-104)

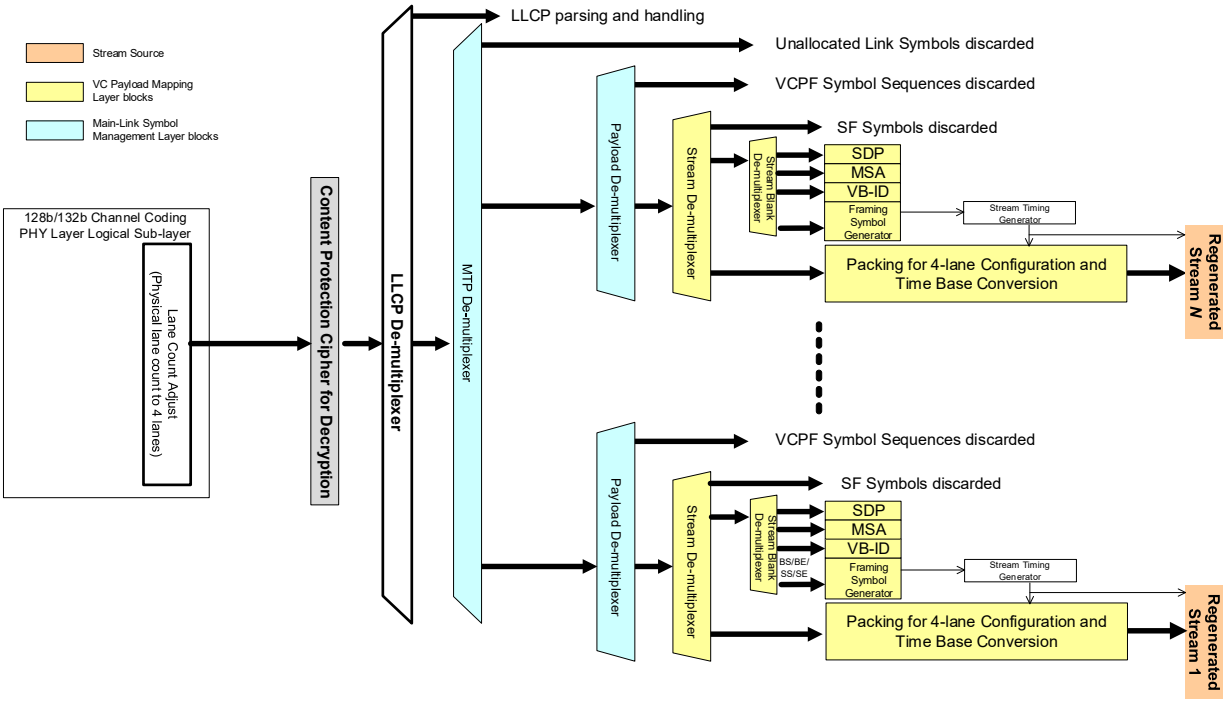


Figure M-2: DP Sink Device 128b/132b Link Layer Logical View without Place Holders (Informative) (Alternative to Figure 2-105)

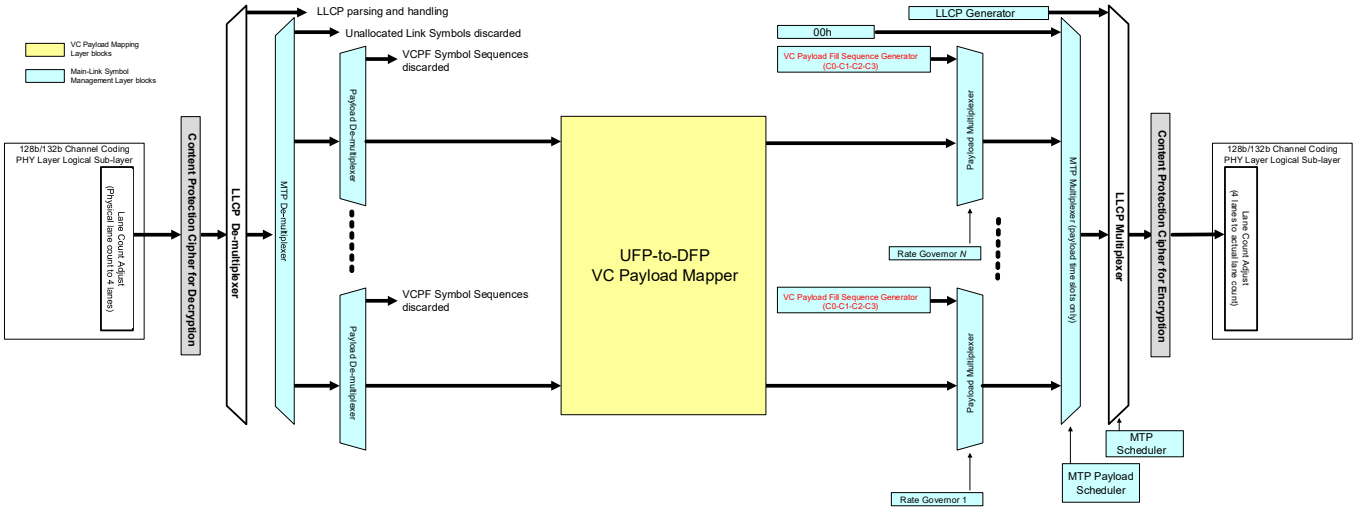


Figure M-3: DP Branch Device 128b/132b Link Layer Logical View without Place Holders (Informative) (Alternative to Figure 2-106)

M.2 Main-Link 128b/132b PHY Logical Sub-layer without Place Holders

Note: *Because there are no place holders, Section 3.5.2.8, Figure 3-36, Figure 3-37, and Figure 3-38 do* ***not*** *apply in the alternative approach.*

M.2.1 Conversion to PHY Logical Main-Link Lane Count

The conversion to PHY Logical Main-Link lane count is the same as that described in Section 3.5.2.7.

M.2.2 128b/132b PHY Logical Sub-layer Operating Sequence without Place Holders (Alternative to Section 3.5.2.2)

This section defines the high-level DPTX and DPRX 128b/132b PHY Logical Sub-layer operating sequence with direct insertion of PHY sync symbols, CDI bits, RS padding bits, and RS parity symbols by the DPTX, and direct removal of PHY sync symbols, CDI bits, RS padding bits, and RS parity symbols by the DPRX.

M.2.2.1 DPTX 128b/132b PHY Logical Sub-layer Operating Sequence (Alternative to Section 3.5.2.2.1)

The operating sequence occurs in the following order (see Figure M-4):

1 Link Layer-to-PHY Logical Sub-layer Main-Link lane count conversion.

2 PHY sync symbol insertion.

3 Intra super symbol shifting.

4 Scrambling.

5 Control Data Indicator (CDI) field insertion and RS padding bit insertion.

6 RS FEC encoding.

7 2-way interleaving of RS parity bytes.

8 RS parity symbol insertion.

9 Pre-coding.

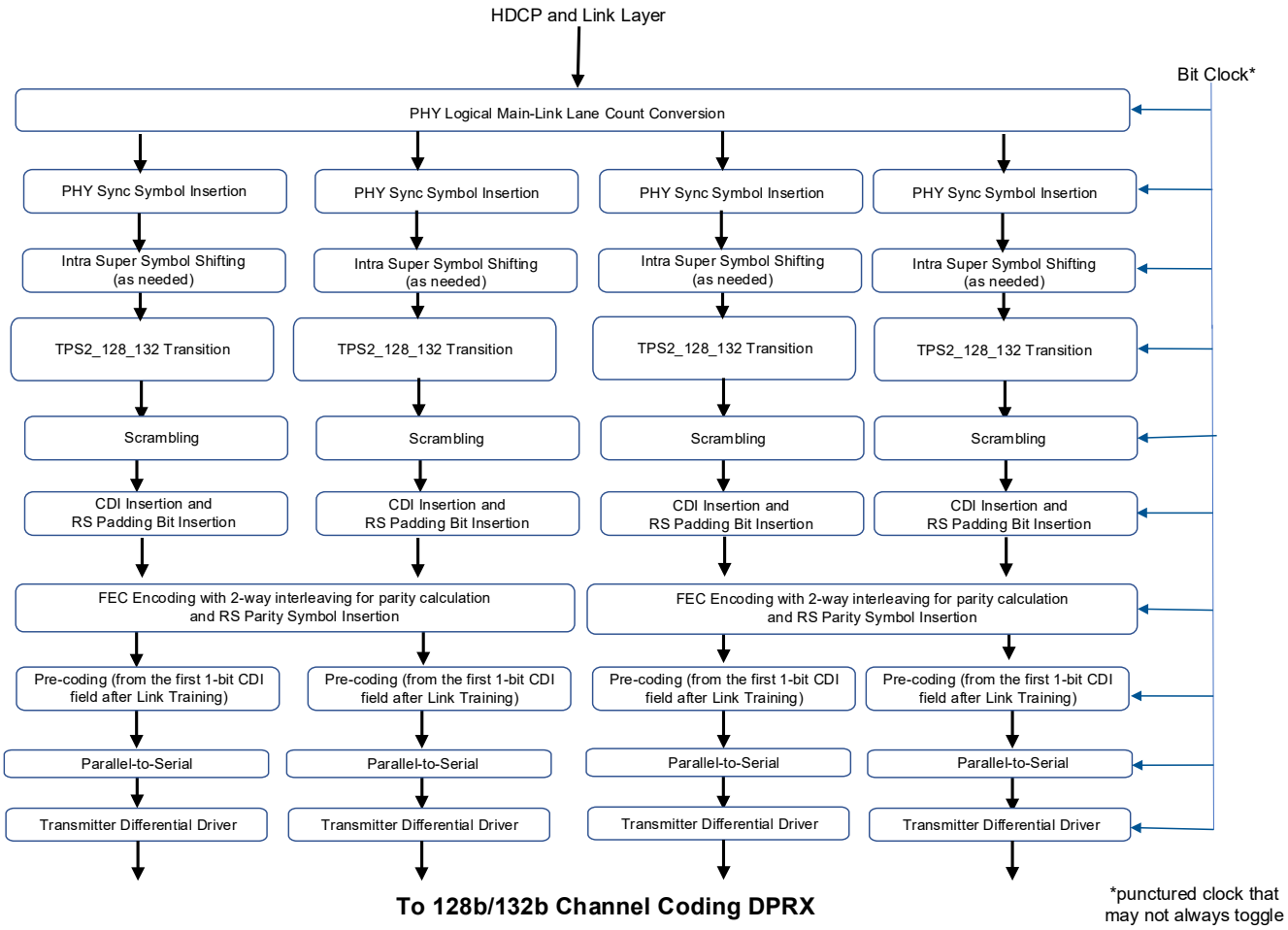


Figure M-4: DPTX 128b/132b PHY Logical Sub-layer Diagram (Informative) (Alternative to Figure 3-29)

M.2.2.2 DPRX 128b/132b PHY Logical Sub-layer Operating Sequence (Alternative to Section 3.5.2.2.2)

The operating sequence occurs in the following order (see Figure M-5):

1 Pre-coding removal.

2 RS parity symbol removal.

3 2-way de-interleaving of RS parity bytes.

4 RS FEC decoding.

5 CDI field removal and RS padding bit removal.

6 De-scrambling.

7 Intra super symbol reverse shifting.

8 PHY sync symbol removal.

9 PHY Logical Sub-layer-to-Link Layer Main-Link lane count conversion.

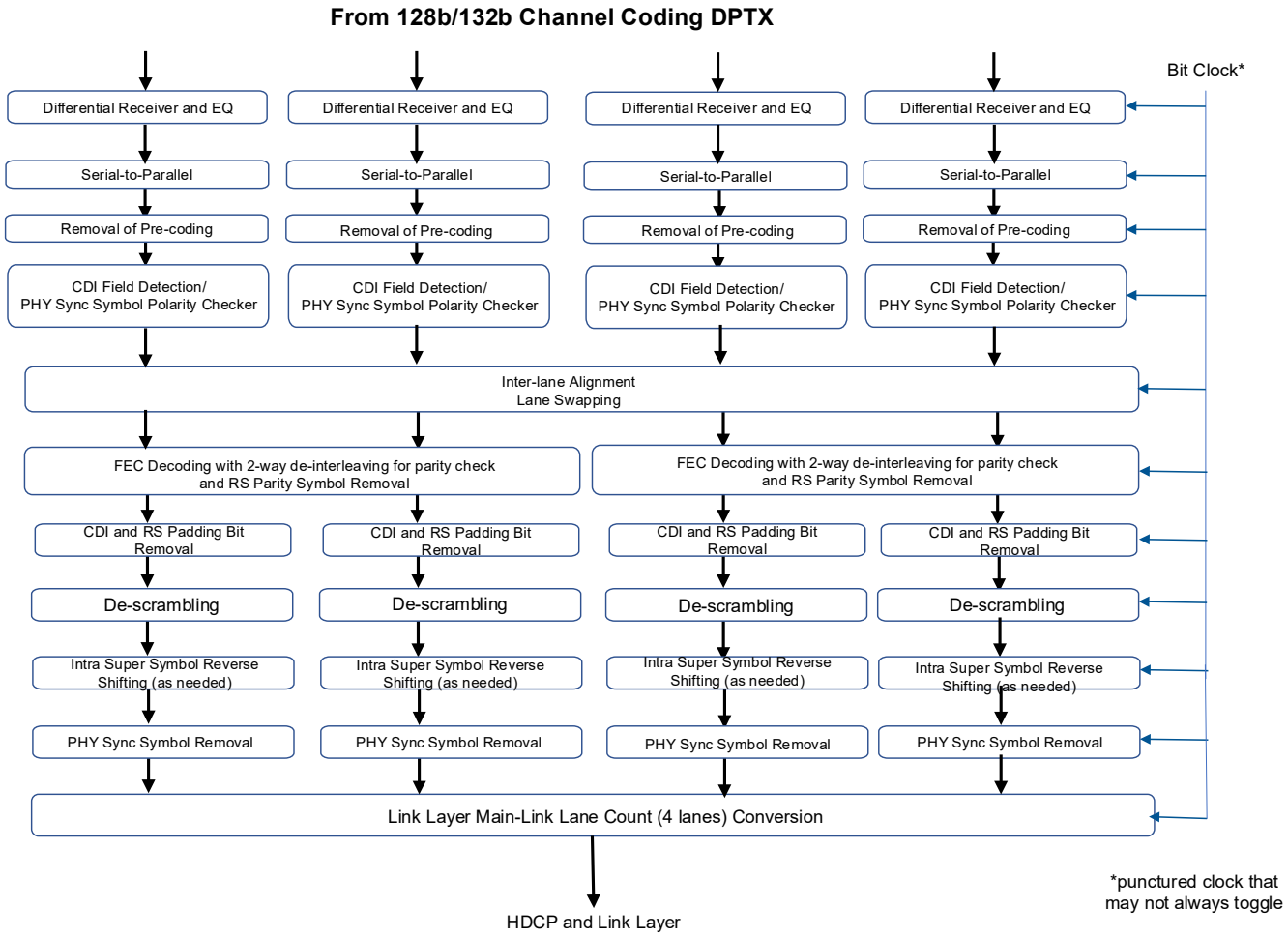


Figure M-5: DPRX 128b/132b PHY Logical Sub-layer Diagram (Informative) (Alternative to Figure 3-30)

M.2.3 Insertion of PHY Sync Symbols, CDI Bits, RS Padding Bits, and RS Parity Symbols at PHY Logical Sub-layer

Figure M-6, Figure M-7, and Figure M-8 illustrate insertion of PHY sync symbols, CDI bits, RS padding bits, and RS parity symbols at the PHY Logical Sub-layer for 4, 2, and 1 enabled physical lanes, respectively. Back-pressure (informative) is applied (i.e., earlier sub-blocks are stalled (informative)) when a PHY sync symbol or RS parity symbol is inserted, –or– after every 32 bits of CDI bits + RS padding bits are inserted.

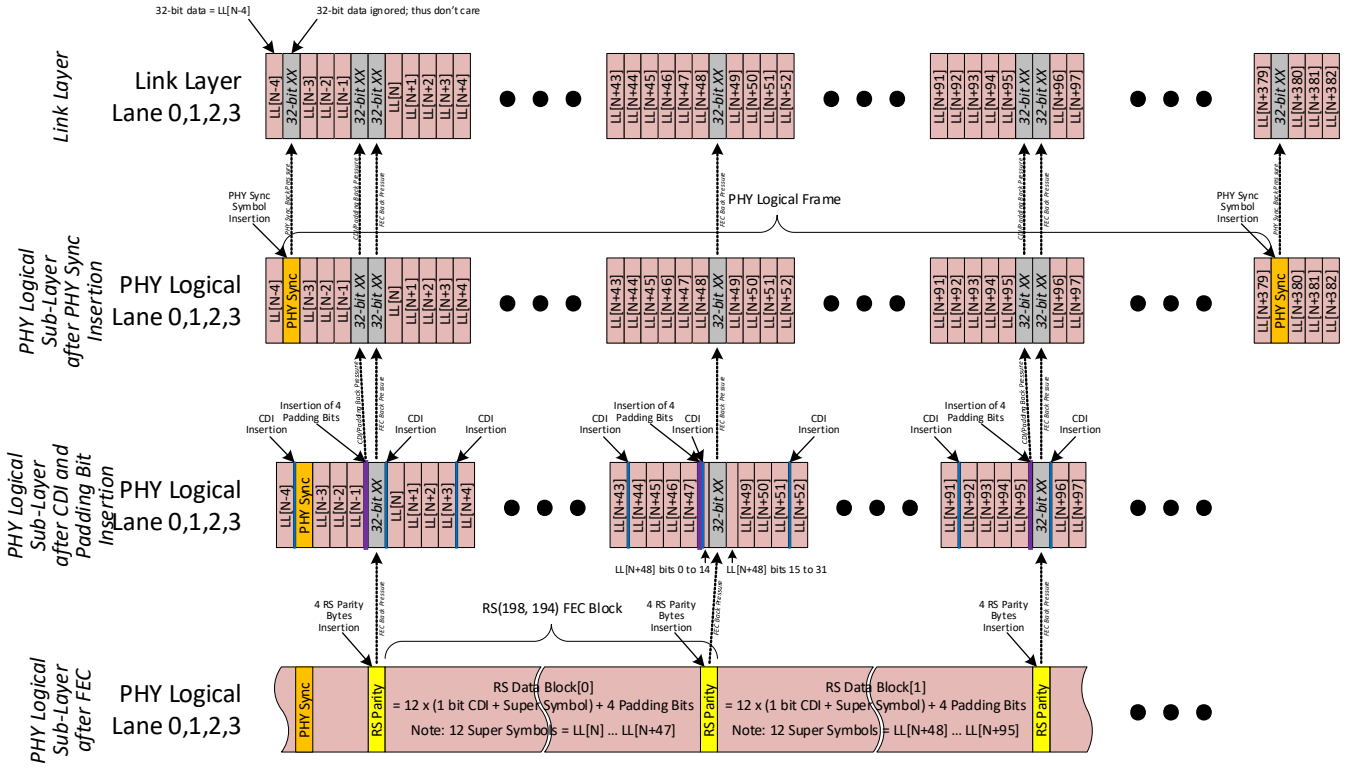


Figure M-6: Insertion of PHY Sync Symbols, CDI Bits, RS Padding Bits, and RS Parity Symbols in 4-lane PHY Logical Main-Link (Informative)

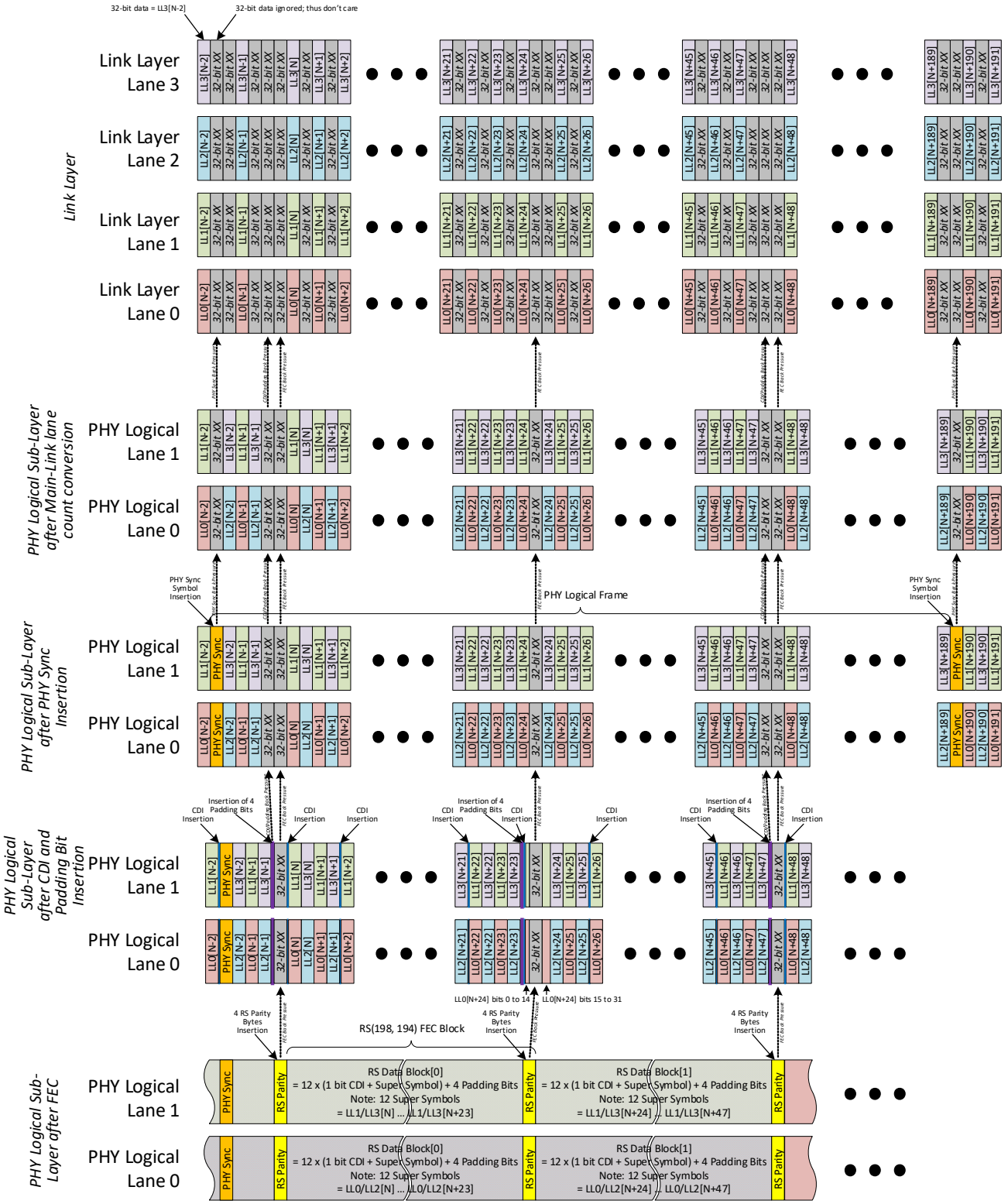


Figure M-7: Insertion of PHY Sync Symbols, CDI Bits, RS Padding Bits, and RS Parity Symbols in 2-lane PHY Logical Main-Link (Informative)

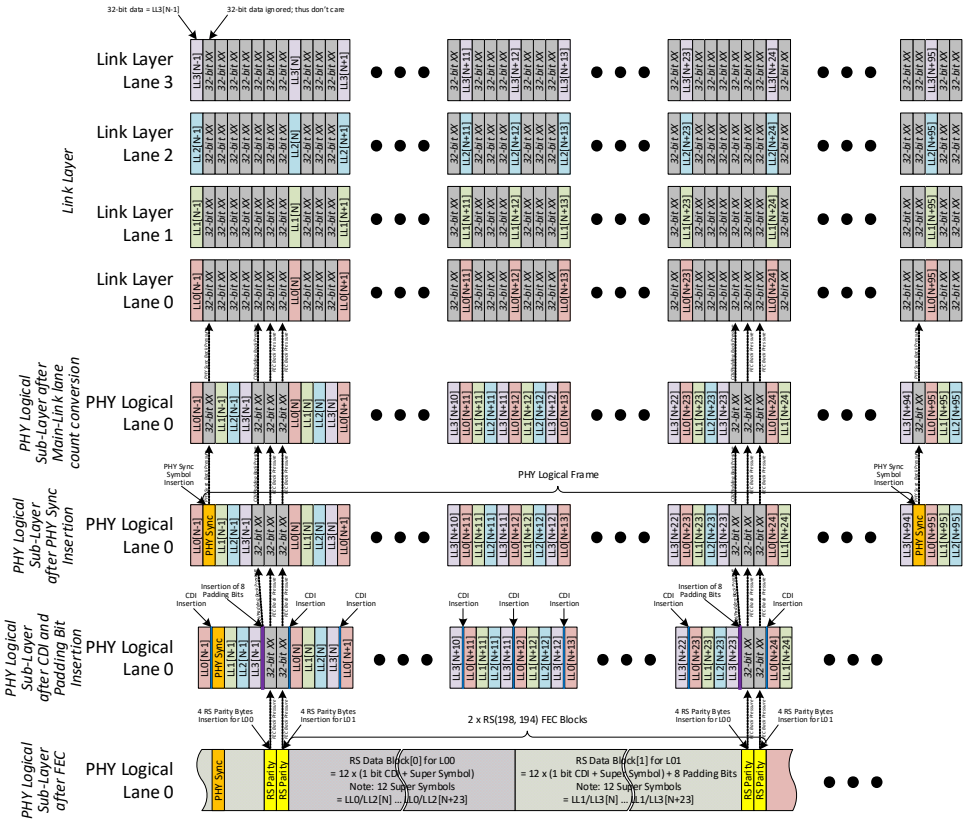


Figure M-8: Insertion of PHY Sync Symbols, CDI Bits, RS Padding Bits, and RS Parity Symbols in 1-lane PHY Logical Main-Link (Informative)

N UHBR*x* PRBS Initial Bit Sequences and Polynomials

New to *DP v2.0*.

This appendix provides the initial bit sequences and polynomials that are used for the UHBR*x* PRBS7, PRBS9, PRBS11, PRBS15, PRBS23, and PRBS31 link quality test patterns.

Note: *Upper left transmitted first and lower right transmitted last.*

N.1 UHBR*x* PRBS7

For PRBS7, the actual 70 bits out of the 127-bit sequence shall be as follows:

```
1 1 1 1 1 1 1
0 0 0 0 0 0 1
0 0 0 0 0 1 1
0 0 0 0 1 0 1
0 0 0 1 1 1 1
0 0 1 0 0 0 1
0 1 1 0 0 1 1
1 0 1 0 1 0 0
1 1 1 1 1 0 1
0 0 0 0 1 1 1
```

$$G(x) = x^7 + x^6 + 1 \text{ (non-inverted signal)}$$

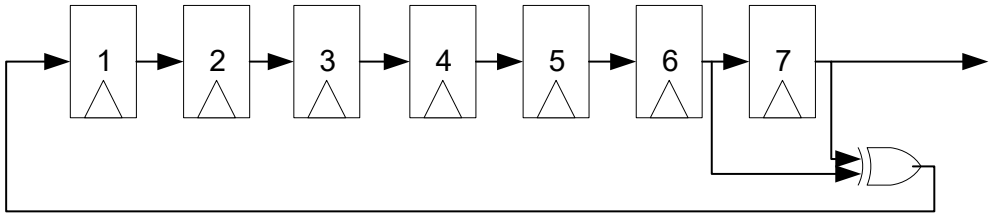


Figure N-1: UHBR*x* PRBS7 Initial Bit Sequences and Polynomial

N.2 UHBR*x* PRBS9

For PRBS9, the actual 90 bits out of the 511-bit sequence shall be as follows:

```
1 1 1 1 1 1 1 1 1
0 0 0 0 0 1 1 1 1
0 1 1 1 1 1 0 0 0
1 0 1 1 1 0 0 1 1
0 0 1 0 0 0 0 0 1
0 0 1 0 1 0 0 1 1
1 0 1 1 0 1 0 0 0
1 1 1 1 0 0 1 1 1
1 1 0 0 1 1 0 1 1
0 0 0 1 0 1 0 1 0
```

$$G(x) = x^9 + x^5 + 1 \text{ (non-inverted signal)}$$

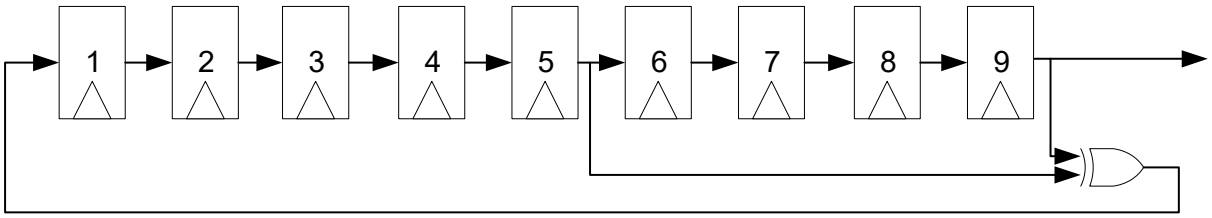


Figure N-2: UHBR*x* PRBS9 Initial Bit Sequences and Polynomial

N.3 UHBR*x* PRBS11

For PRBS11, the actual 110 bits out of the 2047-bit sequence shall be as follows:

```
1 1 1 1 1 1 1 1 1 1 1
0 0 0 0 0 0 0 0 0 1 1
0 0 0 0 0 0 0 1 1 1 1
0 0 0 0 0 1 1 0 0 1 1
0 0 0 1 1 1 1 1 1 1 1
0 1 1 0 0 0 0 0 0 1 0
1 1 1 0 0 0 0 1 0 0 1
0 1 1 0 0 1 0 1 1 0 0
1 1 1 1 0 0 1 1 1 1 1
0 0 1 1 1 1 0 0 0 1 1
```

$$G(x) = x^{11} + x^9 + 1 \text{ (non-inverted signal)}$$

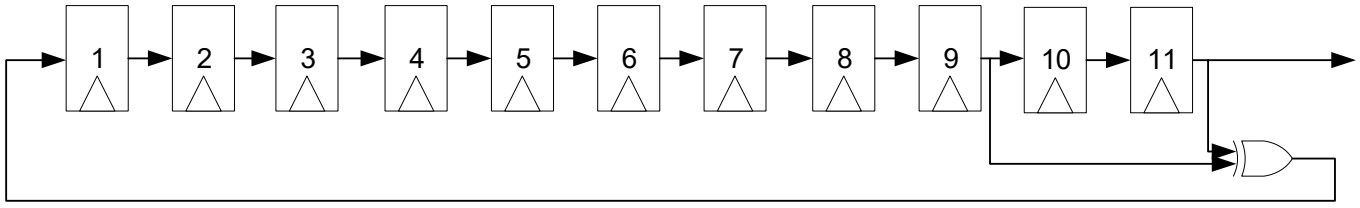


Figure N-3: UHBR*x* PRBS11 Initial Bit Sequences and Polynomial

N.4 UHBR*x* PRBS15

For PRBS15, the actual 150 bits out of the 32767-bit sequence shall be as follows:

```
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
0 0 0 0 0 0 0 0 0 0 0 0 0 1 1
0 0 0 0 0 0 0 0 0 0 0 0 1 0 1
0 0 0 0 0 0 0 0 0 0 0 1 1 1 1
0 0 0 0 0 0 0 0 0 0 1 0 0 0 1
0 0 0 0 0 0 0 0 0 1 1 0 0 1 1
0 0 0 0 0 0 0 0 1 0 1 0 1 0 1
0 0 0 0 0 0 0 1 1 1 1 1 1 1 1
0 0 0 0 0 0 1 0 0 0 0 0 0 0 1
```

$G(x) = x^{15} + x^{14} + 1$ *(non-inverted signal)*

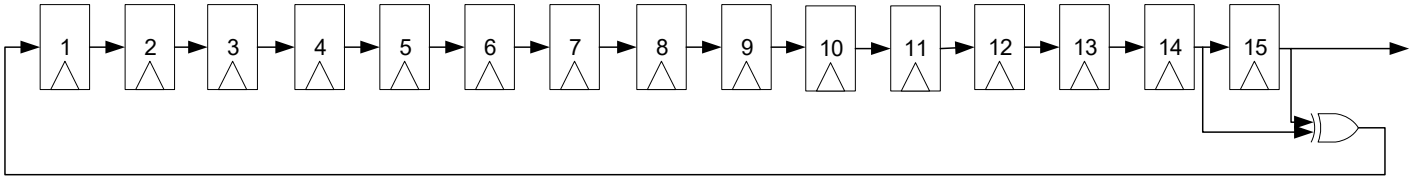


Figure N-4: UHBR*x* PRBS15 Initial Bit Sequences and Polynomial

N.5 UHBR*x* PRBS23

For PRBS23, the actual 253 bits out of the 8,388,607-bit sequence shall be as follows:

```
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1
0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1
0 0 0 0 0 0 0 0 1 1 1 1 1 0 0 0 0 1 1 1 1 1 1
0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0
1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0
1 1 1 0 0 0 0 0 0 0 0 1 1 0 0 0 1 1 1 1 1 0 0
1 1 1 0 0 0 1 1 0 0 0 0 0 1 1 1 1 1 0 0 0 0 0
1 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0
1 1 1 1 1 1 0 0 0 0 0 0 0 0 1 1 1 1 0 1 1 1 1
0 1 1 1 1 1 0 0 0 1 1 1 1 0 0 0 0 0 0 0 0 0 0
```

$G(x) = x^{23} + x^{18} + 1$ *(non-inverted signal)*

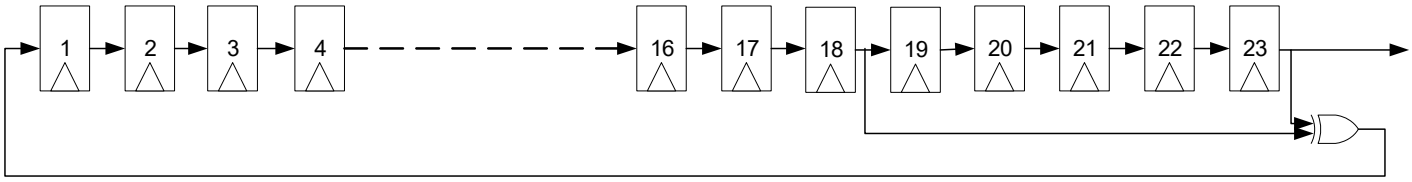


Figure N-5: UHBR*x* PRBS23 Initial Bit Sequences and Polynomial

N.6 UHBR*x* PRBS31

For PRBS31, the actual 310 bits out of the 2,147,483,647-bit sequence shall be as follows:

```
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1
0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1
0 0 0 0 0 0 0 0 1 1 1 1 1 0 0 0 0 0 1 1 1 1 1
0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0
1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0
1 1 1 0 0 0 0 0 0 0 0 1 1 0 0 0 1 1 1 1 1 0 0
1 1 1 0 0 0 1 1 0 0 0 0 0 1 1 1 1 1 0 0 0 0 0
1 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0
1 1 1 1 1 1 0 0 0 0 0 0 0 0 1 1 1 1 0 1 1 1 1
0 1 1 1 1 1 0 0 0 1 1 1 1 0 0 0 0 0 0 0 0 0 0
```

$$G(x) = x^{31} + x^{28} + 1 \text{ (non-inverted signal)}$$

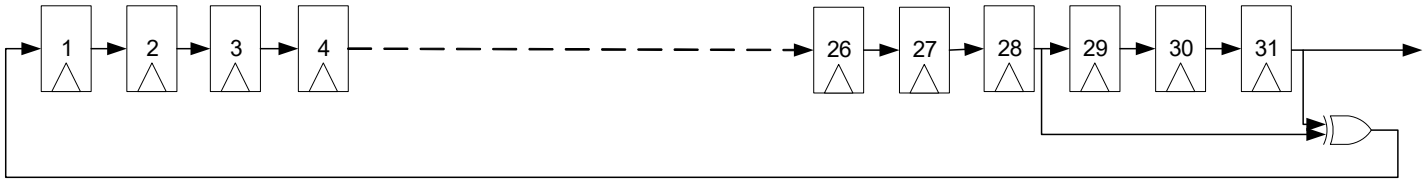


Figure N-6: UHBR*x* PRBS31 Initial Bit Sequences and Polynomial

O Data EYE Mask Differences between HBR3/HBR2 and UHBR*x* Bit Rates

New to *DP v2.0*.

This appendix introduces the EYE mask methodology that is used for UHBR*x* bit rates and contrasts it with the methodology used for HBR3 and HBR2.

O.1 HBR3/HBR2 EYE Mask

The HBR3 and HBR2 bit rates define the EYE mask in terms of EYE height and width (EH and EW, respectively). EH is the peak-to-peak differential voltage (in mV), as measured at the inside of the EYE waveforms. EW is the horizontal opening (in UI). The Data EYE used in compliance is generated using a test pattern, from which RJ and DJ are extracted and extrapolated to a $1E^{-9}$ BER. The data EYE for the device under test is then compared to the EYE mask.

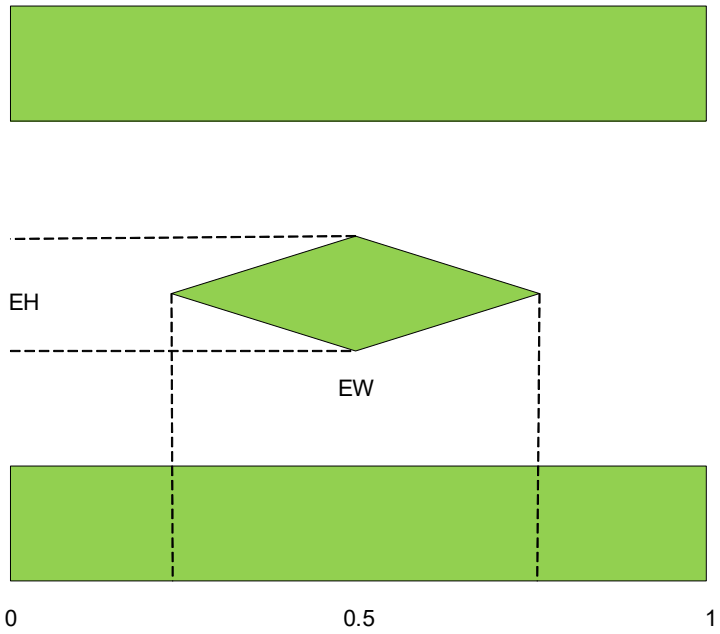


Figure O-1: HBR3/HBR2 EYE Opening Definitions

O.2 UHBR*x* EYE Mask

The EYE mask shape is unchanged from HBR3 and HBR2; however, the metric that defines the EYE has evolved. As illustrated in Figure O-2, the inner EYE mask diamond vertices are now defined differently, as follows:

- EYE mask height is defined by the maximum and minimum deviation from the 0-differential voltage (+Y1 and -Y1). Y1 is the minimum differential peak voltage measurement (in mV).
- Horizontal EYE mask opening has vertices that are defined by the excursion from the outside of the UI (X1 and 1-X1). X1 is the maximum limit (in percentage of UI), and measured at the 0-V differential crossing point.

Due to the 128b/132b channel encoding used in UHBR*x* systems, it is **not** practical to perform RJ/DJ separation. The Data EYE is created by a scope capture that approximates a $1E^{-6}$ BER. The data EYE mask is then directly compared against this measurement without the need for extrapolation.

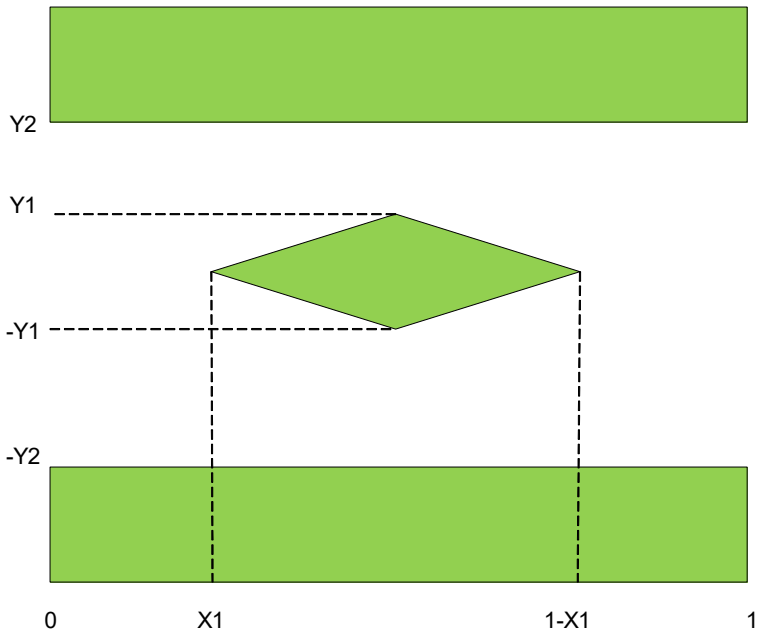


Figure O-2: UHBR*x* EYE Opening Definitions

P Main Contributor History (Previous Versions)

Table P-1: Main Contributor History (Previous Versions)

Company	Name	Contribution	Version
Advanced Micro Devices, Inc.	Quinn Carter	Technical Content	1.1, 1.1a, 1.2
	Nancy Chan	Technical Content	1.1, 1.1a, 1.2, 1.3, 1.4
	Nicholas Chorney	Technical Content	1.2, 1.4, 1.4a
	Jim Foppiano	Technical Content	1.4a
	Mike Foxcroft	Technical Content	1.2
	Richard Fung	Technical Content	1.1, 1.1a, 1.2
	David Glen	Technical Content	1.1, 1.1a, 1.2
	Jim Goodman	Technical Content	1.1, 1.1a
	James Hunkins	Technical Content	1.2a, 1.3, 1.4, 1.4a
	Syed Athar Hussain	Technical Content	1.1, 1.1a, 1.2, 1.2a, 1.3, 1.4, 1.4a
	Sandra Liu	Technical Content	1.2
	Betty Luk	Technical Content	1.1, 1.1a
	Mazen Salloum	Technical Content	1.1, 1.1a
	Frank Sodek	Technical Content	1.3, 1.4
	Minghua Zhu	Technical Content	1.4, 1.4a
Agilent Technologies	Brian Fetz	Technical Content	1.1, 1.1a, 1.2
	Michael Hertz	Technical Content	1.1a
Analogix Semiconductor, Inc.	Mehran Badii	Technical Content	1.3, 1.4, 1.4a
	Jianbin Hao	Technical Content	1.0, 1.1, 1.1a
	Jae Lee	Technical Content	1.2
	Greg Stewart	Technical Content	1.3, 1.4, 1.4a
	Prasanna Swaminathan	Technical Content	1.1, 1.1a
	Craig Wiley	Technical Content	1.0, 1.1, 1.1a
	Ning Zhu	Technical Content	1.0, 1.1, 1.1a, 1.2
Apple, Inc.	Wei Chen	Technical Content	1.1, 1.1a
	Bill Cornelius	Technical Content	1.1, 1.1a, 1.2, 1.4, 1.4a
	Shannon Fields	Technical Content	1.2
	Matt Herndon	Technical Content	1.2
	Girault Jones	Technical Content	1.2
	Rainer Keller	Technical Content	1.3, 1.4

Table P-1: Main Contributor History (Previous Versions) (Continued)

Company	Name	Contribution	Version
Apple, Inc.	Min Chul Kim	Technical Content	1.2
	George Kyriazis	Technical Content	1.2
	Cheung-Wei Lam	Technical Content	1.1, 1.1a, 1.2
	Pete Lawrence	Technical Content	1.2
	Inyeol Lee	Technical Content	1.4a
	Mike Maciesowicz	Technical Content	1.2
	Tim McIntosh	Technical Content	1.3, 1.4, 1.4a
	Anil Pannikkat	Technical Content	1.2
	Sree Raman	Technical Content	1.3, 1.4, 1.4a
	Bob Ridenour	Technical Content	1.2, 1.2a, 1.3, 1.4, 1.4a
	Naftali Sommer	Technical Content	1.4, 1.4a
	Jennifer Tsai	Technical Content	1.4, 1.4a
	Niel Warren	Technical Content	1.2
	Glenn Wheelock	Technical Content	1.2
	Colin Whitby-Strevens	Technical Content	1.1, 1.1a, 1.2a, 1.3, 1.4, 1.4a
		Task Group Co-editor	1.2
ATI Technologies, Inc.	Richard Fung	Technical Content	1.0
	David Glen	Technical Content	1.0
	Jim Goodman	Technical Content	1.0
	Betty Luk	Technical Content	1.0
	Mazen Salloum	Technical Content	1.0
Avatar Tech Pubs	Trish McDermott	Technical Writer	1.3, 1.4, 1.4a
Barco, Inc.	Dirk Ballyn	Technical Content	1.3, 1.4
	Alan Ricker	Technical Content	1.2
Bitec Spain SL	Marco Denicolai	Technical Content	1.3, 1.4, 1.4a
Broadcom Corp.	Christopher Pasqualino	Technical Content	1.0, 1.1, 1.2, 1.4
	Fred Walls	Technical Content	1.4, 1.4a
California Micro Devices	Jeffrey C. Dunnihoo	Technical Content	1.0, 1.1
Dell, Inc.	Joe Giannuzzi	Technical Content	1.0, 1.1, 1.1a
	Joe Goodart	Technical Content	1.0, 1.1, 1.1a
	Lee Mohrmann	Technical Content	1.0, 1.1, 1.1a
	Bruce Montag	Task Group Chair	1.0, 1.1, 1.1a, 1.2
	Jeff Thelen	Technical Content	1.1a, 1.2
Display Labs	Jim Webb	Technical Content	1.0, 1.1, 1.1a
Dolby Labs	Marcus Altman	Technical Content	1.4

Table P-1: Main Contributor History (Previous Versions) (Continued)

Company	Name	Contribution	Version
EIZO Corp. (formerly EISO NANAO Corp.)	Yoshinobu Bamba	Technical Content	1.2, 1.2a, 1.3, 1.4, 1.4a
Foxconn Interconnect Technology, Ltd. (formerly Foxconn Electronics Inc.)	James R. Koser	Technical Content	1.1a
	Glenn Moore	Technical Content	1.2, 1.2a, 1.3, 1.4, 1.4a
	Steve Sedio	Technical Content	1.2
Hardent, Inc.	Simon Bussières	Technical Content	1.4a
	Alain Legault	Technical Content	1.4, 1.4a
	Avrum Warshawsky	Technical Content	1.4a
HP, Inc.	Bob Myers	Task Group Vice-chair	1.0, 1.1, 1.1a, 1.2
Hirose Electric Co., Ltd.	Karl Kwiat	Technical Content	1.2
Hosiden Corp.	James Eilers	Technical Content	1.2
	Hayato Kondo	Technical Content	1.2
	Takahisa Ohtsuji	Technical Content	1.2
InFocus	Jory Olson	Technical Content	1.0, 1.1
Integrated Device Technology, Inc.	Jeff Lukanc	Technical Content	1.1a
	Prashant Shamarao	Technical Content	1.2, 1.2a
Intel Corp.	Nausheen Ansari	Technical Content	1.3, 1.4, 1.4a
	Vishnu Balraj	Technical Content	1.2
	Kiran Bhat	Technical Content	1.2a
	Scott Chen	Technical Content	1.1, 1.1a
	Greg Daly	Technical Content	1.1, 1.1a, 1.2
	Sylvia Downing	Technical Content	1.1, 1.1a, 1.2
	Greg Ebert	Technical Content	1.1, 1.1a, 1.2
	Simon Ellis	Technical Content	1.2
	Michael Hamann	Technical Content	1.1, 1.1a, 1.2, 1.3, 1.4, 1.4a
	George Hayak	Technical Content	1.1, 1.1a, 1.2, 1.2a
	Jamie Johnston	Technical Content	1.1, 1.1a, 1.2, 1.2a, 1.3, 1.4, 1.4a
	Ziv Kabiry	Technical Content	1.4, 1.4a
	Srikanth Kambhatla	Technical Content	1.1, 1.1a, 1.2, 1.2a, 1.3, 1.4, 1.4a
	Anoop Karunan	Technical Content	1.3, 1.4, 1.4a
	Christine Krause	Technical Content	1.3, 1.4, 1.4a
	Jingbo Li	Technical Content	1.3, 1.4, 1.4a
	Yun Lingx	Technical Content	1.1, 1.1a
	Kwasi Mireku	Technical Content	1.1a
	Daniel E. Myers	Technical Content	1.4, 1.4a
	Prakash Radhakrishnan	Technical Content	1.3, 1.4, 1.4a

Table P-1: Main Contributor History (Previous Versions) (Continued)

Company	Name	Contribution	Version
Intel Corp.	Ehud Shoor	Technical Content	1.4, 1.4a
	Lakshmi Uppala	Technical Content	1.1, 1.1a
	Max Vasquez	Technical Content	1.1, 1.1a, 1.2, 1.2a
	Kai A. Wang	Technical Content	1.1a
	Tom Willis	Technical Content	1.1, 1.1a
	Nick Willow	Technical Content	1.1a, 1.2
	Gal Yedidia	Technical Content	1.4, 1.4a
Intersil Corp.	Gourgen Oganessyan	Technical Content	1.2a
JAE Electronics, Inc.	Ron Muir	Technical Content	1.0, 1.1
	Mark Saubert	Technical Content	1.0, 1.1, 1.1a, 1.2
	Toshio Shimoyama	Technical Content	1.0, 1.1, 1.1a, 1.2
Keysight Technologies	Brian Fetz	Technical Content	1.4, 1.4a
	Francis Lin	Technical Content	1.4a
Lattice Semiconductor Corp.	Gang Sun	Technical Content	1.0, 1.1
Lenovo Group	George Diatzikis	Technical Content	1.1, 1.1a, 1.2
	Hiroji Itoh	Technical Content	1.1, 1.1a
	Howard Locker	Technical Content	1.2
Luxtera	Eileen Robarge	Technical Content	1.1, 1.1a
	Jim Webb	Technical Content	1.2
MegaChips Corp. (formerly MegaChips Technology America Corp. and also Kawasaki Microelectronics)	Rahul Kuma Agarwal	Technical Content	1.4, 1.4a
	John Garrett	Technical Content	1.3, 1.4, 1.4a
	Alan Kobayashi	Technical Content and Task Group Chair	1.3, 1.4, 1.4a
	Yoshihiro Uchiyama	Technical Content	1.1a
	Nobuhiro Yanagisawa	Technical Content	1.4, 1.4a
Molex Japan	Mark Bugg	Technical Content	1.2
	JengDe Lin	Technical Content	1.1, 1.1a
	Vincent Lin	Technical Content	1.0
	Scott Sommers	Technical Content	1.0, 1.1a, 1.1, 1.2
	Jason Squire	Technical Content	1.0, 1.1, 1.1a
Novatek Microelectronics Corp.	Andy Lin	Technical Content	1.4, 1.4a

Table P-1: Main Contributor History (Previous Versions) (Continued)

Company	Name	Contribution	Version
NVIDIA Corp.	Raymond Barrios	Technical Content	1.4, 1.4a
	Cameron Buschardt	Technical Content	1.2
	Sunitha Chandra	Technical Content	1.2
	Sherry Cheung	Technical Content	1.2
	Spoorthi D'Silva	Technical Content	1.3, 1.4, 1.4a
	Michael Hopgood	Technical Content	1.2
	Smore Hung	Technical Content	1.4a
	Gregory Kodani	Technical Content	1.2
	Manish Modi	Technical Content	1.2
	Pablo Ortega	Technical Content	1.2a
	Mark Overby	Technical Content	1.2
	Devang Sachdev	Technical Content	1.1a, 1.2
	Varun Sampath	Technical Content	1.3, 1.4, 1.4a
	Bill Simms	Technical Content	1.1, 1.1a, 1.2
	David Stears	Technical Content	1.1a, 1.2, 1.2a, 1.3, 1.4, 1.4a
	William Tsu	Technical Content	1.0, 1.1, 1.1a
	David Wyatt	Technical Content	1.2
NXP Semiconductors (formerly Philips Semiconductor)	Glenn Adler	Technical Content	1.0, 1.1
	Michael Epstein	Technical Content	1.0, 1.1
	Alexandre Esquenet	Technical Content	1.2
	Dave Evoy	Technical Content	1.2
	Arjan Hoogendoorn	Technical Content	1.1a
	Ken Jaramillo	Technical Content	1.2, 1.2a
	Patrick LeJoly	Technical Content	1.2
	Nic Roozeboom	Technical Content	1.2
	Marc Vauclair	Technical Content	1.0, 1.1
	Bart Vertenten	Technical Content	1.2
	Patrick Yu	Technical Content	1.0, 1.1
Parade Technologies, Ltd.	Jimmy Chiu	Technical Content	1,0, 1.1, 1.1a
	Ding Liu	Technical Content	1.1, 1.1a, 1.2
	Mark Qu	Technical Content	1.1, 1.1a, 1.2
	Craig Wiley	Technical Content	1.2, 1.2a, 1.3, 1.4
		Technical Content and Vice Chair	1.4a
	Jack Zhao	Technical Content	1.0, 1.1, 1.1a

Table P-1: Main Contributor History (Previous Versions) (Continued)

Company	Name	Contribution	Version
Qualcomm, Inc.	James Goel	Technical Content	1.4, 1.4a
	Chris Wiesner	Technical Content	1.4, 1.4a
	George Wiley	Technical Content	1.0, 1.1
Quantum Data	Jeff Stenhouse	Technical Content	1.2a
RealTek Semiconductor Corp.	Jay Lin	Technical Content	1.4a
S3 Graphics	Ram Ganapathi	Technical Content	1.2
Samsung	Brian Berkeley	Technical Content	1.2
Samsung AMLCD	Brian Berkeley	Technical Content	1.1a
	J.K. Park	Technical Content	1.1a
Samsung Information Systems America	Ian Miller	Technical Content	1.0, 1.1
Samsung Electronics Co., Ltd.	Jalil Kamali	Technical Content	1.4
	Guarav Malhotra	Technical Content	1.4
	Dale Stolitzka	Technical Content	1.3, 1.4, 1.4a
SMK Corp.	Naoyuki Ono	Technical Content	1.1a
Sony Corp.	Katsuhiro Shimizu	Technical Content	1.2
Spectra7	Andrew Kim	Technical Content	1.4a
	Jim McGrath	Technical Content	1.4a
STMicroelectronics, Inc. (also formerly Genesis Microchip)	Jeff Frankel	Technical Content	1.1a
	John Garrett	Technical Content	1.2, 1.2a
	Alan Kobayashi	Task Group Editor	1.0, 1.1, 1.1a, 1.2
		Technical Content and Task Group Chair	1.2a
	Ali Noorbakhsh	Technical Content	1.0, 1.1, 1.1a
	Larry Prather	Technical Content	1.0, 1.1, 1.1a, 1.2
	Bob Rutkowski	Technical Content	1.1
	Vincent Wang	Technical Content	1.2
Synaptics, Inc.	Bruce Chin	Technical Content	1.4, 1.4a
	Prashant Shamarao	Technical Content	1.3, 1.4, 1.4a
Synopsys	Bala Babu	Technical Content	1.4a
SyntheSys Research	Bent Hessen-Schmidt	Technical Content	1.2
	Sudheer Vemulapalli	Technical Content	1.1a
TE Connectivity, Ltd. (formerly Tyco Electronics)	Doron Lapidot	Technical Content	1.0, 1.1, 1.1a, 1.2
	Jim Leidy	Technical Content	1.0, 1.1, 1.1a, 1.2
	Jim McGroth	Technical Content	1.3, 1.4
Tektronix, Inc.	John Calvin	Technical Content	1.1, 1.1a, 1.2
	Ken Price	Technical Content	1.2, 1.2a

Table P-1: Main Contributor History (Previous Versions) (Continued)

Company	Name	Contribution	Version
Texas Instruments	Jason Acevedo	Technical Content	1.1a, 1.2
	Falk Alicke	Technical Content	1.2
	Mike Campbell	Technical Content	1.3, 1.4, 1.4a
	Gary Chard	Technical Content	1.1a, 1.2
	Julie Hwang	Technical Content	1.2
	Pradeep Katikaneni	Technical Content	1.1a
	Yoon Lee	Technical Content	1.3, 1.4
	Brian Quach	Technical Content	1.3, 1.4
	Ajinder Pal Singh	Technical Content	1.2
THine Electronics, Inc.	Jun Okamura	Technical Content	1.0, 1.1
	Yohei Ishizone	Technical Content	1.0, 1.1
Unigraf	Sergey Grushin	Technical Content	1.4a
VESA	Bill Lempesis	Contributor	1.4a
VESA Compliance Program Manager	James Choate	Technical Content	1.4, 1.4a
ViewSonic	Alain d'Hautecourt	Technical Content	1.0, 1.1, 1.1a
VTM Group/ VESA Consultant	Bob Crepps	Technical Content	1.2, 1.3, 1.4, 1.4a
Xponent Photonics	Hank Blauvelt	Technical Content	1.0, 1.1
	Larry Stark	Technical Content	1.1